TPD7104AF
Application note

Description

TPD7104AF is a high-side gate driver IC for N-channel MOSFET with 12 V power supply. The MOSFET used is driven by the internal charge pump circuit. By selecting the optimum MOSFET for the operating condition, a high-side switch with the optimum specifications can be configured for the system from small to large currents. This IC has a power reverse connection protection function in addition to the load short protection function and the diagnostic function, which contributes to the safety improvement of the system. In addition, PS-8, 2.9 mm × 2.8 mm small surface-mount package is adopted, enabling the system to be miniaturized.

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1. Product overview

The automotive market is increasingly becoming electronic and electrified, requiring control that is more sophisticated. On the other hand, it is becoming increasingly important for ECUs to achieve greater compactness and safety. TPD7104AF is a high-side gate driver IC for N-channel MOSFET, targeting applications such as semiconductor relays and load switches for battery lines used in junction boxes. By choosing the best N-channel MOSFET for the systems, it is possible to accommodate a variety of applications. In addition, TPD7104AF has a power reverse connection protection function that protects ICs even when the batteries are reversely connected. By incorporating high-performance IC chips incorporating state-of-the-art BiCD0.13 μm into PS-8, which is a 2.9 mm × 2.8 mm compact surface-mount package, optimal board layouts can be achieved when many high-side switches are mounted on a compact ECU.

2. Application circuit example

2.1. Application example to power relay

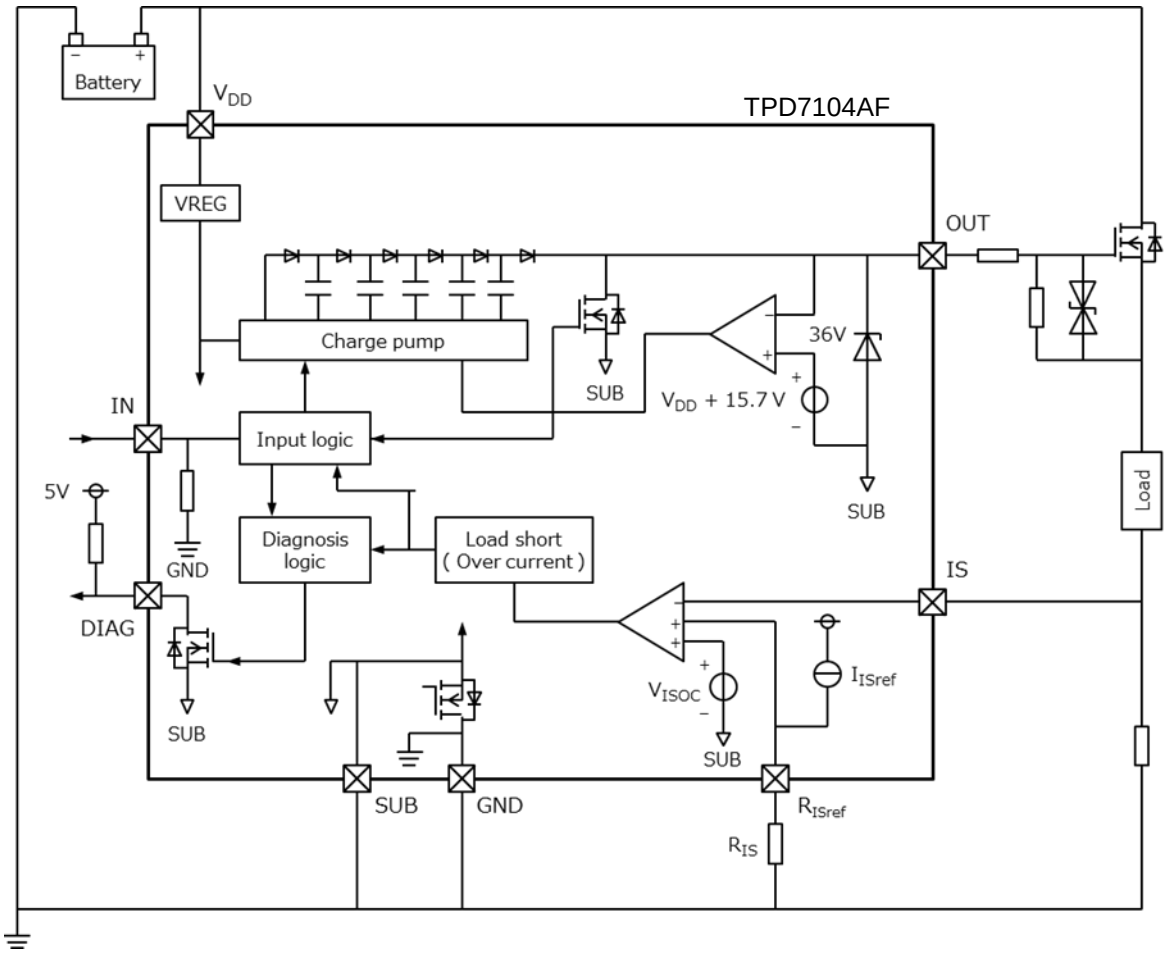


Fig. 2.1 Application example of TPD7104AF when used in the power relay part

2.2. Application example to reverse connection protection of power supply

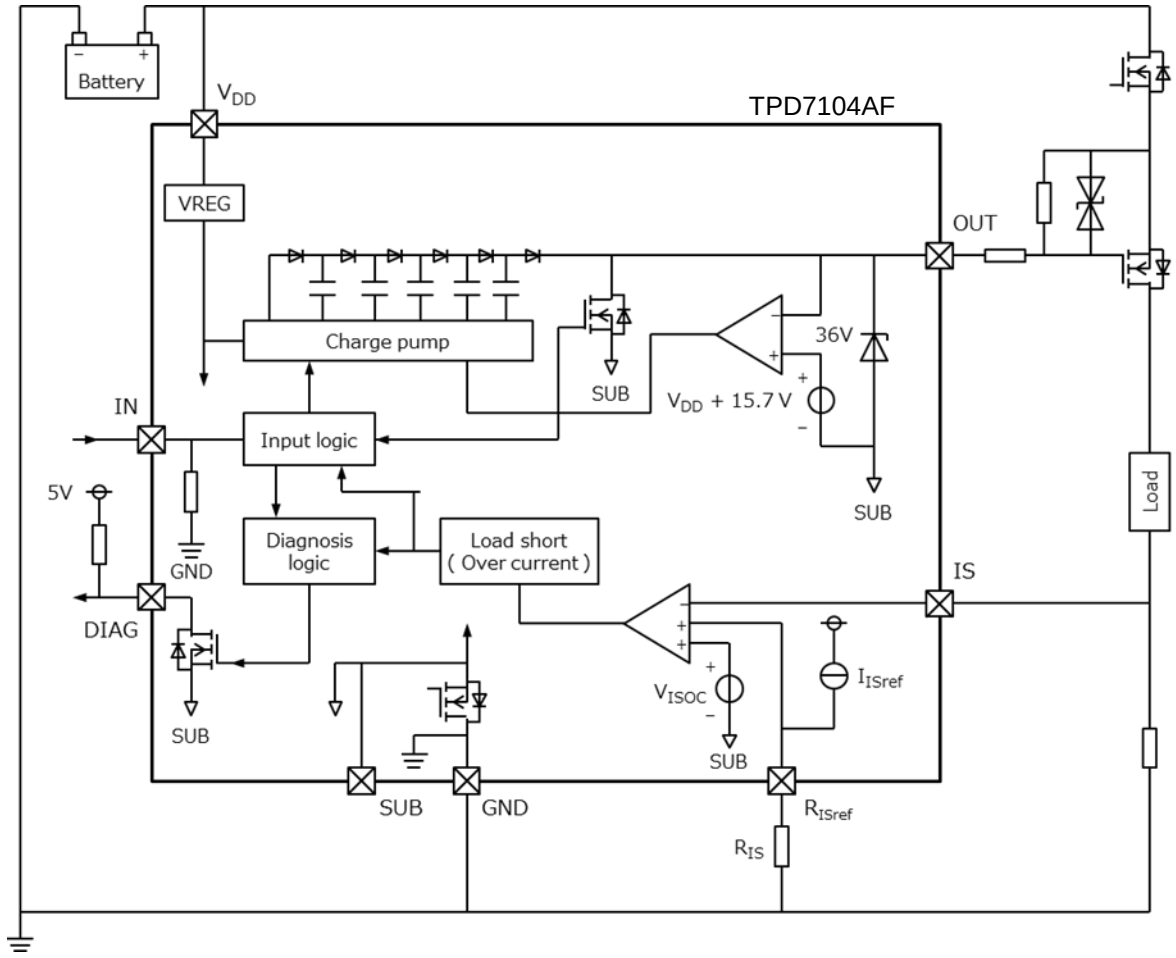


Fig. 2.2 Application example of TPD7104AF when used for power supply reverse connection protection

3. Terminal equivalent circuit diagram

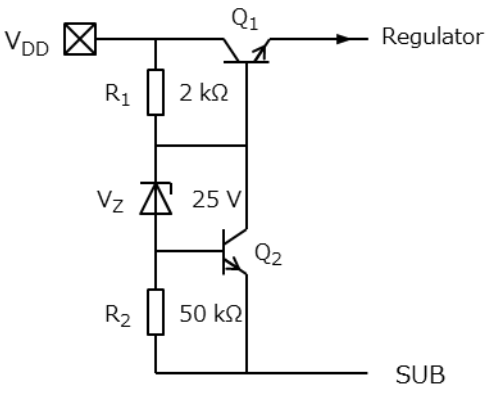


Fig. 3.1 Equivalent circuit of V_{DD} pin

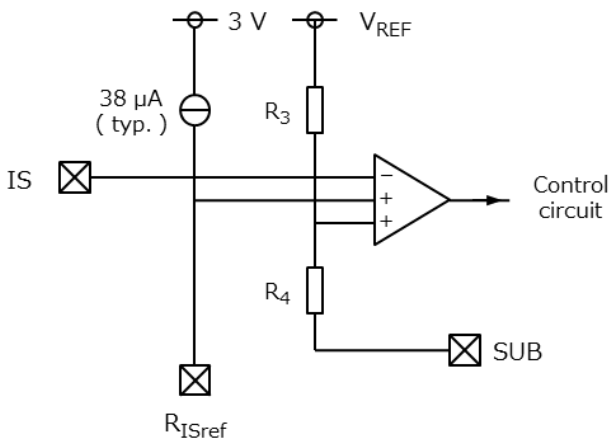


Fig. 3.2 Equivalent circuit of IS and R_{ISref} pins

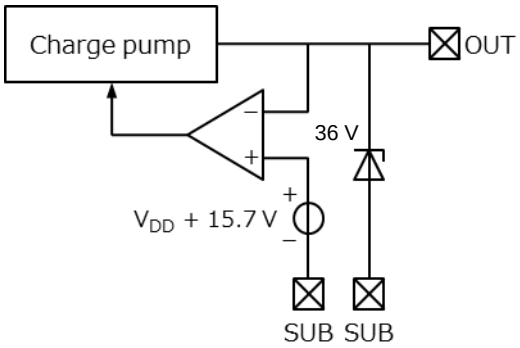


Fig. 3.3 Equivalent circuit of OUT pin

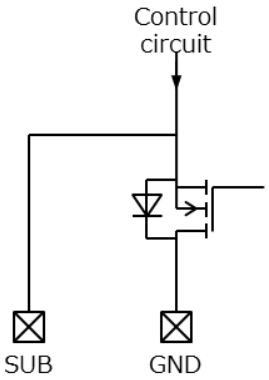


Fig. 3.4 Equivalent circuit of SUB and GND pins

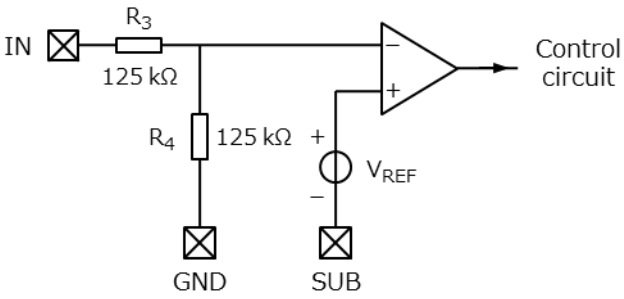


Fig. 3.5 Equivalent circuit of IN pin

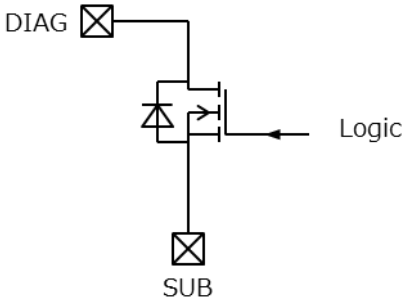


Fig. 3.6 Equivalent circuit of DIAG pin

4. Description of each circuit

4.1. Reverse power supply connection protection circuit

TPD7104AF has a power supply reverse connection protection circuit to prevent the IC from being destroyed by current flowing from the GND pin to V_{DD} pin directions when the battery is reversely connected. This circuit connects the N-channel MOSFET in the opposite direction between the GND (SUB pin) and GND pins of the control circuit inside the IC. When the power supply voltage V_{DD} and GND are at the normal potential, the gate of the power supply reverse connection protective MOSFET is driven through V_{DD}, and MOSFET is turned on. At this time, the current drawn in the IC flows from MOSFET source to the GND pin through the drain. When the battery is connected in reverse, MOSFET is turned off and the withstand voltage of this MOSFET prevents current from flowing into GND pin of the IC and protects the IC from being destroyed. When using the power supply reverse protection function, use the SUB pin in the open state. Also, when the power supply reverse protection circuit is not used, short circuit the GND and SUB terminals. Note that the external N-channel MOSFET is turned off when the battery is connected in reverse using the reverse connected power supply protective function.

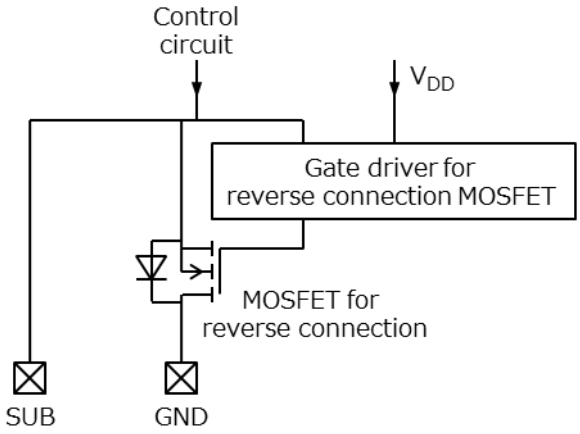


Fig. 4.1 Reverse power connection protection circuit

4.2. Load short (overcurrent) protection circuit

TPD7104AF has a load short circuit protection circuit to protect the system when the OUT terminal is shorted to GND or in an overload condition. This circuit detects the current by comparing the voltage generated in the reference voltage set in the IC (V_{ISOC}= 1.02 V (typ.)) or the resistor connected to the load short detection level setting pin R_{ISref} with the voltage of the current detection resistor R_{SHUNT} connected between the load short detection pin IS and GND. When the load short detection level setting pin R_{ISref} is open, the reference voltage becomes the load short detection voltage V_{ISOC}= 1.02 V (typ.) inside the IC. If a resistance R_{IS} is connected to the load short detection level setting pin and $R_{IS} \times I_{ISref}$ (38 μA (typ.)) < V_{ISOC}, the load short is detected by the current value determined by ($R_{IS} \times I_{ISref}$) / R_{SHUNT}. When a load short is detected, the OUT pin output is set to the "L" level, the external N-channel MOSFET is shut down, DIAG is inverted from the "L" level to the "H" level, and the OUT and DIAG operate latching to maintain that state. The latch is released by once inputting the input signal V_{IN} as the "L" level and then inputting the "H" level again. In addition, the load short detection circuit incorporates a filter circuit of 1.8 μs (designed value) to prevent malfunction due to noise, etc., and DIAG output and output voltage change with a delay time obtained by adding the transmission time of the internal circuit to this filter time.
The load short detection current is obtained by the equations (4 - 1) and (4 - 2).

When using R_{ISref} pin open

$$\text{Load short detection current} = \frac{V_{ISref}}{R_{SHUNT}} \quad \cdots (4-1)$$

When connecting a resistor to R_{ISref} pin

$$\text{Load short detection current} = \frac{I_{ISref} \times R_{IS}}{R_{SHUNT}} \quad \cdots (4-2)$$

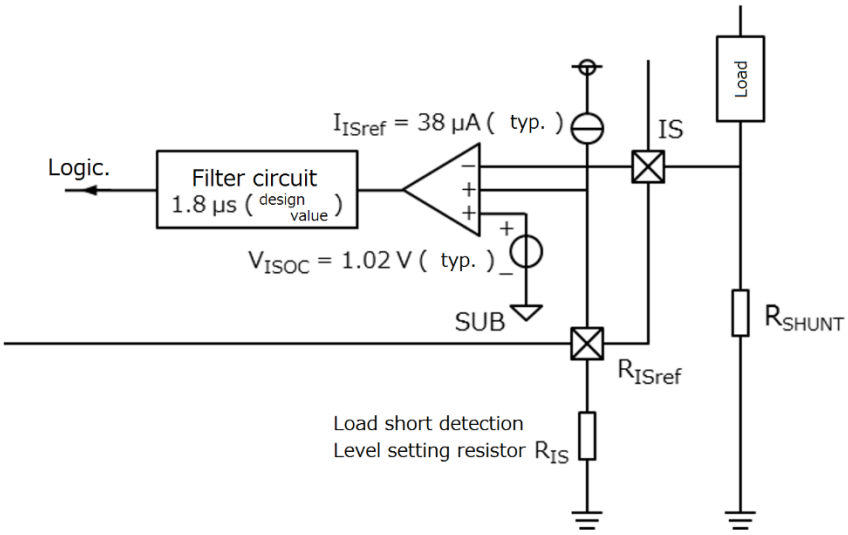


Fig. 4.2 Load short detection circuit

As shown in Fig. 4.3, V_{RISref} of the load short detection value takes precedence over that of the small value, and the reference voltage value for the load short detection becomes V_{ISOC} when the setting is such that the load short detection value becomes $R_{ISref} \times R_{IS} > V_{ISOC}$.

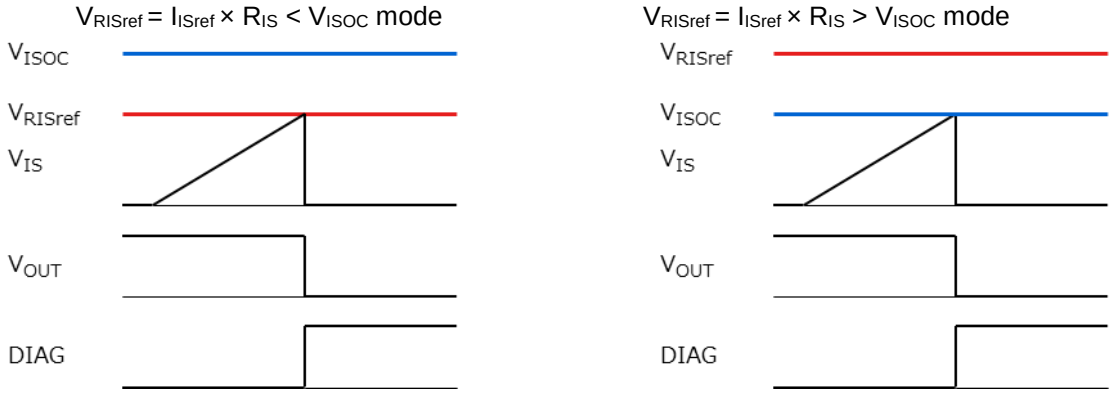


Fig. 4.3 Relationship between V_{RISref} and V_{ISOC}

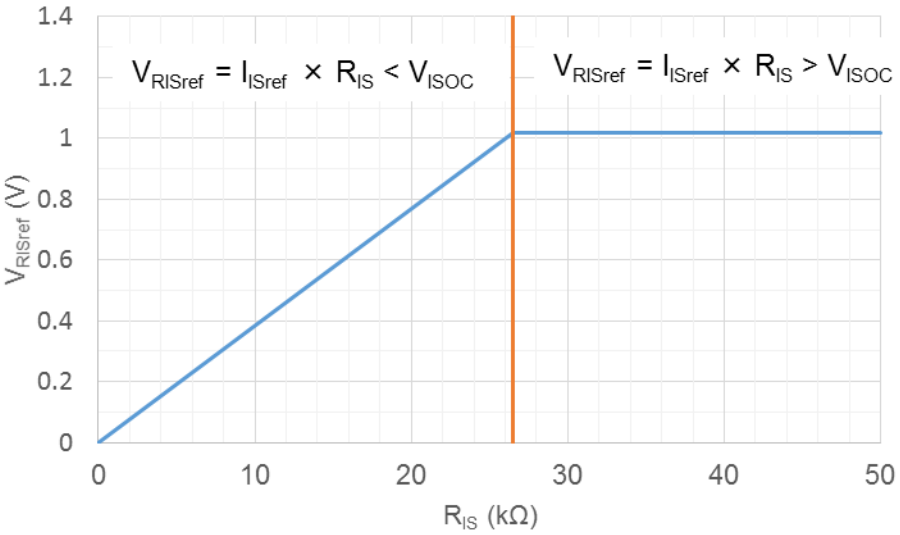


Fig. 4.4 V_{RISref} - R_{IS}

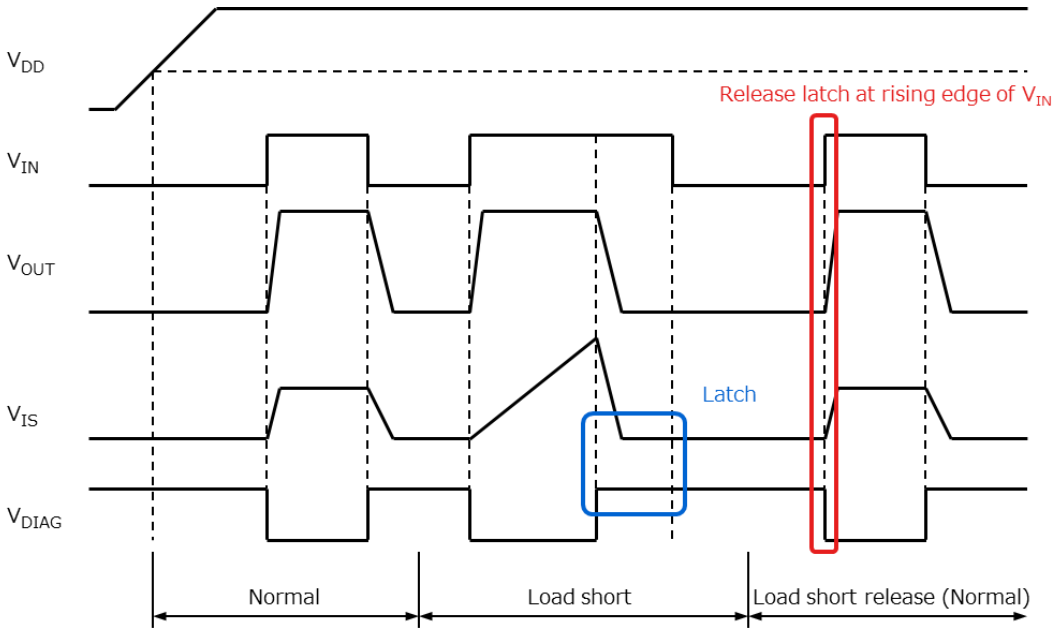


Fig. 4.5 Timing chart at load short-circuit

4.3. Charge pump circuit

The charge pump circuit is a boost power supply circuit for generating the gate-driving voltage of an external N-channel MOSFET. For high-side switches, when the N-channel MOSFET is turned on, the potential of the source is nearly equal to the supply voltage. To maintain the on state, the gate must be supplied with a supply voltage of +10 to 15 V and a voltage greater than or equal to the supply voltage. A charge pump circuit is a circuit that generates a voltage that is greater than or equal to this power supply voltage in the IC. TPD7104AF employs a Dickson type charge-pump circuit composed of diodes, capacitors, and inverter circuits built in ICs as shown in Fig. 4.6. The boosted voltage $V_{CP(OUT)}$ is obtained by equations (4 - 3).

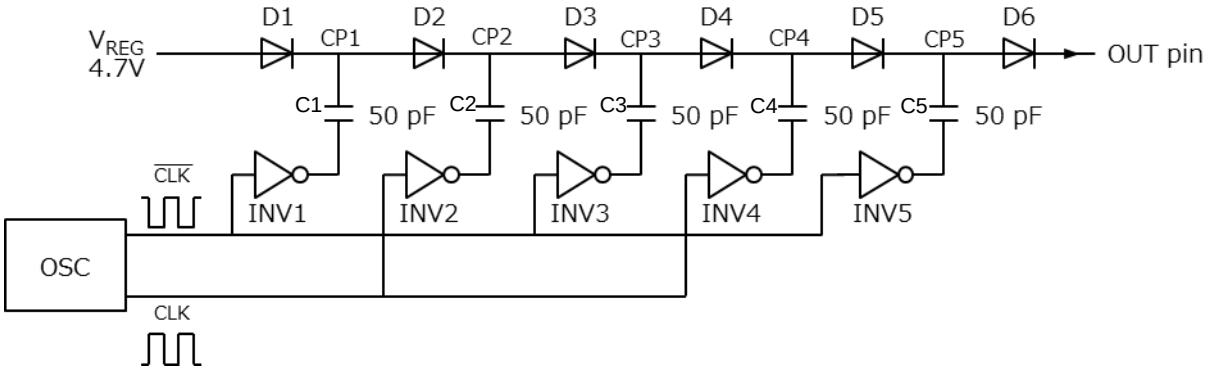


Fig. 4.6 Charge pump equivalent circuit

$$V_{CP(OUT)} = N \times (V_{REG} - V_F) \quad \cdots (4 - 3)$$

N	: Number of stages
V_{REG}	: Power supply voltage for control circuit (V)
V_F	: Diode forward voltage (V)

Fig. 4.7 describes the operation of the charge pump circuit of Dickson method. Let us assume that the voltage amplitude to CLK and $\overline{CLK}$ are equal to the voltage amplitude to V_{REG}.

Operation 1

When $\overline{CLK}$ is "L" level, capacitor C1 is charged from V_{REG} through diode D1, causing the voltage across C1 to become V_{REG} - V_F and voltage across CP1 swings between $2V_{REG}$ - V_F and V_{REG} - V_F.

Operation 2

When $\overline{CLK}$ is "H" level and CLK is at the "L" level, the charge stored in C1 charges C2 through D2, causing the voltage across C2 to $2V_{REG}$ to $2V_F$, and voltage across CP2 swings between $3V_{REG}$ -$2V_F$ and $2V_{REG}$ - $2V_F$.

Operation 3

When $\overline{CLK}$ is "L" level and CLK reaches "H" level, the charge stored in C2 charges C3 via D3, causing the voltage across C3 to $3V_{REG}$ to $3V_F$, and voltage across CP3 swings between $4V_{REG}$ - $3V_F$ and $3V_{REG}$ - $3V_F$.

Operation 4

When $\overline{CLK}$ is "H" level and CLK reaches "L" level, the charge stored in C3 charges C4 via D4 and the voltage across C4 is $4V_{REG} - 4V_F$, and voltage across CP4 swings between $5V_{REG} - 4V_F$ and $4V_{REG} - 4V_F$.

Operation 5

When $\overline{CLK}$ is "L" level and CLK reaches "H" level, the charge stored in C4 is charged via D5 to C5 and the voltage across C5 is $5V_{REG} - 5V_F$, and voltage across CP5 swings between $6V_{REG} - 5V_F$ and $5V_{REG} - 5V_F$.

Operation 6

The charge stored in C5 drives the gates of the external N-channel MOSFET with the voltage eventually boosted to $6 \times (V_{REG} - V_F)$ via D6.

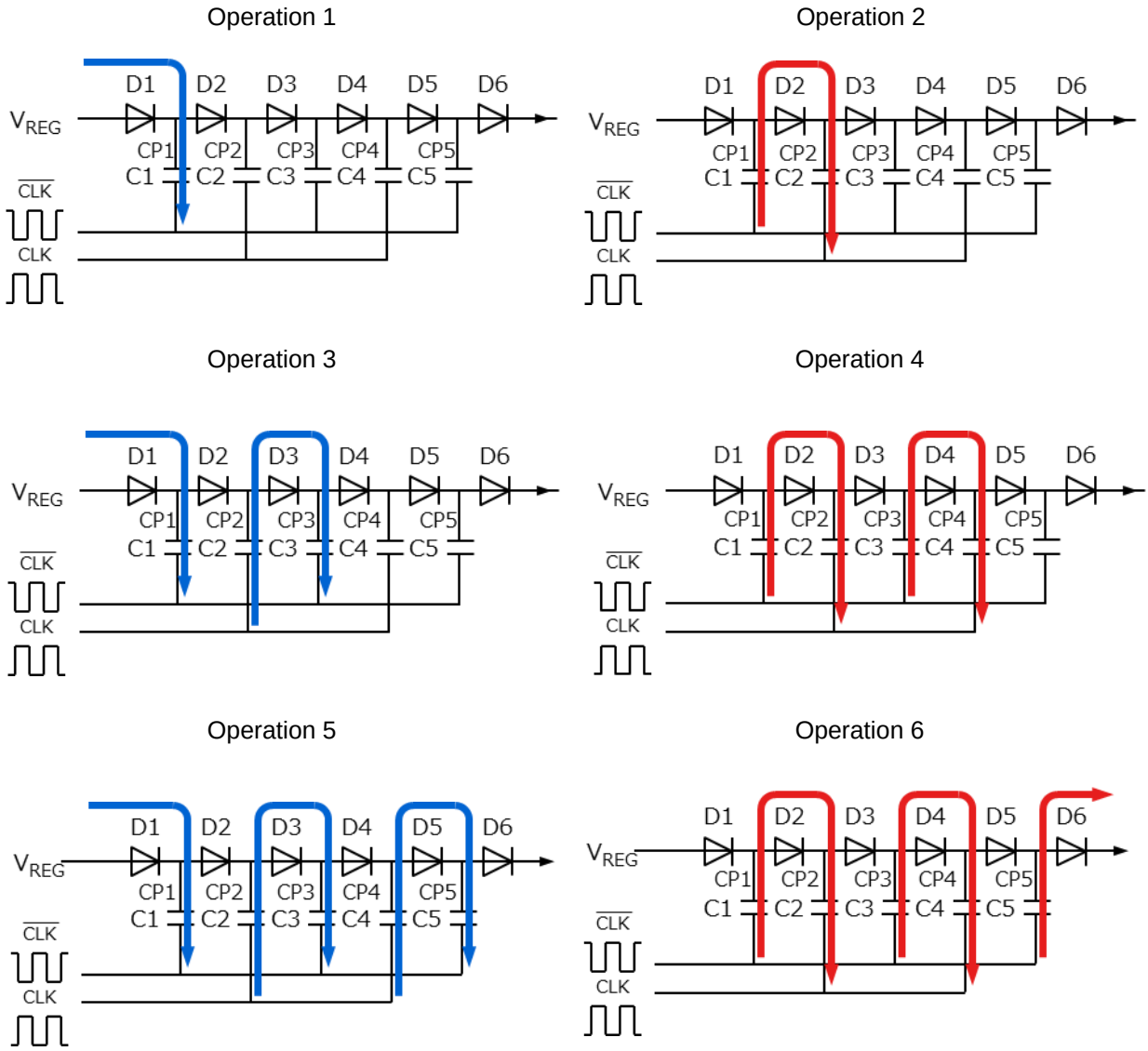


Fig. 4.7 Charge pump circuit operation

The voltage waveforms at the nodes of the charge pump circuit are as shown in Fig. 4.8. When V_{REG} = 4.7 V, V_F = 0.7 V, the voltage boosting voltage obtained from Eq. (4 - 3) becomes $V_{CP(OUT)}$ = 24 V, which is almost the same voltage as $V_{CP(OUT)}$ shown in Fig. 4.8.

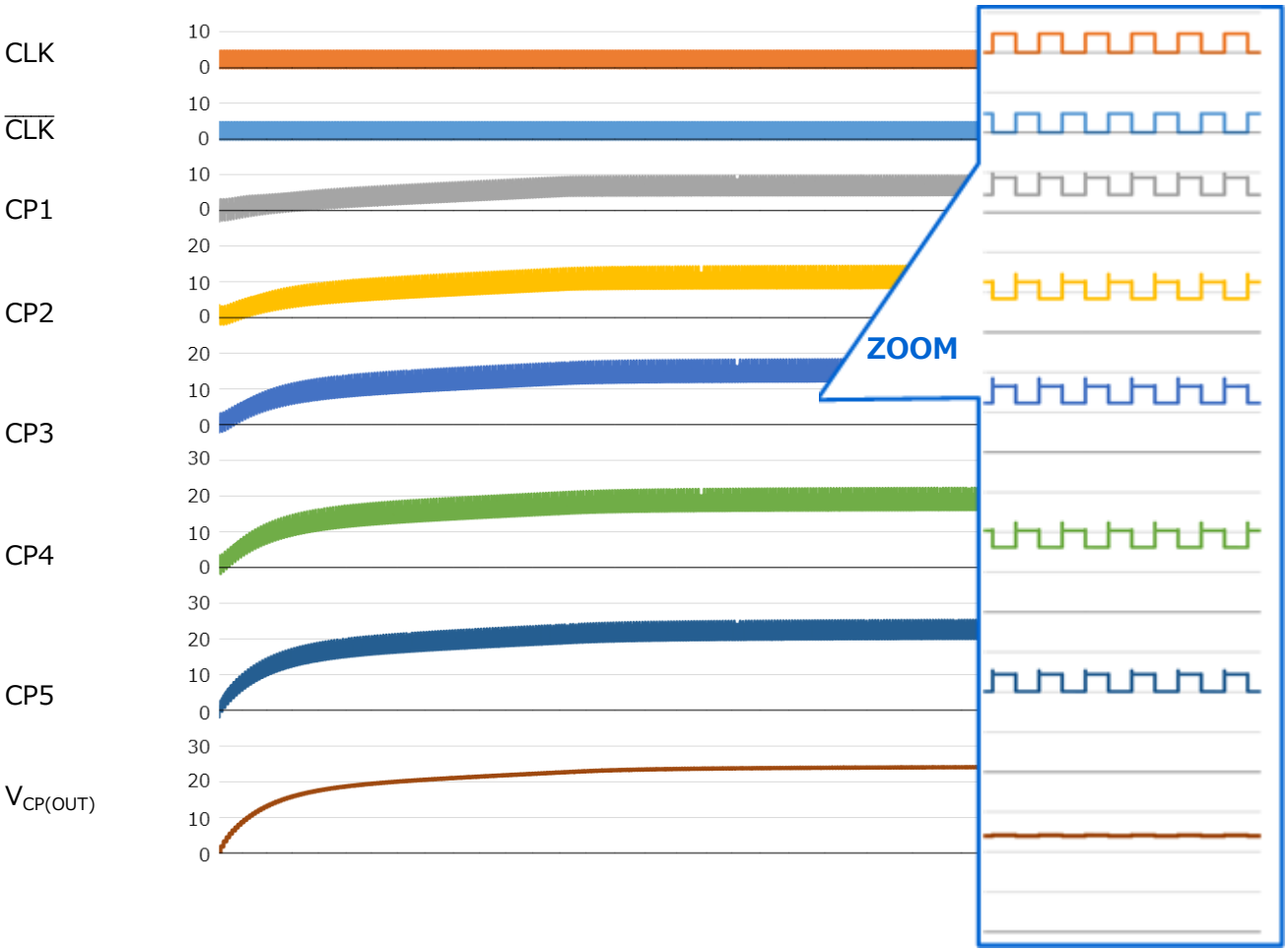


Fig. 4.8 Operation waveforms of each node in charge pump circuit

4.4. Charge pump voltage monitor circuit

A charge pump voltage monitor circuit is incorporated in TPD7104AF to prevent the voltage boosted by the charge pump circuit from abnormally rising due to external noises and other factors, and from exceeding the gate-to-source voltage rating of the external N-channel MOSFET. This circuit stops the charge pump circuit so that the voltage does not rise further if the voltage boosted by the charge pump rises above the supply voltage V_{DD}+ 15.7 V, 36 V Zener diode is also incorporated between the OUT and SUB terminals to protect the internal elements.

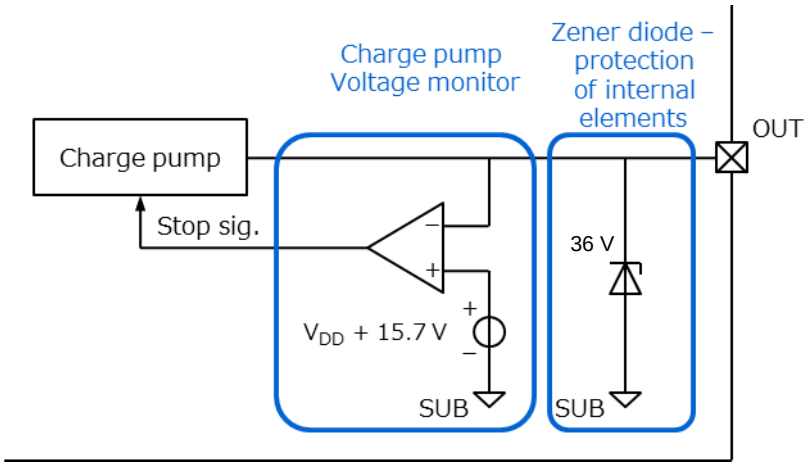


Fig. 4.9 Charge pump voltage monitor circuit diagram

4.5. Overvoltage protection

To prevent excessive voltage from being applied to V_{DD} pin and exceeding the withstand voltage of the control circuits inside the IC, a series regulator as shown in Fig. 4.10 is incorporated in V_{DD} terminals. This series regulator supplies power to each control circuit from the power supply for the control circuit connected to the subsequent stage. The output voltage of this series regulator is given by equation (4 – 4).

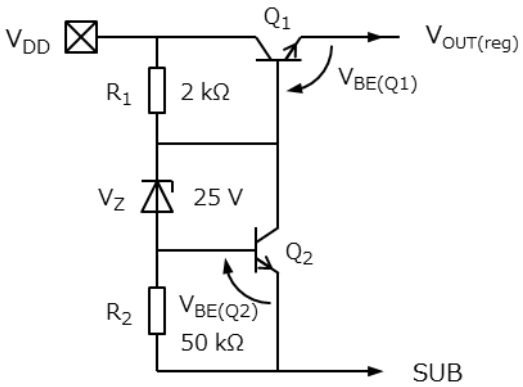


Fig. 4.10 Overvoltage protection circuit

$$V_{OUT(reg)} \approx V_Z + V_{BE(Q2)} - V_{BE(Q1)} \qquad \cdots (4 - 4)$$

Fig. 4.11 shows an operation diagram of this circuit. When the power supply voltage V_{DD} increases, the output voltage of this series regulator is clamped at about 25 V.

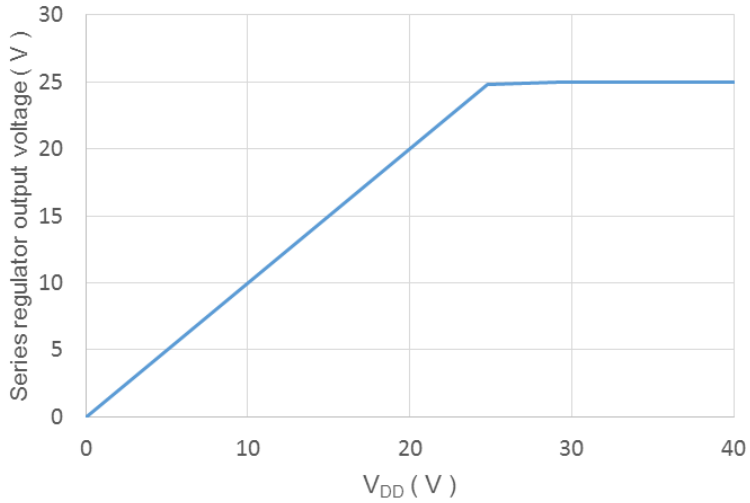


Fig. 4.11 Image of overvoltage protection circuit operation

5. Electrical characteristics measurement circuit diagram

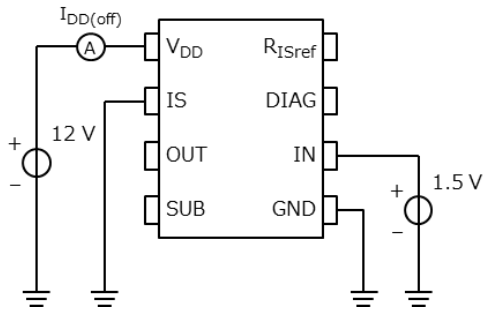


Fig. 5.1 Supply current measurement circuit $I_{DD(off)}$

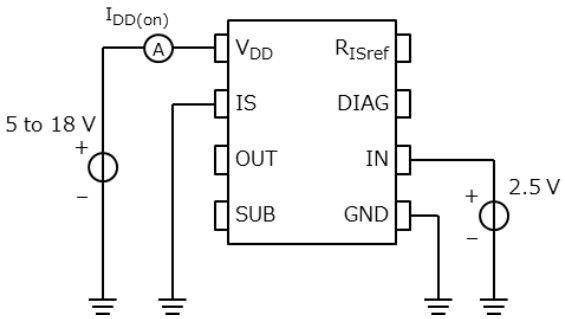
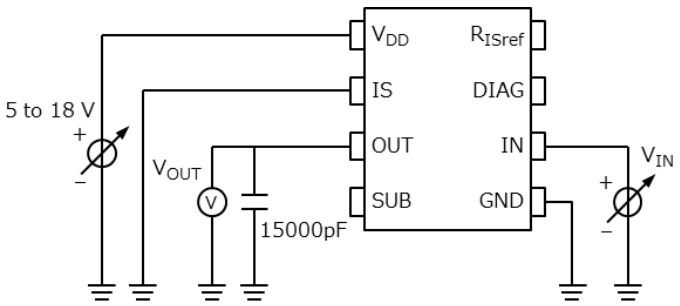


Fig. 5.2 Supply current measurement circuit $I_{DD(on)}$



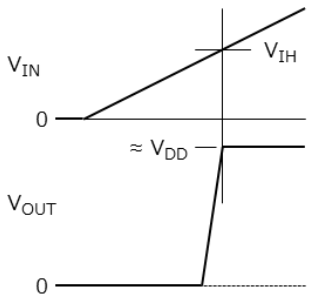


Fig. 5.3 Input voltage measurement circuit V_{IH}

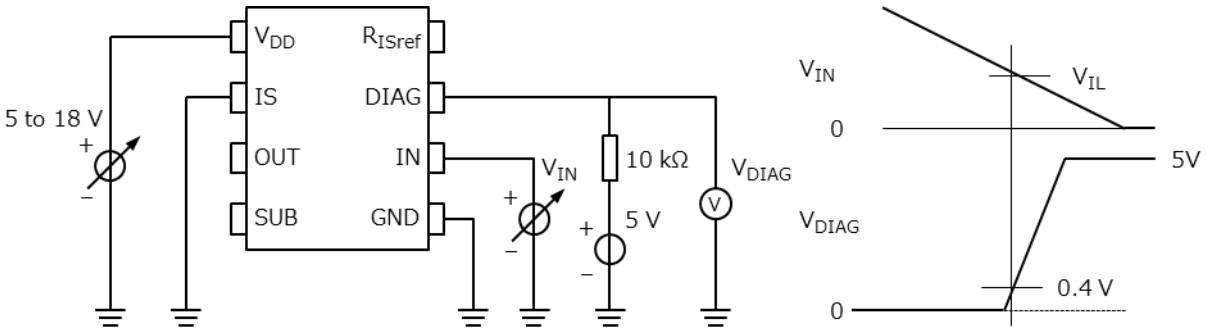


Fig. 5.4 Input voltage measurement circuit V_{IL}

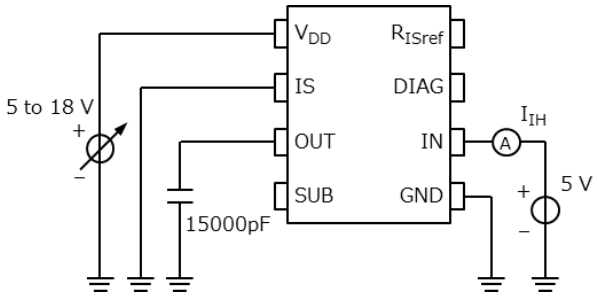


Fig. 5.5 Measurement circuit I_{IH}

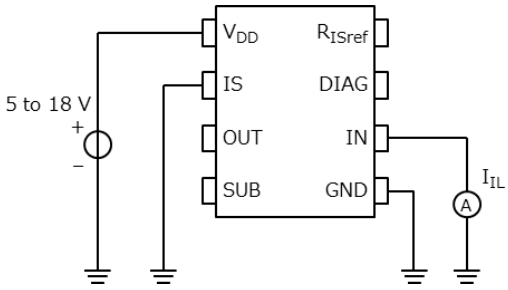


Fig. 5.6 Measurement circuit I_{IL}

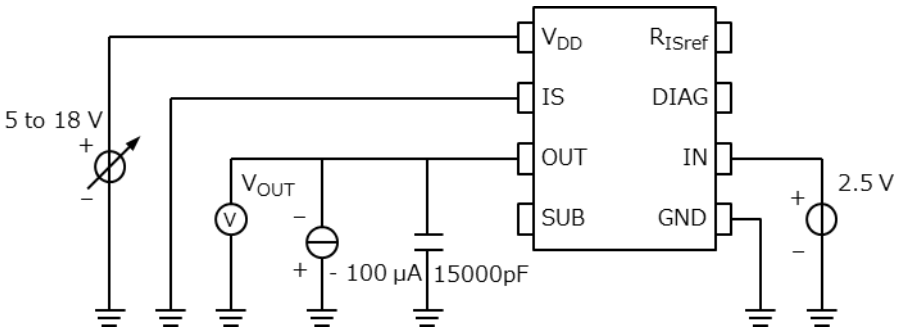


Fig. 5.7 Output voltage measurement circuit $V_{OUT1,2}$

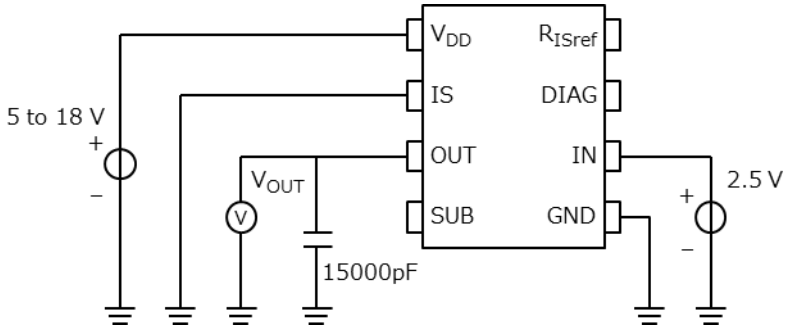


Fig. 5.8 Output clamp voltage measurement circuit V_{clamp}

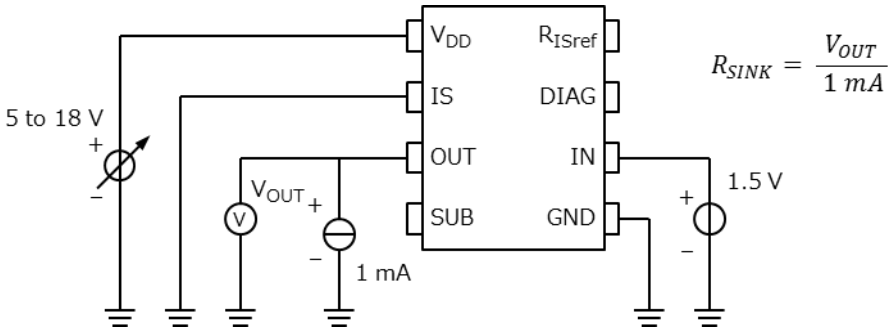


Fig. 5.9 Output resistance measurement circuit R_{SINK}

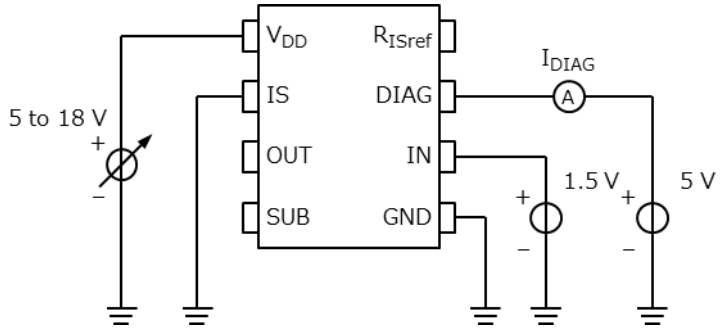


Fig. 5.10 Diagnosis output leakage current measurement circuit I_{DIAGH}

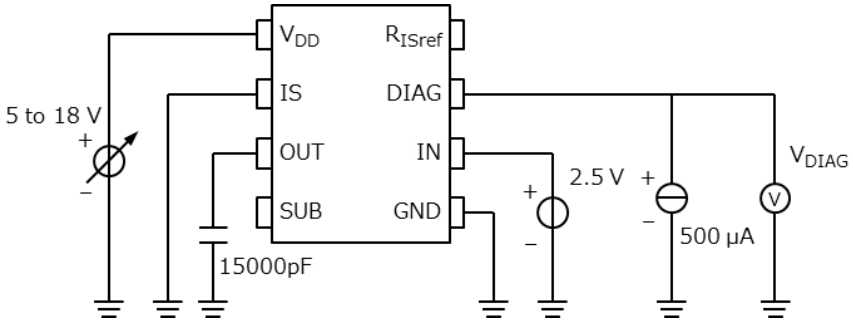


Fig. 5.11 Diagnosis output voltage measurement circuit V_{DIAGL}

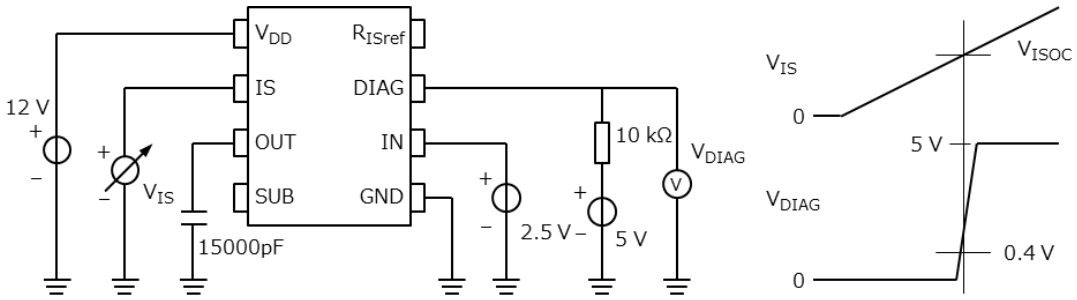


Fig. 5.12 Short circuit detection voltage measurement circuit V_{ISOC}

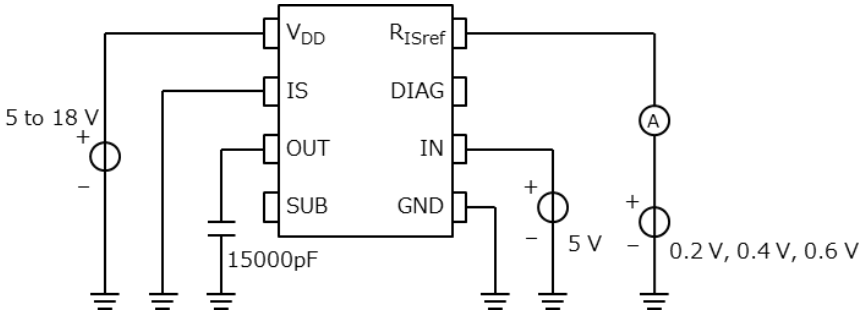


Fig. 5.13 R_{ISref} pin output current measurement circuit $I_{ISref(1),(2),(3)}$

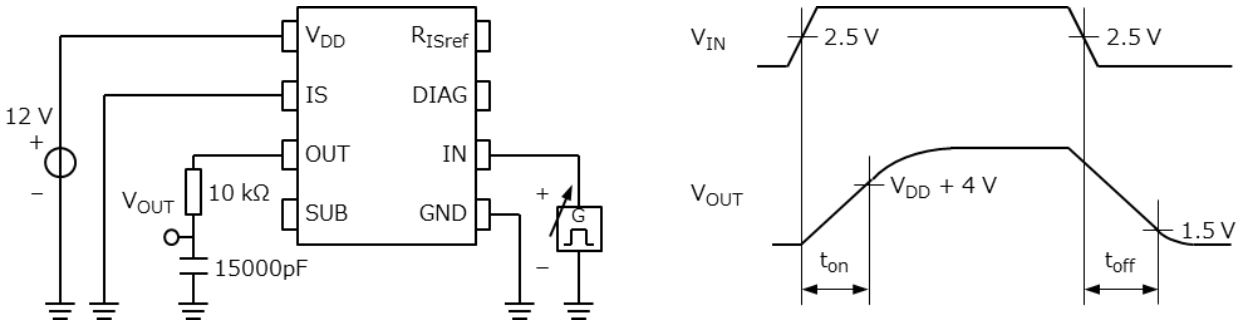


Fig. 5.14 Switching time measurement circuit t_{on} , t_{off}

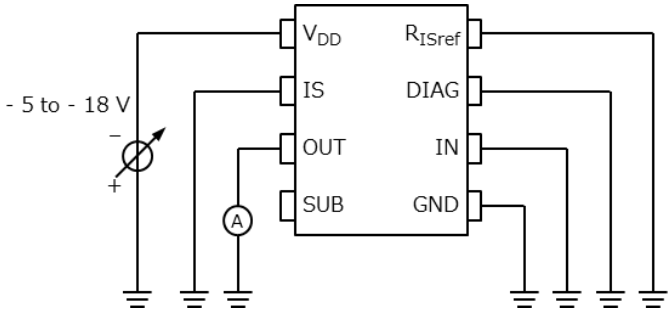


Fig. 5.15 Measurement circuit $I_{REV(1),(2)}$ when the power supply is connected in reverse

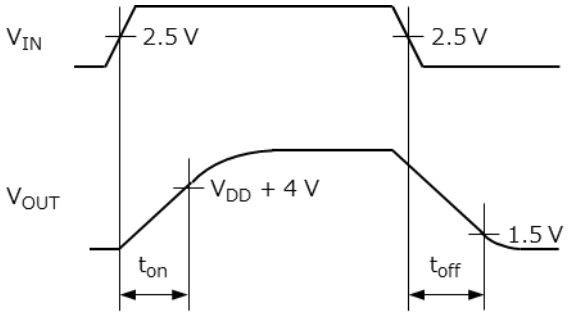
6. Definition and terminology

6.1. Absolute maximum rating

Term	Symbol	Description
Power supply voltage (DC)	$V_{DD(1)}$	A dc-voltage rating that does not destroy, deteriorate characteristics, or reduce reliability when applied to a V_{DD} terminal.
Power supply voltage (pulse)	$V_{DD(2)}$	Pulsed voltage rating that does not cause the ICs to break, decrease characteristics or reduce reliability when applied to V_{DD} terminals.
Reverse connection of power supply	$-V_{DD(3)}$	Voltage rating that does not cause the IC to break, deteriorate characteristics or reduce reliability even when a positive power supply is applied to the GND pin and a negative power supply is applied to V_{DD} pin.
Input voltage	V_{IN}	Voltage rating at which ICs will not cause breakdown, degradation of characteristics or reliability deterioration even when applied to V_{IN} terminals.
Output source current	$I_{OUT(-)}$	A current rating at which ICs can flow out of output terminals that will not cause damage, deterioration of characteristics, or loss of reliability.
Output sink current	$I_{OUT(+)}$	The current rating at which the IC can be drawn from the output terminals that will not cause damage, deterioration of characteristics, or deterioration in reliability.
IS Voltage	V_{IS}	Voltage rating that does not cause the IC to break, deteriorate characteristics or reduce reliability when applied to the IS pin.
Diagnostic outputs (DIAG) voltages	V_{DIAG}	Voltage rating at which ICs will not cause breakdown, degradation of characteristics or reliability deterioration even when applied to DIAG terminals.
Diagnostic outputs (DIAG) current	I_{DIAG}	A current rating at which ICs can flow to DIAG terminals that will not cause damage, degradation of characteristics, or loss of reliability.
Power dissipation	P_D	Maximum allowable power consumption that does not cause damage to the IC over the entire operating range.
Operating temperature	T_{opr}	Ambient temperature range for normal operation of the IC.
Junction temperature	T_j	Maximum junction temperature at which operation of the IC is allowed.
Storage temperature	T_{stg}	Ambient temperature range that can be stored or transported without applying voltage.

6.2. Electrical characteristics

Term	Symbol	Description
Operating supply voltage	$V_{DD(opr)}$	The power supply voltage range within which the normal operation and electrical characteristics of the IC are guaranteed at the prescribed junction temperature range.
Supply current	$I_{DD(off)}$	Current value that flows to V_{DD} pin when the input voltage V_{IN} is kept at a voltage lower than V_{IL} at the preset junction temperature and the operation of the IC is turned off.
Supply current	$I_{DD(on)}$	Current value that flows to V_{DD} pin when the input voltage V_{IN} is kept at a voltage higher than V_{IH} and the IC operation is turned on in the preset junction temperature range.
High-level input voltage	V_{IH}	The minimum voltage at the input terminal V_{IN} that ensures that the internal control circuitry operates properly and the external N-channel MOSFET is turned on at the preset junction temperature range.
Low-level input voltage	V_{IL}	The maximum voltage at the input terminal V_{IN} that ensures that the internal control circuitry operates normally and turns off the external N-channel MOSFET at the preset junction temperature.
Input current	I_{IH}	Current value that flows into V_{IN} when the voltage specified by the measuring condition is applied to the input terminal V_{IN} at the predetermined junction temperature range.
Input current	I_{IL}	Current value that flows out of V_{IN} when the voltage specified by the measuring condition is applied to the input terminal V_{IN} at the predetermined junction temperature range.
High level output voltage	V_{OUTH1} V_{OUTH2}	Voltage value output to the output terminal OUT when the voltage and current specified by the measurement conditions are applied in the preset junction temperature range.
Output clamp voltage	V_{clamp}	Voltage clamp value of the output terminal OUT when the voltage specified by the measurement conditions is applied at the preset junction temperature range.
Output resistance	R_{SINK}	Resistance value between the output terminal OUT and SUB terminal when voltage and current specified by the measurement conditions are applied at the preset junction temperature range.
Diagnostic output leakage current	I_{DIAGH}	Leakage current that flows to the diagnostic output terminal DIAG when the voltage specified by the measurement conditions is applied in the preset junction temperature ranges.
Diagnostic output voltage	V_{DIAGL}	The on-voltage value of the diagnostic output pin DIAG when the voltage and current specified by the measuring conditions are applied at the predetermined junction temperature ranges.
Load short detection voltage	V_{ISOC}	Load short detection reference voltage value in the IC when the voltage specified by the measurement conditions is applied in the preset junction temperature range.
R_{ISref} terminal output current	I_{ISref}	Voltage value generated at the load short detection level-setting pin when the voltage specified by the measurement conditions is applied in the preset junction temperature range.

Term	Symbol	Description
Switching time	t_{on} t_{off}	Delay time from 50 % of the rising edge of the input voltage to +4 V of the rising V_{DD} of the output voltage and from 50 % of the falling edge of the input voltage to 1.5 V of the falling edge of the output voltage. 
Output current for reverse connection	$I_{REV(1)}$ $I_{REV(2)}$	Current value that flows to the output terminal OUT when the voltage specified by the measurement condition is applied at the preset junction temperature range.

7. Evaluation board

7.1. Appearance of evaluation board

We prepare this product and an evaluation board that mounts peripheral devices. This function allows you to check the function and the protection diagnosis function at the actual load.

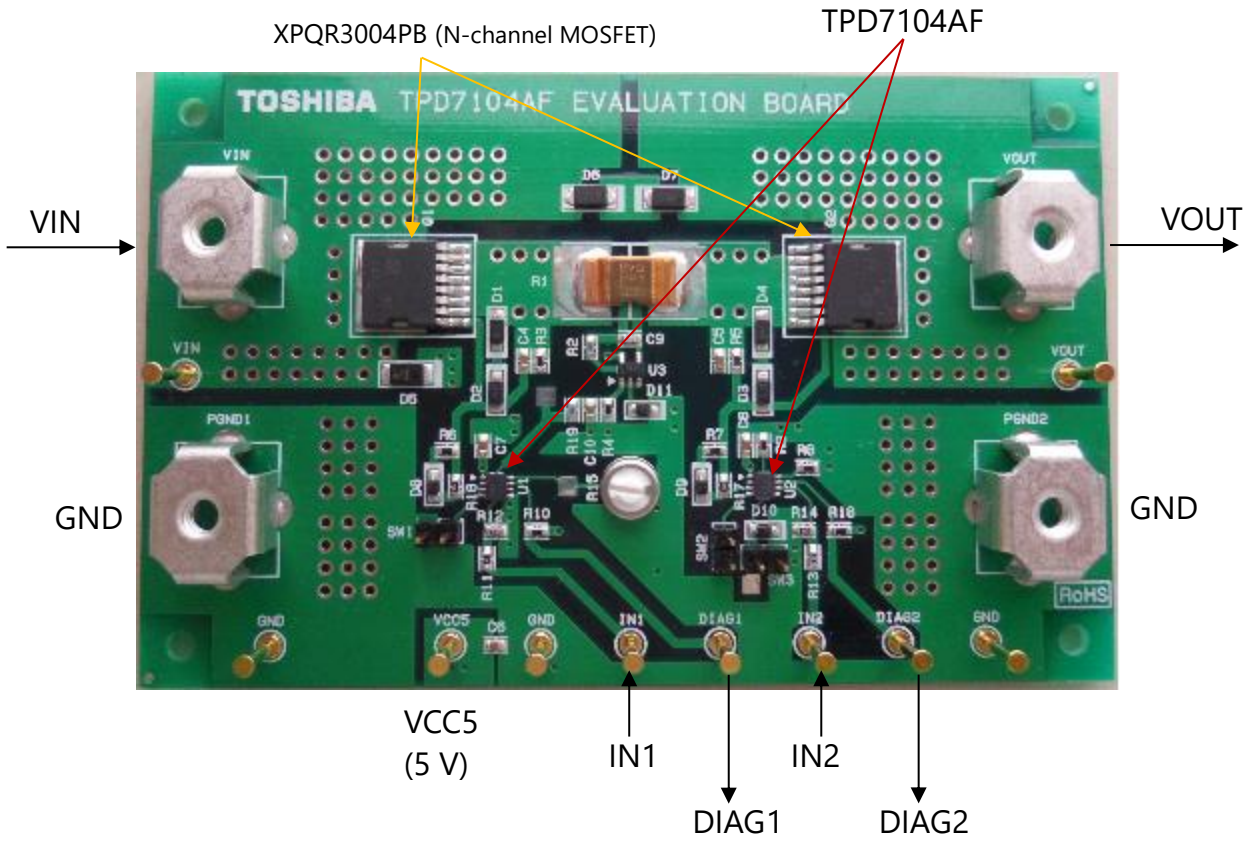


Fig. 7.1 TPD7104AF evaluation board

7.2. Circuit diagram for evaluation board

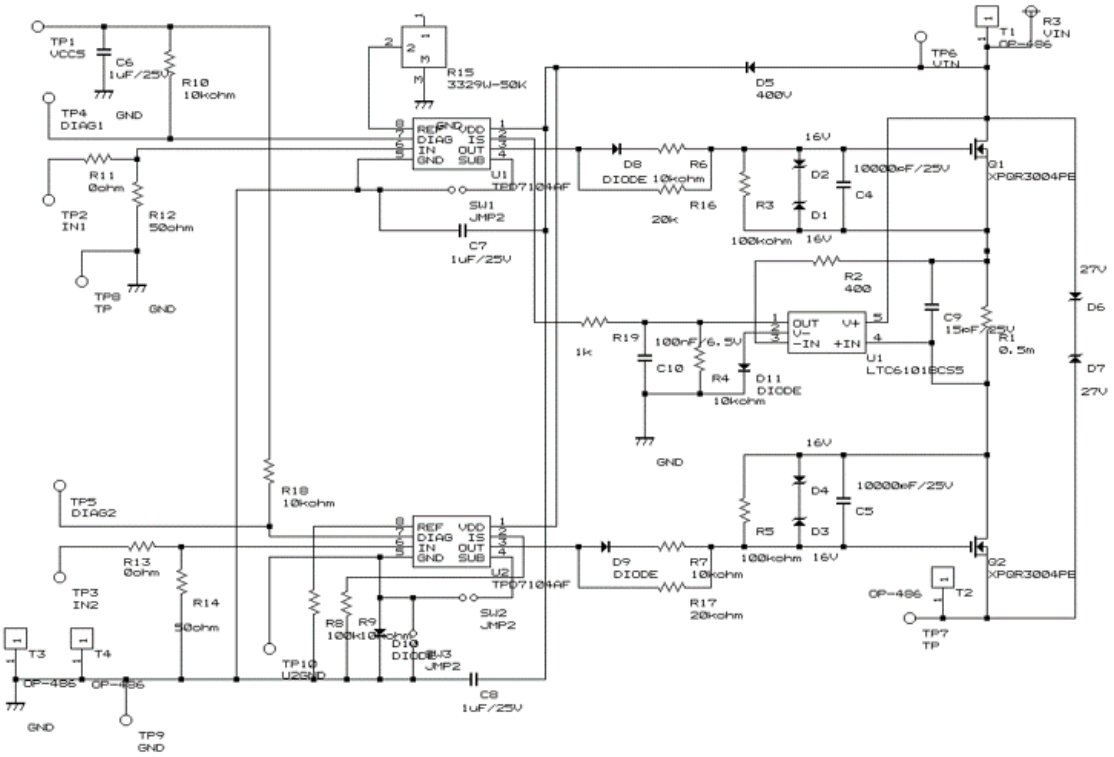


Fig. 7.2 Circuit diagram of TPD7104AF evaluation board

7.3. Bill of materials

Table 7.1 BOM list

No.	item	p/n	maker	spec.	location	PKG	QTY	Note.
1	IC	TPD7104AF	Toshiba	driver IC	U1,U2	PS-8	2	
2		LTC6101HVACS5	LT	sense amp.	U3	TSOT-23	1	
3	Power MOS	XPQR3004PB	Toshiba	Nch/40V	Q1,Q2	L-TOGL	2	
4	R	BVS-M-R0005-1.0	Isabellenhuette	0.5mohm	R1		1	
5				300ohm	R2	1608	1	
6		ERJP03F1003V	Panasonic	100kohm	R3,R5,R8	1608	3	
7		ERJP03F1002V	Panasonic	10kohm	R4,R6,R7,R9,R10,R18	1608	5	
8		ERJ3GEY0R00V	Panasonic	0ohm	R11,R13	1608	2	
9		RR0816Q-510-D	Susumu	51ohm	R12,R14	1608	2	
10		3329H	BOURNS	0 - 50kohm	R15	-	1	
11		CR0603-FX-2002ELF	BOURNS	20kohm	R16,R17	1608	2	
12				1kohm	R19	1608	1	
13	C	GRM155B11E103KA01D	Murata	10000pF/25V	C4,C5	1005	2	
14		GRM188B31E105KA	Murata	1uF/25V	C6,C7,C8	1608	3	
15		C0603CH1E150J	TDK	15pF/25V	C9	0603	1	
16				100nF	C10	1608	1	
17	TP	ST2-2-2			TP1～TP8		8	
18	D	CRZ16	Toshiba	16V Zdi	D1,D2,D3,D4	S-FLAT	4	
19		CMG06A	Toshiba	400V/1A	D5	M-FLAT	1	
20		CMZ27	Toshiba	27V/1W	D6,D7	S-FLAT	2	
21		1SS352	Toshiba	80V/100mA	D8,D9,D10,D11	SOD-323	4	
22	terminal	OP-486	Osada	40A DC max	T1,T2,T3,T4		4	
23	jumper	XJ8T	Omron	2 poles/2.54mm	SW1,SW2,SW3	-	3	

7.4. **Board layout**

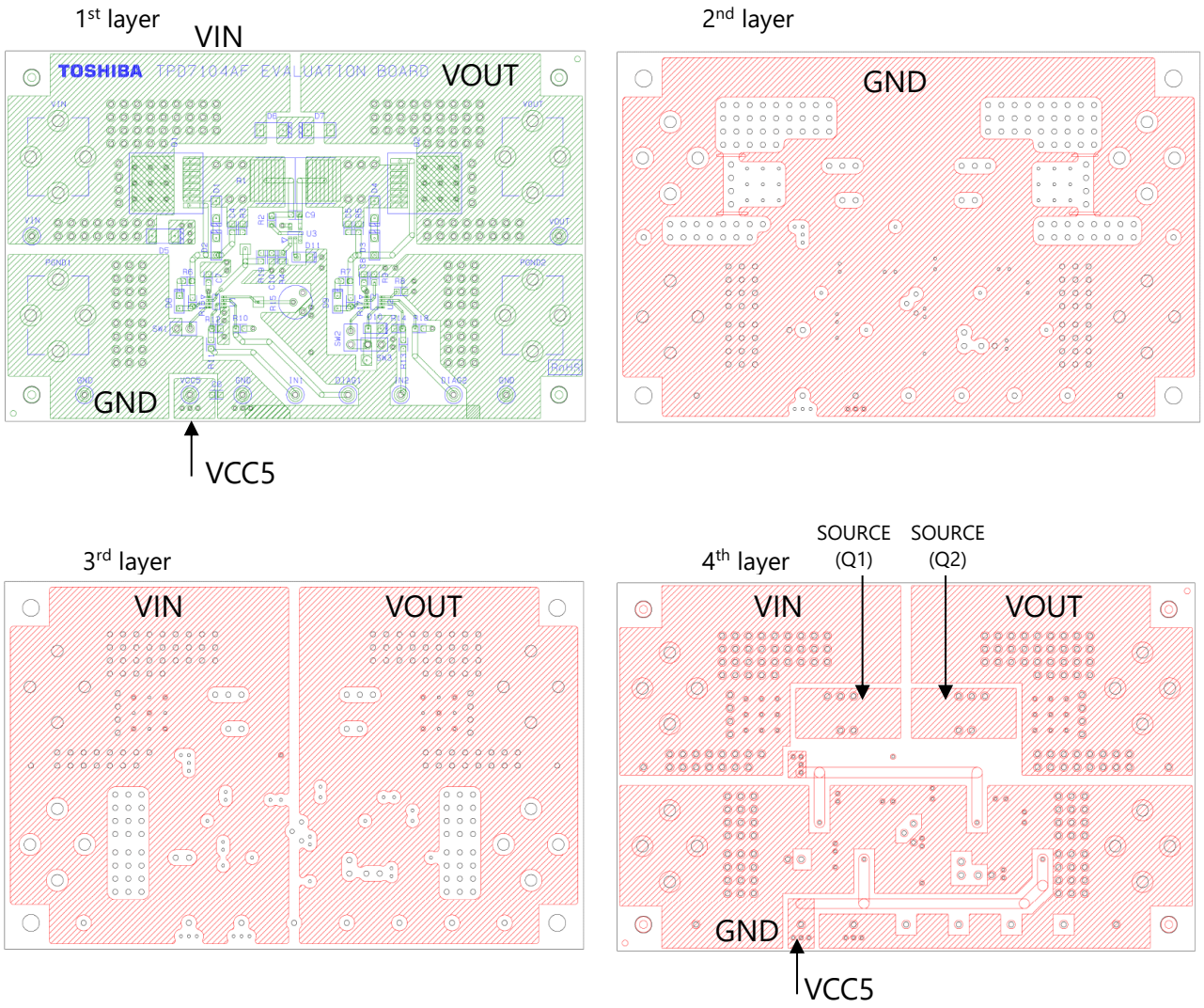


Fig. 7.3 Layout of TPD7104AF evaluation board

Points to note in the description

1. Block diagram
   Function blocks, circuits, constants, etc. in the block diagram are partially omitted or simplified for explanation of functions.

2. Equivalent circuit
   The equivalent circuit may be partially omitted or simplified for explanation of the circuit.

IC usage consideration

Notes on handing of ICs

The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Exceeding the maximum rating may cause destruction, damage and deterioration, and may result in injury due to explosion or burning.

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