Thermal Design for Schottky Barrier Diodes (SBDs) in the US2H Package

Outline:

The US2H package is a thermally enhanced package specifically designed for diodes. This application note describes the advantages of Schottky barrier diodes (SBDs) in the US2H package as well as the power losses of and the thermal design for SBDs.

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1. Introduction

Electronic devices are becoming increasingly sophisticated while becoming progressively smaller and less power-consuming. This is driving the need for semiconductor devices that are physically smaller, consume less power, and dissipate heat more efficiently than the current devices. Toshiba has developed Schottky barrier diode (SBD) chips suitable for use in rectification circuits of DC-DC converters and reverse-current blocking circuits for electronic device applications. We are expanding the lineup of SBDs in the small, thermally enhanced US2H package.

This application note compares the results of heat dissipation simulations of the CUHS15F40 in the US2H package and the CUS10F40 in the equivalently sized USC (SOD-323) package. It describes the heat dissipation performance of the US2H package and discusses key considerations for using SBDs, including power losses caused by reverse current and thermal design for efficient heat dissipation. It also describes the structure and characteristics of SBDs, their power losses, and the considerations for thermal design.

2. Overview of the US2H and USC packages

The US2H is a small, thermally enhanced package with a backside electrode called an exposed thermal pad (E-pad). On the other hand, the electrodes of the USC package have a gull-wing , which has the advantages of easy mounting and good mounting visibility. Figure 2.1 compares the outline dimensions of the US2H and USC packages.

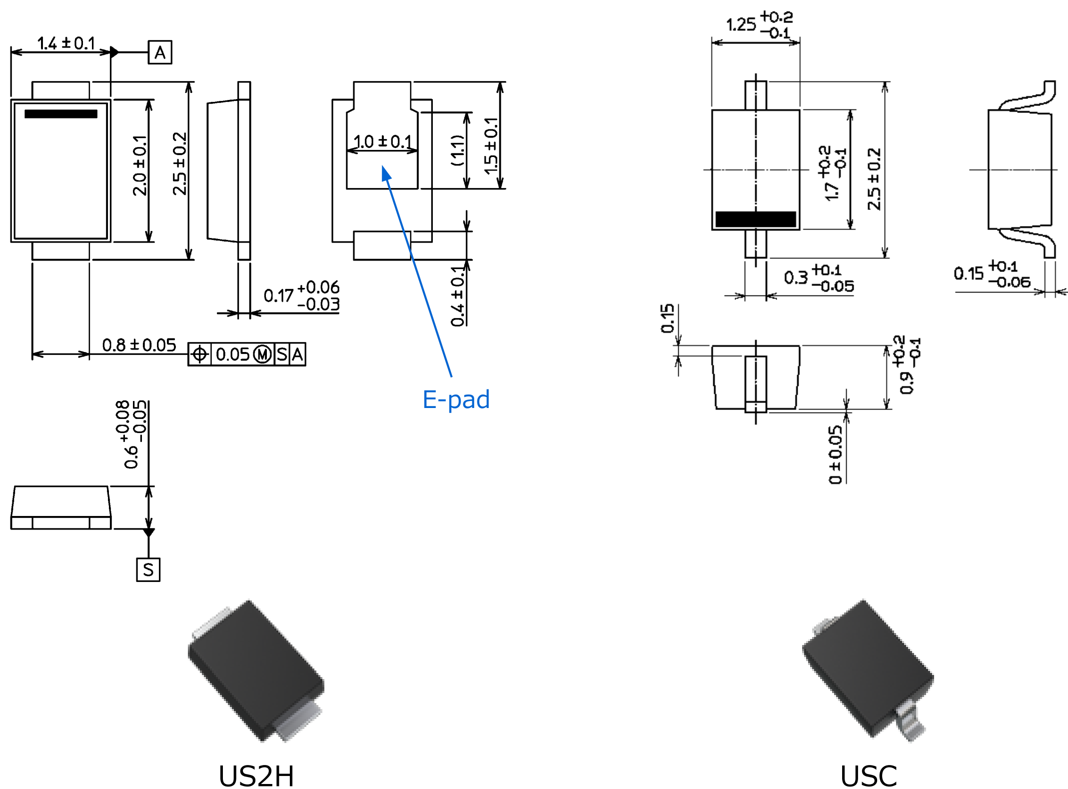

Figure 2.1 Comparison of the outline dimensions of the US2H and USC packages

3. Heat dissipation advantages of the US2H package

Table 3.1 compares the absolute maximum ratings of the CUHS15F40 in the US2H package and the CUS10F40 in the USC package, and Table 3.2 compares their electrical characteristics. CUHS15F40 and CUS10F40 have similar characteristics, although there are differences in average rectified current and junction voltage characteristics.

Table 3.1 Comparison of the absolute maximum ratings of the CUHS15F40 and CUS10F40

Absolute maximum ratings (Unless otherwise specified, T_a=25°C)

Characteristic	Symbol	Note	Ratings		Unit
			CUHS15F40	CUS10F40	
Reverse voltage	V_R		40	40	V
Average rectified current	I_O	(Note 1)	1.5	1.0	A
Non-repetitive peak forward current	I_{FSM}	(Note 2)	10	5	A
Junction temperature	T_j		150	150	°C
Storage temperature	T_{stg}		-55 to 150	-55 to 150	°C

Note 1: Mounted on an FR4 board (25.4 × 25.4 × 1.6 mm, Cu Pad: 645 mm^2)

Note 2: Pulse width = 10 ms

Table 3.2 Comparison of the electrical characteristics of the CUHS15F40 and CUS10F40

Electrical characteristics (Unless otherwise specified, T_a=25°C)

Characteristic	Symbol	Note	Test Condition	CUHS15F40			CUS10F40			Unit
				Min	Typ.	Max	Min	Typ.	Max	
Forward voltage	$V_{F(1)}$	(Note 3)	I_F = 100 mA	–	–	–	–	0.32	0.38	V
	$V_{F(2)}$		I_F = 500 mA	–	0.40	0.45	–	0.46	0.53	
	$V_{F(3)}$		I_F = 1 A	–	0.49	0.54	–	0.60	0.67	
	$V_{F(4)}$		I_F = 1.5 A	–	0.57	0.63	–	–	–	
Reverse current	$I_{R(1)}$	(Note 3)	V_R = 10 V	–	3	–	–	2.7	15	μA
	$I_{R(2)}$		V_R = 40 V	–	6	50	–	4.9	20	
Total capacitance	C_t		V_R = 0 V, f = 1 MHz	–	130	–	–	74	–	pF

Note 3: Pulse measurement

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Figure 3.1 compares the transient thermal impedance of the CUHS15F40 and CUS10F40. At a pulse width of 1000 seconds, the CUHS15F40 provides 45% lower steady-state thermal resistance than the CUS10F40 because the CUHS15F40 is housed in the US2H package with an E-pad on the backside. Therefore, the CUHS15F40 can handle larger power than the CUS10F40 even though they are roughly the same size.

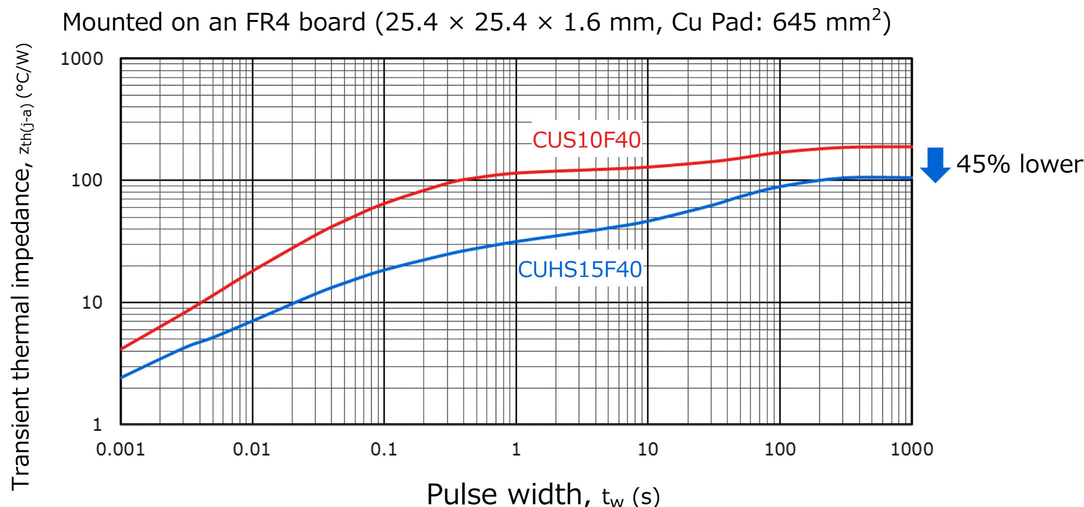

Figure 3.1 Comparison of the transient thermal impedance of the CUHS15F40 and CUS10F40(reference data)

Figure 3.2 and Figure 3.3 compare the simulated mold surface temperature of the CUHS15F40 and CUS10F40 mounted on an FR-4 board measuring 25.4 × 25.4 × 1.6 mm (with 100% copper coverage) after the same power is applied to them. When large power was applied, the mold surface temperature of the CUHS15F40 increased only to 144°C whereas that of the CUS10F40 reached 287°C, substantially exceeding its maximum rated junction temperature. When small power was applied, the mold surface temperature of the CUHS15F40 increased only to 83°C whereas that of the CUS10F40 reached 145°C. These simulation results indicate the excellent heat dissipation performance of the US2H package.

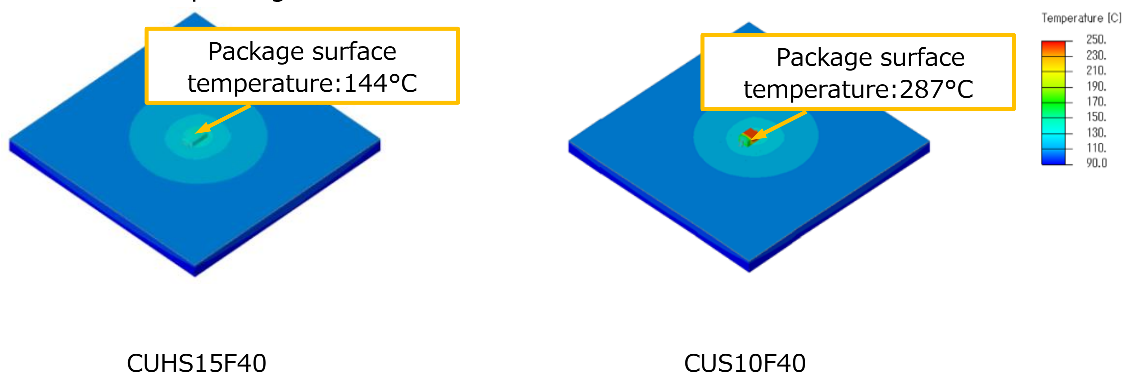

Figure 3.2 Package surface temperature of the CUHS15F40 and CUS10F40 mounted on an board after large power was applied

Note: mounted on an FR-4 board measuring 25.4 × 25.4 × 1.6 mm (with 100% copper coverage)

It is assumed that the same power is applied to each.

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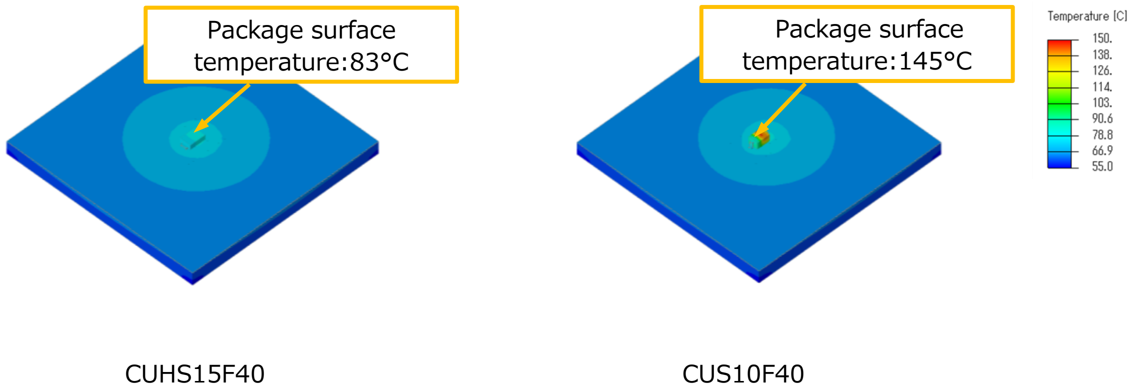

Figure 3.3 Package surface temperature of the CUHS15F40 and CUS10F40 mounted on an board after small power was applied

Note: mounted on an FR-4 board measuring 25.4 × 25.4 × 1.6 mm (with 100% copper coverage)

It is assumed that the same power is applied to each.

Next, we mounted the CUHS15F40 and CUS10F40 on FR-4 boards measuring 25.4 × 25.4 × 1.6 mm, each with a different copper coverage area, as shown in Figure 3.4, and simulated their thermal resistance. Figure 3.5 plots the simulation results. These curves indicate that the copper area helps improve heat dissipation performance.

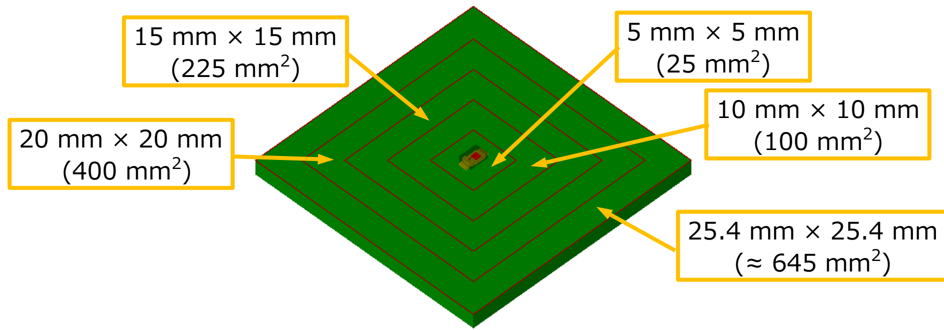

Figure 3.4 FR-4 boards with different copper areas used for thermal resistance simulations

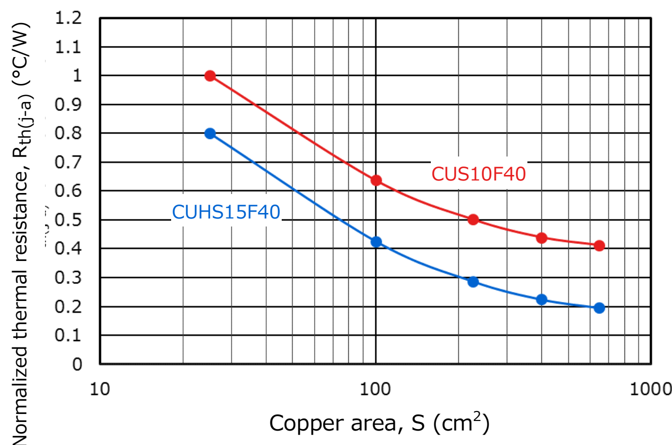

Figure 3.5 Normalized thermal resistance-vs-copper area curves (reference data)

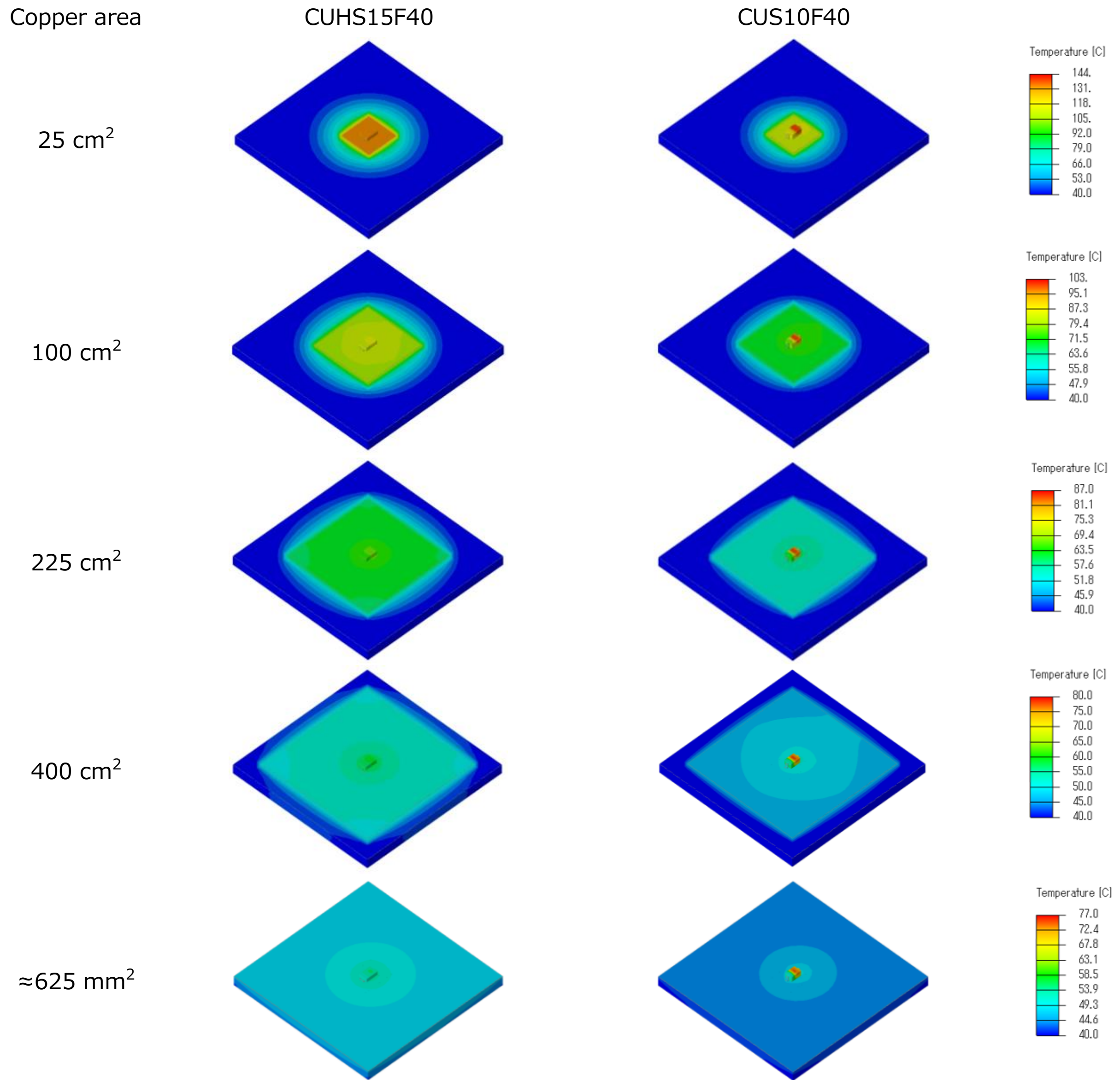

Figure 3.6 Package surface temperature vs copper area

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4. SBD overview

4.1. SBD structure

Figure 4.1 shows an example of an SBD structure. An SBD is a type of diode formed by the metal-to-semiconductor junction that behaves as a rectifier. The Schottky barrier diode (SBD) is named after Walter Hans Schottky. A Schottky junction is formed between a metal and an n-type semiconductor. In an SBD, electrons act as majority carriers. Therefore, SBDs can handle higher frequency than typical pn diodes.

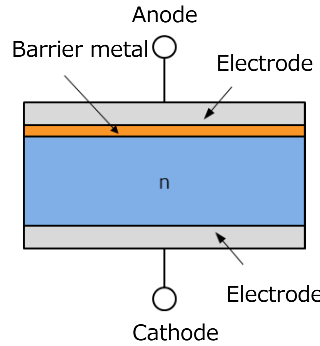

Figure 4.1 Example of an SBD structure

4.2. Band diagrams of a metal and an n-type semiconductor

A metal has a Fermi level between valence and conduction bands and does not have a forbidden band as shown in Figure 4.2. Therefore, a metal has a huge amount of holes in a valence band and a huge amount of electrons in a conduction band.

Figure 4.3 shows a band diagram of an n-type semiconductor. The n-type semiconductor has a forbidden band between valance and conduction bands in which no electron states can exist. The Fermi level is located within the forbidden band.

A Schottky junction is formed when an n-type semiconductor is joined with a metal that has a lower Fermi level than that of the n-type semiconductor. The Schottky junction behaves as a rectifier. In contrast, an ohmic junction is formed when an n-type semiconductor is joined with a metal that has a higher Fermi level than that of the n-type semiconductor. The ohmic junction behaves as a resistor.

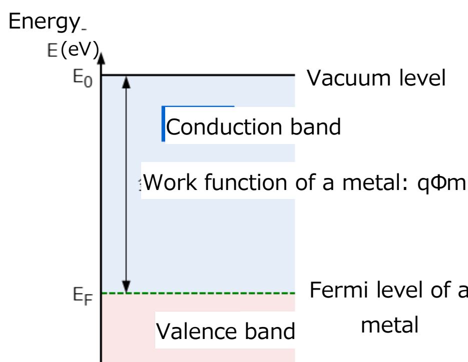

Figure 4.2 Band diagram of a metal

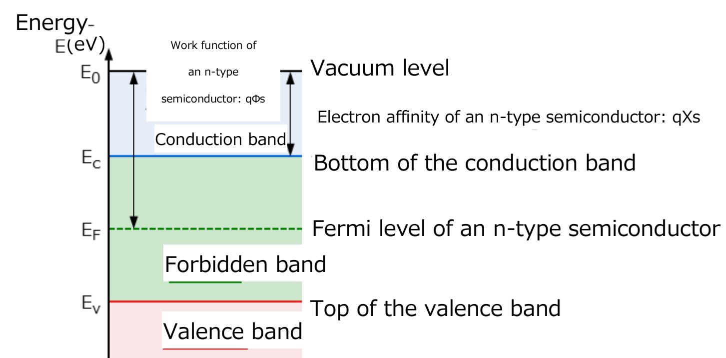

Figure 4.3 Band diagram of an n-type semiconductor

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4.3. Band diagram of an SBD in an unbiased state

When a metal and an n-type semiconductor are joined together, some electrons diffuse into the metal from the n-type semiconductor, making their Fermi level constant. At the same time, the lowest level of the conduction band (E_C) and the highest level of the valence band (E_V) of the n-type semiconductor change as shown in Figure 4.4. At this time, diffusion energy of $q \cdot \Phi_{bi} = q \cdot (\Phi_m - \Phi_s)$ is generated between the metal and the n-type semiconductor, causing a depletion layer to be formed by positive ions on the n-type semiconductor side. A depletion layer hardly expands into the metal even when electrons flow into it from the n-type semiconductor because the metal has a huge amount of electrons. When the Schottky junction is unbiased, little current flows because most electrons cannot exceed the diffusion energy level of the depletion layer, $q \cdot \Phi_{bi} = q \cdot (\Phi_m - \Phi_s)$.

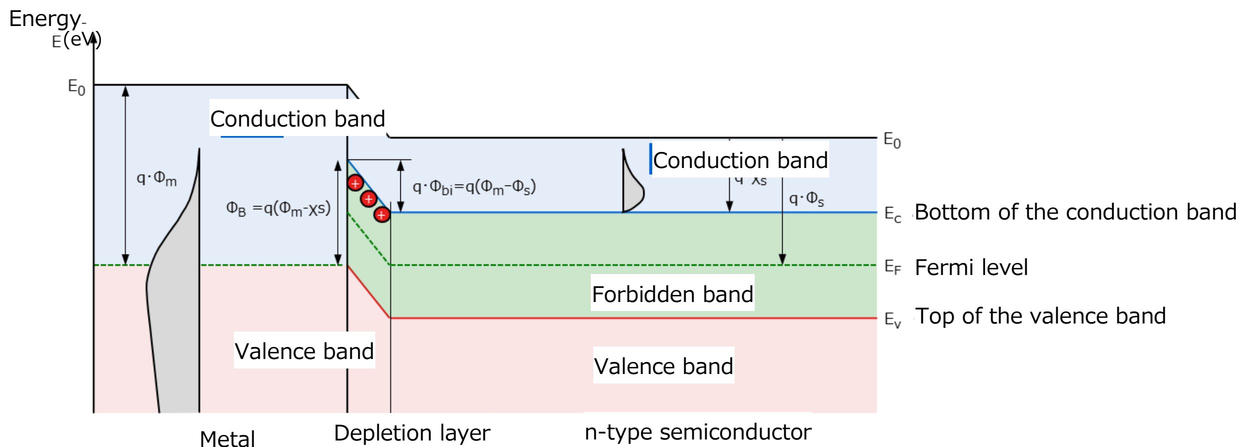

Figure 4.4 Band diagram of a Schottky junction in an unbiased state

4.4. Band diagram of a Schottky junction in the reverse-biased state

When a reverse bias of V_R is applied across the Schottky junction, the energy level of the n-type semiconductor drops. Therefore, few electrons can exceed the diffusion energy, $q \cdot \Phi_{bi} = q \cdot (\Phi_m - \Phi_s + V_R)$. Some of the electrons exceeding the diffusion energy flow as reverse current. Equation 4-1 represents the reverse current (current density) of an SBD in the reverse-biased state. SBDs with a lower Schottky barrier (Φ_B) provide higher reverse current.

$$I_R = A^* \cdot T^2 \cdot e^{-\frac{\Phi_B}{K \cdot T}} \qquad (4\text{-}1)$$

I_R:	Reverse current at temperature T	(A)
A^*:	Richardson constant	$(A/cm^2 \cdot K^2)$
T:	Absolute temperature	(K)
Φ_B:	Schottky barrier	(eV)
K:	Boltzmann constant (1.381×10^{-23})	$(J \cdot K^{-1})$

SBDs provide greater reverse current than typical pn diodes. The power dissipation of an SBD due to reverse current is not negligible when it is reverse-biased at high voltage or at high temperature. Therefore, an increase in reverse current causes an increase in power dissipation, which in turn causes an increase in reverse current. This vicious circle leads to a sharp increase in junction

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temperature and might degrade or destroy the SBD. To prevent this vicious circle, thermal design should be considered carefully.

In particular, when using SBDs with high reverse current, it is necessary to verify that they work properly under the worst-case conditions, taking reverse bias voltage, ambient temperature, and other usage conditions into consideration.

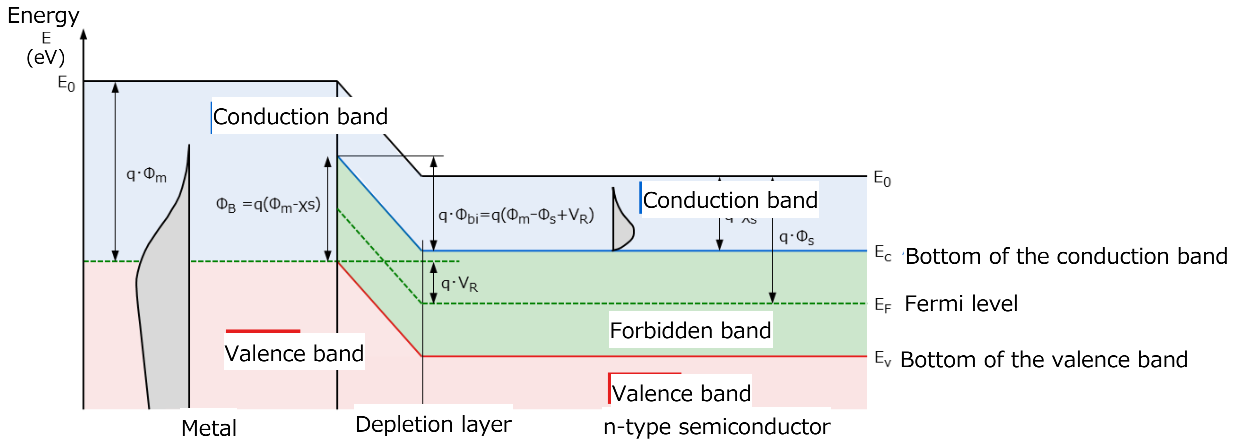

Figure 4.5 Band diagram of a Schottky junction in the reverse-biased state

$$I_R = A^* \cdot T^2 \cdot e^{-\frac{\Phi_B}{K \cdot T}} \tag{4-2}$$

I_R:	Reverse current at temperature T	(A)
A^*:	Richardson constant	($A/cm^2 \cdot K^2$)
T:	Absolute temperature	(K)
Φ_B:	Schottky barrier	(eV)
K:	Boltzmann constant (1.381×10^{-23})	($J \cdot K^{-1}$)

4.5. JBS structure

Despite low forward voltage, an SBD exhibits large reverse current. Toshiba's product portfolio includes SBDs designed with a Junction Barrier Schottky (JBS) structure that makes it possible to reduce reverse current despite low forward voltage.

Figure 4.6 shows the cross-sectional view of an SBD with the JBS structure, which has p-type regions buried in the n^- region. When an SBD is reverse-biased, depletion layers begin to expand across n-type and diffused p-type regions. As the reverse bias voltage is increased, adjacent depletion layers merge, suppressing an increase in reverse current.

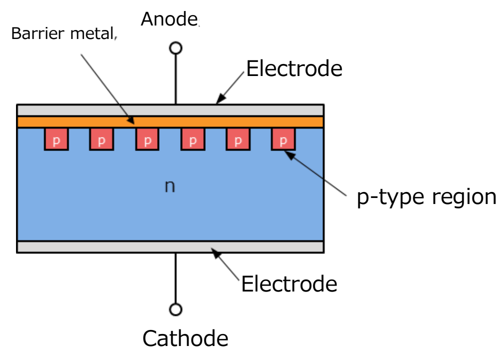

Figure 4.6 JBS structure

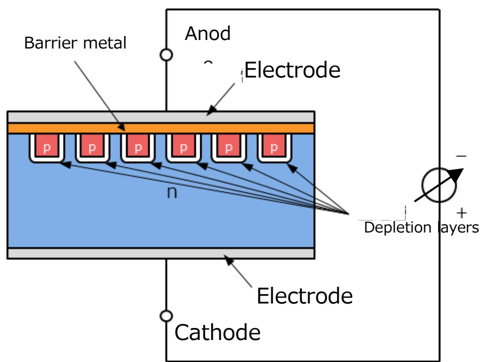

Figure 4.7 Formation of depletion layers by the application of a reverse bias across the Schottky junction

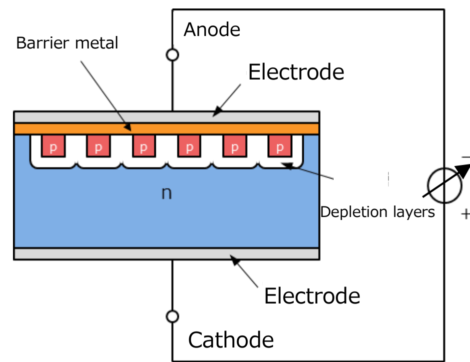

Figure 4.8 Expansion of depletion layers by an increase in reverse bias across the Schottky junction

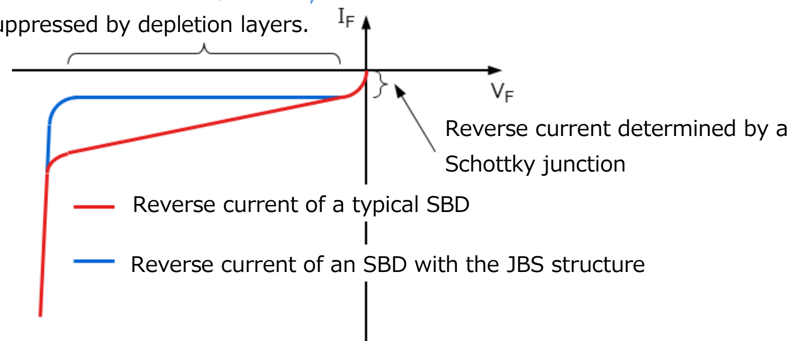

Figure 4.9 Comparison of the reverse current characteristics of SBDs with typical and JBS structures

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5. Power losses of a diode

Figure 5.1 shows an example of a switching waveform of a typical diode. This section describes the power losses of a diode, referring to this figure.

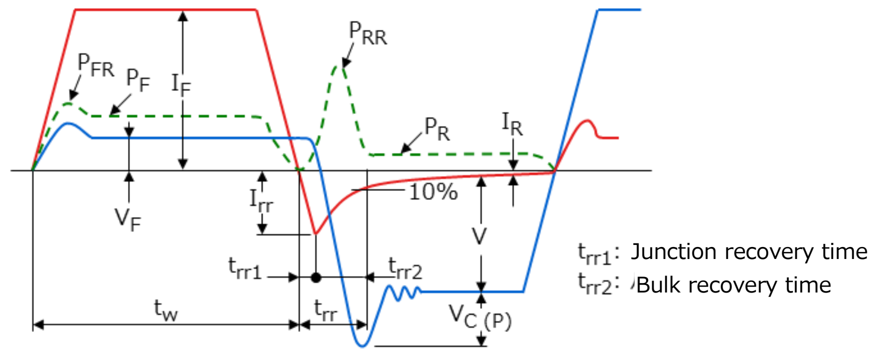

Figure 5.1 Example of a diode's switching waveform

(1) Forward power loss (P_F)

Normally, when a diode is forward-biased, the forward voltage (V_F) decreases as the device temperature increases. The device temperature settles at a certain point. Equation 5.1 represents the forward power loss (P_F) dissipated by a diode when the forward current is flowing constantly.

$$P_F = V_F \cdot I_F \qquad (5\text{-}1)$$

P_F:	Forward power loss	(W)
V_F:	Forward voltage	(V)
I_F:	Forward current	(A)

(2) Reverse power loss (P_R)

The power loss due to reverse leakage current (I_R) is negligibly smaller than forward power loss at low temperature. However, since I_R increases exponentially with temperature, the power loss due to I_R cannot be ignored at high temperature. SBDs and fast rectifier diodes have higher I_R than typical rectifier diodes. In particular, a rise in temperature and an increase in current during operation make SBDs susceptible to thermal runaway, possibly leading to device destruction. For SBDs, it is necessary to calculate the permissible power dissipation at high temperature, taking forward and reverse power losses into consideration, and use it as a basis for thermal and safety design. In addition, it is essential to perform verification using actual hardware in order to ensure that SBDs work properly under the worst-case conditions.

Equation 5.2 represents the reverse power loss (P_R) dissipated by a diode when it is reverse-biased.

$$P_R = V_R \cdot I_R \quad (5\text{-}2)$$

P_R:	Reverse power loss	(W)
V_R:	Reverse voltage	(V)
I_R:	Reverse current	(A)

(3) Forward switching loss (P_{fr})

The forward switching loss (P_{fr}) is the loss that occurs when a rapidly rising rectangular pulse is applied to a diode in the forward direction. The application of such a pulsed current to a diode causes its forward voltage to rise instantaneously above the steady-state forward voltage (V_F), resulting in a substantial power loss (see Figure 5.1).

This is because when a rapidly rising pulse is applied to a diode, it does not enter a conducting state immediately and the diode exhibits high resistance during a certain period even in the forward direction. This phenomenon is called forward recovery. The forward recovery time (t_{fr}) is not dependent on the operating frequency, but on the rise time.

(4) Reverse switching loss (P_{rr})

The reverse switching loss (P_{rr}) is the loss that occurs when a rapidly rising reverse voltage is applied to a diode while it is forward-biased. P_{rr} is the loss dissipated during the reverse recovery time (t_{rr}) because of reverse current (see Figure 5.1). The reverse switching loss (P_{rr}) is approximated as follows:

$$P_{rr} \simeq \frac{1}{2} i_{rr} \cdot t_{rr} \cdot V_R \cdot f = Q_R \cdot V_R \cdot f \quad (5\text{-}3)$$

i_{rr}:	Maximum reverse current	(A)
t_{rr}:	Reverse recovery time	(s)
V_R:	Reverse voltage (in a steady state)	(V)
Q_R:	Accumulated charge	(C)
f:	Frequency	(Hz)

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A power loss occurs during the t_{rr2} period of t_{rr}. Since the power loss during t_{rr1} is small, Equation 5-3 can be approximated as:

$$P_{rr} \simeq \frac{1}{6} i_{rr} \cdot t_{rr2} \cdot V_R \cdot f \quad (5\text{-}4)$$

i_{rr}:	Maximum reverse current	(A)
t_{rr2}:	Bulk recovery time	(s)
V_R:	Reverse voltage (in a steady state)	(V)
Q_R:	Accumulated charge	(C)
f:	Frequency	(Hz)

In contrast to the pn diode, an SBD does not have reverse recovery time (t_{rr}) due to carrier recombination since it is a unipolar device. However, a reverse recovery waveform equivalent to t_{rr} is observed because of junction capacitance. Still, the reverse recovery current and the time during which it persists are much smaller, compared to high-efficiency diodes (HEDs)*2, as shown in Figure 5.2.

*2: Also known as low-loss diodes (LLDs)

Test conditions: i_F=1 A, di/ dt=-30 A/ μs, Ta=25°C

Vertical axis: Current (0.5 A/div)
Horizontal axis: Time (50 ns/div)

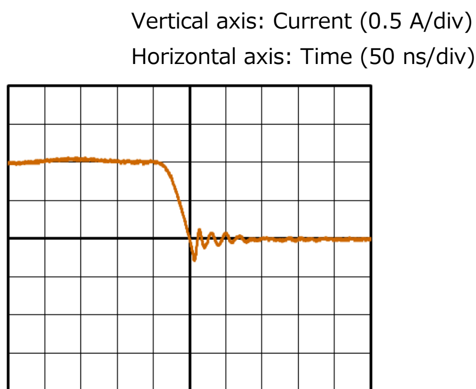

Figure 5.2 Example of an SBD recovery waveform

Vertical axis: Current (0.5 A/div)
Horizontal axis: Time (50 ns/div)

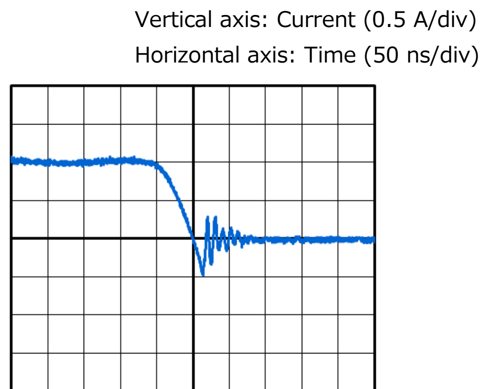

Figure 5.3 Example of an HED recovery waveform

Figure 5.4 shows a DC-DC converter in which an SBD is used as a freewheeling diode. In this case, the SBD exhibits a forward power loss (P_F), reverse power loss (P_R), and reverse switching loss (P_{rr}). At this time, the total power loss of the SBD can be calculated using Equation 5-5.

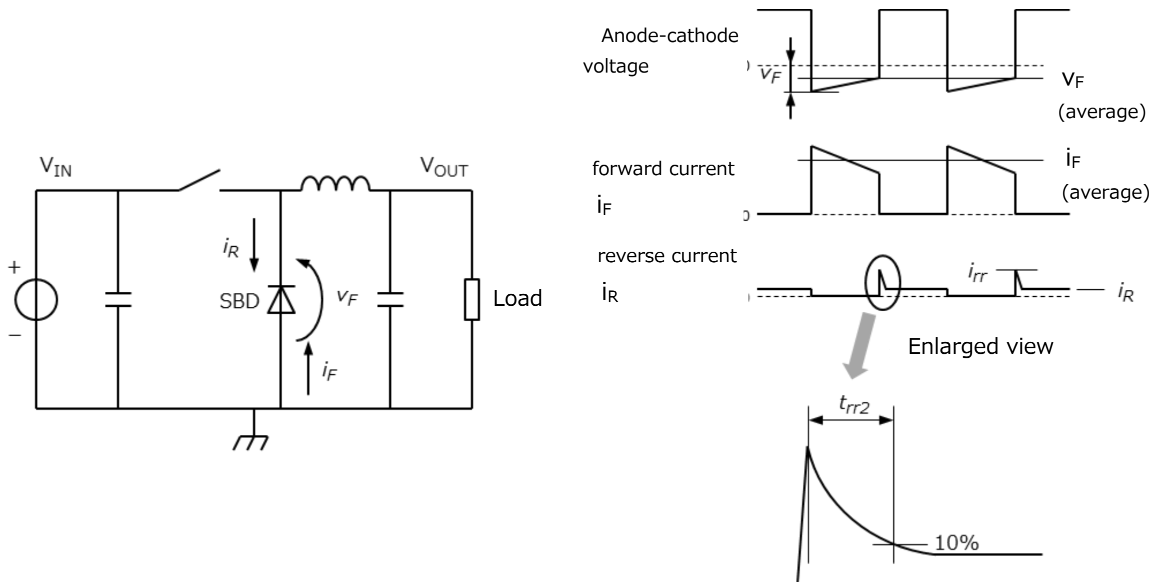

Figure 5.4 Example of voltage and current waveforms of an SBD in a DC-DC converter

$$P_d = P_F + P_R + P_{rr}$$
$$= v_{F(Ave)} \cdot i_{F(Ave)} + V_{OUT} \cdot i_R + \frac{1}{6} i_{rr} \cdot t_{rr2} \cdot V_{OUT} \cdot f \qquad (5\text{-}5)$$

i_{rr}:	Maximum reverse current	(A)
t_{rr2}:	Bulk recovery time	(s)
V_R:	Reverse voltage (in a steady state)	(V)
Q_R:	Accumulated charge	(C)
f:	Frequency	(Hz)

6. Thermal design

6.1. Thermal design

(1) Maximum allowable power dissipation and equivalent thermal circuit

The power dissipation of a diode (P_d) is a function of the ambient or case temperature, maximum junction temperature (T_{jmax}), and thermal resistance as expressed by Equation 6-1:

$$P_{dmax(T_a)} = \frac{T_{jmax} - T_a}{R_{th(j-a)}} \quad , P_{dmax(T_C)} = \frac{T_{jmax} - T_C}{R_{th(j-c)}} \qquad (6\text{-}1)$$

T_{jmax}:	Maximum rated junction temperature	(°C)
$P_{dmax(Ta)}$:	Thermal resistance of a diode without a heatsink	(°C/W)
T_a:	Ambient temperature	(°C)
$P_{dmax(Tc)}$:	Thermal resistance of a diode with a heatsink	(°C/W)
T_c:	Case temperature	(°C)

A heat flow can be modeled by analogy to an electrical circuit. Using this model, the heat flow from the junction of a diode to the ambient air is derived from thermal resistances and thermal capacitances. Figure 6.1 shows an equivalent thermal circuit in a thermally steady state.

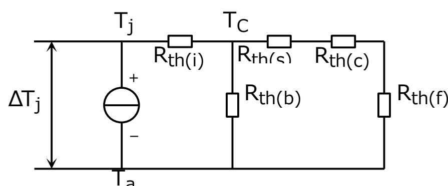

Figure 6.1
Equivalent thermal circuit

$R_{th(i)}$: Junction-to-case thermal resistance

$R_{th(b)}$: Case-to-ambient thermal resistance

$R_{th(s)}$: Thermal resistance of silicone grease or TIM*3

$R_{th(c)}$: Contact thermal resistance between case and heatsink

$R_{th(f)}$: Thermal resistance of a heatsink

*3 Thermal interface material (TIM)

The thermal resistance values shown in the equivalent thermal circuit of Figure 6.1 can be explained as follows:

① Junction-to-case thermal resistance: $R_{th(i)}$

The thermal resistance from the junction of a diode to the case ($R_{th(i)}$) depends on the structure and material of the diode and differs from diode to diode. To measure the junction-to-case thermal resistance, the case of the diode must be cooled to maintain a constant temperature. When the case temperature (T_c) is held at 25°C, the maximum allowable power dissipation ($P_{dmax(Tc)}$) of a diode can be calculated as follows:

$$P_{dmax(Tc)} = \frac{T_{jmax} - T_C}{R_{th(i)}} = \frac{T_{jmax} - 25°C}{R_{th(i)}} \quad (6\text{-}2)$$

$P_{dmax(Tc)}$:	Maximum allowable power dissipation of a diode	(W)
T_{jmax}:	Maximum rated junction temperature	(°C)
T_C:	Case temperature (T_C= 25°C)	(°C)
$R_{th(i)}$:	Junction-to-case thermal resistance	(°C/W)

In the datasheets for through-hole diodes that can be attached to a heatsink, the maximum allowable power dissipation is specified either at T_C = 25°C or assuming the use of an infinite heatsink. $P_{dmax(Tc)}$ is determined by the thermal resistance of the diode as indicated by Equation 6-2.

② Contact thermal resistance: $R_{th(c)}$

Contact thermal resistance ($R_{th(c)}$) varies according to the condition of the contact surface between the case of a diode and a heatsink. This condition is greatly affected by factors such as the evenness, coarseness, and area of contact, as well as the attachment of the diode to the heatsink. The influence of the coarseness and unevenness of the contact surface can be reduced by applying silicone grease or attaching silicone rubber to the contact surface.

③ Isolation plate's thermal resistance: $R_{th(s)}$

If it is necessary to provide electrical isolation between a diode in an electrically non-isolated through-hole package and a heatsink, an isolation plate must be inserted between them. The thermal resistance of this isolation plate ($R_{th(s)}$) varies with the materials, thickness, and area of the plate and is not negligible. For packages isolated by mold resin, the thermal resistance specified for a diode includes the isolator's thermal resistance ($R_{th(s)}$).

④ Heatsink's thermal resistance: $R_{th(f)}$

The thermal resistance of a heatsink can be considered as the distributed thermal impedance of a heat path from the surface of a heatsink to the ambient air. The thermal resistance of a heatsink depends on the condition of the ambient air, a difference in temperature between the heatsink and the ambient air, and the effective cubic volume of the heatsink. It is difficult to mathematically express $R_{th(f)}$. Actually, $R_{th(f)}$ is obtained by measurement. Figure 6.2 shows an example of thermal resistance data measured for a diode at the center of a vertically standing heatsink. Various heatsinks are available from many vendors. Optimal heatsinks should be selected, referring to the thermal resistance data shown in their technical datasheets.

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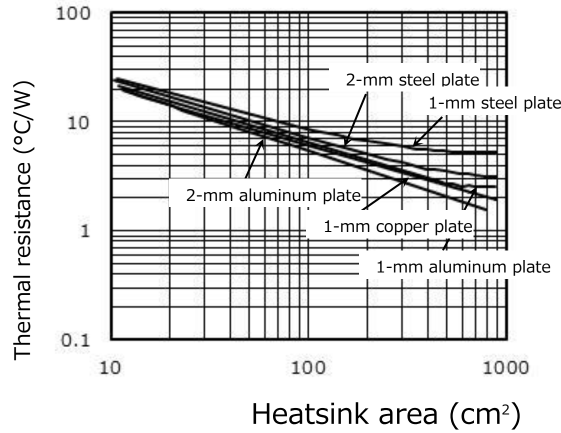

Figure 6.2 Heatsink surface area vs thermal resistance

From the equivalent circuit of Figure 6.1, the junction-to-ambient thermal resistance ($R_{th(j-a)}$) can be calculated as follows:

$$R_{th(j-a)} = R_{th(i)} + \frac{R_{th(b)} \cdot \left(R_{th(s)} + R_{th(c)} + R_{th(f)}\right)}{R_{th(b)} + R_{th(s)} + R_{th(c)} + R_{th(f)}} \quad (6\text{-}3)$$

$R_{th(j-a)}$:	Junction-to-ambient thermal resistance	(°C/W)
$R_{th(i)}$:	Junction-to-case resistance	(°C/W)
$R_{th(b)}$:	Case-to-ambient thermal resistance	(°C/W)
$R_{th(s)}$:	Thermal resistance of an isolating plate	(°C/W)
$R_{th(f)}$:	Thermal resistance of a heatsink	(°C/W)

The case-to-ambient thermal resistance ($R_{th(b)}$) varies with the material and shape of the case. $R_{th(b)}$ is significantly larger than $R_{th(i)}$, $R_{th(c)}$, $R_{th(s)}$, and $R_{th(f)}$. Therefore, Equation 6-3 can be simplified to:

$$R_{th(j-a)} = R_{th(i)} + R_{th(c)} + R_{th(s)} + R_{th(f)} \quad (6\text{-}4)$$

Since no heatsink is generally used for small diodes, $R_{th(j-a)}$ can be calculated as:

$$R_{th(j-a)} = R_{th(i)} + R_{th(b)} \quad (6\text{-}5)$$

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The datasheets for small diodes show the maximum allowable power dissipation at a T_a of 25°C, which is calculated using Equation 6-6 unless otherwise noted:

$$P_{dmax(T_a=25\ °C)} = \frac{T_{jmax} - 25\ °C}{R_{th(j-a)}} \qquad (6\text{-}6)$$

$P_{dmax(Ta=25°C)}$:	Maximum allowable power dissipation of a diode at an ambient temperature of 25°C	(W)
T_{jmax}:	Maximum rated junction temperature	(°C)
$R_{th(j-a)}$:	Junction-to-ambient resistance	(°C/W)

Equation 6-5 can be used to create a thermal design that satisfies the maximum rating requirement for DC dissipation. When diodes are used in a switching circuit, great care is required to ensure that the peak transient T_j value does not exceed T_{jmax}.

(2) Pulse response of junction temperature

Generally, the thermal impedance of a diode is modeled as a distributed constant circuit consisting of thermal capacitances (C) and thermal resistances (R) as shown in Figure 6.3.

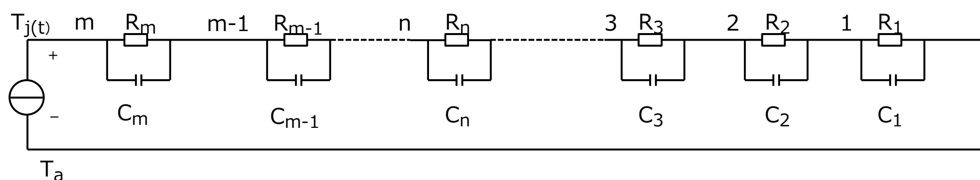

Figure 6.3 Transient thermal impedance model

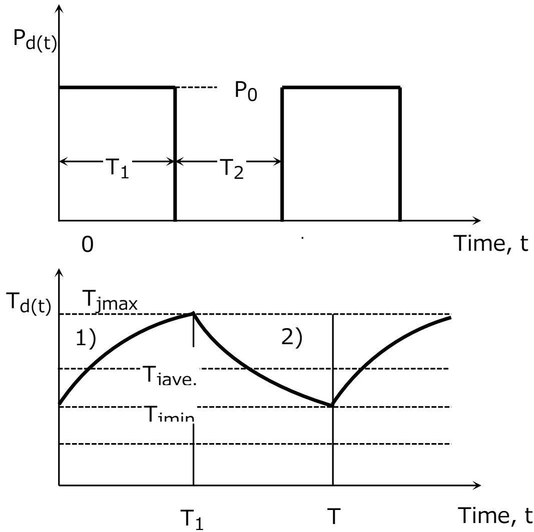

Figure 6.4 Change in junction temperature caused by pulse power dissipation

When the pulse dissipation ($P_{j(t)}$) shown in Figure 6.4 is applied to the circuit of Figure 6.3, a change in junction temperature $T_{d(t)}$ that appears at the mth parallel RC circuit under stable thermal conditions can be calculated as follows:

1) In the region where $P_{d(t)} = P_0$:

$$T_{d(t)} = \sum_{n-1}^{m} [(P_0 \cdot R_n) - T_{n\ min}] \left[1 - e^{\left(\frac{-t}{C_n \cdot R_n}\right)}\right] + T_{n\ min}$$

2) In the region where $P_{d(t)} = 0$:

$$T_{d(t)} = \sum_{n-1}^{m} \left[T_{n\ max} \cdot e^{\left(\frac{-t}{C_n\ R_n}\right)}\right]$$

For typical diodes, the actual $P_{d(t)}$ value can be approximated by substituting 4 for n. However, if the C and R values are indefinite, it is difficult to calculate T_j. Therefore, T_{jmax} is generally calculated using transient thermal impedance as follows: Figure 6.5 shows an example of typical transient thermal impedance characteristics. Suppose that a single rectangular pulse (with a pulse width of t and a peak value of P_0) is applied. From the figure, we read the transient thermal impedance at a pulse width of t, and then use Equation 6-7 to calculate T_{jmax}.

$$T_{jmax} = z_{th(t)} \cdot P_O + T_a \qquad (6\text{-}7)$$

T_{jmax}:	Maximum rated junction temperature	(°C)
$z_{th(t)}$:	Transient thermal impedance at a pulse width of t	(°C/W)
P_O:	Diode's power dissipation	(W)
T_a:	Ambient temperature	(°C)

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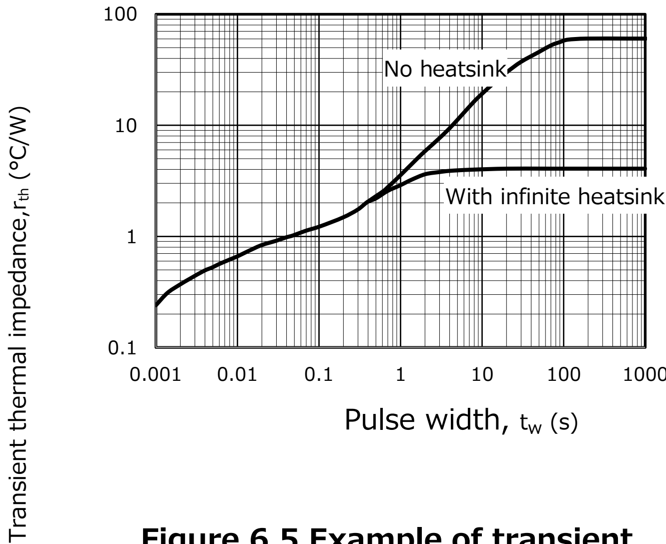


Figure 6.5 Example of transient thermal impedance curves

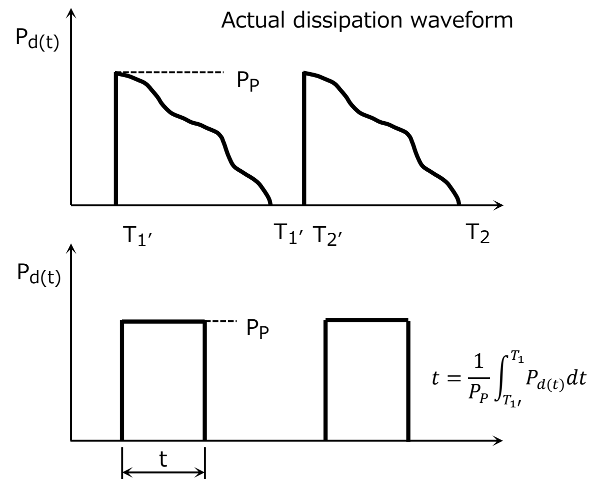
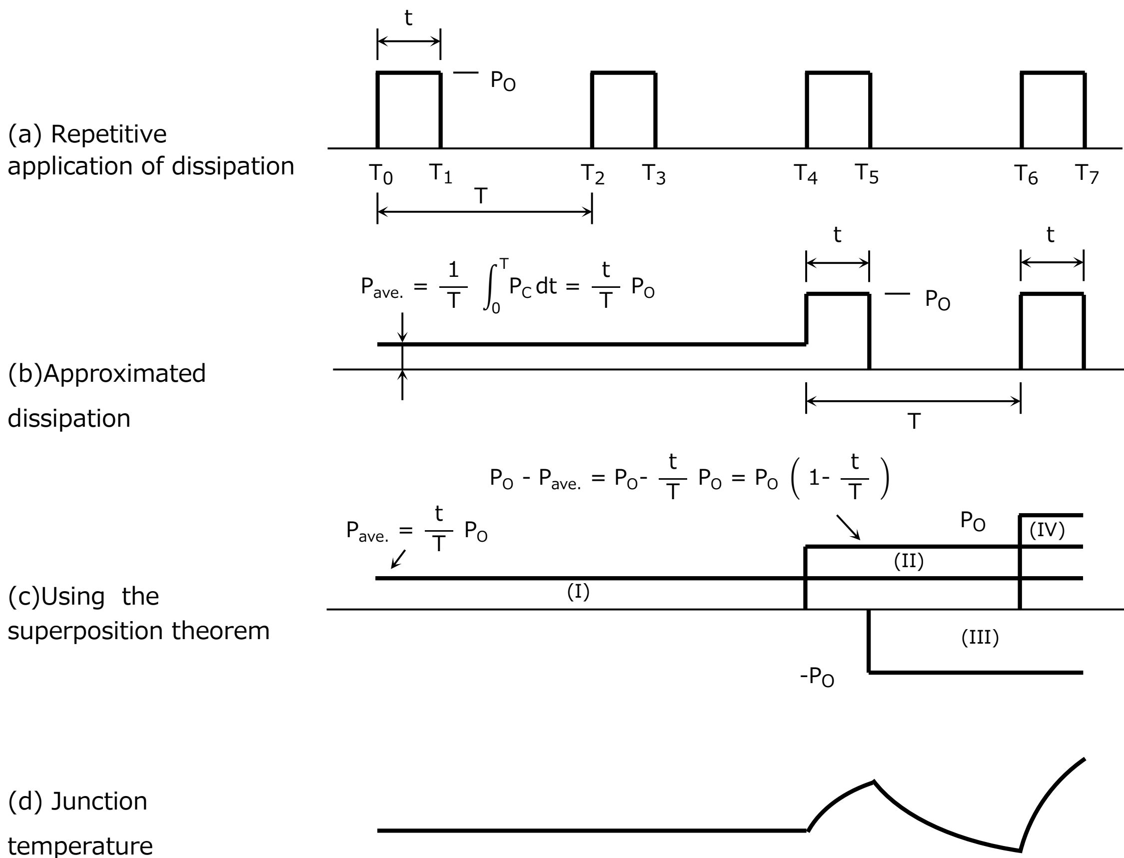


Figure 6.6 Approximation of a power dissipation waveform

When a repetitive pulse train with a cyclic period of T is applied as shown in Figure 6.6, T_{jmax} is given by Equation 6-12 using the superposition theorem.



$$\Delta T_{j(I)} = P_O \cdot \frac{t}{T} \cdot R_{th(j-a)} \qquad (6\text{-}8)$$

$$\Delta T_{j(II)} = P_O \cdot \left(1 - \frac{t}{T}\right) \cdot z_{th(T+t)} \qquad (6\text{-}9)$$

$$\Delta T_{j(III)} = -P_O \cdot z_{th(T)} \qquad (6\text{-}10)$$

$$\Delta T_{j(IV)} = P_O \cdot z_{th(t)} \qquad (6\text{-}11)$$

$$T_{jmax} = P_O \cdot \left[\frac{t}{T} \cdot R_{th(j-a)} + \left(1 - \frac{t}{T}\right) \cdot z_{th(T+t)} - z_{th(T)} + z_{th(t)}\right] + T_a \qquad (6\text{-}12)$$

Great care should be exercised in the thermal design for pulsed power applications to ensure that T_{jmax} given by Equation 6-12 does not exceed the maximum rated junction temperature of the diode.

The above description assumes that a rectangular waveform is applied to a diode. However, for actual diode applications, the $P_{d(t)}$ waveform seldom becomes rectangular. In such cases, approximate the power dissipation waveform to a rectangular wave as shown in Figure 6.7 and use Equation 6-12 to estimate T_{jmax}. To obtain a rectangle with an area equal to a half-sine or triangular area, multiply the peak value of P_P by 0.7 in the case of (a) and (b), and multiply the pulse width by 0.91 for (a) and by 0.71 for (b). In the case of (c) and (d), use the same peak value of P_P, and multiply the pulse width by 0.63 for (c) and by 0.5 for (d).

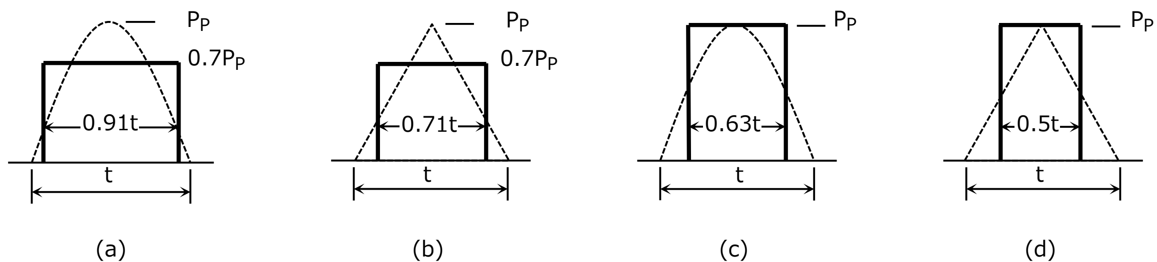


Figure 6.7 Approximating sine and triangular waves to rectangular waves

If it is necessary to obtain thermal impedance at a pulse width less than the minimum pulse width for the transient thermal impedance shown in a datasheet, transient thermal impedance can be approximated as follows:

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$$z_{th(tw1)} = z_{th(tw2)} \cdot \sqrt{\frac{t_{w1}}{t_{w2}}} \qquad (6\text{-}13)$$

$z_{th(tw1)}$:	Transient thermal impedance at a pulse width of t_{w1}	(°C/W)
$z_{th(tw2)}$:	Transient thermal impedance at a minimum pulse width of t_{w2} shown in a datasheet	(°C/W)
t_{tw1}:	Pulse width at which transient thermal impedance is to be calculated	(s)
t_{tw2}:	Minimum pulse width for the transient thermal impedance shown in the datasheet	(s)

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