1.6kW Server Power Supply

Design Guide

RD001-DGUIDE-02

TOSHIBA ELECTRONIC DEVICES & STORAGE CORPORATION

Table of Contents

1. Introduction

This design guide describes the circuit design and the layout of the 1.6 kW server power supply (this power supply). Refer to the *1.6 kW Server Power Supply Reference Guide* for its specification, operation and performance.

Components marked "Not Mounted" in the BOM are not used in this power supply even if component designators are shown in the circuit diagram. They are intended as reserved spaces for components necessary to modify circuit constants when designing an actual circuit.

1.1. Power MOSFETs Used

Toshiba offers the 600/650 V DTMOSIV series suitable for primary sides (PFC and main switch) on AC-DC converters and the low-voltage U-MOSVIII/IX series suitable for a secondary sides (synchronous rectification and ORing circuits) on AC-DC converters. Designers can choose appropriate MOSFETs from extensive product lineups according to their design specification. Devices used in this power supply are shown below.

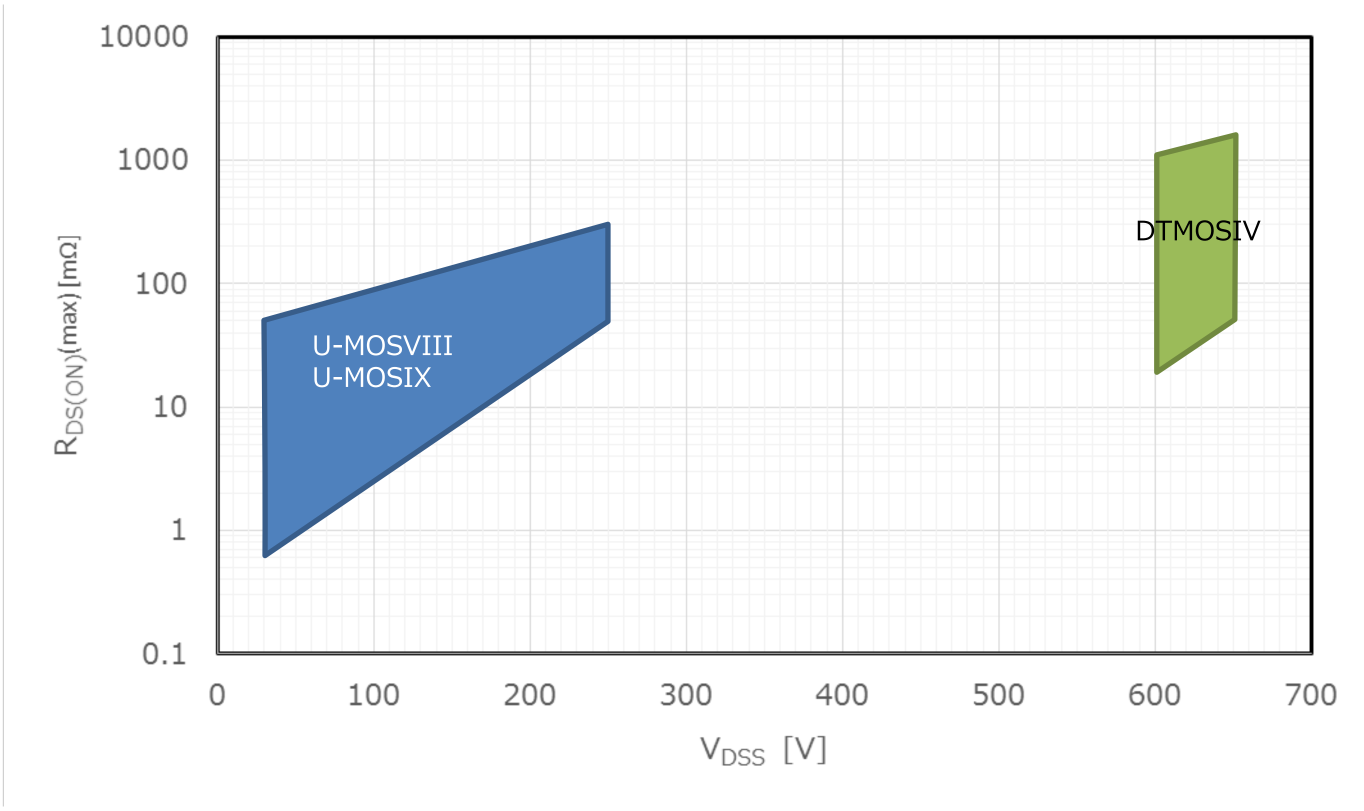

Fig. 1.1.1 Coverage of the U-MOSVIII/XI and DTMOSIV Series

TK25N60X

In the semi-bridgeless PFC circuit

V_{DSS}=600 V, $R_{DS(ON)}$@V_{GS}=10 V (max)=125 mΩ, TO-247

DTMOSIV-H process: Fast switching and reduced switching loss

TK25N60X5

In the phase-shift full-bridge (PSFB) circuit

V_{DSS}=600 V, $R_{DS(ON)}$@V_{GS}=10 V (max) =140 mΩ, TO-247

High-speed diode process: Reduced loss during reverse recovery

TPH3R70APL

In the synchronous rectification circuit on the secondary side of the PSFB

V_{DSS}=100 V, $R_{DS(ON)}$@V_{GS}=10 V (max) =3.7 mΩ, SOP Advance

Latest U-MOSIX-H process: Reduced synchronous rectification loss

TPHR9003NC

In the output ORing circuit

V_{DSS}=30 V, $R_{DS(ON)}$@V_{GS}=10 V (max)=0.9 mΩ, SOP Advance

Low on-resistance U-MOSVIII process: Reduced ORing circuit loss

2. Circuit Design

This section describes major considerations for the design of this power supply circuit.

2.1. AC Line Circuit Design

Fig. 2.1.1 shows the AC line circuit of this power supply.

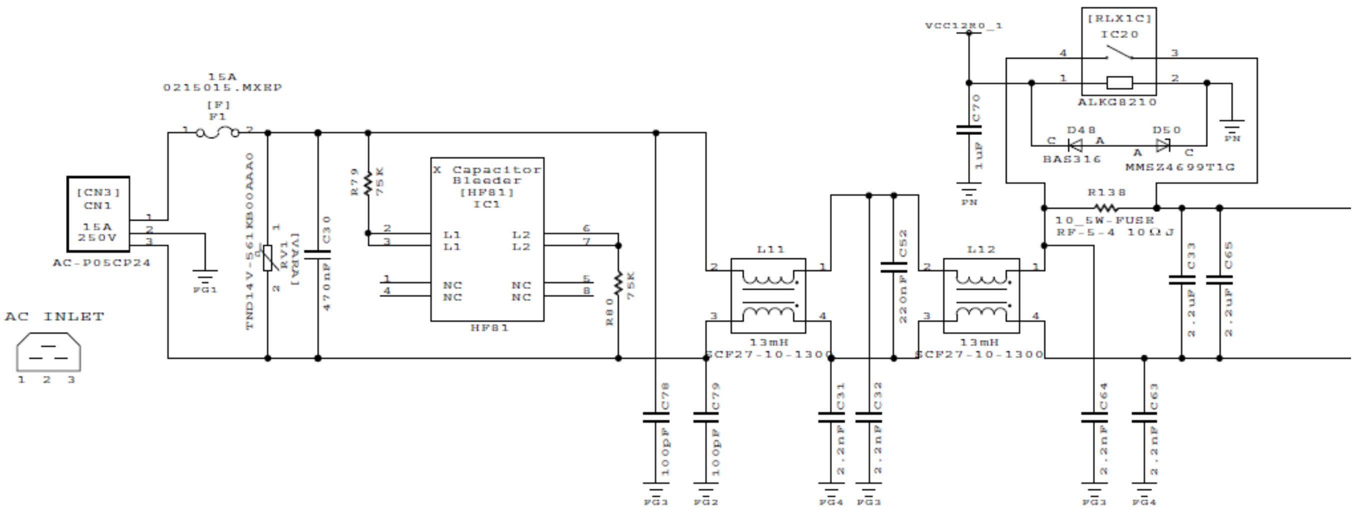

Fig. 2.1.1 AC line Circuit

Fuse

The AC line circuit contains a fuse (F1) so that the AC input is disconnected in the event of an abnormal increase in the AC line current. A fuse is chosen according to the maximum AC line current, which is given by the following equation:

Maximum AC line current = maximum power/conversion efficiency/power factor/input RMS voltage (min)

This power supply provides a 1.6 kW output when the input is at 200 VAC system, and an 800 W output when the input is at 100 VAC system. If the PFC efficiency did not vary according to the AC input voltage, the maximum power would be constant regardless of the AC input voltage. In practice, however, the PFC efficiency decreases with the AC input voltage. Therefore, it should be assumed that the input voltage is 90 V (the minimum RMS voltage for the 100 V AC mains) when calculating the maximum AC line current. Suppose that input voltage (minimum RMS value) is 90 V, the maximum power is 800 W, the efficiency is 90%, and the power factor is 0.99. Then, the maximum AC line current of the 1.6 kW server power supply will be about 10 A. Considering a margin, a 15 A is used in this power supply. In selecting a fuse, an inrush current during power-up and safety certification should be considered in addition to the maximum AC line current

Varistor

The AC line circuit contains a ceramic varistor (RV1) for protection against a voltage surge caused by a lightning strike. A varistor should be chosen according to the actual AC line voltage. This power supply uses a varistor with an RMS voltage of 350 VAC and a varistor voltage of 560 V, considering voltage margins because the AC line has a maximum RMS voltage of 264 V and an instantaneous peak voltage of 373 V. In selecting a varistor, it is necessary to consider its surge current tolerance, energy tolerance and other characteristics. A failure mode of Varistor is short mode generally. When a varistor is used, it is recommended to install a fuse on the AC input side.

IC for the discharging of the X capacitors

After the AC input is disconnected, the X capacitors (C30, C33, C52 and C65) must immediately be discharged in order to prevent an electric shock hazard. This power supply contains the HF81 discharge IC for the X capacitors. This IC helps reduce system power consumption since it shuts off the discharge path while AC power is being supplied. When the AC input is disconnected, a circuit formed by this IC and external resistors (R79 and R80) discharges the X capacitors to reduce the capacitor voltage to 37% or less of the initial value within 1 second. This power supply contains two external resistors (75 kΩ) necessary to discharge 5 μF capacitance since the capacitance of the X capacitors totals around 5 μF. It is necessary to adjust external resistor values if the X capacitors values are modified to reduce noise. The discharge resistors can be used alone without the HF81 IC to save costs. In that case, however, it is necessary to ensure that a system’s power-saving requirement will be satisfied since the discharge resistor causes continuous power loss while AC power is being supplied.

Components for EMI prevention

For common-mode noise prevention, this power supply contains the Y capacitors (C31, C32, C78, C79, C63 and C64) and common-mode choke coils (L11 and L12). For differential-mode noise prevention, this power supply contains the X capacitors (C30, C33, C52 and C65). The noise level is affected by the PCB layout and the chassis design. The Y capacitors and common-mode choke coils should be changed, added or removed as needed. Since increasing the values of the Y capacitors increases leakage current, it is necessary to ensure that the safety standard requirements are satisfied.

Components for inrush current prevention

In order to suppress inrush current upon turn-on of the AC input, this power supply contains a resistor with an integrated fuse (R138) as well as a relay (IC20). When this power supply is powered up in a correct sequence, a current flows via R138 (10 Ω) since the relay is off during turn-on of the AC input. As a result, an inrush current is suppressed. The relay turns on upon detection of a 12 V power supply on the primary side after the external 12 V power supply on the primary side turns on, following the turn-on of the AC input. When the relay turns on, a current flows through the relay which has lower resistance; this reduces a power loss while this power supply is on. It is necessary to ensure that the relay meets the on/off timing parameters of the system specification.

12 V power supplies on the primary and secondary sides

According to this power supply specification, the 12 V power supplies must be applied externally. If the system specification requires that the 12 V power supplies on the primary and secondary sides be generated from an AC line, off-line converters or similar devices should be used.

2.2. PFC Circuit Design

In order to build a high-efficiency PFC circuit, it has a semi-bridgeless topology using the Texas Instruments UCC28070A controller. This section describes basic design considerations for the semi-bridgeless circuit of this power supply. Refer to the datasheet and application notes for the UCC28070A for details on the circuit design around the controller. Refer to the *1.6 kW Server Power Supply Reference Guide* for details on its specification.

Simulation circuit which can simulate the PFC circuit operation is provided on the web as "RD001-SPICE01". Refer to this file when the circuit is being designed if necessary. Maximum step size is changeable for actual calculation. However, if different value from original one is chosen, calculation time will increase.

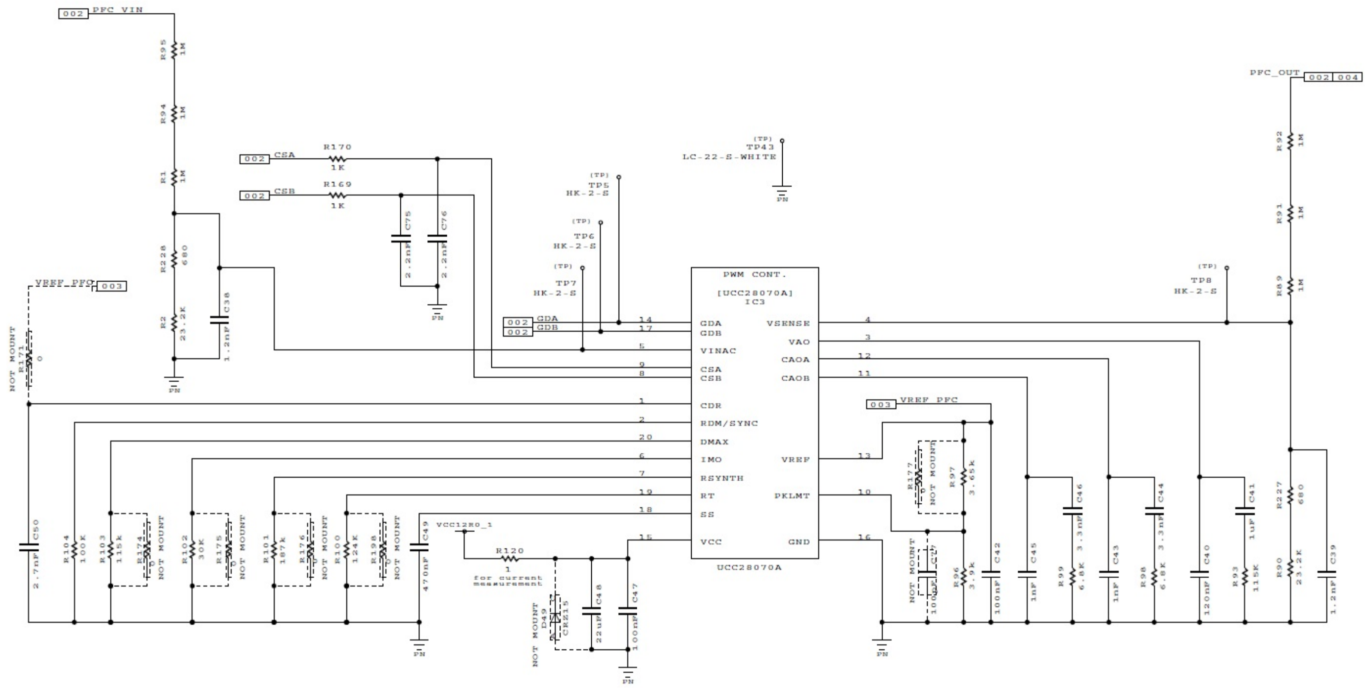

Fig. 2.2.1 PFC Circuit 1 (around Controller)

<u>Output voltage</u>

The output voltage of the PFC circuit, PFC_OUT, can be programmed with external resistors (R89, R90, R91, R92 and R227). The output voltage is controlled by comparing VSENSE (i.e., the voltage sensed at the output terminal, divided by the above resistors) with the internal reference voltage (3.0 V) of the UCC28070A PFC controller. The output voltage is given by following equation:

$$\mathrm{PFC\_OUT(V)} = \frac{3.0\times(\mathrm{R89}+\mathrm{R91}+\mathrm{R92}+\mathrm{R227})}{(\mathrm{R90}+\mathrm{R227})}$$

To change the output voltage of the PFC circuit, the values of the resistors for monitoring the AC line voltage (R1, R2, R94, R95 and R228) also must be changed. The output voltage of the PFC circuit in this power supply is initially programmed to around 380 V using the following resistors:

R90=R2=23.2 kΩ, R227=R228=680 Ω, R1=R89=R91=R92=R94=R95=1 MΩ

Adjust these values to program the output voltage as required.

Switching frequency

The switching frequency of the PFC circuit can be programmed with an external resistor (R100). The switching frequency is given by the following equation:

$$f_{PWM}(\mathrm{kHz}) = \frac{7500}{\mathrm{R100}\left(\mathrm{k\Omega}\right)}$$

Initially, the switching frequency is programmed to around 60 kHz with R100 = 124 kΩ. Adjust the R100 value to program the switching frequency as required.

Soft-start

The soft-start time of the PFC circuit can be programmed with an external capacitor (C49). The soft-start time is given by the following equation:

$$T_{SS}(\mathrm{s}) = \mathrm{C49} \times \frac{2.25(\mathrm{V})}{10(\mu\mathrm{A})}$$

Initially, the soft-start time is programmed to around 106 ms with C49 = 470 nF. Adjust the C49 value to program the soft-start time as required. It is necessary to ensure that the current limiter does not operate during soft-start operation and that the output voltage returns to a normal range during restart operation after the hold-up period.

The figures below show examples of simulation result of soft-start time. Fig. 2.2.2 shows soft-start time at C49 = 470 nF and Fig. 2.2.3 shows soft-start tine at C49 = 220 nF. It is confirmed that soft-start time varies depending on C49 value.

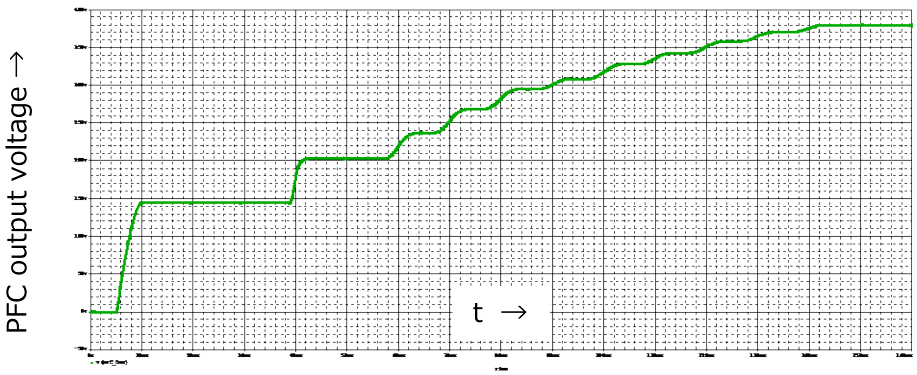

Fig. 2.2.2 Simulation result at C49 = 470 nF

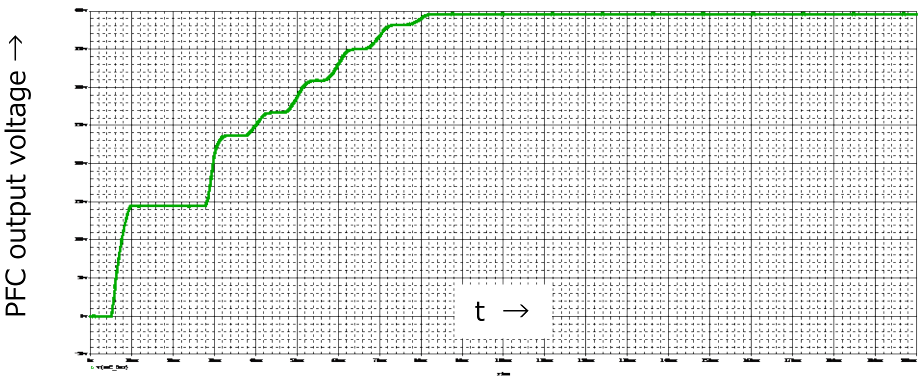

Fig. 2.2.3 Simulation result at C49 = 220 nF

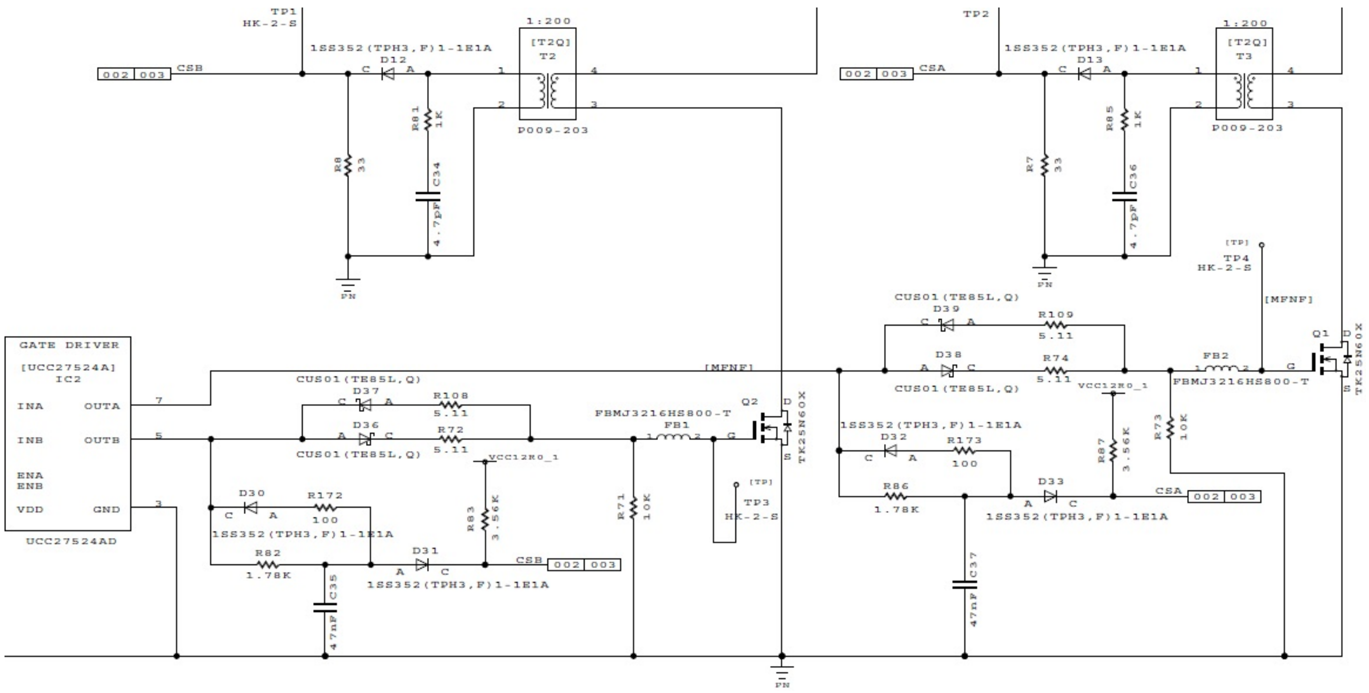

Fig. 2.2.4 PFC Circuit 2 (around Power MOSFETs)

Current limiter

The current limit of the PFC circuit can be programmed with current transformers (T2 and T3), current sense resistors (R7and R8) and limit-setting resistors (R96 and R97). When a current reaches the programmed limit, the UCC28070A disables the gate drive signals (GDA and GDB). The current limit is given by the following equation:

$$\mathrm{I\_limit} = \left(\frac{\mathrm{POUT} \times \sqrt{2}}{\mathrm{efficiency}, \eta(\%) \times \mathrm{VinAC}} \right) \times \mathrm{margin}$$

Suppose that POUT=800 W, efficiency=90%, ΔI = 4.45 A, margin = 1.2. Then, when VinAC=90 V, the current is initially limited to 18.78 A.

Adjust these values to program the current limit as required.

Gate drive circuit

The design of the gate drive circuit affects both efficiency and EMI noise. In general, since efficiency and EMI noise have a trade-off relationship, balancing them is necessary. If EMI noise must be reduced, it is recommended to increase the values of the gate resistors (R72, R74, R108 and R109) and check the resulting noise level. The gate drive circuit of this power supply is configured so as to allow the MOSFET turn-on and turn-off times to be adjusted separately. If it is known when noise is generated (during either the turn-on or turn-off period), it is unnecessary to adjust all resistors. If noise occurs during the turn-on period, noise can be reduced by adjusting R72 and R74. If noise occurs during the turn-off period, noise can be reduced by adjusting R108 and R109. Increasing the values of the gate resistors slows down switching, decreasing efficiency. If the gate resistors are adjusted, it is necessary to ensure that the efficiency and the thermal performance meet their specification requirements. If the noise level is improved by adjusting either one of the turn-on or turn-off periods, the resulting efficiency degradation can be smaller compared with a situation where both turn-on and turn-off periods need to be adjusted.

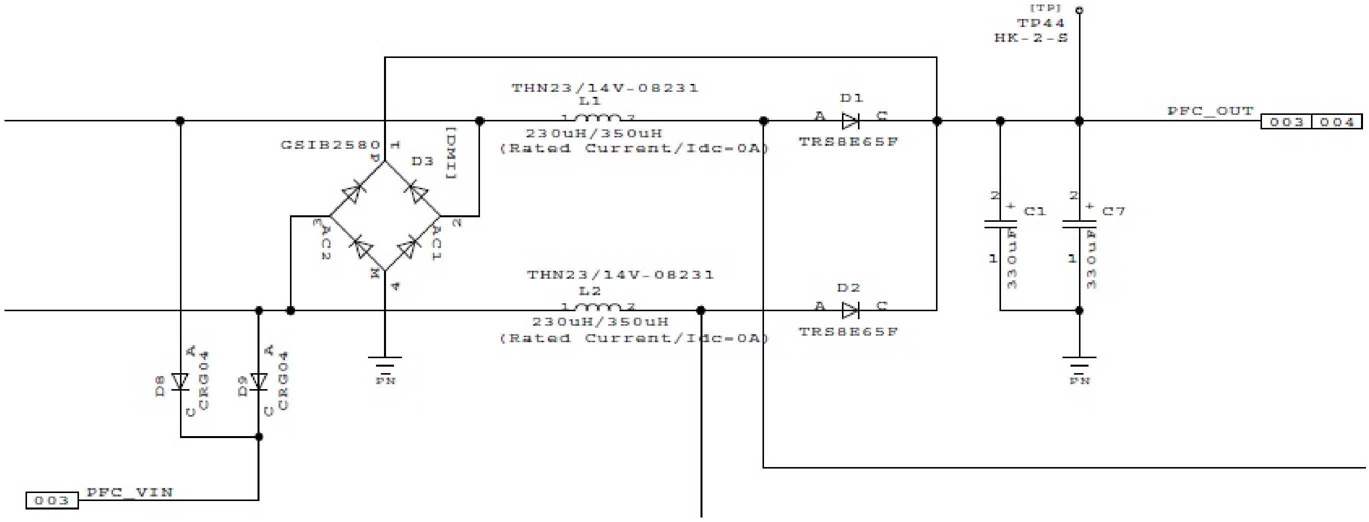

Fig. 2.2.5 PFC Circuit 3 (around Bridge Diodes and Inductors)

Bridge diode

A bridge configuration diode (D3) is used for the rectification diodes. Since this power supply uses a semi-bridgeless topology, the diodes between Pin 2 and Pin 1 and those between Pin 3 and Pin 1 participate in rectification only during power-up (and not thereafter). It is possible to replace this diode bridge (D3) with a combination of a half-bridge and surface-mount diodes. The surface-mount diodes must have a sufficient current capability to withstand an inrush current.

Output capacitors

The values of the output capacitors (C1 and C7) are calculated based on the required hold-up time, which is given by the following equation:

$$\mathrm{Thold} = \mathrm{Cout} \times \frac{(\mathrm{Vout\_PFC}^2 - \mathrm{Vmin}^2)}{2 \times \mathrm{Pout}}$$

where, Cout = output capacitance value, Vout_PFC = output voltage,
Vmin = minimum output voltage limit, and Pout = maximum output power

The initial hold-up time is programmed to 13.6 ms, assuming:

Cout = 660 μF, Vout_PFC = 380 V, Vmin = 280 V, Pout = 1600 W

Adjust the values of the output capacitors to program the hold-up time as required. If there is a requirement for output current ripple, calculate the values of output capacitances necessary to meet the current ripple specification. Compare them with the capacitor values necessary to meet the hold-up time requirement and use capacitors with the larger values. In selecting output capacitors, it is also necessary to consider the nominal tolerance of capacitor values and the aging degradation of capacitors.

Inductors

If the inductor ripple current, ΔI, is set within 30% of the AC line peak current (ACin_peak), the values of the inductors (L1 and L2) are given by the following equation:

$$\mathrm{ACin\_peak} = \frac{\mathrm{Pout} \times \sqrt{2}}{\mathrm{VinAC} \times \eta}$$

where, VinAC = input voltage, Vout_PFC = PFC output voltage, F = switching frequency, and
η = PFC efficiency

$$\Delta \mathrm{I} = \mathrm{ACin\_peak} \times 30\%$$

$$\mathrm{L} = \sqrt{2} \times \mathrm{VinAC} \times \frac{(\mathrm{Vout\_PFC} - \mathrm{VinAC})}{\mathrm{Vout\_PFC} \times \Delta \mathrm{I} \times \mathrm{F}}$$

If VinAC = 90 V, Vout_PFC = 380 V, F=60 kHz , Pout=900 W, η=90% and L is 343 μH, then L is calculated to be 343 μH. Therefore, a 350 μH inductor is used in this power supply.
The peak current that flows through the inductors is given by the following equation:

$$\mathrm{IL\_peak} = \mathrm{ACin\_peak} + \frac{\Delta \mathrm{I}}{2}$$

Since ACin_peak = 15.7 A and ΔI=4.7 A, IL_peak is calculated to be 18.1 A. Therefore, inductors rated above 18.1 A should be used.

2.3. Phase-Shift Full-Bridge (PSFB) Circuit Design

This power supply provides 12 V, following the semi-bridgeless PFC circuit. The PSFB circuit uses the UCC28950 controller from Texas Instruments to improve efficiency since it is capable of zero-voltage switching (ZVS) operation for a wide range of loads. This section describes the design considerations for the PSFB circuit of this power supply. Refer to the data sheet and application notes for the UCC28950 on the details of a circuit design around the controller. Refer to the *1.6 kW Server Power Supply Reference Guide* for its specification.

Simulation circuit which can simulate the PSFB circuit operation is provided on the web as “RD001-SPICE02”. Refer to this file when the circuit is being designed if necessary. Maximum step size is changeable for actual calculation. However, if different value from original one is chosen, calculation time will increase.

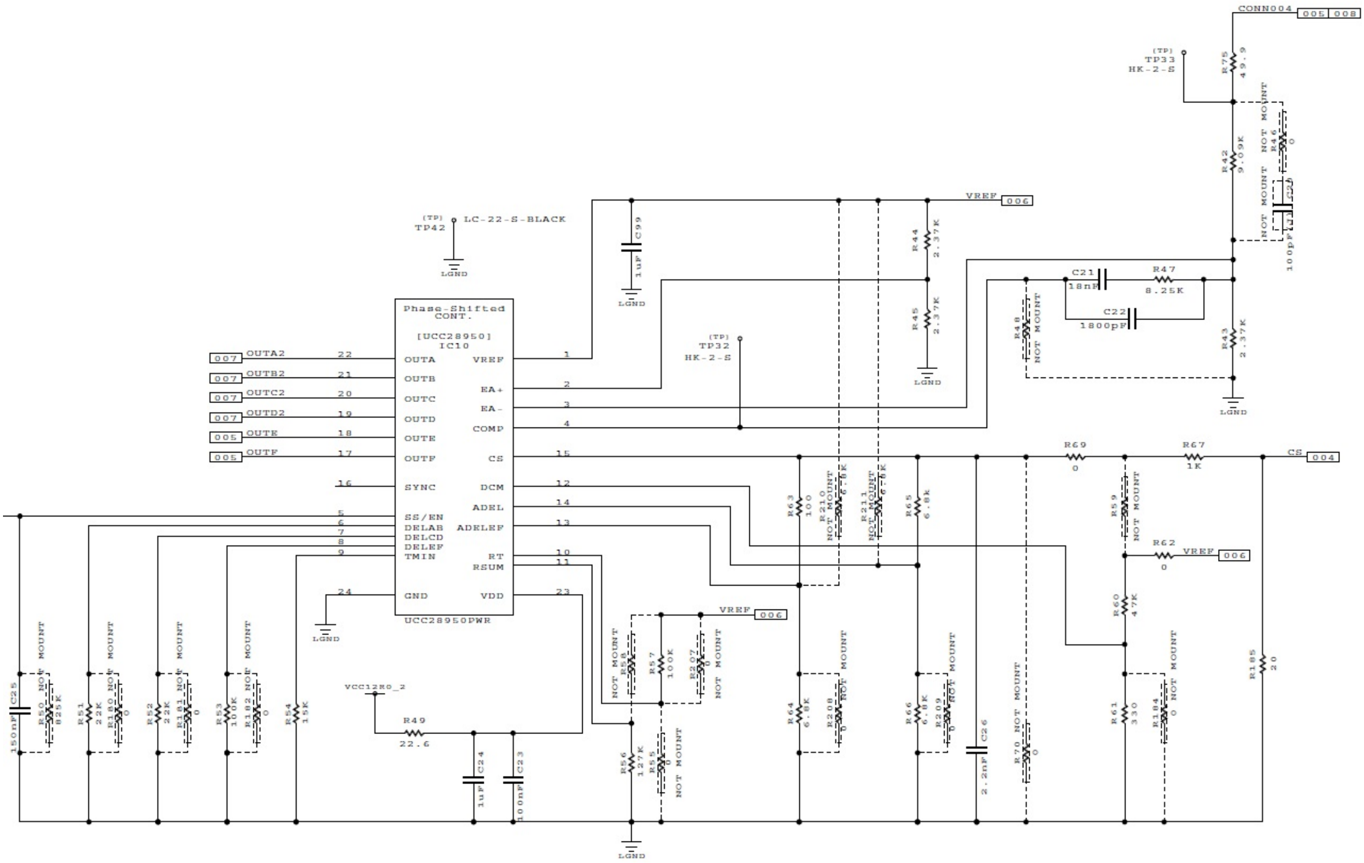

Fig. 2.3.1 PSFB Circuit 1 (around Controller)

Output voltage

The output voltage of the PSFB circuit can be programmed with external resistors (R42, R43, R44, R45 and R75). Its output voltage is calculated as follows, based on the values of these resistors and the internal reference voltage, VREF, of the UCC28950 (5.0 V):

$$\mathrm{VOUT(V)} = \frac{\mathrm{VREF(V)} \times \mathrm{R45} \times (\mathrm{R43} + \mathrm{R42} + \mathrm{R75})}{(\mathrm{R44} + \mathrm{R45}) \times \mathrm{R43}}$$

Initially, the output voltage is programmed to 12.14 V with R42=9.09 kΩ, R43=R44=R45=2.37 kΩ and R75= 49.9 Ω. Adjust the values of these resistors to program the output voltage as required.

The figures below show examples of simulation result of output voltage. Fig. 2.3.2 shows output voltage at R44 = 2.37 kΩ and Fig. 2.3.3 shows output voltage at R44 = 2.2 kΩ. It is confirmed that output voltage varies depending on R44 value.

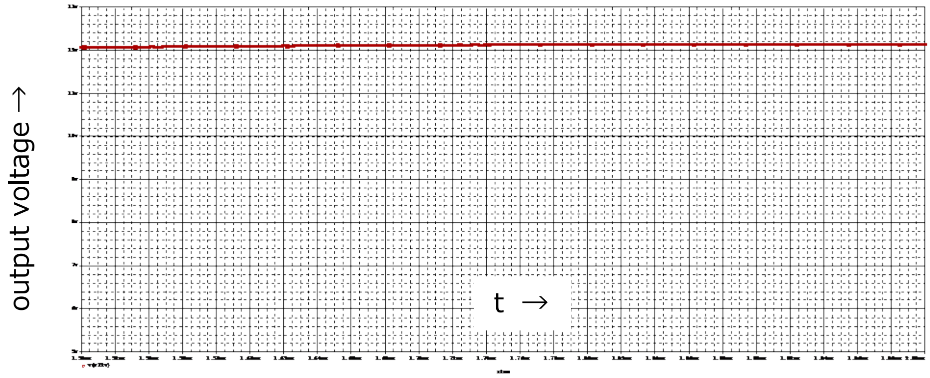

Fig. 2.3.2 Simulation result at R44 = 2.37 kΩ

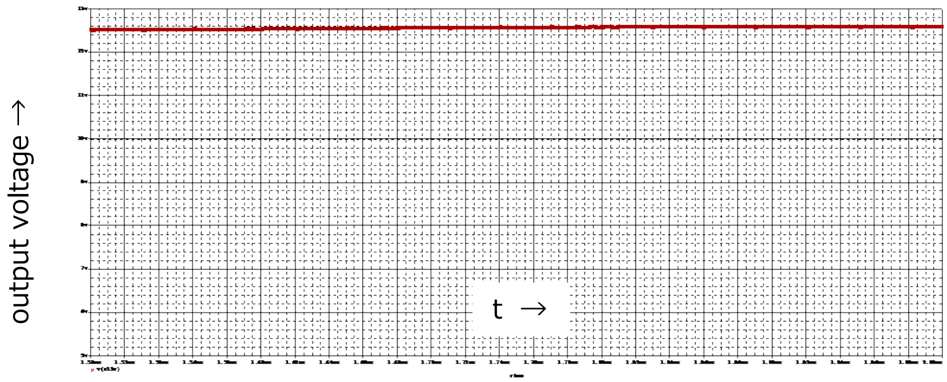

Fig. 2.3.3 Simulation result at R44 = 2.2 kΩ

Switching frequency

The switching frequency of the PSFB circuit can be programmed with an external resistor (R57). Its switching frequency is given by the following equation:

$$f_{PWM}(kHz) = \frac{2.5 \times 10^3}{\left(\frac{R57\left(k\Omega\right)}{VREF(V) - 2.5} + 1\right)}$$

Initially, the switching frequency is programmed to 60.98 kHz with R57 = 100 kΩ. Adjust the R57 value to program the switching frequency as required.

Soft-start

The soft-start time can be programmed with an external capacitor (C25). It is given by the following equation:

$$T_{SS}(s) = \frac{C25(\mu F) \times \left(\frac{VREF(V) \times R45}{R44 + R45} + 0.55\right)}{25}$$

Initially, the soft start time is programmed to 18.3 ms with C25 = 150 nF. Adjust the C25 value to program the soft-start time as required. It is necessary to ensure that the current limiter does not operate during the soft-start period.

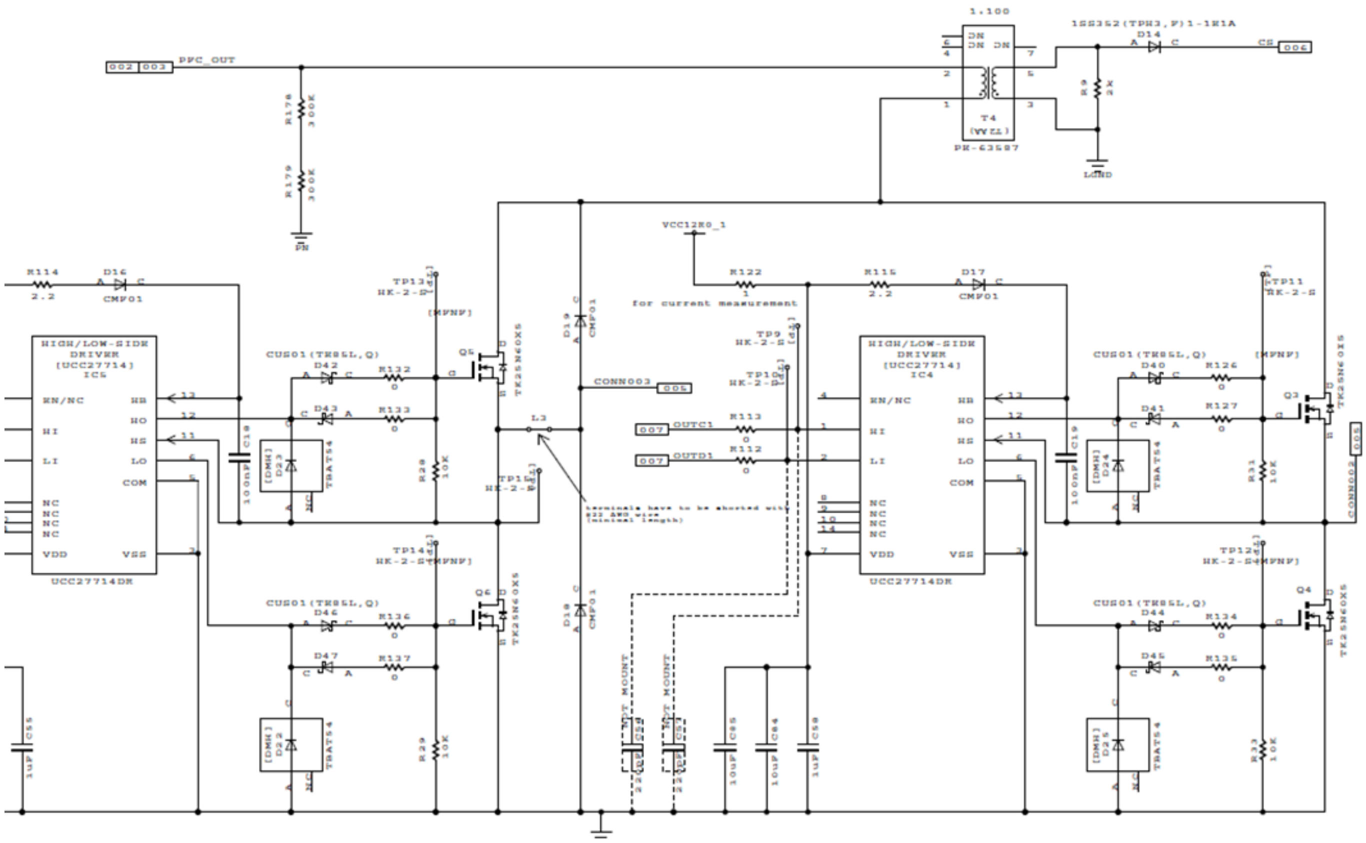

Fig. 2.3.4 PSFB Circuit 1 (around Power MOSFETs on Primary Side)

Current limiter

The current limiter of the PSFB circuit can be programmed with a current transformer (T4), a current sense resistor (R185) and the internal threshold voltage of the UCC28950 for current limiting (2.0 V). When a current reaches the limit, the UCC28950 controls the MOSFET drive on the primary side to prevent an abnormal current from flowing to the secondary side. The current limit is given by the following equation:

$$I\_limit = \frac{2.0}{R185 \times \text{transfomer turns ratio}}$$

Initially, the current limit is programmed to 10 A with R185=20 Ω and a transformer with a turns ratio of 100:1. Adjust these value to program the current limit as required.

Gate drive circuit

The gate drive circuit affects both efficiency and EMI noise. In general, since efficiency and EMI noise have a trade-off relationship, balancing them is necessary. The PSFB circuit is designed for ZVS operation. However, if the PSFB circuit has a hard-switching region that causes EMI noise, it is recommended to increase the values of the gate series resistors (R126, R127, and R132 to R137) for the MOSFETs (Q3 to Q5) concerned and check the resulting noise level. As is the case with the gate drive circuit for the PFC, the gate drive circuit for the PSFB can also be adjusted for turn-on and turn-off periods separately. If the noise level is improved by adjusting either one of the turn-on or turn-off periods, the resulting efficiency degradation can be smaller compared with a situation where both turn-on and turn-off periods need to be adjusted.

Transformers

When the on-duty cycle of the PSFB synchronous rectification circuit in the steady state is programmed to 60%, the secondary side requires a rectangular waveform at around 20 V since the output voltage is 12 V. Center-tapped transformers (T5 and T6) with a turns ratio of 20:1:1 are used since the PFC output voltage of the 1.6 kW server power supply is 380 V. This causes a 19 V rectangular waveform to appear on the secondary side. In addition, it is necessary to carefully consider isolation voltage between the primary and secondary sides, winding temperature rise, magnetic flux saturation, core loss and so on. Refer to the bill of material for the specification of the transformers in the 1.6kW server power supply.
The 1.6 kW server power supply performs ZVS operation by using leakage inductance of the transformers. Insufficient resonance due to leakage inductance makes it impossible to achieve ZVS operation, which in turn causes its efficiency to decrease or the EMI noise to increase. When a transformer has been replaced, it is necessary to ensure that ZVS is achieved for a wide range of loads. If ZVS is not achieved due to a lack of resonance as a result of transformer replacement, attach a resonant coil (L3) on the PCB to enable ZVS for a wide range of loads. Initially, the 1.6 kW server power supply can achieve ZVS with transformer leakage inductance and does not need a resonant coil; therefore, a jumper is attached to L3.

Output capacitors

It is necessary to ensure that the output capacitors meet the system requirement for the output voltage ripple range. The output voltage ripple, Vripple, is a composite waveform of ripple current, ΔI, generated by switching and output capacitor ESR, capacitance (Cap) and ESL. Let the switching voltage be Vsw, the output voltage be Vout and the switching frequency be F. Then, the voltages generated by ESR, Cap and ESL are given by the following equations:

$$\mathrm{Vripple\_ESR} = \Delta\mathrm{I} \times \mathrm{ESR}$$

$$\mathrm{Vripple\_Cap} = \frac{\Delta\mathrm{I}}{8 \times \mathrm{Cout} \times \mathrm{F} \times 2}$$

$$\mathrm{Vripple\_ESL} = \frac{\mathrm{Vsw} \times \mathrm{ESL}}{\mathrm{L}}$$

where,

$$\Delta\mathrm{I} = \frac{(\mathrm{Vsw} - \mathrm{Vout}) \times \mathrm{Vout}}{\mathrm{Vsw} \times \mathrm{F} \times 2 \times \mathrm{L} \times 2(\mathrm{phases})}$$

ΔI is calculated to be 20.5 A if Vsw=19 V, Vout = 12.14 V, F=60.98 kHz and L=3.5 μH.
Initially, Vripple_ESR=82 mV, Vripple_Cap=2.8 mV, and Vripple_ESL=5.4 mV when Cout = 1500 μF x 5 pcs, ESR=20 mΩ, ESL=5 nH and L=3.5 μH.
Since the voltage generated by Cap is not in phase with the voltages generated by ESR and ESL, they cannot be added in a simple manner. However, a simple addition can be used as a guide because Vripple Cap is very small. Adjust the values of output capacitors to meet the required ripple voltage. It is necessary to ensure that both undershoot and overshoot voltages at load transients are within the range of voltage specifications and that ripple current is within the rated range of the output capacitor.

2.4. ORing Circuit Design

This power supply contains an ORing circuit for the 12 V output to achieve N+1 redundant operation if needed. The ORing circuit consists of the TPS2412 controller from Texas Instruments (IC8) and switching MOSFETs (Q15 to Q24). If the output of this power supply is parallel-connected with other power supply outputs and the output voltage from this power supply is higher than the other outputs, the TPS2412 turns on the MOSFETs to supply a current to the output. If the output voltage from this power supply is lower than the others, the TPS2412 turns off the MOSFETs to prevent a current from flowing back into this power supply. This section describes design considerations for the ORing circuit in this power supply. Refer to the datasheet and application notes for TPS2412 for details on the circuit design around the controller. It is necessary to choose a MOSFET and its quantity that meet system requirements for a voltage drop and a power loss due to on-resistance. This power supply has 10 instances of the TPHR9003NC. Since the MOSFET on-resistance increases at high temperature, the system ambient temperature and a MOSFET temperature rise at the maximum load must be considered for MOSFET selection.

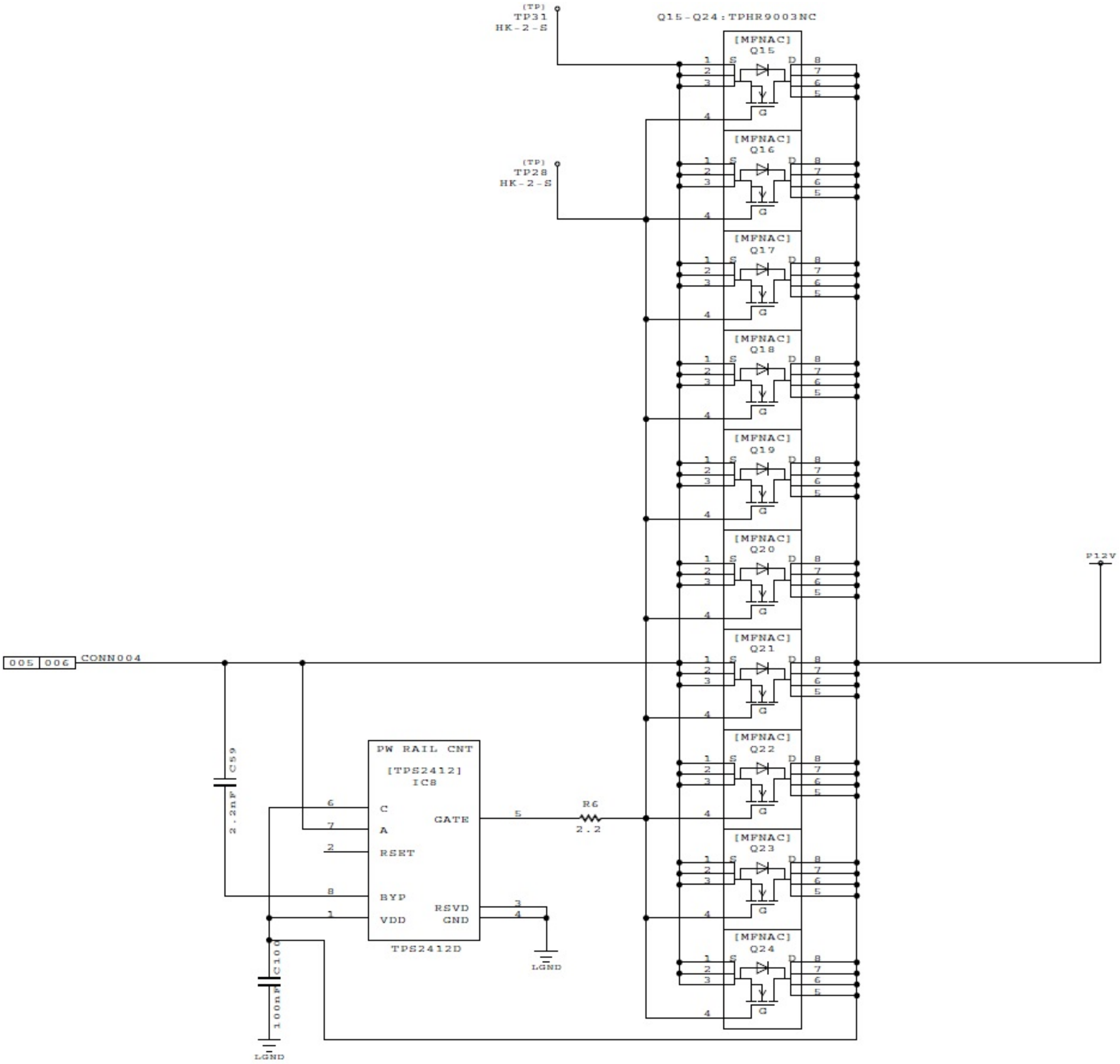

Fig. 2.4.1 ORing Circuit

3. PCB Design

This section describes considerations for the PCB design for this power supply.

3.1. PWB Trace Design

Creepage distances

It is necessary to provide appropriate clearance and creepage distances to meet a system's safety requirements. The 1.6 kW server power supply have creepage distances shown below. It is necessary to carefully consider creepage distances because the required creepage and clearance distances vary depending on the system environment, materials used, their contamination levels, humidity and altitude (atmosphere pressure).

Table 3.1.1 Minimum Design Creepage Distances

Line 1	Line 2	Creepage Distance between Line1 and Line 2
L on primary side	N on primary side	2.5 mm
PFC output	PN (GND on primary side)	4 mm
All lines on primary side	FG	4 mm
Primary side (coupler)	Secondary side (coupler)	8 mm
Primary side (transformer)	Secondary side (transformer)	10 mm

Current capability

Each trace on the PWB must have an appropriate width to prevent any problem from occurring due to a temperature rise and an IR drop caused by traces when the maximum current for each trace flows.

3.2. PFC Circuit Trace Design

This section describes PCB design considerations for the PFC circuit. Refer to the datasheet and application notes for the Texas Instruments UCC28070A for a layout around the controller.

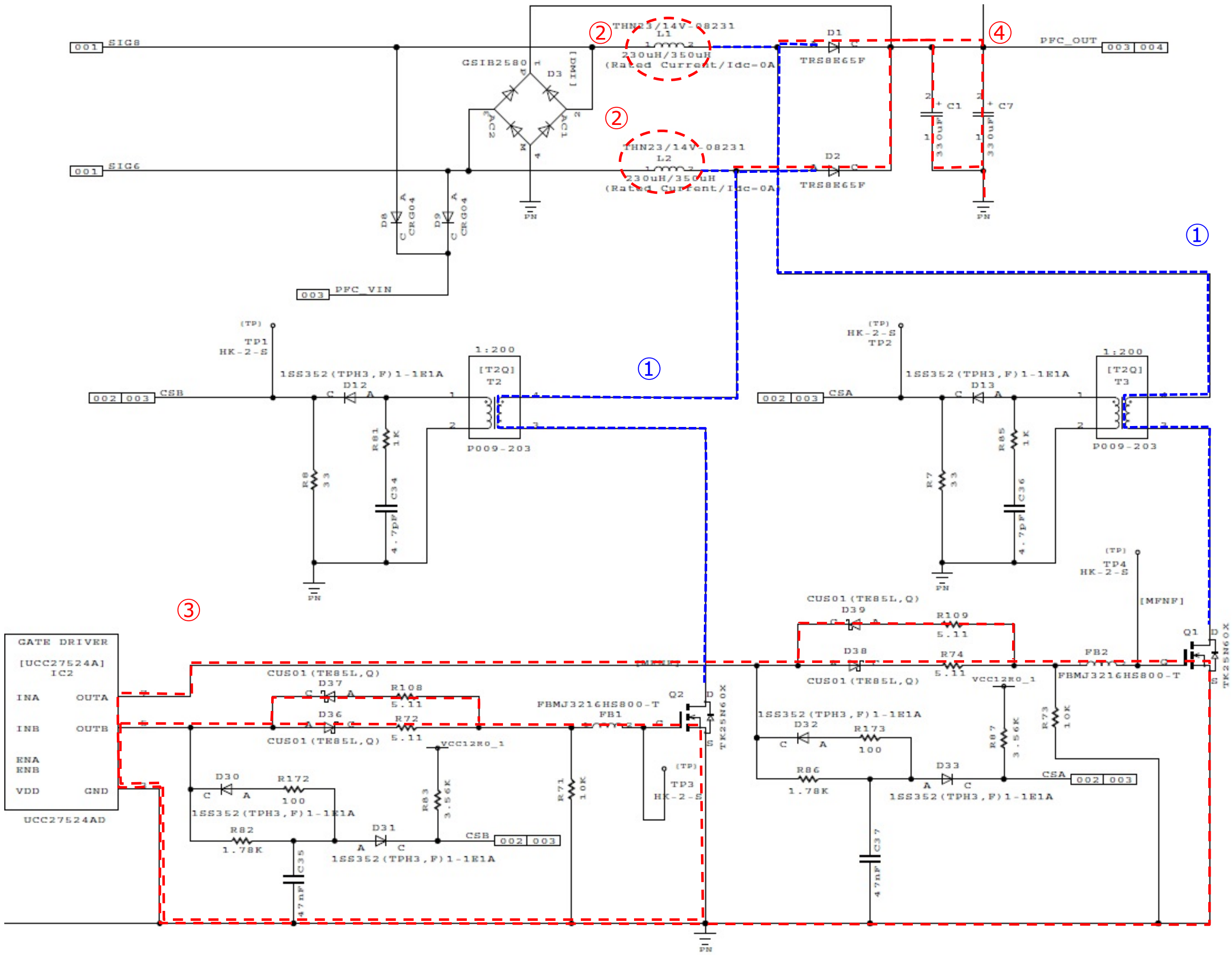

Fig. 3.2.1 Considerations for the PFC Circuit

1. Place the UCC28070A PFC controller (IC3) far from the following areas:
   Around switching nodes: Line between L1, Q1 and D1, and line between L2, Q2 and D2 (① in the figure)
   Around PFC choke coils: Within 2.5 cm from L1 and L2 (② in the figure)
   Drivers output: Loops formed by IC2-Q1-GND (PN) and IC2-Q2-GND (③ in the figure)
   Around PFC output: Loops formed by L1-D1-C1/C7-GND(PN)-C33/C65 and
   L2-D2-C1/C7-GND(PN)-C33/C65 (④ in the figure)
2. Place each component to minimize the area around the switching node that has a large voltage swing (① in the figure).
3. Minimize the lengths of the drivers output lines (③ in the figure). In order to achieve this, IC2 must be placed near Q1 and Q2. Provide an appropriate trace width to handle the drive current (around 2 A at the peak).
4. If the return paths for the drive current are separate from the GND (PN) plane, separate them from the source terminals of Q1 and Q2.

5. Place the step-up diodes (D1 and D2) and the output capacitors (C1 and C7) as close to each other as possible.
6. Use a Kelvin connection to connect the current sensing lines (CSA and CSB) to GND (PN) and create a feedback loop to IC3 through an area that has low current and voltage swings.

The following image shows the layout of the PFC circuit of this power supply (Layer 1).

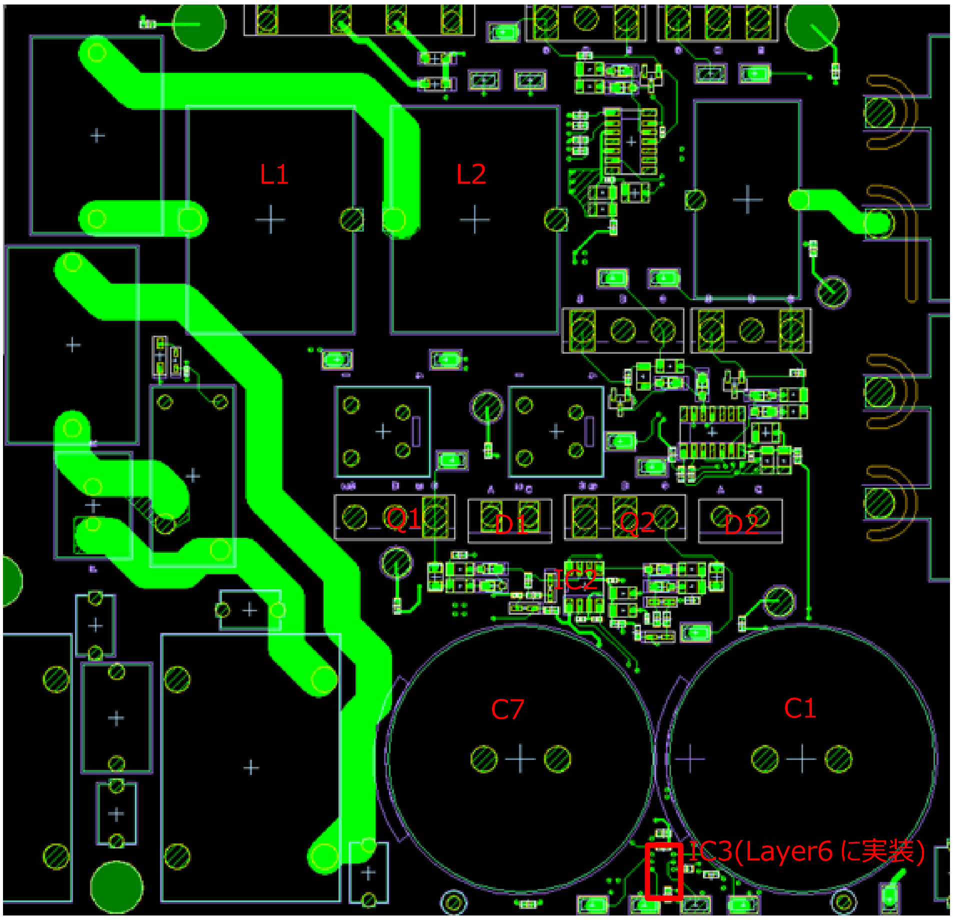

Fig. 3.2.2 PFC Circuit Layout

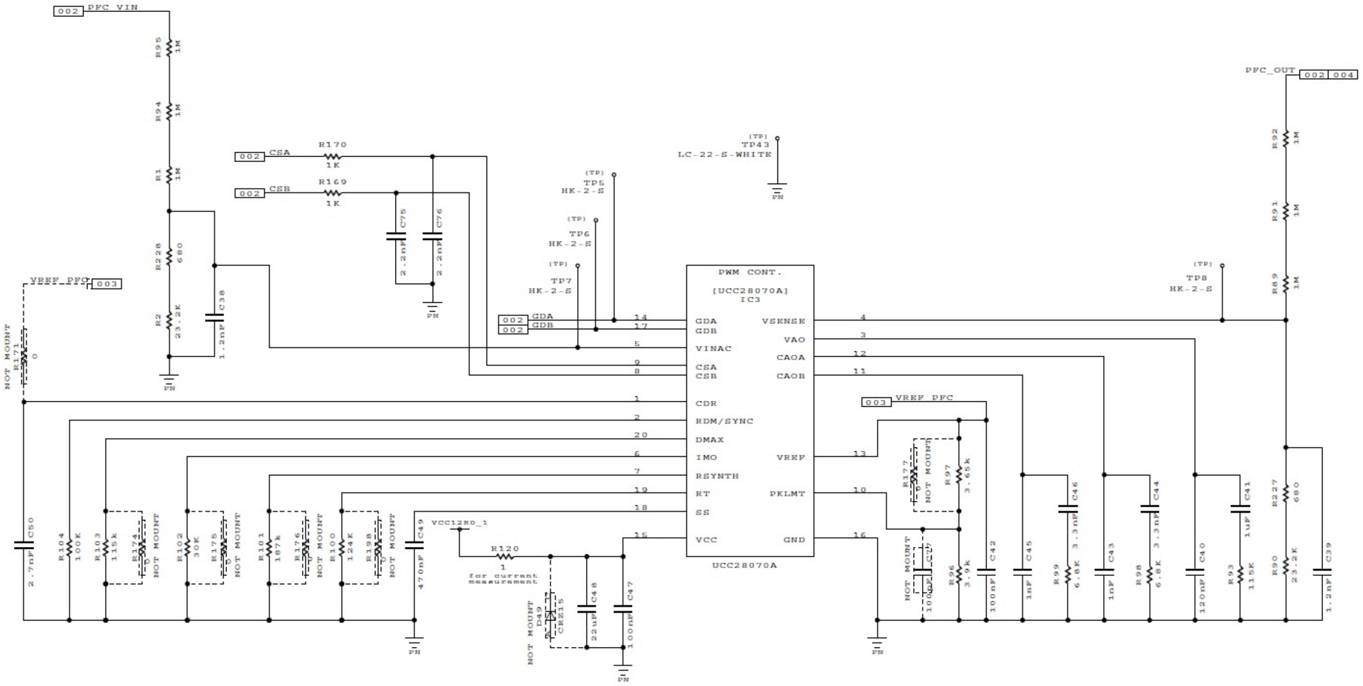

Fig. 3.2.3　PFC Circuit (around Controller)

1. Place all components shown in the figure in the vicinity of IC3.
2. Combine the GND (PN) lines to connect to the IC3 GND terminal. If all components can be placed in the vicinity of IC3, and the GND return paths of the switching and drive currents are not close to the components, the GND lines can be connected to a GND (PN) plane in the vicinity of each component.

3.3. PSFB Circuit Trace Design

This section describes PCB design considerations for the PSFB circuit. Refer to the datasheet and application notes for the Texas Instruments UCC28950 for a layout around the controller.

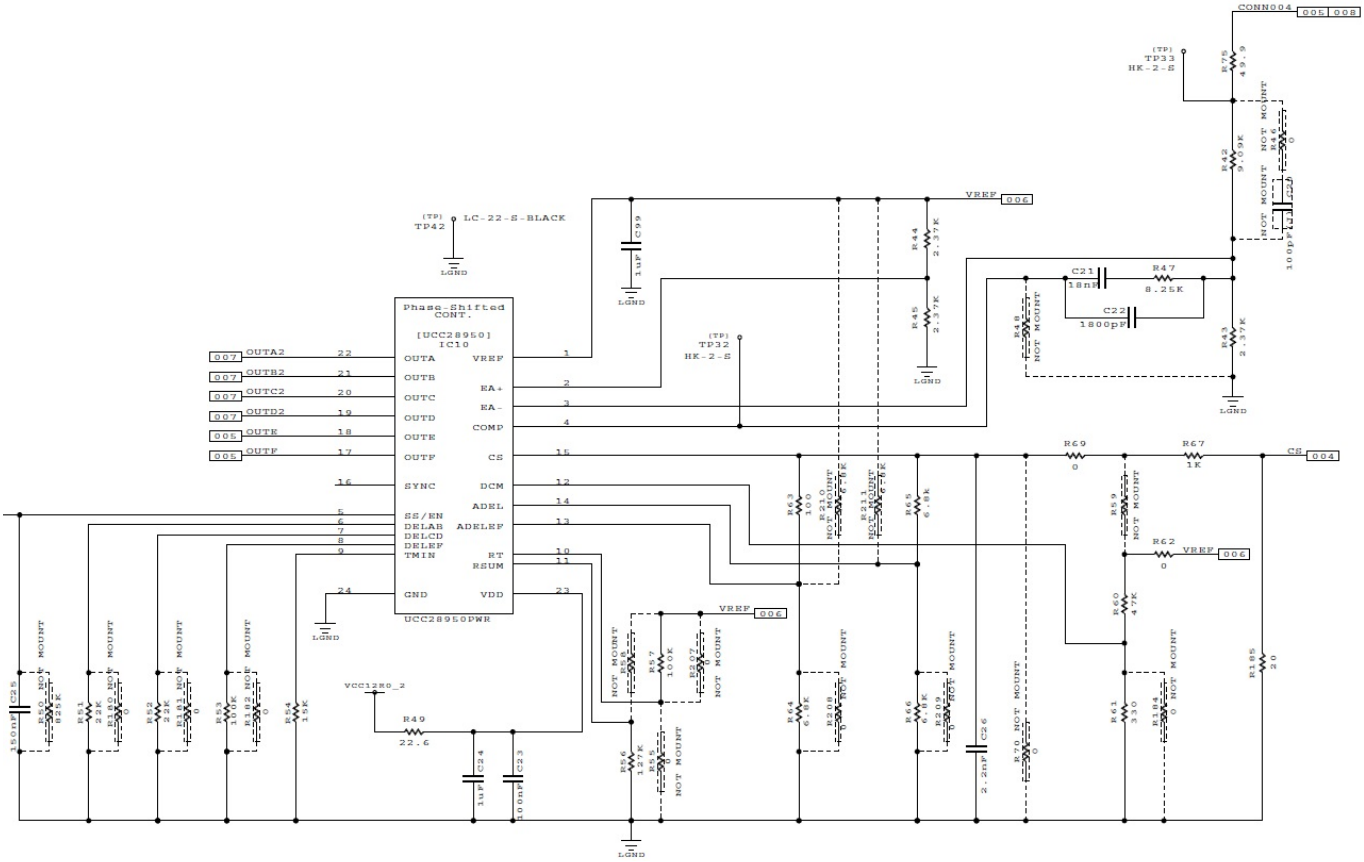

Fig. 3.3.1 PSFB Circuit (around Controller)

1. Place the UCC28950 PSFB controller (IC10) far from the high-current switching circuit on the secondary side, the transformers and the reactors.
2. Place all components shown in the figure near IC10.
3. Combine the GND lines (LGND in the figure) to a single point and connect it with the IC10 GND terminal. If all components can be placed near IC10, and the GND return paths for the switching and driving currents are not near components, the GND lines can be connected to a GND (LGND) plane in the vicinity of each component.

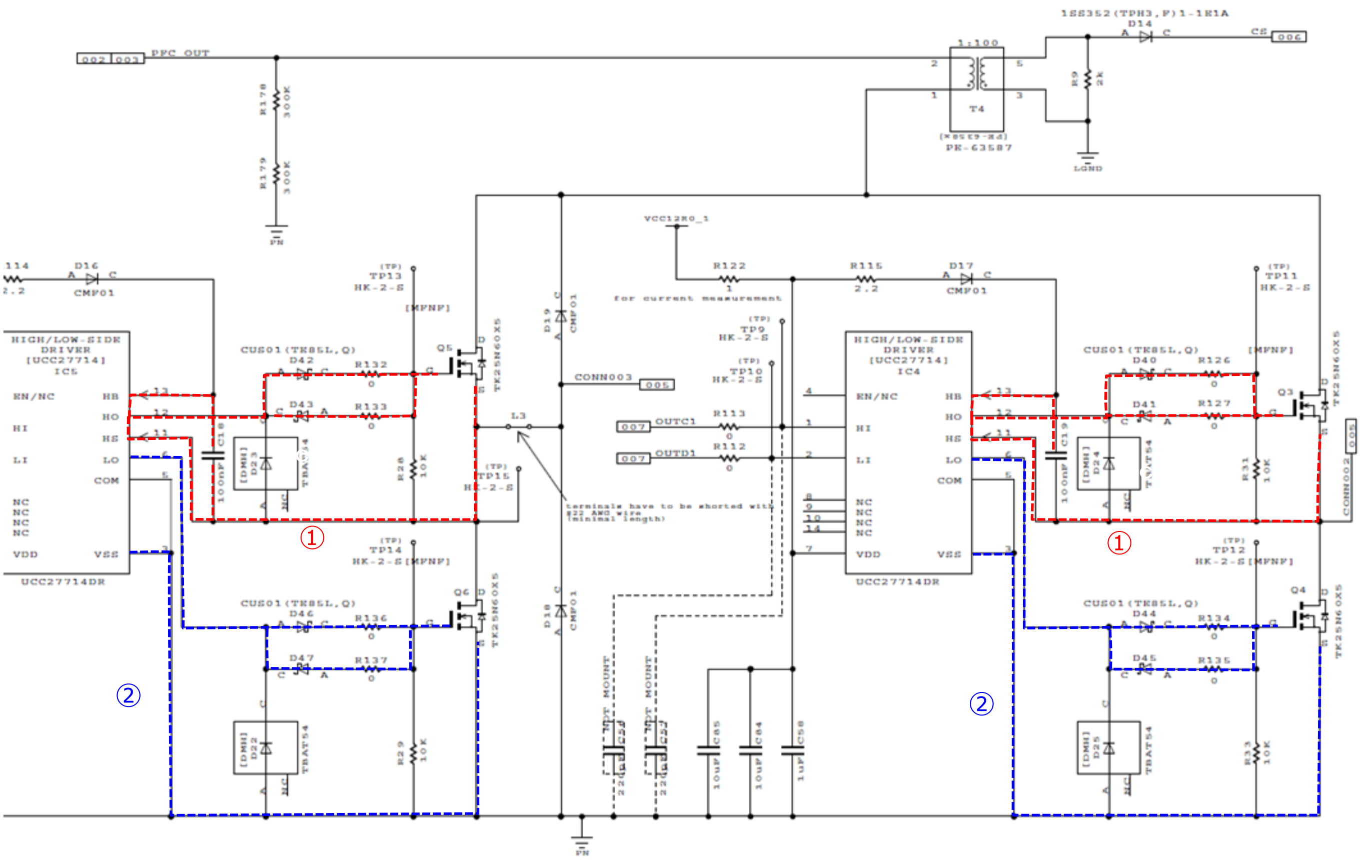

Fig. 3.3.2 Considerations for PSFB Circuit 1

1. Place each component to minimize the areas around switching nodes that have a large voltage swing (① in the figure and lines with the same potential as for ①).
2. Minimize the lengths of driver output lines (① and ② in the figure). In order to achieve this, IC5 must be placed near Q5 and Q6, and IC4 must be placed near Q3 and Q4. Provide an appropriate trace width to handle the peak drive current.
3. Separate the return paths for the Q3 and Q5 drive currents from the source terminals of Q3 and Q5.
4. To separate the return paths for the Q4 and Q6 drive currents from the GND (PN) plane, separate them from the source terminals of Q4 and Q6.
5. Use a Kelvin connection to connect the current sensing line (CS) to GND (LGND) and provide a feedback loop to IC10 through an area that has low current and voltage swings.

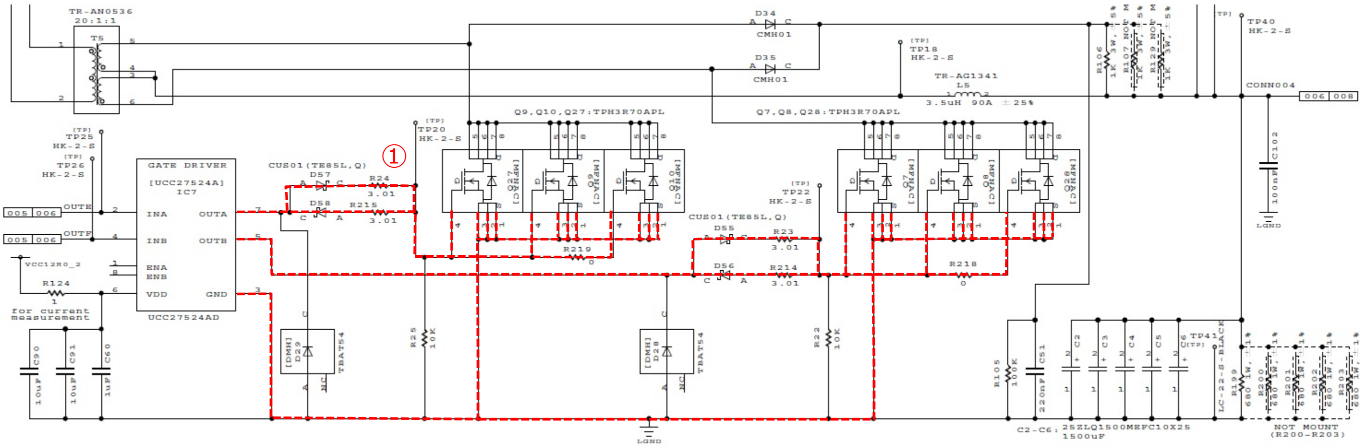

Fig. 3.3.3 Considerations for PSFB Circuit 2

Minimize the lengths of the driver output lines (① in the figure). In order to achieve this, IC7 must be placed near Q7 to Q10, Q27 and Q28. Provide an appropriate trace width to handle the peak drive current. If a GND (LGND) plane is not used for the return paths for the drive current, separate them from the source terminals of Q7 to Q10, Q27 and Q28.

The PSFB in this power supply consists of two phases. It is necessary to apply the same design considerations to both phases.

The following figure shows the layout of the PSFB circuit of this power supply (Layer 1).

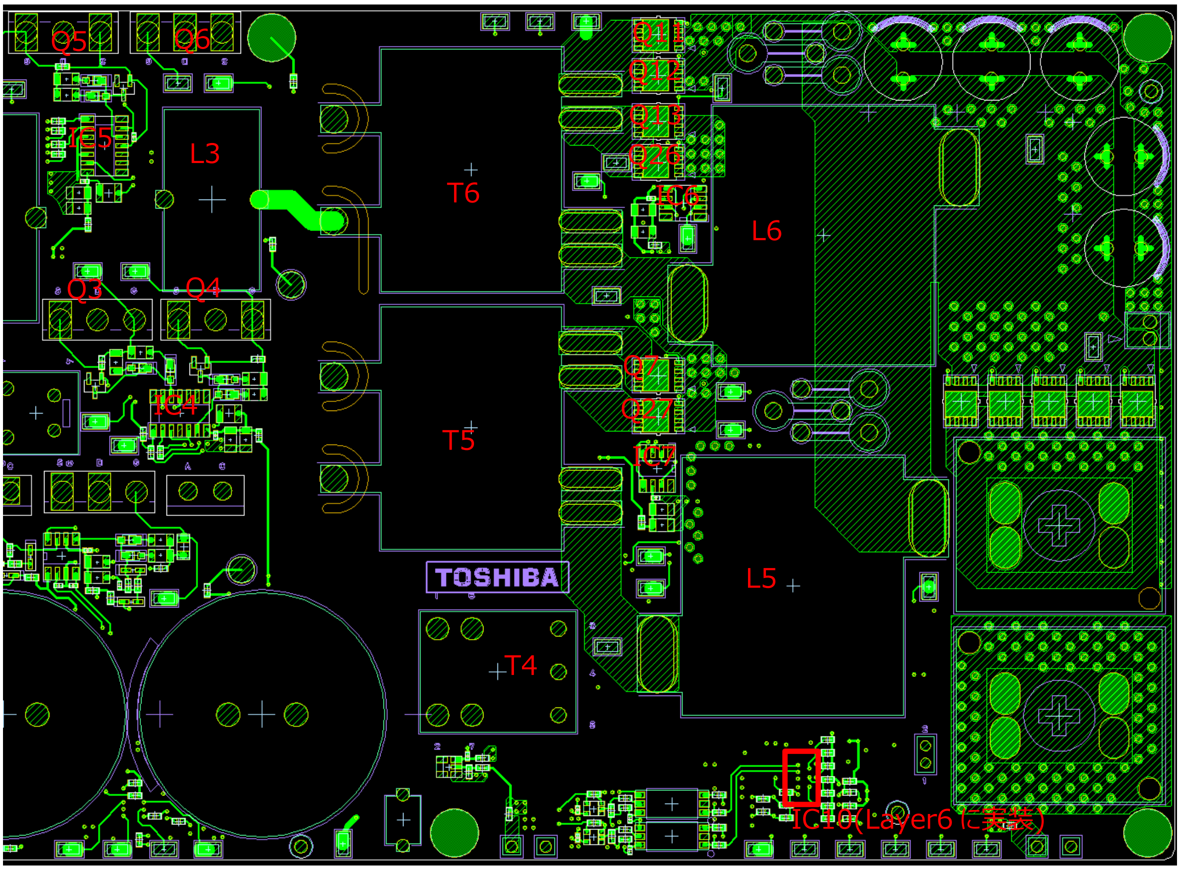

Fig. 3.3.4 PSFB Circuit Layout

3.4. Component Placement (Thermal Design)

This power supply contains a fan because power devices (e.g., MOSFETs, transformers and diodes) heat up when a high-load condition persists. The fan takes the air from the PCB side (right-hand side in the figure) and exhausts the air out of the PCB (left-hand side in the figure). The heatsinks are covered with an aluminum plate to provide air flow paths and thereby improve heat dissipation. Thermal design is necessary to provide each component with an appropriate margin relative to the rated temperature at a system's maximum temperature and load conditions.

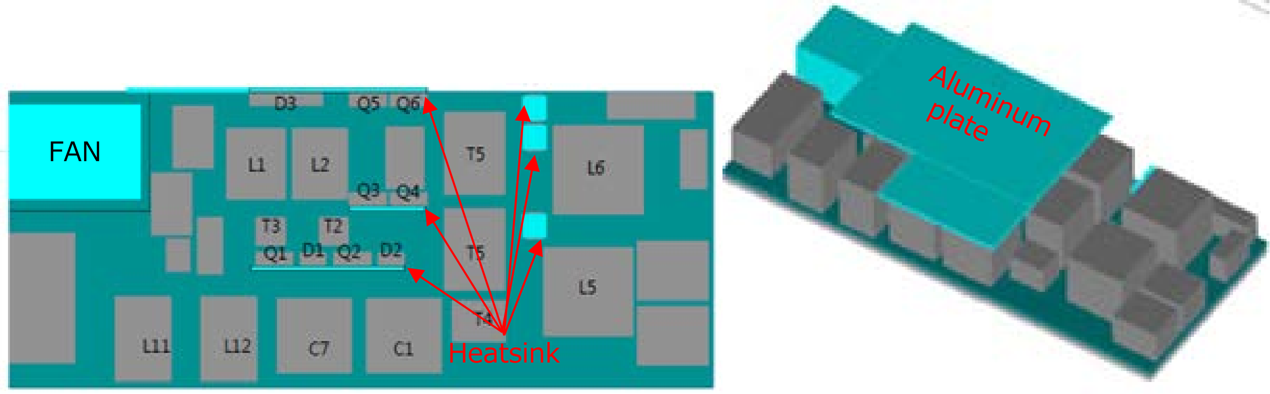

Fig. 3.4.1 Components Placement

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