Load Switch
Application and Operation of the TCK301G, TCK302G, and TCK303G

Reference Guide

RD006-RGUIDE-02

TOSHIBA ELECTRONIC DEVICES & STORAGE CORPORATION

Table of Contents

1. Overview

Fabricated using a high-voltage CMOS process, the TCK301G, TCK302G, and TCK303G load switches operate with an input voltage of up to 28V. These load switches provide inrush current limiting, thermal shutdown, overvoltage lockout, undervoltage lockout, and a flag output signal.

These features make the TCK301G, TCK302G, and TCK303G suitable rapid charging, which is nowadays considered important for applications powered by lithium-ion and other rechargeable batteries, as well as for high-current, high-voltage power management required for systems incorporating power-saving features.

Among the many features of the TCK301G, TCK302G, and TCK303G, this reference guide focuses on their operation and application of the slew rate control circuitry designed for inrush current limiting that is crucial for high-current switching applications.

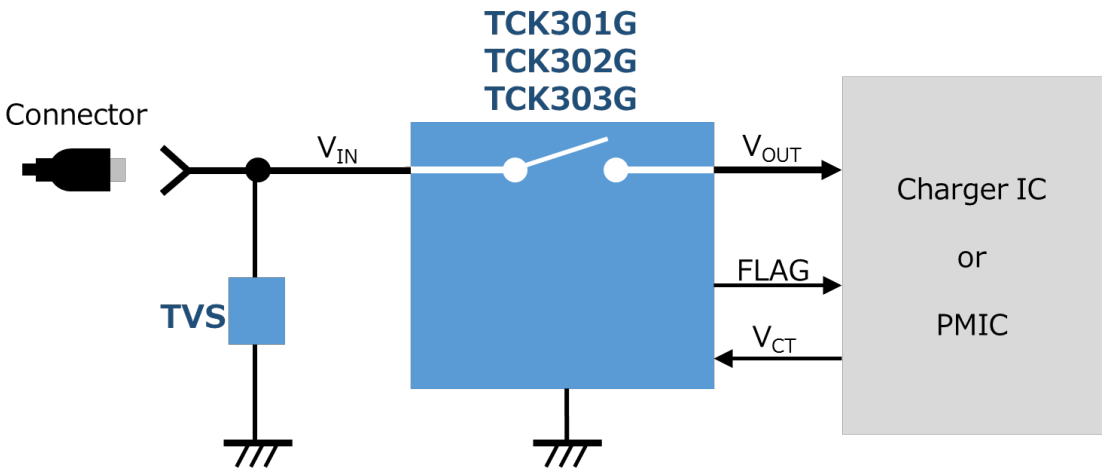
For detail of the other protection features and other details of the TCK301G, TCK302G, and TCK303G, see their datasheet.

To download the datasheet for the TCK301G, TCK302G and TCK303G → Click Here

1.1. Target applications

- Main switches of USB PD-enabled rapid-charging circuits for electronic devices with USB Type-C™ ports
- Main switches of 5 to 12V power supply input circuits that support various modes of rapid charging and wireless power transfer
- Switches for the power management of systems requiring power-saving modes

Circuit example: Main switch of a rapid-charging circuit



* Toshiba offers TVS diodes for charger and other high-current applications.

For details of TVS diodes → Click Here

2. Application circuit example and bill of materials

2.1. Application circuit example

Figure 2.1.1 shows an example of an application circuit for the TCK301G, TCK302G, and TCK303G.

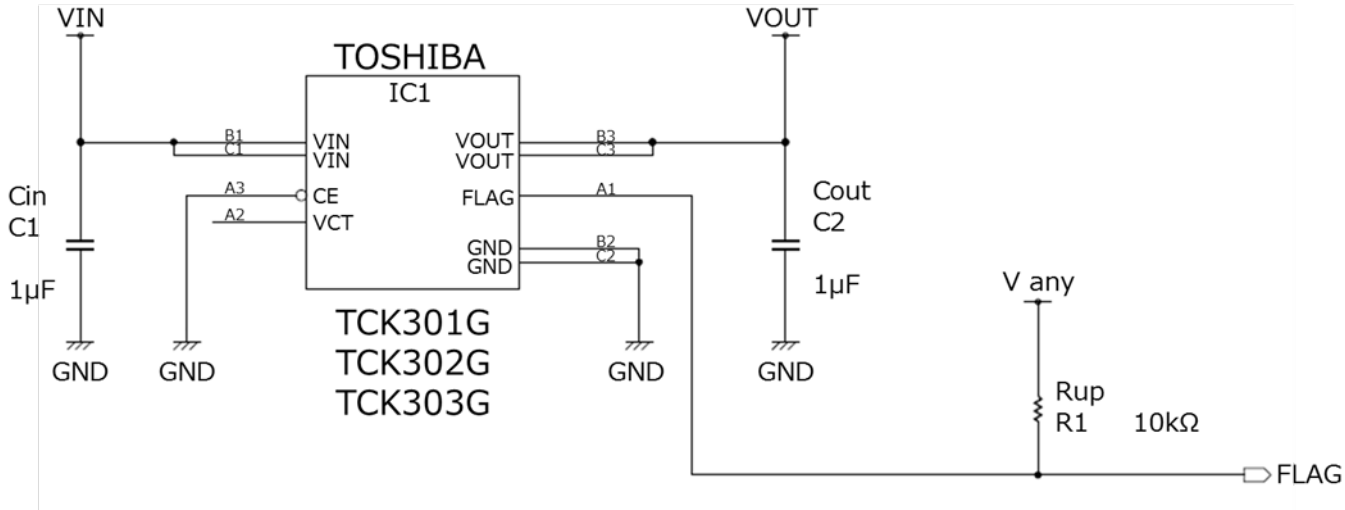


Figure 2.1.1 Application circuit for the TCK301G, TCK302G, and TCK303G

2.2. Bill of materials

Table 2.2.1 Bill of materials

No.	Ref.	Qty	Value	Part Number	Manufacturer	Description	Packaging	Typical Dimensions mm (inches)
1	IC1	1	—	TCK301G TCK302G TCK303G	TOSHIBA	Load Switch IC	WCSP9	1.5 x 1.5
2	R1	1	10kΩ			Carbon, ±5%	—	1.0 x 0.5 (0402)
3	C1	1	1µF			Ceramic, 50V, ±10%	—	3.2 x 1.6 (1206)
4	C2	1	1µF			Ceramic, 50V, ±10%	—	3.2 x 1.6 (1206)

3. Inrush current limiting

The TCK301G, TCK302G, and TCK303G incorporate a slew rate control driver (i.e., a slow starter circuit) designed to limit inrush current during switching transitions. In cases where a power management IC supplies power to multiple lines, a system might experience an overall shutdown or failure if inrush current momentarily exceeds the current limit of the power management IC during its switching transitions. A similar situation might also occur in the load circuit. To prevent a system shutdown or failure, it is necessary to limit the inrush current. Figure 3.1 illustrates the output voltage (V_{OUT}) and output current (I_{OUT}) waveforms from circuits with and without a slew rate control driver.

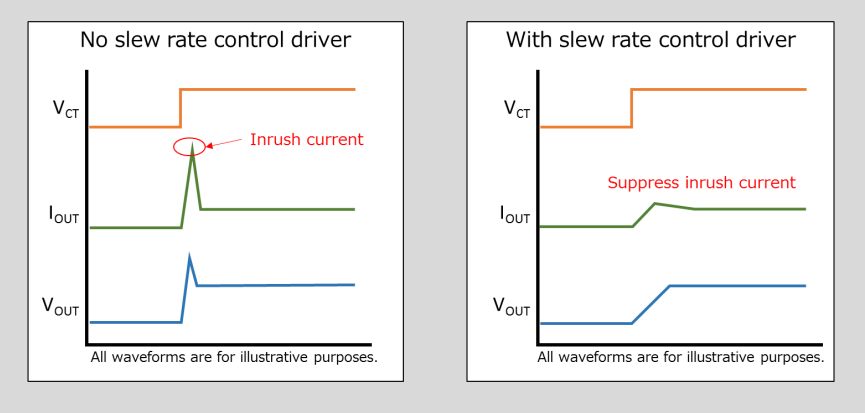
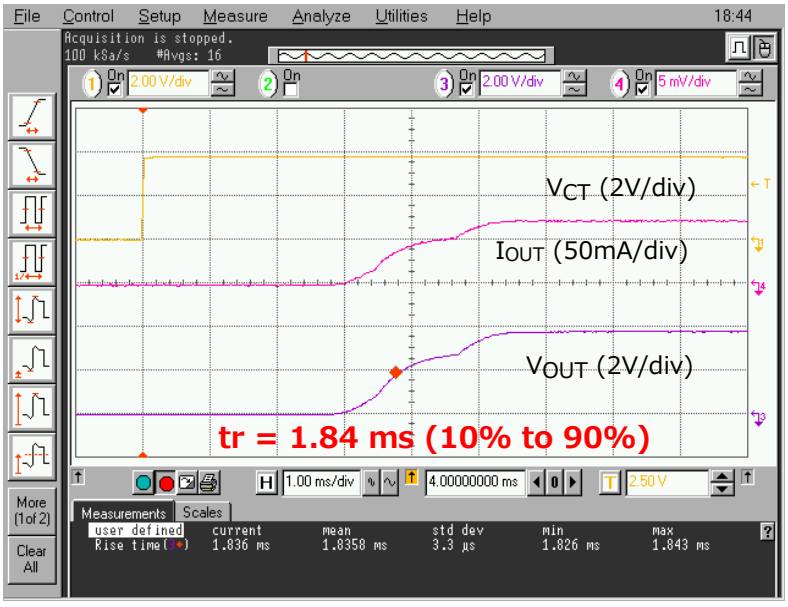


Figure 3.1 Output voltage (V_{OUT}) and output current (I_{OUT}) waveforms from circuits with and without a slew rate control driver

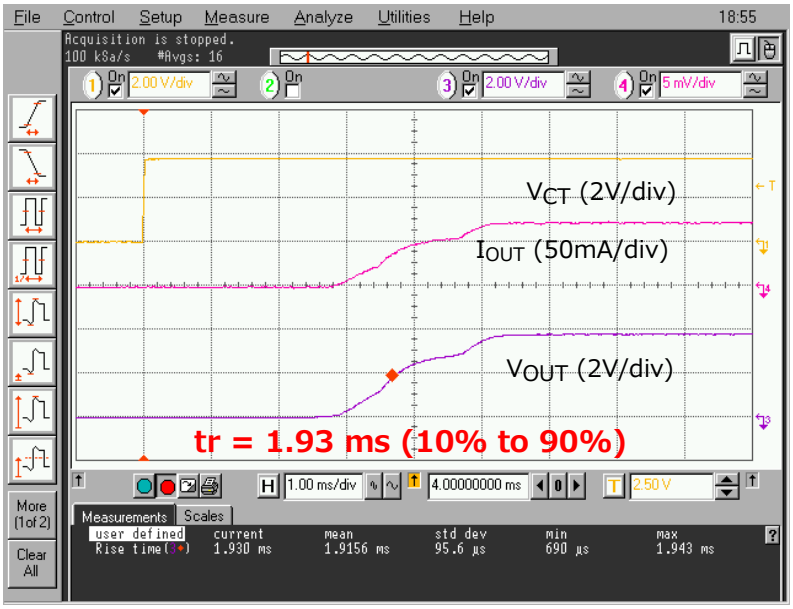
The V_{OUT} rise time and the transient inrush current depend on the slow starter circuit that is determined by the time constant of the internal driver circuit, as well as capacitance (C_L) and equivalent resistance (R_L). Figure 3.2 shows an example of the V_{OUT} and I_{OUT} waveforms measured under typical test conditions.



Test conditions:
V_{IN} = 3.8V,
$\overline{CE}$ = Open,
V_{CT} = 0 ⇔ 3.8V,
Ta = 25°C,
R_L = 50Ω,
C_L = 1µF,
C_{IN} = 1µF

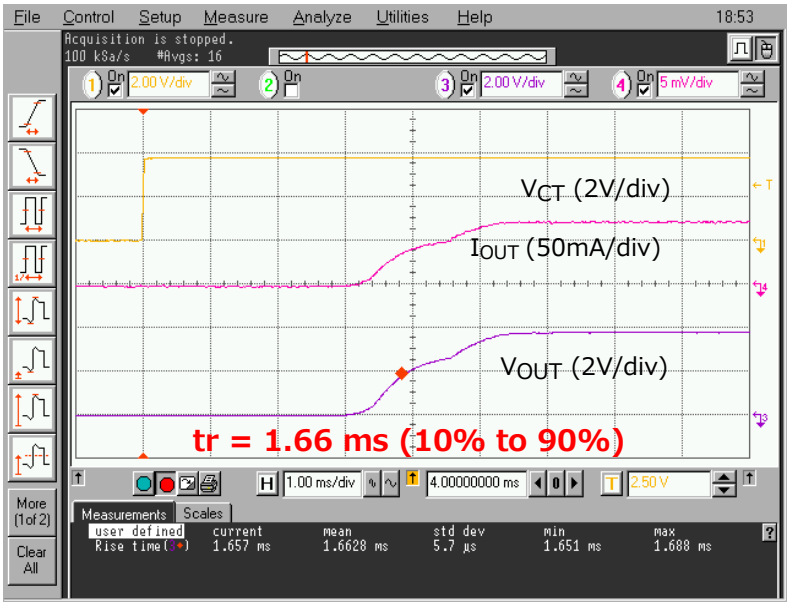
Figure 3.2 V_{OUT} and I_{OUT} waveforms of the TCK303G (under typical test conditions)

Figure 3.3 and Figure 3.4 show examples of V_{OUT} and I_{OUT} waveforms measured at the maximum and minimum operating ambient temperatures specified in the datasheet. Figure 3.3 shows the waveforms at 85°C while Figure 3.4 shows the waveforms at -40°C.



Test Conditions:
V_{IN} = 3.8V,
$\overline{CE}$ = Open,
V_{CT} = 0 ⇔ 3.8V,
Ta = 85°C,
R_L = 50Ω,
C_L = 1µF,
C_{IN} = 1µF

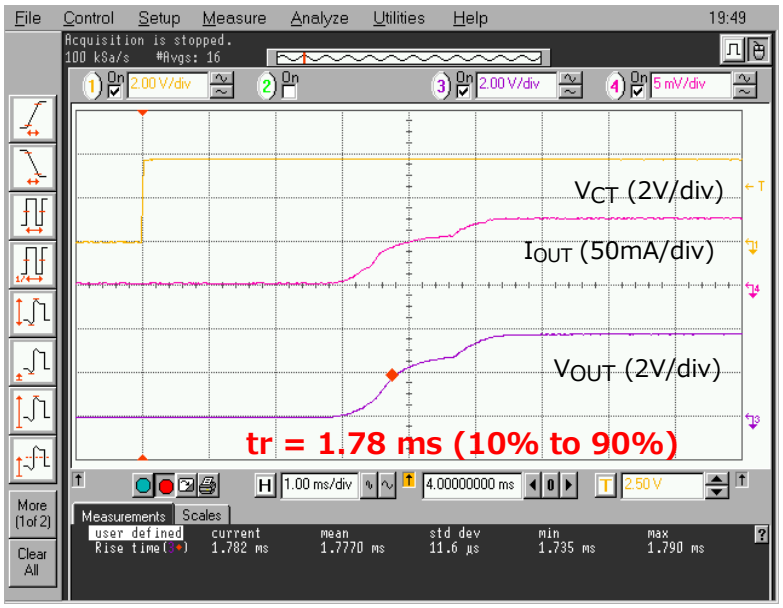
Figure 3.3 V_{OUT} and I_{OUT} waveforms of the TCK303G (at 85°C ambient temperature; otherwise, under typical test conditions)



Test Conditions:
V_{IN} = 3.8V,
$\overline{CE}$ = Open,
V_{CT} = 0 ⇔ 3.8V,
T_a = -40°C,
R_L = 50Ω,
C_L = 1µF,
C_{IN} = 1µF

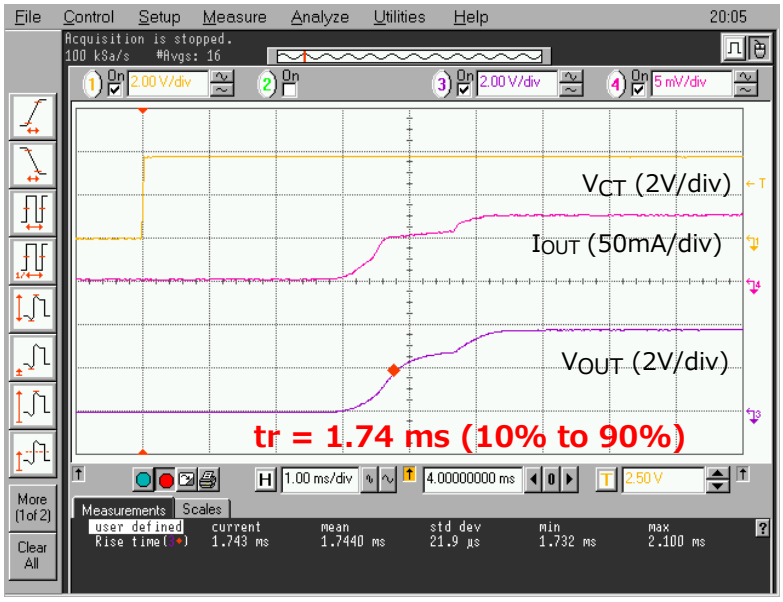
Figure 3.4 V_{OUT} and I_{OUT} waveforms of the TCK303G (at -40℃ ambient temperature; otherwise, under typical test conditions)

Figure 3.5 and Figure 3.6 show examples of V_{OUT} and I_{OUT} waveforms measured with different capacitances (C_L). A larger C_L causes the charge current to increase, resulting in a faster V_{OUT} rise time and higher I_{OUT}, compared with the case of a typical C_L. The TCK301G, TCK302G, and TCK303G incorporate a slow starter circuit, which causes the output current to change slowly in order to suppress inrush current. Due to the slow starter circuit, the V_{OUT} waveforms with C_L values of 2.2µF and 4.7µF shown in Figure 3.5 and Figure 3.6 are stable and do not differ significantly from the waveform with a typical C_L value of 1µF shown in Figure 3.2.



Test conditions:
$\overline{V_{IN}}$ = 3.8V,
$\overline{CE}$ = Open,
V_{CT} = 0 ⇔ 3.8V,
T_a = 25°C,
R_L = 50Ω,
C_L = 2.2µF,
C_{IN} = 1µF

Figure 3.5 V_{OUT} and I_{OUT} waveforms of the TCK303G (C_L=2.2µF; otherwise, under typical test conditions)



Test conditions:
$\overline{V_{IN}}$ = 3.8V,
$\overline{CE}$ = Open,
V_{CT} = 0 ⇔ 3.8V,
T_a = 25°C,
R_L = 50Ω,
C_L = 4.7µF,
C_{IN} = 1µF

Figure 3.6 V_{OUT} and I_{OUT} waveforms of the TCK303G (C_L=4.7µF; otherwise, under typical test conditions)

4. Design considerations

- External capacitors

  Add external input and output capacitors at least 1μF to achieve the guaranteed performance and improve the stability of a power supply.

- Board assembly

  Provide as large a GND plane as possible to reduce wire impedance. Voltage overshoot and undershoot may happen depending on transient responses of the input and output voltage and current, a PCB layout, and internal parasitic of an IC.

- Reverse-current blocking

  The TCK301G, TCK302G, and TCK303G have a reverse-current blocking circuit. While the n-channel output MOSFET is off and the input voltage (V_{IN}) is within the operating range, the reverse-current blocking circuit constantly monitors the output voltage (V_{OUT}) and prevents a current from flowing from V_{OUT} to V_{IN} in the reverse direction. The purpose of the reverse-current blocking circuit is to protect a power supply and other circuits connected to the V_{IN} pin.

- Protection circuits

  The TCK301G, TCK302G, and TCK303G have reverse-current blocking circuit, thermal shutdown, overvoltage lockout, and undervoltage lockout circuits which are not intended to guarantee that the ICs always remain below their absolute maximum ratings. You should apply the above design considerations, and derate the absolute maximum rated values as described in the Toshiba Semiconductor Reliability Handbook to ensure that none of the absolute maximum ratings will be exceeded under any circumstances. It is also recommended to add fail-safe and other safety features to an application system.

- Power dissipation

  Designing PCB, the IC temperature remains well below the maximum rated temperature during operation even at the maximum power dissipation point. For PCB design, ambient temperature, input voltage, and output current, and other environmental conditions should also be considered.

5. Product overview

5.1. TCK301G, TCK302G and TCK303G

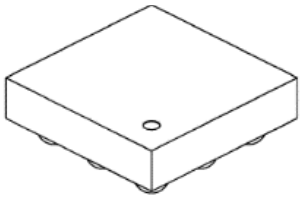
5.1.1 Overview

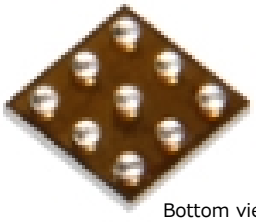
Fabricated using a high-voltage CMOS process, the TCK301G, TCK302G, and TCK303G load switches operate with an input voltage of up to 28V. These load switches feature a typical low on-resistance of 73mΩ (at V_{IN} = 4.5V and I_{OUT} = 1.0A), a maximum output current of 3A, and a wide operating input voltage range from 2.3V to 28V.

- Small package: WCSP9 with a 0.5mm ball pitch (1.5mm x 1.5mm, t**:** 0.5mm typical), PD = 1.65W
- High input voltage: V_{IN} (max) = 28V
- High output current: I_{OUT} (DC) = 3.0A
- Low on-resistance: R_{ON} = 73mΩ (typical) at V_{IN} = 4.5V and I_{OUT} = 1.0A
- Inrush current limiting (slew rate control) circuit
- Overvoltage lockout (OVLO): TCK301G = 6.6V, TCK302G = 10.5V, TCK303G = 15.5V (typical)
- Undervoltage lockout (UVLO): 2.9V (typical)
- FLAG output
- The FLAG output indicates input overvoltage and undervoltage conditions even when the output is disabled via the V_{CT} pin.
- Output startup hold time: 15ms
- Reverse-current blocking (switch-off state)
- Thermal shutdown circuit

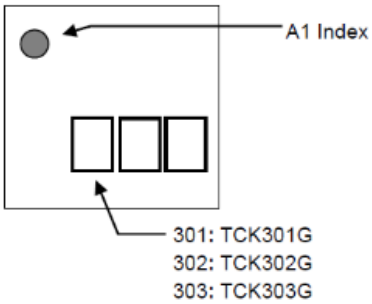
5.1.2. External view and pin assignment

External view and pin

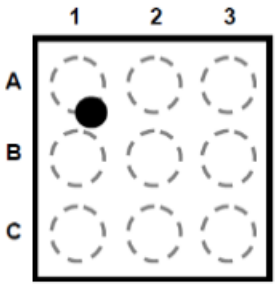




Bottom view



Pin assignment (Top view)



	1	2	3
A	FLAG	V_{CT}	$\overline{CE}$
B	V_{IN}	GND	V_{OUT}
C	V_{IN}	GND	V_{OUT}

Figure 5.1.1 External view, marking, and pin assignment of the TCK301G, TCK302G, and TCK303G

5.1.3 Product list

Table 5.11 Product list

Part Number	Overvoltage Lockout	$\overline{CE}$ Pin	V_{CT} Active Logic	V_{CT} Resistor
TCK301G	6.6 V (typ.)	Active-Low	Active-High	Pull-up
TCK302G	10.5V (typ.)	Active-Low	Active-High	Pull-up
TCK303G	15.5V (typ.)	Active-Low	Active-High	Pull-up

5.1.4 Internal block diagram

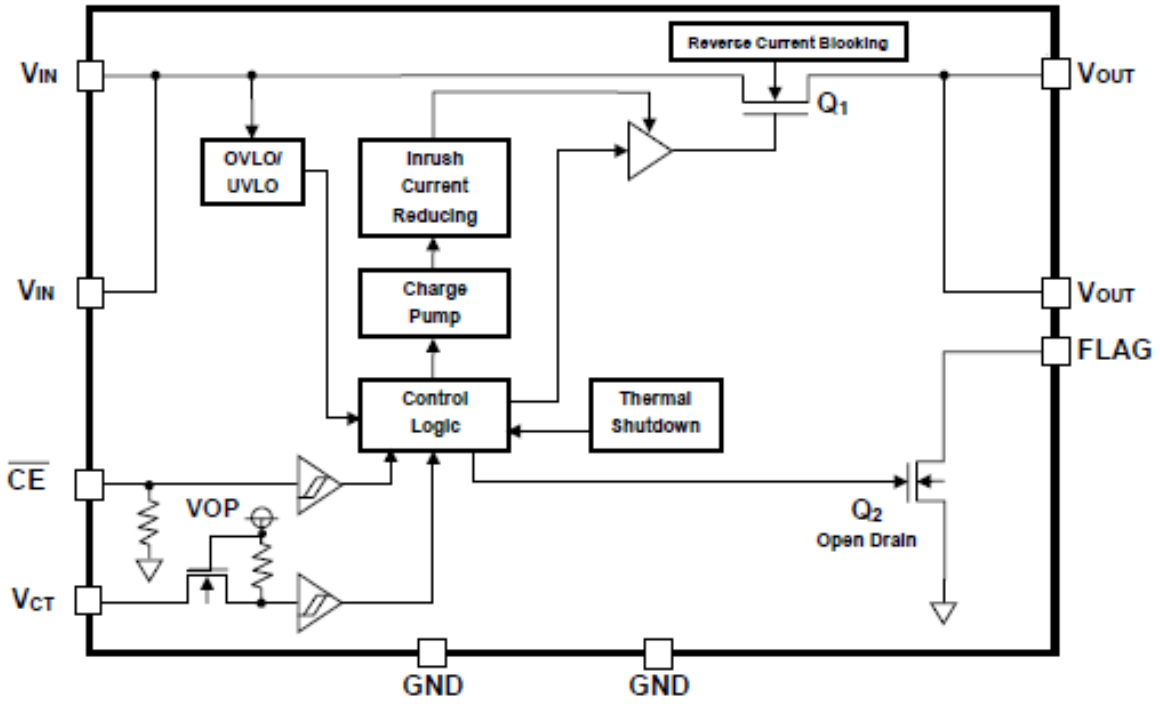


Figure 5.1.2 Internal block diagram of the TCK301G, TCK302G, and TCK303G

5.1.5 Operation logic table

Table 5.1.2 Operation logic table of the TCK301G, TCK302G and TCK303G

		$\overline{CE}$: "L"			$\overline{CE}$: "H"
		$V_{UVL} < V_{IN} < V_{OVL}$	$V_{UVL} > V_{IN}$ or $V_{IN} > V_{OVL}$	Thermal Shutdown	-
VCT: "H" or open	Q1 (V_{OUT})	ON (V_{OUT})	ON (V_{OUT})	ON (V_{OUT})	OFF (Output disabled)
	Q2 (FLAG)	ON (LOW)	OFF (High-Z)	OFF (High-Z)	OFF (High-Z)
	Reverse-Current Blocking	Disabled	Disabled	Disabled	Enabled
VCT: "L"	Q1 (V_{OUT})	OFF (Output disabled)	OFF (Output disabled)	OFF (Output disabled)	OFF (Output disabled)
	Q2 (FLAG)	ON (LOW)	OFF (High-Z)	OFF (High-Z)	OFF (High-Z)
	Reverse-Current Blocking	Enabled	Enabled	Enabled	Enabled

5.1.6 Pin description

Table 5.1.3 Pins of the TCK301G, TCK302G and TCK303G

Pin	Name	Description
A1	FLAG	Open-drain acknowledge output After hold time, if V_{IN} is between the operation range, FLAG goes "L". Otherwise, FLAG goes "High-Z".
B1, C1	V_{IN}	Power Input. Integrated overvoltage lockout (OVLO) and undervoltage lockout (UVLO) circuits.
A2	V_{CT}	Switch control. The V_{CT} input is internally connected to VOP via a pullup resistor.
B2, C2	GND	Ground
A3	$\overline{CE}$	Chip Enable. The $\overline{CE}$ pin has an internal pulldown resistor. A Low on $\overline{CE}$ enables V_{OUT}. When $\overline{CE}$ is High or open, V_{OUT} is disabled.
B3, C3	V_{OUT}	Output.

END OF DOCUMENT

Terms of Use

This terms of use is made between Toshiba Electronic Devices and Storage Corporation (“We”) and customers who use documents and data that are consulted to design electronics applications on which our semiconductor devices are mounted (“this Reference Design”). Customers shall comply with this terms of use. Please note that it is assumed that customers agree to any and all this terms of use if customers download this Reference Design. We may, at its sole and exclusive discretion, change, alter, modify, add, and/or remove any part of this terms of use at any time without any prior notice. We may terminate this terms of use at any time and for any reason. Upon termination of this terms of use, customers shall destroy this Reference Design. In the event of any breach thereof by customers, customers shall destroy this Reference Design, and furnish us a written confirmation to prove such destruction.

1. Restrictions on usage

1. This Reference Design is provided solely as reference data for designing electronics applications. Customers shall not use this Reference Design for any other purpose, including without limitation, verification of reliability.
2. This Reference Design is for customer's own use and not for sale, lease or other transfer.
3. Customers shall not use this Reference Design for evaluation in high or low temperature, high humidity, or high electromagnetic environments.
4. This Reference Design shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable laws or regulations.

2. Limitations

1. We reserve the right to make changes to this Reference Design without notice.
2. This Reference Design should be treated as a reference only. We are not responsible for any incorrect or incomplete data and information.
3. Semiconductor devices can malfunction or fail. When designing electronics applications by referring to this Reference Design, customers are responsible for complying with safety standards and for providing adequate designs and safeguards for their hardware, software and systems which minimize risk and avoid situations in which a malfunction or failure of semiconductor devices could cause loss of human life, bodily injury or damage to property, including data loss or corruption. Customers must also refer to and comply with the latest versions of all relevant our information, including without limitation, specifications, data sheets and application notes for semiconductor devices, as well as the precautions and conditions set forth in the "Semiconductor Reliability Handbook".
4. When designing electronics applications by referring to this Reference Design, customers must evaluate the whole system adequately. Customers are solely responsible for all aspects of their own product design or applications. WE ASSUME NO LIABILITY FOR CUSTOMERS' PRODUCT DESIGN OR APPLICATIONS.
5. No responsibility is assumed by us for any infringement of patents or any other intellectual property rights of third parties that may result from the use of this Reference Design. No license to any intellectual property right is granted by this terms of use, whether express or implied, by estoppel or otherwise.
6. THIS REFERENCE DESIGN IS PROVIDED "AS IS". WE (a) ASSUME NO LIABILITY WHATSOEVER, INCLUDING WITHOUT LIMITATION, INDIRECT, CONSEQUENTIAL, SPECIAL, OR INCIDENTAL DAMAGES OR LOSS, INCLUDING WITHOUT LIMITATION, LOSS OF PROFITS, LOSS OF OPPORTUNITIES, BUSINESS INTERRUPTION AND LOSS OF DATA, AND (b) DISCLAIM ANY AND ALL EXPRESS OR IMPLIED WARRANTIES AND CONDITIONS RELATED TO THIS REFERENCE DESIGN, INCLUDING WARRANTIES OR CONDITIONS OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, ACCURACY OF INFORMATION, OR NONINFRINGEMENT.

3. Export Control

Customers shall not use or otherwise make available this Reference Design for any military purposes, including without limitation, for the design, development, use, stockpiling or manufacturing of nuclear, chemical, or biological weapons or missile technology products (mass destruction weapons). This Reference Design may be controlled under the applicable export laws and regulations including, without limitation, the Japanese Foreign Exchange and Foreign Trade Law and the U.S. Export Administration Regulations. Export and re-export of this Reference Design are strictly prohibited except in compliance with all applicable export laws and regulations.

4. Governing Laws

This terms of use shall be governed and construed by laws of Japan.