

MOSFET Parallel Operation (TK62N60X) Reference Guide

RD010-RGUIDE-02

TOSHIBA ELECTRONIC DEVICES & STORAGE CORPORATION

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1. Introduction

For power supply and other applications that MOSFETs are used as switching devices, in order to develop a new design with a higher output power based on an existing design, it is necessary to:

1. design a new topology or circuit configuration, or
2. replace MOSFETs with higher current rating (i.e., low on-resistance) without modification of the topology or circuit configuration.

The latter approach helps save a lot of development time. However, there is a limitation in increasing the current rating of a MOSFET without changing the package. To increase the output power of a design, it might be necessary to use MOSFETs in larger packages or use multiple MOSFETs in parallel. Paralleling MOSFETs has several advantages over replacing existing MOSFETs with those in larger packages. For example, since MOSFETs are common heat sources, paralleling MOSFETs makes it possible to spread heat sources apart from one another. In addition, using the same MOSFETs as in an existing system means that the same heat spreaders in the existing systems can be used.

When you choose to develop a new circuit design, you can create a printed circuit board in such a manner as to allow paralleling of multiple MOSFETs. Then, you can use the same board for different system models just by adjusting the number of parallel MOSFETs according to the output power requirement. This helps save design time and makes it possible to use the same parts across multiple system models.

As described above, paralleling MOSFETs provides various benefits for system designers. However, parallel MOSFETs might cause oscillation and other problems unless their placement and routing are symmetrical and a gate drive circuit is properly designed.

This reference guide describes the operation of parallel MOSFETs, referring to the results of simulation. As an example, the following descriptions use the TK62N60X, Toshiba's 600V MOSFET of the DTMOSIV series in the TO-247 package, which is ideal for use in the power factor correction (PFC) circuits and primary-side main switches for AC-DC power supplies. The focus of this reference guide is on providing design considerations for parallel MOSFETs to increase the output of a power supply unit.

To download the datasheets for the MOSFETs of the DTMOSIV series→

[Click Here](#)

2. Verification of MOSFET operation by simulation

2.1. Simulation model

This section describes the simulation model of the TK62N60X used for verification. The PSpice model of the TK62N60X available on Toshiba’s website characterizes only the chip design. In order to simulate the operation of the TK62N60X including the effect of its package, it is necessary to externally add the parasitic inductances of the TO-247 package to the PSpice model. Figure 2.1.1 illustrates the internal structure of the TO-247 package and its parasitic inductances. The bonding wires between the MOSFET chip and each of the package terminals have inductances, which are labeled I_g , I_s and I_d in Figure 2.1.1. Figure 2.1.2 shows a simulation model including the internal parasitic inductances of the TO-247 package for TK62N60X.

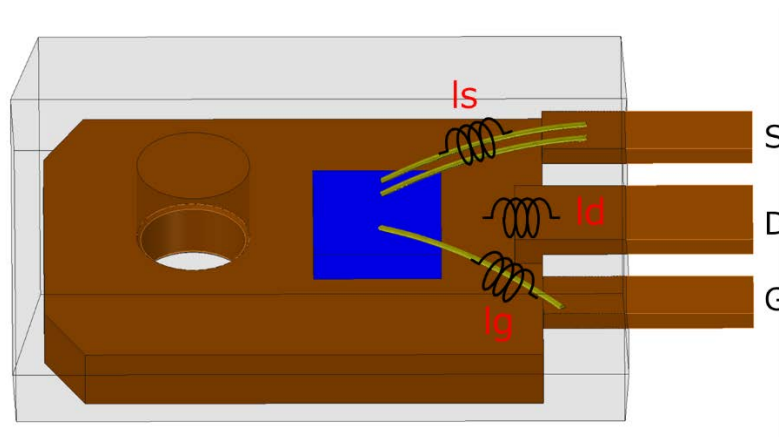


Figure 2.1.1 Bonding wires in the TO-247 package

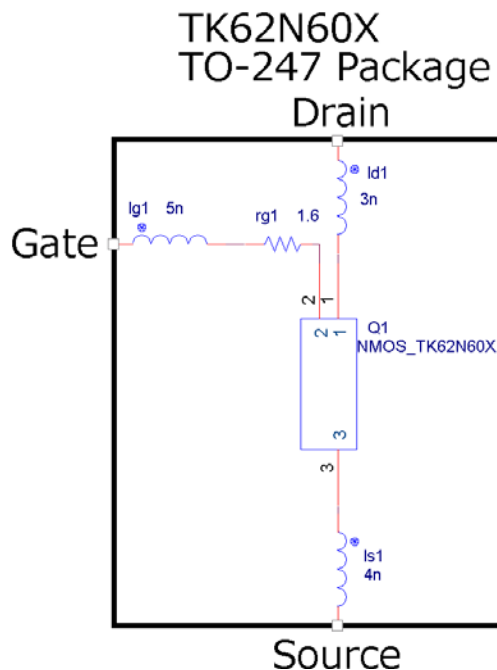


Figure 2.1.2 Simulation model

2.2. PCB trace inductance

The PCB trace inductance can be calculated through an electromagnetic field analysis. Figure 2.2.1 shows the analysis conditions, and Table 2.2.1 shows the analysis results.

1. Copper trace thickness: 100 μm
2. Trace widths: Drain and source lines = 10 mm, gate line = 3 mm
3. Trace length: 50 mm
4. Frequency: 1 MHz

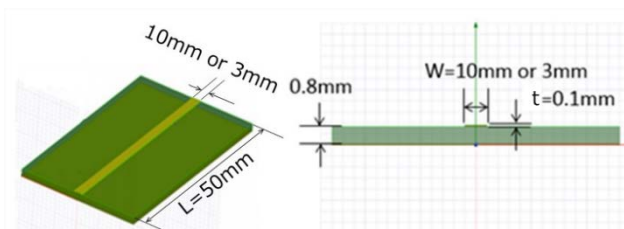


Figure 2.2.1 Conditions for the electromagnetic field analysis

Table 2.2.1 Results of the electromagnetic field analysis

Analysis Results with W = 3 mm		Analysis Results with W = 10 mm	
Inductance per mm of trace	Inductance when L = 50 mm	Inductance per mm of trace	Inductance when L = 50 mm
0.207 nH/mm	10.4 nH	0.0844 nH/mm	4.22 nH

Since the inductance increases in proportion to the trace length, it is necessary to assume the length of each trace. Figure 2.2.2 shows the relationships between devices and trace inductances as well as the inductance labels. Table 2.2.2 lists the lengths and inductances of these traces.

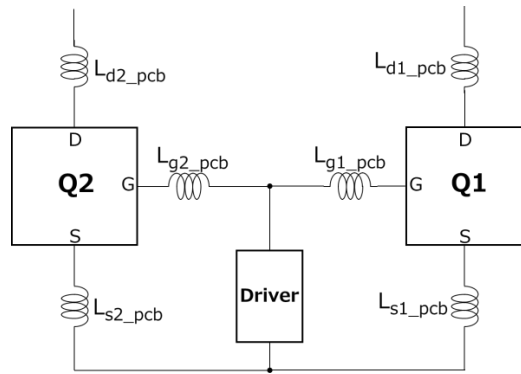


Figure 2.2.2 Relationships between devices and trace inductances

Table 2.2.2 PCB trace inductance

FET	Trace	Description	Trace Length	Trace Width	Trace Inductance
Q1	Lg1_pcb	Driver output to FET gate terminal	20 mm	3 mm	4.2 nH
	Ls1_pcb	FET gate terminal to driver GND	30 mm	10 mm	2.6 nH
	Ld1_pcb	Inductor L to FET drain terminal	50 mm	10 mm	4.3 nH
Q2	Lg2_pcb	Driver output to FET gate terminal	20 mm	3 mm	4.2 nH
	Ls2_pcb	FET source terminal to driver GND	30 mm	10 mm	2.6 nH
	Ld2_pcb	Inductor L to FET drain terminal	50 mm	10 mm	4.3 nH

2.3. Simulation circuit

Figure 2.3.1 shows the simulation circuit for verification. We performed a simulation under the following conditions:

(The PSpice circuit that can be simulated with OrCAD is available for download under the name of RD010-SPICE01.)

1. Supply voltage: $V4 = 300\text{ V}$
2. Inductance: $L = 250\text{ }\mu\text{H}$, initial current (IC) = 20 A
3. MOSFET driver: Supply voltage ($V2$) = 10 V
Output resistor ($R9$) = $1\text{ }\Omega$ (common push-pull output)
 $Trise(TR) = Tfall(TF) = 10\text{ ns}$

* The assumption is that the device temperature remains constant at 25°C without self-heating.

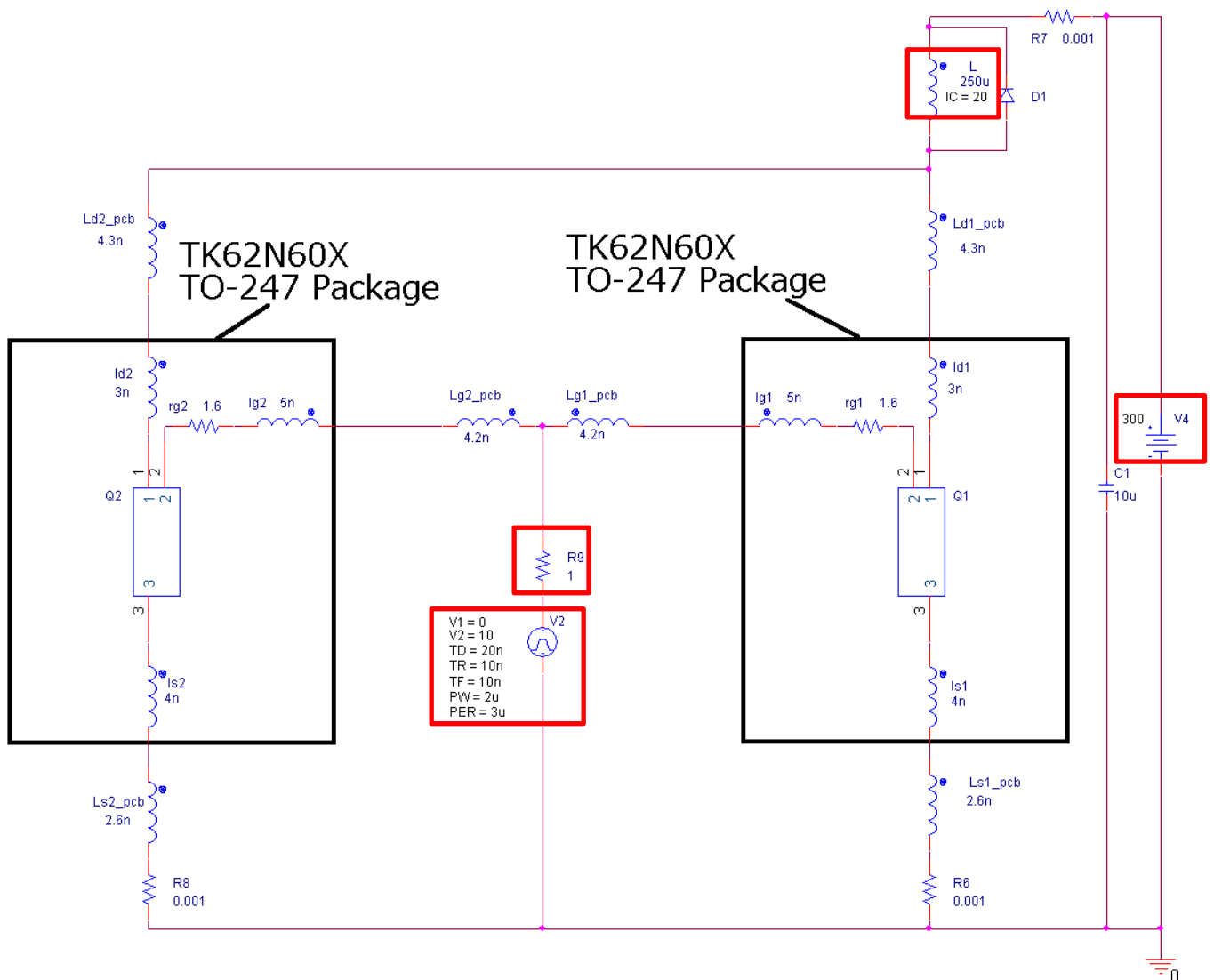


Figure 2.3.1 Simulation circuit

2.4. Waveforms under ideal conditions (with symmetrical traces)

Figure 2.3.1 shows a simulation model in which the board traces connected to each MOSFET terminal have an equal inductance and the two parallel MOSFETs are routed completely symmetrically. First, we performed a simulation under these ideal conditions. Table 2.4.1 shows the parameters used for this simulation.

Table 2.4.1 Simulation parameters (ideal conditions)

FET	Source Trace Length	Parasitic Inductance of Source Trace	External Gate Resistor
Q1	30 mm	Ls1_pcb = 2.6 nH	None (directly connected to Q2)
Q2	30 mm	Ls2_pcb = 2.6 nH	None (directly connected to Q1)

Figure 2.4.1 and Figure 2.4.2 show the simulation results. When Q1 and Q2 have an ideally symmetrical layout, their operations are perfectly balanced and have identical waveforms.

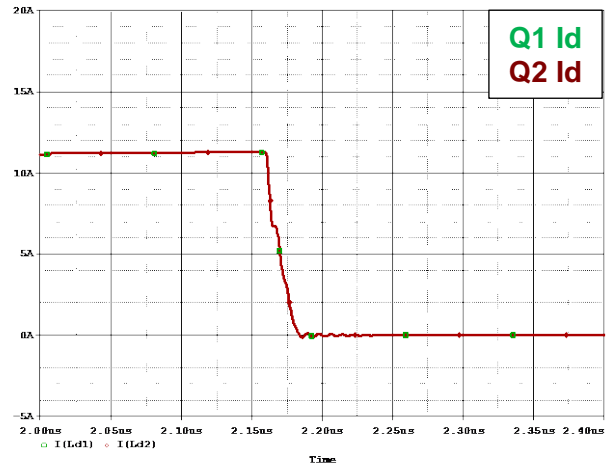
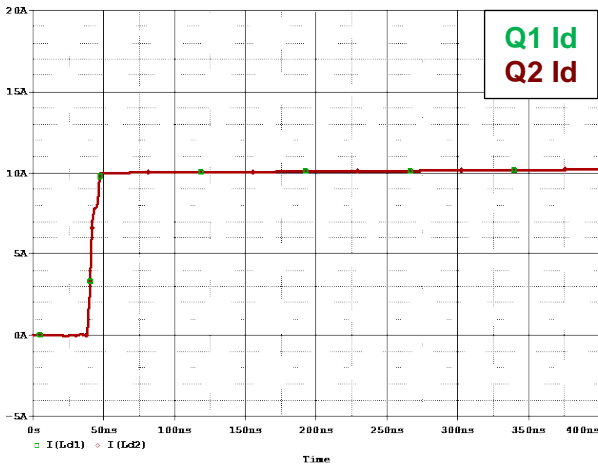
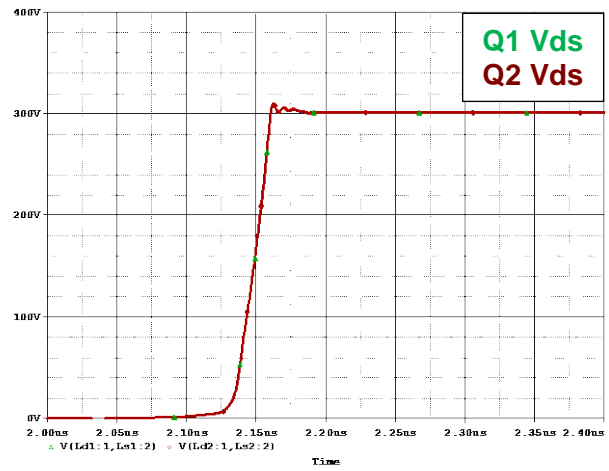
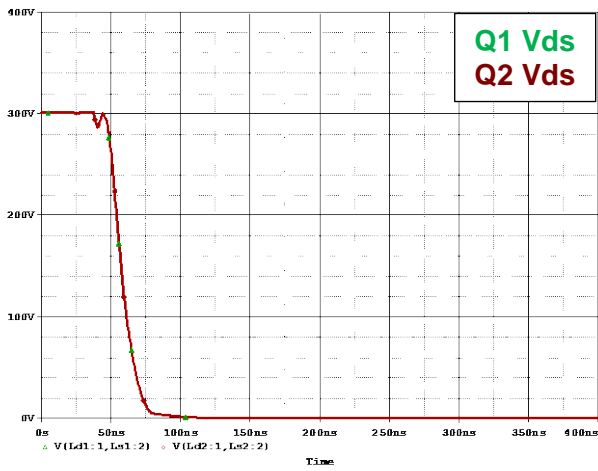
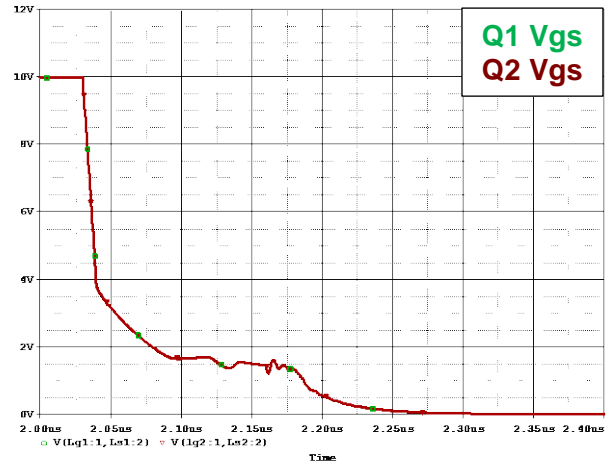
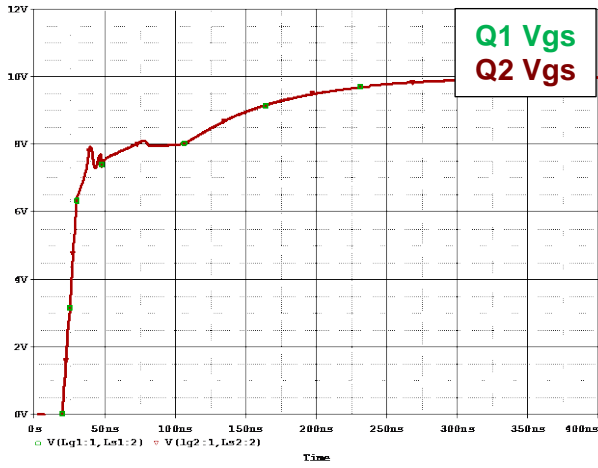


Figure 2.4.1 Turn-on waveforms under ideal conditions

Figure 2.4.2 Turn-off waveforms under ideal conditions

2.5. Asymmetrically layout MOSFETs

Next, we performed a simulation on parallel MOSFETs with an asymmetrical trace layout. The source trace of Q3 in Figure 2.5.1 is 60 mm long—30 mm longer than that of Figure 2.3.1. The 60-mm source trace of Q3 has an inductance of 5.1 nH. Table 2.5.1 shows the parameters used for this simulation.

Table 2.5.1 Simulation parameters (asymmetrical layout)

FET	Source Trace Length	Parasitic Inductance of Source Trace	External Gate Resistor
Q3	60 mm (30 mm + 30 mm)	Ls1_pcb = 5.1 nH	None (directly connected to Q3)
Q4	30 mm	Ls2_pcb = 2.6 nH	None (directly connected to Q4)

Figure 2.5.1 shows the simulation circuit.

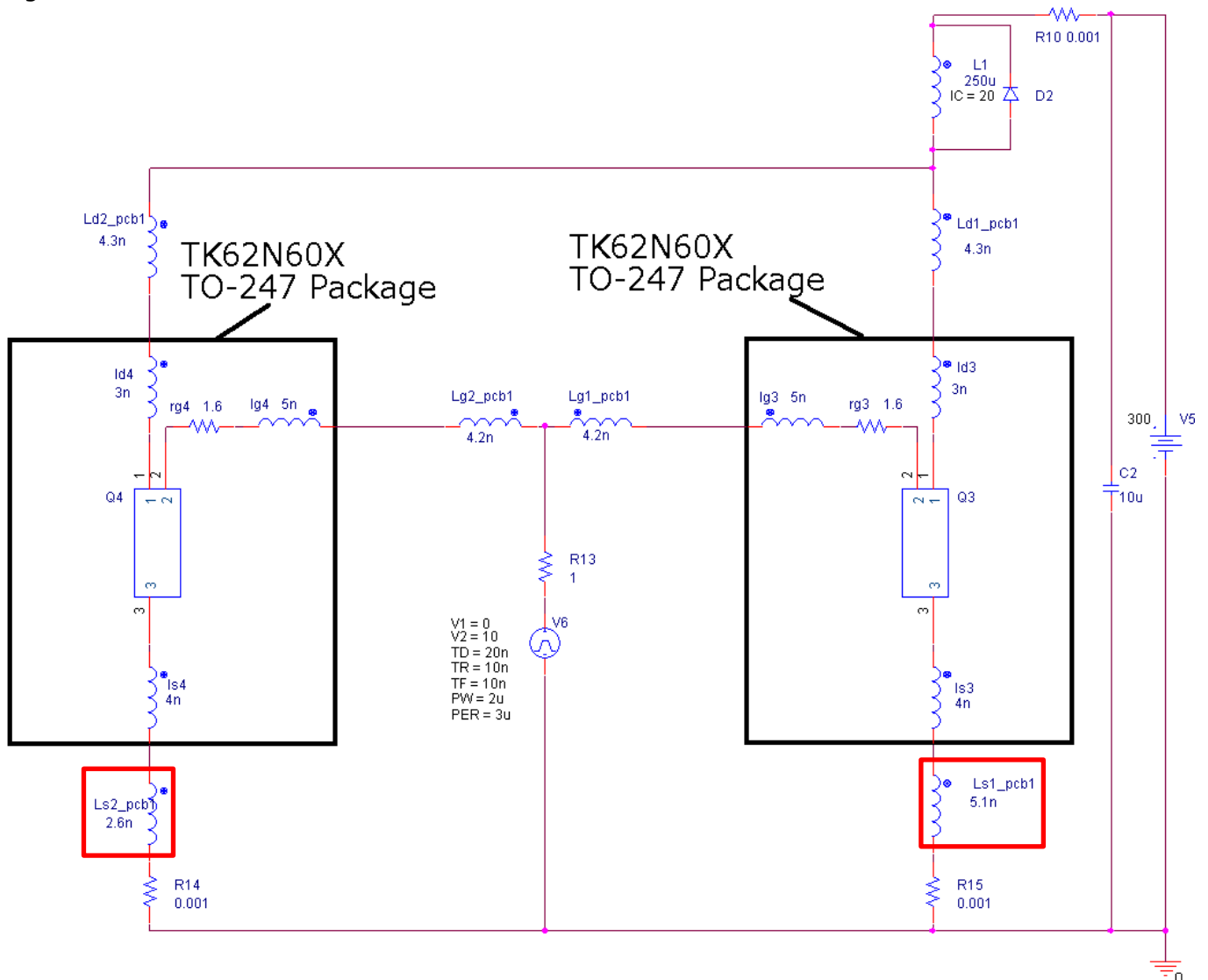


Figure 2.5.1 Simulation circuit

Figure 2.5.2 and Figure 2.5.3 show the simulation results. In Figure 2.5.3, V_{gs} oscillation is observed, and it indicates that an asymmetrical layout causes an oscillation. Figure 2.5.2 also indicates that MOSFET Q3 with larger source trace inductance turns on later than the other MOSFET Q4, and it is observed current concentration on Q4. An asymmetrical layout is undesirable in terms of both oscillation and current imbalance. It is important to create a layout as symmetrical as possible for parallel MOSFETs.

(Note: In actual operation, a MOSFET with larger current concentration dissipates much heat. This causes its on-resistance to increase, limiting a current. As a result, a current flowing to the other MOSFET increases. Therefore, the currents flowing to the parallel MOSFETs become balanced immediately after turn-on. Since this simulation is not considered heat generation, it took a longer for the currents to the parallel MOSFETs to be balanced.)

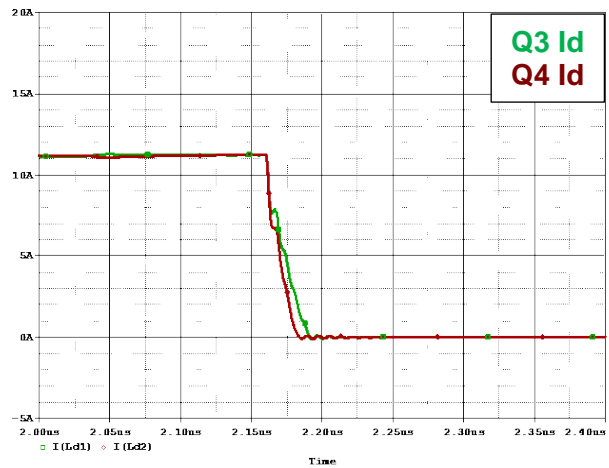
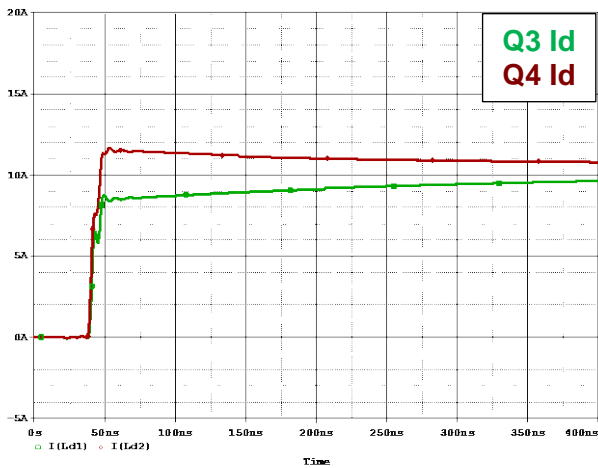
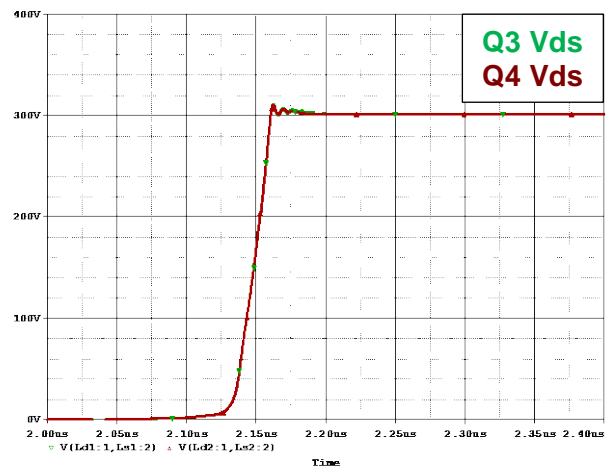
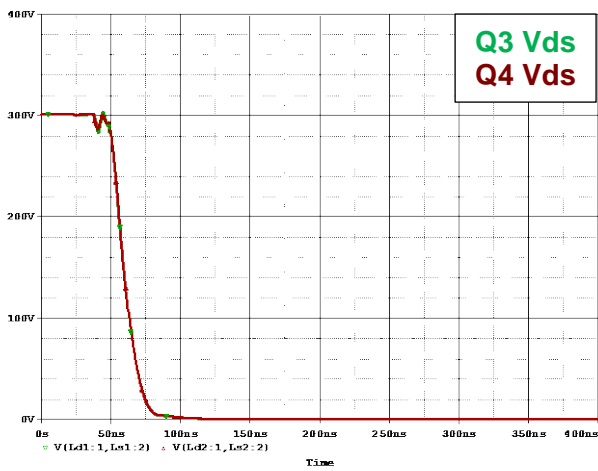
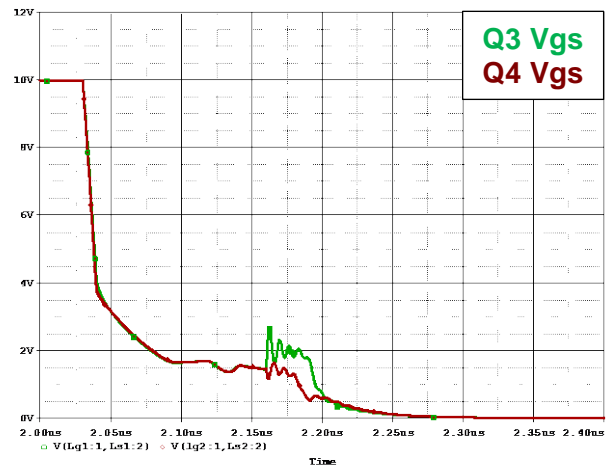
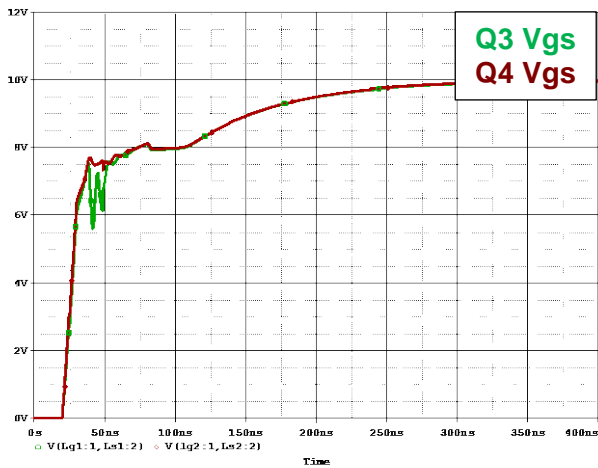


Figure 2.5.2 Turn-on waveforms of asymmetrically layout parallel MOSFETs

Figure 2.5.3 Turn-off waveforms of asymmetrically layout parallel MOSFETs

2.6. Adding resistors to the gates of each MOSFETs

Next, to the circuit shown in Section 2.5 that occurred oscillation, we added 4.7 Ω resistors between the gates of the parallel MOSFETs and their drivers. Table 2.6.1 shows the parameters used for the simulation of this circuit.

Table 2.6.1 Simulation parameters (with gate resistors added)

FET	Source Trace Length	Parasitic Inductance of Source Trace	External Gate Resistor
Q5	60 mm	Ls1_pcb = 5.1 nH	R17 = 4.7 Ω (for Q5)
Q6	30 mm	Ls2_pcb = 2.6 nH	R18 = 4.7 Ω (for Q6)

Figure 2.6.1 shows the simulation circuit.

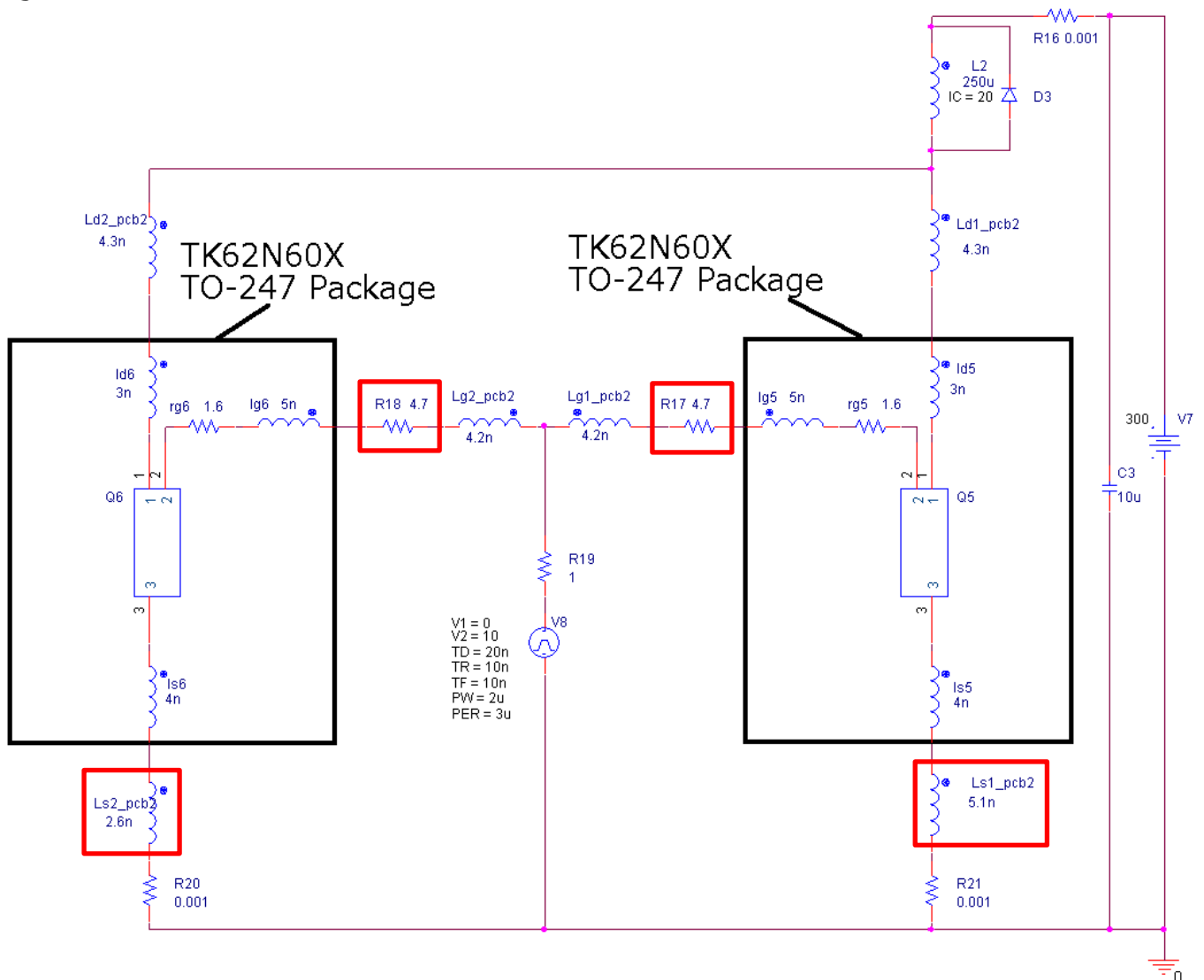


Figure 2.6.1 Simulation circuit

Figure 2.6.2 and Figure 2.6.3 show the simulation results, which is not observed oscillation. Since it is difficult to create a completely symmetrical layout for parallel MOSFETs, appropriate resistors should be added to the gate of each -MOSFETs. A slight difference in the value of gate resistors does not affect the MOSFET operation and it is acceptable to use general resistors with $\pm 10\%$ tolerance for this purpose. Oscillation was not observed, but unbalanced currents is still occurred during a switching transition.

(Note: In actual operation, a MOSFET with larger current concentration dissipates much heat. This causes its on-resistance to increase, limiting a current. As a result, a current flowing to the other MOSFET increases. Therefore, the currents flowing to the parallel MOSFETs become balanced immediately after turn-on. Since this simulation is not considered heat generation, it took a longer for the currents to the parallel MOSFETs to be balanced.)

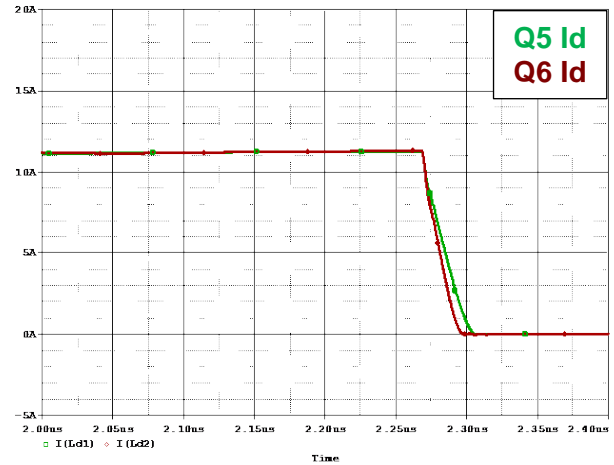
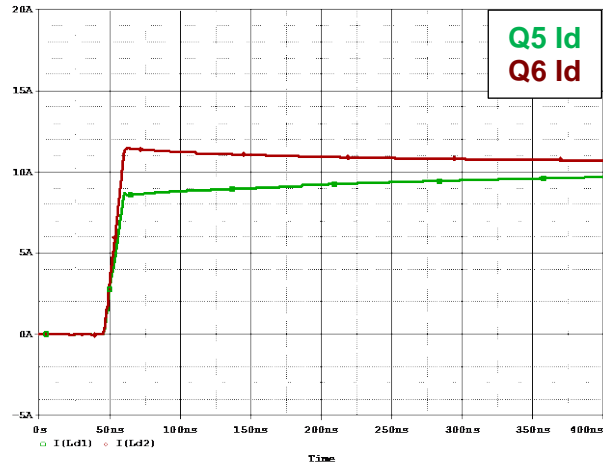
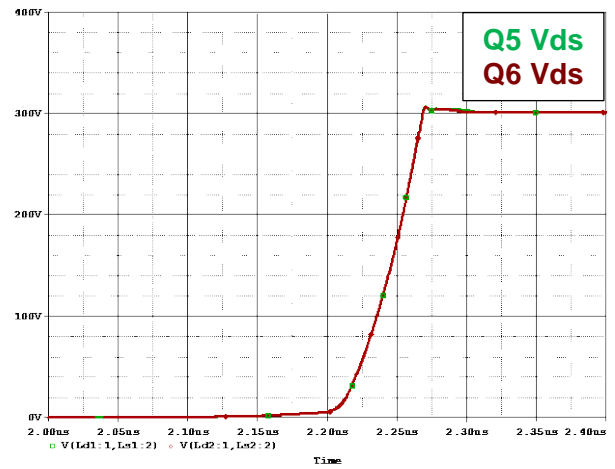
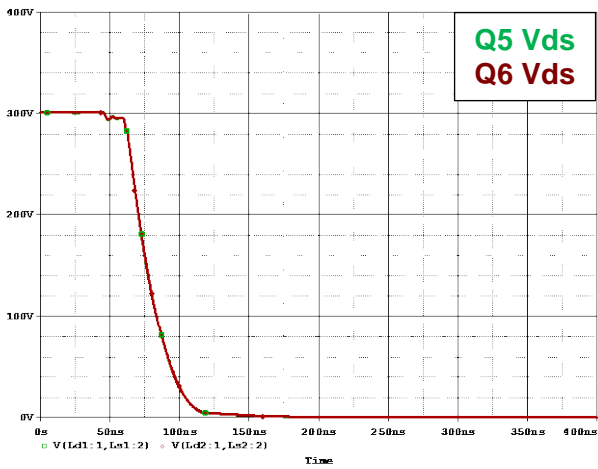
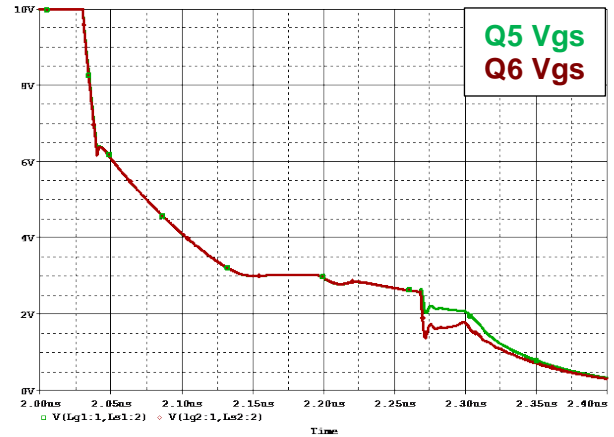
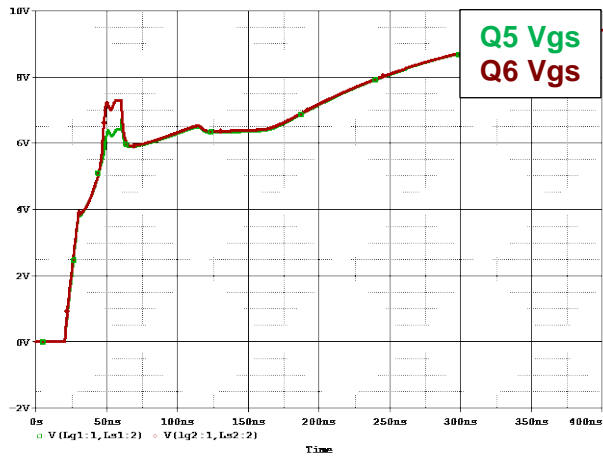


Figure 2.6.2 Turn-on waveforms of parallel MOSFETs with external gate resistors

Figure 2.6.3 Turn-off waveforms of parallel MOSFETs with external gate resistors

3. Conclusion

We verified the operation of parallel MOSFETs using the TK62N60X of the DTMOSIV series. As a result, we confirmed that it is important to create a board layout as symmetrical as possible for parallel MOSFETs and add gate resistors between driver IC and MOSFET.

When their layout is asymmetrical, the parallel MOSFETs do not turn on simultaneously due to a difference in the source trace inductance, causing a current imbalance during a switching transition. It is necessary to select MOSFETs with appropriate current ratings considering this current imbalance and verify their operation using an actual board.

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