MOSFET in 4-Pin
TO-247-4L Package
(TK25Z60X)

Reference Guide

RD011-RGUIDE-01

TOSHIBA ELECTRONIC DEVICES & STORAGE CORPORATION

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1. Introduction

A super-junction structure was developed to improve the trade-off between on-resistance and breakdown voltage for high-voltage power MOSFETs, 600V or above. The use of a super-junction structure helps reduce the on-resistance and increase the switching speed of MOSFETs. However, as the switching speed increases, the source wire inductance in a package has begun to affect the switching speed. This inductance sometimes limits to increase the MOSFET switching speed and efficiency.

If the voltage caused by parasitic inductances and a sharp change in turn-off current is added on the gate voltage of a MOSFET, the gate goes into oscillation. In addition, a voltage induced by a change in drain current during turn-on and a parasitic source inductance in the MOSFET might exert a negative feedback effect on the gate drive and it is impossible to obtain desired switching performance and efficiency.

The TO-247-4L package provides solutions for these problems. TO-247-4L is a 4-pin package in which the source wire is separated into a drain current path and a gate drive path. Therefore, the TO-247-4L package has the gate, drain, and source pins, and a source pin for the gate drive. This package structure helps reduce the internal source wire inductance effect.

Toshiba’s TK25N60X of the DTMOSIV-H series is housed in the 3-pin TO-247 package. The TK25N60X provides high-speed switching characteristics ideal for power factor correction (PFC) circuits for AC-DC power supply applications. This reference guide first shows the results of simulation of the 3-pin TK25N60X. Then it identifies problems to be solved to increase the MOSFET switching speed.

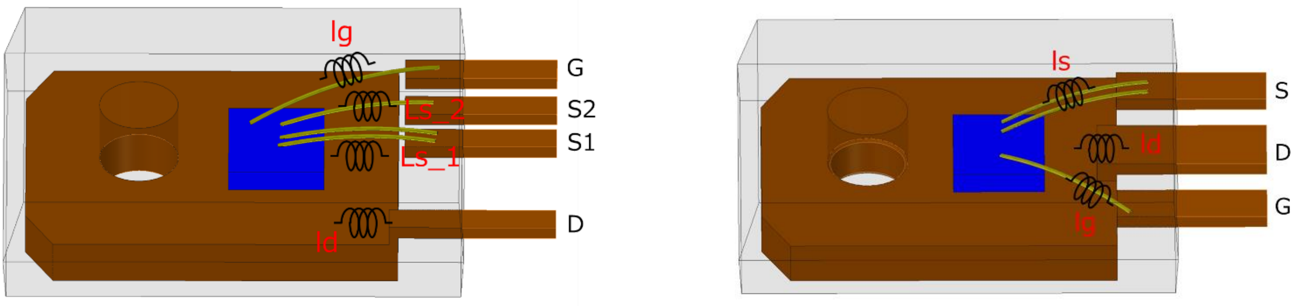
Next, this reference guide demonstrates how the TK25Z60X in the 4-pin TO-247-4L package helps solve these problems, referring to the results of circuit simulations. The focus is on showing that the 4-pin TO-247-4L package enables the TK25Z60X to switch at a higher speed and thus improve the power supply efficiency.

To download the datasheets for the MOSFETs in the TO-247-4L package → Click Here

2. Verification of MOSFET operation by simulation

2.1. Simulation models

This section describes the simulation models of the TK25N60X in the 3-pin TO-247 package and the TK25Z60X in the 4-pin TO-247-4L package used for verification. The PSpice models of the TK25N60X and TK25Z60X available on Toshiba's website provide the characteristics of only the MOSFET chip. In order to simulate their operations including the effect of the package, it is necessary to add package parasitic inductances externally to the PSpice models. Figure 2.1.1 compares the internal structure and parasitic inductances of the TO-247 and TO-247-4L packages. The bonding wires between the MOSFET chip and each of the package leads have inductances as shown in Figure 2.1.1. Figure 2.1.2 shows simulation models including the internal parasitic inductances of the TO-247 and TO-247-4L packages.



(a) TO-247-4L **(b) TO-247**

Figure 2.1.1 Bonding wires in the package

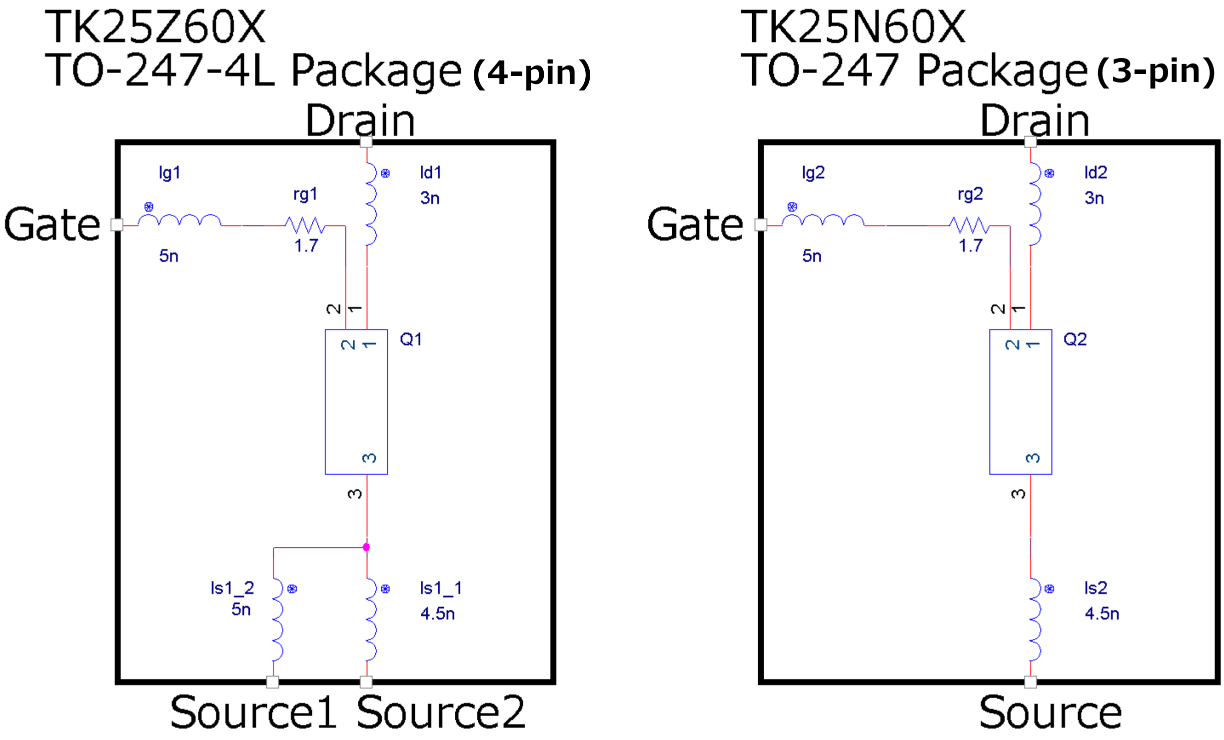


Figure 2.1.2 Simulation models

2.2. PCB trace inductances

The PCB trace inductance can be calculated through an electromagnetic field analysis. Figure 2.2.1 shows the analysis conditions, and Table 2.2.1 shows the analysis results.

1. Copper trace thickness: 0.1 mm
2. Trace widths: Drain and source lines = 10 nm, gate line = 3 mm
3. Trace length: 50 mm
4. Frequency: 1 MHz

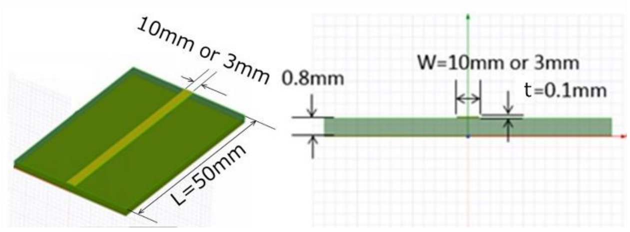
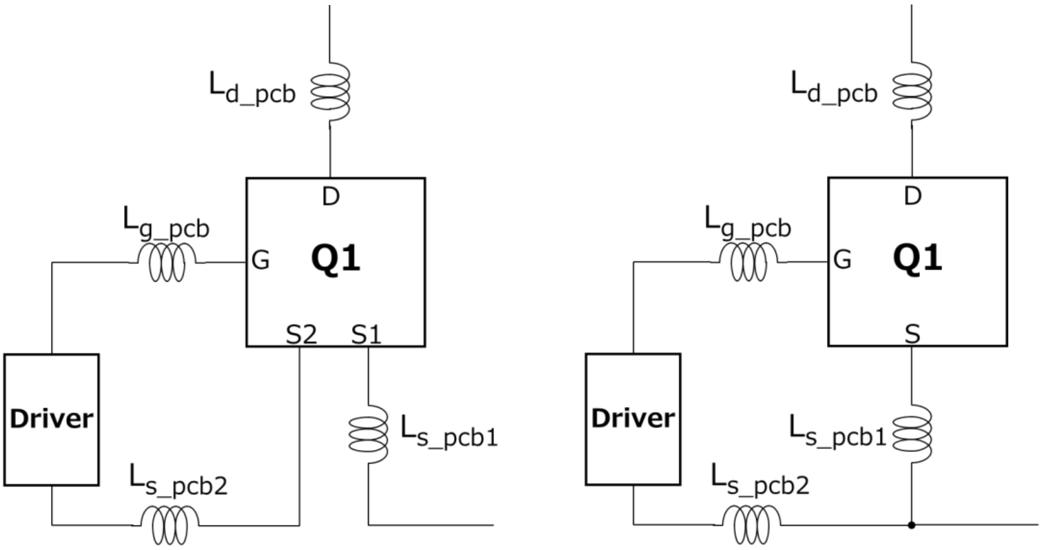


Figure 2.2.1 Conditions for the electromagnetic field analysis

Table 2.2.1 Results of the electromagnetic field analysis

Analysis Results with W = 3 mm		Analysis Results with W = 10mm	
Inductance per mm of trace	Inductance when L = 50 mm	Inductance per mm of trace	Inductance when L = 50 mm
0.207 nH/mm	10.4 nH	0.0844 nH/mm	4.22 nH

The inductance increases in proportion to the trace length. It is necessary to be calculated based on the length of each trace. Figure 2.2.2 shows the relationships between devices and trace inductances as well as the inductance labels. Table 2.2.2 lists the lengths and inductances of these traces.



(a) 4-pin package **(b) 3-pin package**

Figure 2.2.2 Relationships between devices and trace inductances

Table 2.2.2 **PCB trace inductances**

FET	Trace	Description	Trace Length	Trace Width	Trace Inductance
TK25Z60X (4-pin)	Lg_pcb	Driver output to FET gate terminal	50 mm	3 mm	4.2 nH
	Ls_pcb1	FET source terminal to power GND	30 mm	10 mm	2.6 nH
	Ls_pcb2	FET source terminal to driver GND	9.5mm	3 mm	2 nH
	Ld_pcb	Inductor L to FET drain terminal	50 mm	10 mm	4.2 nH
TK25N60X (3-pin)	Lg_pcb	Driver output to FET gate terminal	50 mm	3 mm	4.2 nH
	Ls_pcb1	FET source terminal to power GND	30 mm	10 mm	2.6 nH
	Ls_pcb2	FET source terminal to driver GND	9.5 mm	3 mm	2 nH
	Ld_pcb	Inductor L to FET drain terminal	50 mm	10 mm	4.2 nH

2.3. Simulation for the MOSFET in the 3-pin package

2.3.1. Operation with a 20-Ω gate resistor

Figure 2.3.1.1 shows the circuit simulated. The simulation conditions are as follows:

1.Supply voltage: V8 = 300 V

2.Inductance: L = 250 μH, initial current (IC) = 10 A

3.MOSFET driver: Supply voltage (V7) = 10 V

Output resistor (R32) = 0.5 Ω (common push-pull output), Trise = Tfall = 10 ns

4.External gate resistor: Rgate4 = 20 Ω

* The assumption is that the device temperature remains constant at 25°C without self-heating.

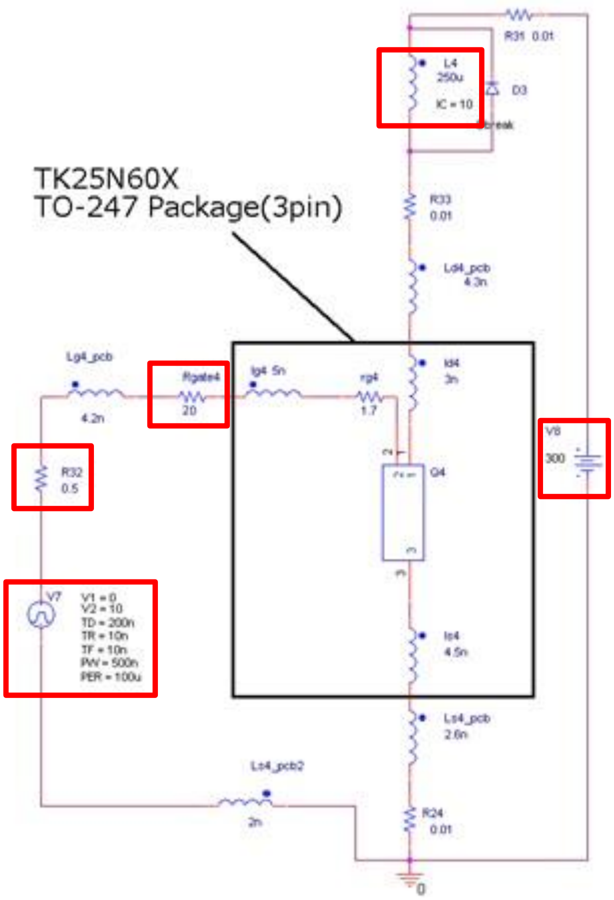


Figure 2.3.1.1 Simulation Circuit

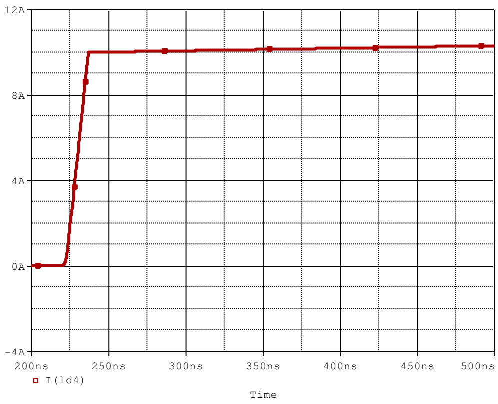


Figure 2.3.1.2 Turn-on current waveform

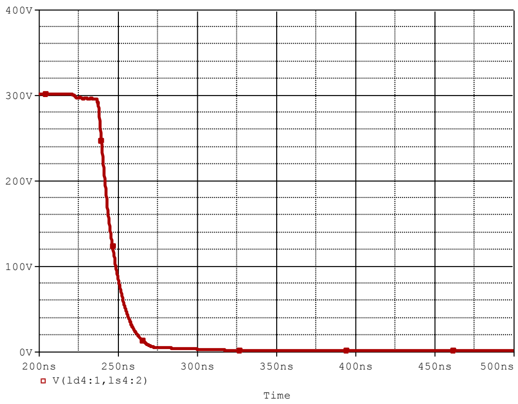


Figure 2.3.1.3 Turn-on voltage waveform

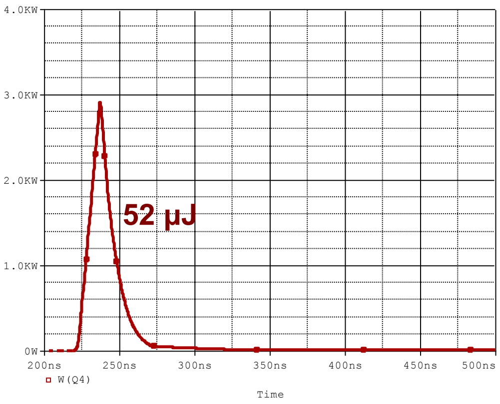


Figure 2.3.1.4 Turn-on switching loss

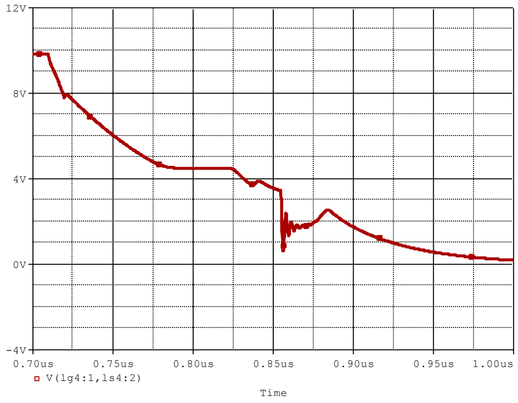


Figure 2.3.1.5 Turn-off gate waveform

Figure 2.3.1.4 shows the waveform that current value multiplies voltage value during turn-on. Integrating this curve over time gives turn-on switching loss, which is calculated to be 52 µJ. Figure 2.3.1.5 shows the turn-off gate waveform. As shown, the gate-source voltage (Vgs) did not oscillate.

Next, we replaced the external 20-Ω gate resistor with a 10-Ω resistor to reduce the turn-on switching loss in order to increase the power supply efficiency.

2.3.2. Operation with a 10-Ω gate resistor

The following shows the results of a simulation with a 10-Ω gate resistor.

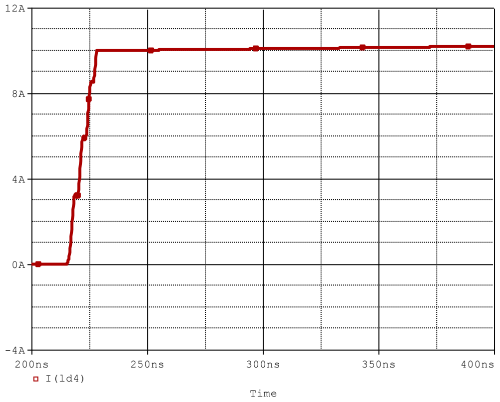


Figure 2.3.2.1 **Turn-on current waveform**

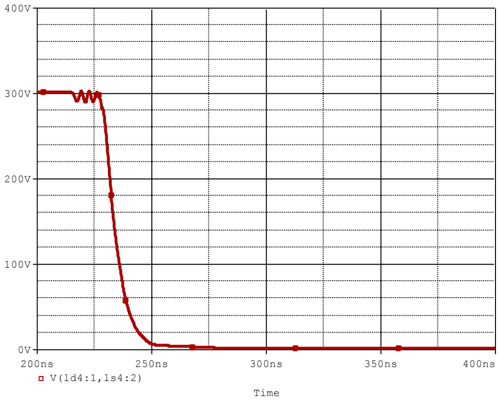


Figure 2.3.2.2 **Turn-on voltage waveform**

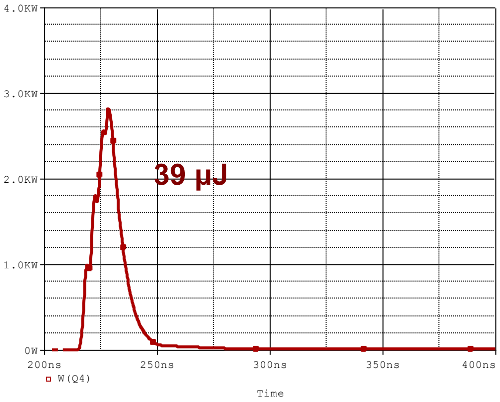


Figure 2.3.2.3 **Turn-on switching loss**

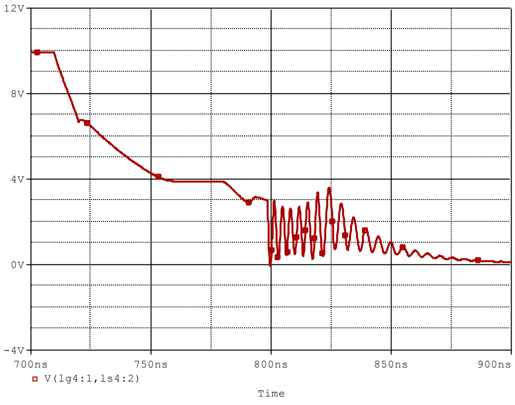


Figure 2.3.2.4 Turn-off gate waveform

The turn-on switching loss was 39 μJ, a 25% reduction from the circuit using a 20-Ω gate resistor. However, the gate voltage (Vgs) oscillated during turn-off. If the gate voltage oscillation conducts to the ground line, the ground bounce could cause a malfunction of the surrounding parts or EMI noise. Careful verification is necessary for actual applications.

Next, we replaced the MOSFET with the 4-pin TK25Z60X and performed a simulation without changing any component values.

2.4. Simulation for the MOSFET in the 4-pin package

2.4.1. Comparison with the MOSFET in the 3-pin package (Rg = 10 Ω)

Figure 2.4.1.1 shows the simulation circuit. The PCB trace inductances listed in Table 2.2.2 were used for this simulation. The 4-pin MOSFET (Q3) and the 3-pin MOSFET (Q4) were simulated under the same conditions with a 10-Ω gate resistor.

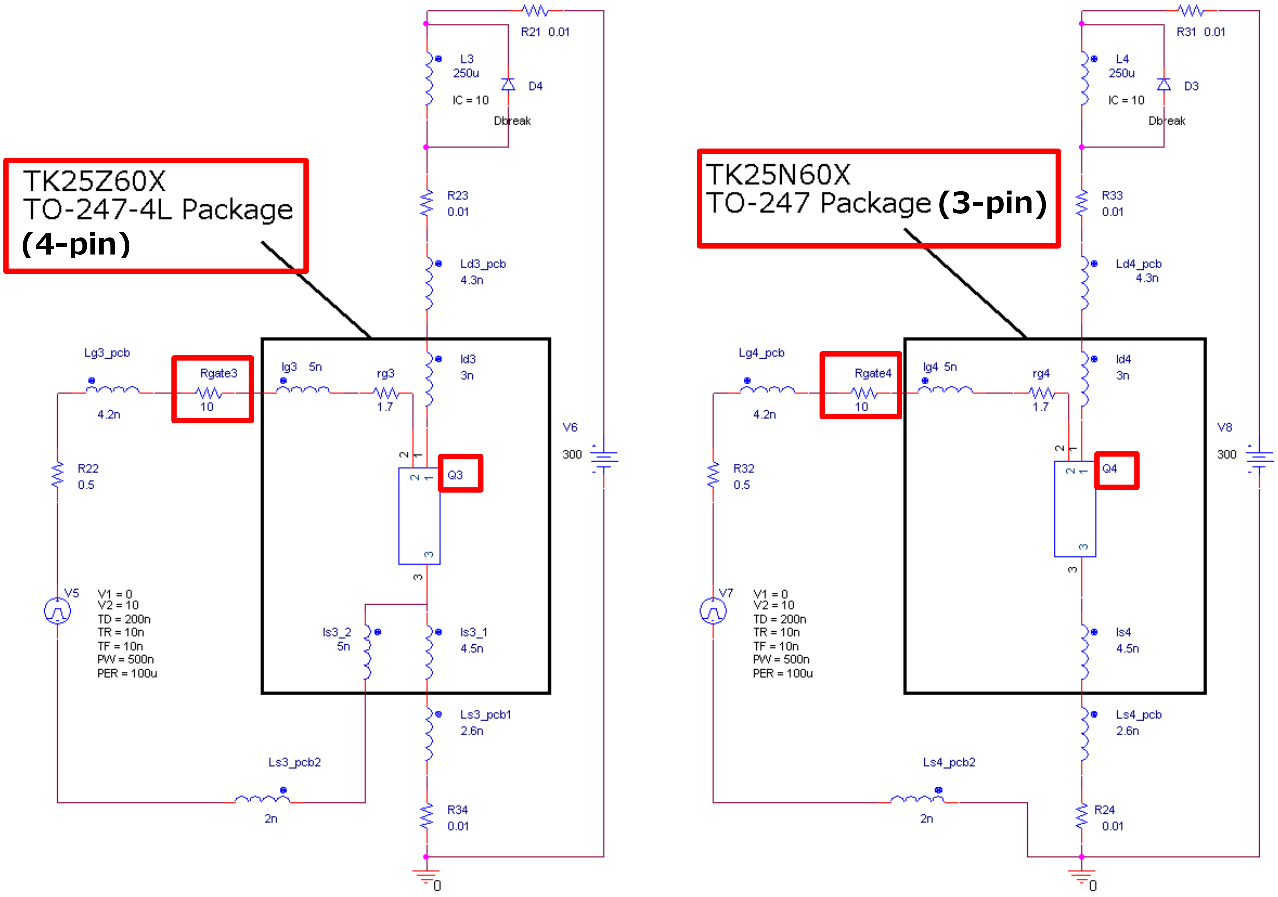


Figure 2.4.1.1 Simulation Circuit

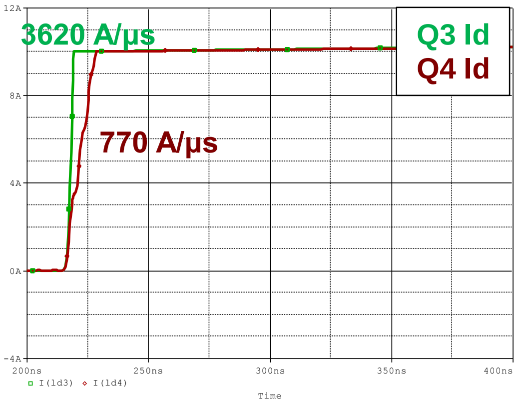


Figure 2.4.1.2 Turn-on current waveform

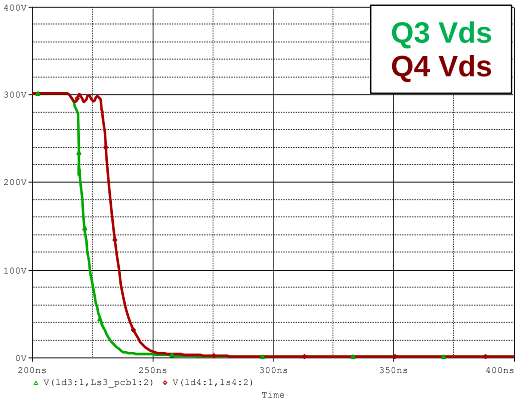
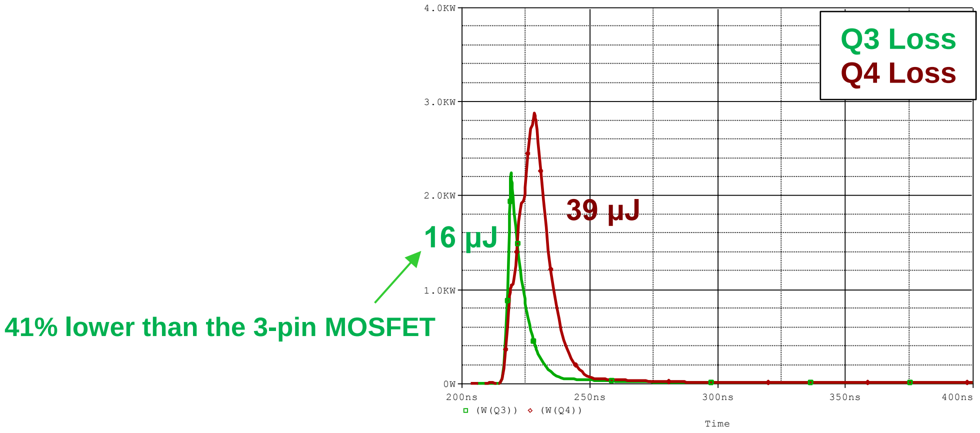


Figure 2.4.1.3 Turn-on voltage waveform



41% lower than the 3-pin MOSFET

Figure 2.4.1.4 Turn-on switching loss

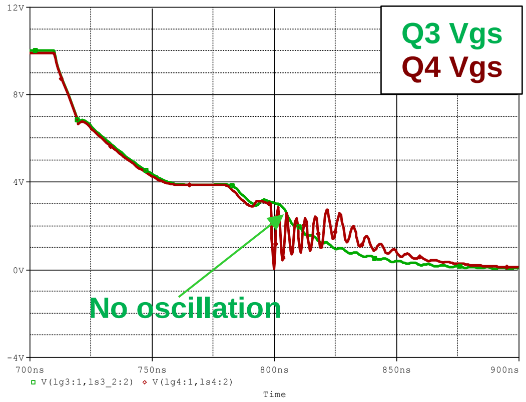
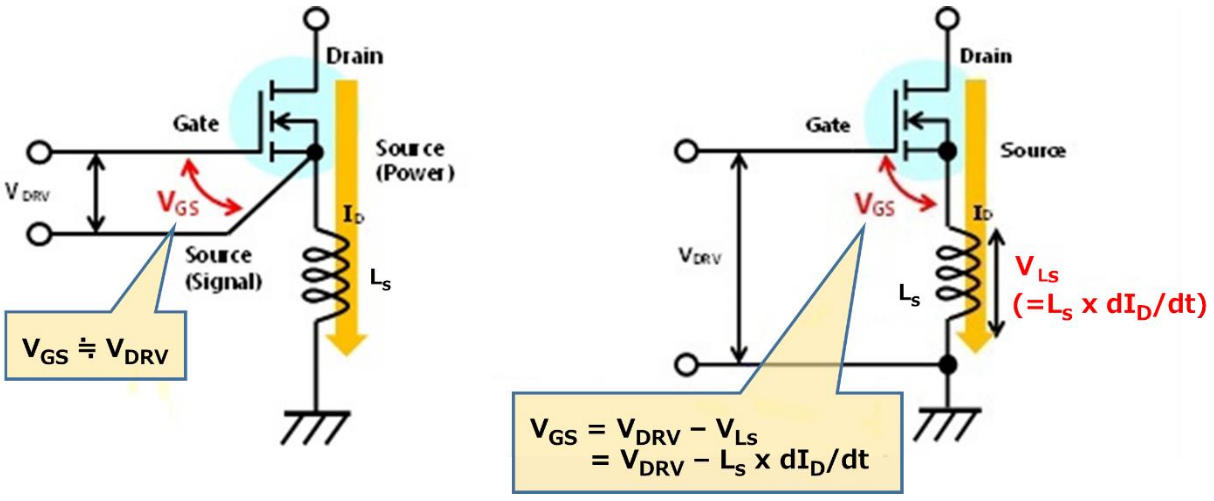


Figure 2.4.1.5 Turn-off gate waveform

The MOSFET in the 4-pin package did not have gate voltage oscillation during turn-off. It was confirmed that the use of the 4-pin TO-247-4L package is effective in suppressing gate voltage oscillation during turn-off.

In addition, the MOSFET in the 4-pin package had a higher switching speed and 41% less switching loss than the MOSFET in the 3-pin package. Because the 4-pin TO-247-4L package has separate gate drive path and drain current lines, the MOSFET does not suffer from a negative feedback effect on the gate drive. However, in the case of the 3-pin package, the source inductance (package lead + PCB trace) and the voltage induced by a rapid change in turn-on current exert a negative feedback effect on the gate drive. Figure 2.4.1.6 shows the gate drive path in the 3-pin and 4-pin packages. In the case of the 3-pin package, the voltage applied to the gate (V_{GS}) during turn-on is equal to the driver output voltage (V_{DRV}) minus a voltage induced by a drain current change due to the source inductance. In contrast, V_{GS} is almost equal to V_{DRV} in the case of the 4-pin package.

Next, we replaced the gate resistor with even a smaller-value resistor to determine whether it is possible to further reduce the switching loss and thereby increase power supply efficiency.



(a) 4-pin package (b) 3-pin package

Figure 2.4.1.6 Schematics of gate driving paths

2.4.2. Simulation for the MOSFET in the 4-pin package (Rg = 3.3 Ω)

In order to further increase the switching speed of the 4-pin MOSFET, we replaced the external 10-Ω gate resistor (Rgate3) in Figure 2.4.1.1 with a 3.3-Ω resistor. The following shows the simulation results.

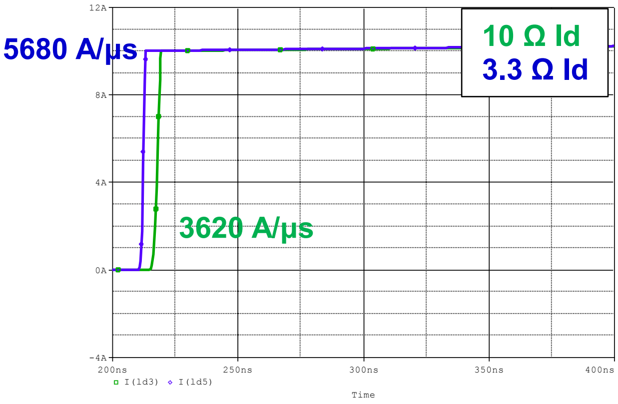


Figure 2.4.2.1 Turn-on current waveform

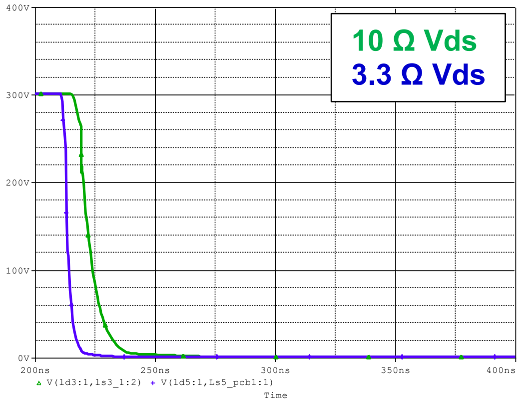


Figure 2.4.2.2 Turn-on voltage waveform

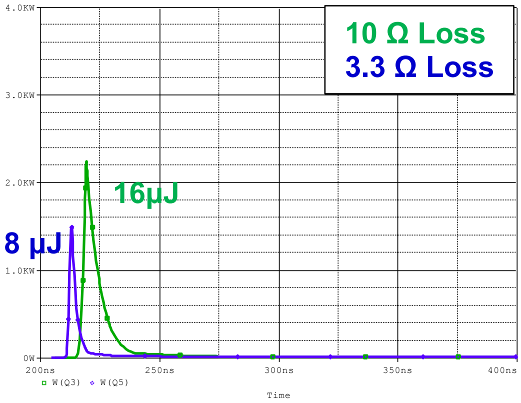


Figure 2.4.2.3 Turn-on switching loss

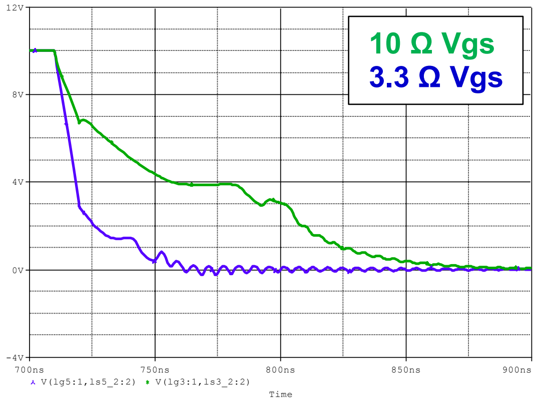


Figure 2.4.2.4 Turn-off gate waveform

The use of an external 3.3-Ω gate resistor increased the turn-on switching speed, reducing the switching loss by roughly 50%. In addition, gate voltage oscillation did not occur during turn-off. Whereas it was difficult to use a small-value gate resistor for a MOSFET in the 3-pin TO-247 package due to gate voltage oscillation, the MOSFET in the 4-pin TO-247-4L is less susceptible to gate voltage oscillation and thus allows the use of a small-value gate resistor. The MOSFET in the 4-pin package provides higher switching speed and higher efficiency.

3. Conclusion

We performed circuit simulations to analyze the switching characteristics of the TK25Z60X, a super-junction MOSFET in the 4-pin TO-247-4L package of the DTMOSIV-H series, in comparison with the TK25N60X in a 3-pin TO-247 package.

The MOSFET in the 3-pin package suffered gate voltage oscillation when an external gate resistor (Rg) value was reduced to increase the MOSFET switching speed and efficiency. In contrast, the 4-pin MOSFET was free from gate voltage oscillation. If the use of a MOSFET in a 3-pin package causes gate voltage oscillation due to the effects of PCB traces and the gate driving circuit, a MOSFET in a 4-pin package can be used as a solution. In addition, the MOSFET in a 4-pin package provides faster switching and lower turn-on loss than the MOSFET in a 3-pin package.

We also confirmed that, to reduce switching loss, a smaller external gate resistor can be used for the MOSFET in a 4-pin package. Even with a small gate resistor, gate voltage oscillation did not occur. The use of a MOSFET in the 4-pin TO-247-4L package is beneficial when you need to reduce switching loss.

Table 3.1 summarizes the simulation results.

Table 3.1 Simulation results

Product	Package	External gate resistor	Id slew rate	Turn-Off Gate Oscillation	Turn-On Switching Loss	Turn-On Switching Loss (Relative to the TK25N60X using 20-Ω gate resistor)
TK25Z60X	TO-247-4L (4-pin)	3.3 Ω	5680 A/µs	N	8 µJ	15%
		10 Ω	3620 A/µs	N	16 µJ	31%
TK25N60X	TO-247 (3-pin)	10 Ω	770 A/µs	Y	39 µJ	75%
		20 Ω	680 A/µs	N	52 µJ	—

The turn-on switching loss of the TK25Z60X in the 4-pin package with a 3.3-Ω external gate resistor was only 15% of that of the TK25N60X in the 3-pin package with a 20-Ω external gate resistor. For a typical PFC circuit with a 1.0-kW output, this translates to an efficiency increase of roughly 0.5%.

As described above, the use of a 4-pin package makes the MOSFET less susceptible to gate voltage oscillation and allows faster switching than a 3-pin package.

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