500 Server Power Supply

Design Guide

RD049-DGUIDE-01

TOSHIBA ELECTRONIC DEVICES & STORAGE CORPORATION

Contents

1. Introduction

This Design Guide describes the circuit design and the layout of the 500 W server power supply (this power supply). Refer to the *500 W Server Power Supply Reference Guide* for its specification, operation, and performance.

Components marked “Not Mounted” in the BOM are not used in this power supply even if component designators are shown in the circuit diagram. They are intended as reserved spaces for components necessary to modify circuit constants when designing an actual circuit.

1.1. Power MOSFET Used

Toshiba has the 600/650 V DTMOS series, which is suitable for the primary side (PFC/main switch) of AC-DC converters, and the low-voltage U-MOS series, which is suitable for the secondary side (synchronous rectifier and ORing). Both series offer an extensive lineup, allowing you to select the most suitable product according to the design specifications. The following is an introduction to the products used in this power supply.

TK090A65Z

In the PFC circuit

V_{DSS} = 600 V, $R_{DS(ON)}$(max) = 90 mΩ@V_{GS} = 10 V, TO-220SIS package

DTMOSVI process: high-speed switching and reduced switching loss

TK20A60W5

In the primary side of the LLC circuit

V_{DSS} = 600 V, $R_{DS(ON)}$(max) = 175 mΩ@V_{GS} = 10 V, TO-220SIS package

DTMOSIV process with built-in high-speed diode: reduced loss during reverse recovery operation

TPH1R306P1

In the synchronous rectification circuit on the secondary side of the LLC circuit

V_{DSS} = 60 V, $R_{DS(ON)}$(max) = 1.28 mΩ@V_{GS} = 10 V, SOP Advance package

U-MOSIX-H process: suitable for switching applications, and optimized cell construction to suppress surge-voltage during switching

TPHR9203PL

In the output ORing circuit

V_{DSS} = 30 V, $R_{DS(ON)}$(max) = 0.92 mΩ@V_{GS} = 10 V, SOP Advance package

U-MOSIX-H process: low on-resistance to reduce power dissipation in ORing circuit

2. Circuit Design

This section describes the points of circuit design of this power supply.

2.1. AC Line Circuit Design

Fig. 2.1 shows the AC line circuit and explains the basic design method.

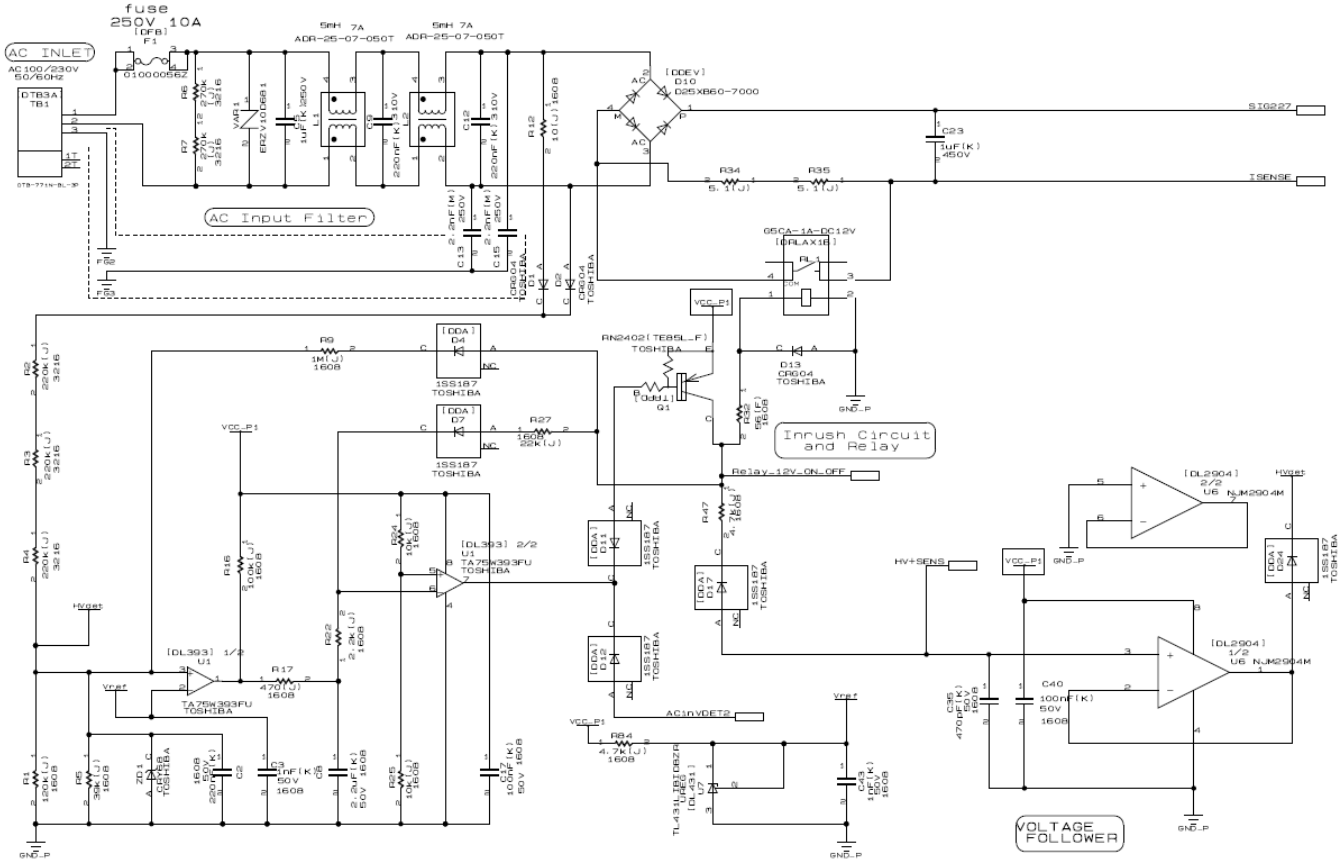

Fig. 2.1 AC Line Circuit

Fuse

A fuse (F1) is used to shut off the AC line when an excessive current flows through the AC line. Select a fuse from the maximum AC line current value. Using the maximum power, Pout, PFC power supply efficiency, η1, LLC power supply efficiency, η2, power factor, PF, and AC line voltage value, $VinAC_{min}$, calculate the maximum AC line current, $ACin_{peakrms}$ with the following equation.

$$ACin_{peakrms} = \frac{Pout}{\eta 1 \times \eta 2 \times PF \times VinAC_{min}}$$

The output specification of this power supply is 500 W. Since the power supply efficiency of the PFC decreases when the AC line voltage is low, the AC line current effective value (max) is calculated by setting the AC line voltage effective value (min) to 90 V of the minimum value of the 100 V system.

Assuming that the input voltage (min AC value) = 90 V, the maximum power = 500 W, the PFC power supply efficiency (η1) = 94 %, the LLC power supply efficiency (η2) = 94 %, and the power

factor = 0.99, the maximum AC line current value of this power supply is approximately 6.4 A. Select a 10 A fuse with margins to this power supply

When selecting a fuse, it is necessary to consider the inrush current when the AC power is turned on, whether the product has obtained the safety standards to be complied with, etc., in addition to the maximum current above.

Varistor

A metal oxide varistor (VAR1) is used to protect the circuitry when surge voltages due to lightning strike are applied to the AC line. Select a varistor using the voltage value of the AC line. Since the maximum AC line voltage of this power supply is 264 V and the maximum instantaneous voltage value is 373 V, a varistor with a maximum allowable circuit voltage of 420 V (AC rms value) and a varistor voltage of 680 V is used in addition to the margin.

Select the product considering not only the maximum allowable circuit voltage and varistor voltage, but also the surge current withstand capability and energy withstand capability. In addition, since a failure mode of varistor is short mode generally, insert a fuse to the front stage (input side of the AC line) of the varistor.

X capacitor discharge resistance

X capacitors Cx (C5, C9, C12) need resistors Rdis (R6, R7) for discharging. Set the resistance value to meet the safety standards. For example, if the safety standard that the system should comply with requires that the line voltage become less than or equal to the safety voltage (Vsafe) within t seconds after the AC plug is unplugged, to satisfy the standard even if the AC plug is unplugged when the AC line voltage is peaked, set the discharge resistance value that satisfies the following equation.

$$Rdis \leq \frac{t}{Cx \times ln\left(\frac{VinAC \times \sqrt{2}}{Vsafe}\right)}$$

When t is set to 2 seconds and Vsafe is set to 60 V, Rdis is 759 kΩ or less when Cx is 1.44 μF and VinAC is the highest, 264 V. Rdis is assumed to be 540 kΩ (R6 and R7 are 270 kΩ) considering variations in capacitance and resistance values and design margins. In addition, the loss of resistance is as follows.

$$Rloss = \frac{VinAC^2}{Rdis}$$

The total power loss (Rloss) in the discharge-resistor Rdis is 129 mW when VinAC is 264 V. Reducing the resistance value of the discharging resistor makes it easier to satisfy the safety standards, but the power loss (Rloss) of the resistor increases. If power loss due to resistance is unacceptable for the system, use an IC for X-CON discharge that connects the discharge path of the X-CON only when AC power is lost.

EMI countermeasure parts

Y capacitors (C13, C15) and common mode chokes (L1, L2) are used to suppress common mode noise. In addition, X capacitors (C5, C9, C12) are used to suppress differential noise. Since each

noise level is affected by the PCB layout and the chassis design, change, delete, or add the aforementioned parts as necessary. Note that this power supply does not have a sufficient Y-capacitor because it does not have a chassis. When designing a system with a chassis, install a Y capacitor sufficient to prevent common mode noise. Note that when installing a Y capacitor, if the capacitance value is increased, the leakage current will increase. Therefore, confirm that safety standards are satisfied.

Inrush current countermeasures

Resistors (R34, R35) and relay (RL1) are used to suppress inrush current when AC power is turned on. When the AC power is turned on, inrush current is suppressed because the relay (RL1) becomes open and AC-line current flows to the resistors (R34 and R35). After the AC power supply is turned on, when the specified conditions are satisfied, the (RL1) conducts. When the relay (RL1) conducts, the resistors (R34 and R35) that have suppressed the AC-line current are short-circuited, thereby reducing power dissipation during operation. Resistors (R34 and R35) must be specified to withstand inrush current. Also, confirm that the conditions and timing for opening and continuity of the relay (RL1) satisfy the required specifications.

Bridge diode

Use bridge diode (D10) for rectifying diode. Match the product ratings with the inrush current value and the maximum applied voltage.

2.2. Power Factor Correction (PFC) Circuit Design

To improve the power factor, PFC circuitry using a CCM-mode PFC controller (UCC28180D) manufactured by Texas Instruments is used. Fig. 2.2 shows the PFC circuit 1 (around the controller) and explains the basic design method. For detailed designs of the surroundings, refer to the datasheet and related documents of the PFC Controller (UCC28180D).

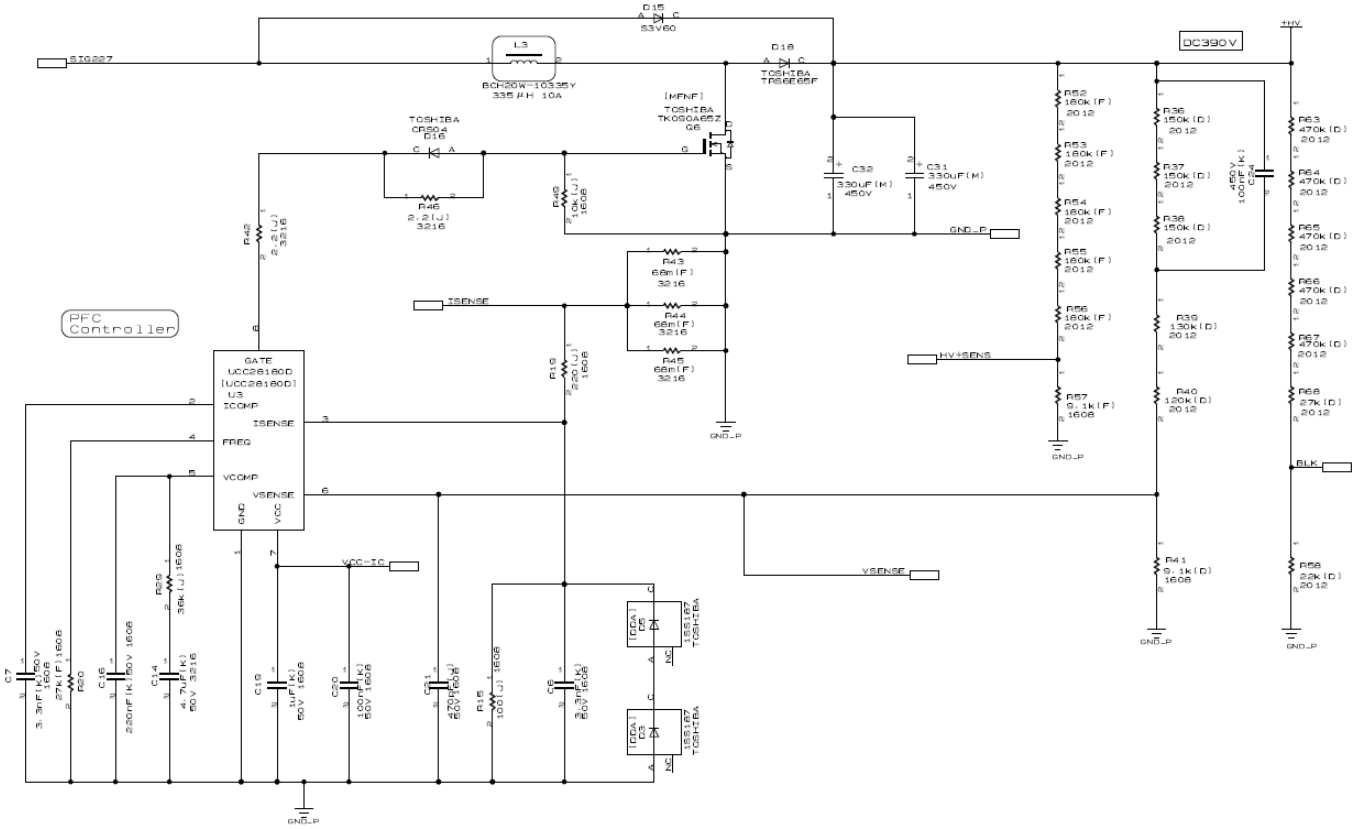

Fig. 2.2 PFC Circuit 1 (Around the Controller)

Output voltage

Fig. 2.3 shows the output voltage setting circuit. The PFC output-voltage (Vout_PFC) is set by resistors (R36-R41). The PFC controller controls the output voltage (Vout_PFC) so that the output terminal sense voltage (VSENSE) divided by these resistors matches the internal reference voltage Vref_PFC (5 V) of the PFC controller (UCC28180D). Calculate the output voltage (Vout_PFC) at Ta = 25 °C using the following equation as the bias current Ibias_PFC to VSENSE pin voltage (100nA).

$$Vout\_PFC = \frac{Vref\_PFC \times (R36+R37+R38+R39+R40+R41)}{R41} + Ibias\_PFC \times (R36+R37+R38+R39+R40)$$

The setting of the output voltage (Vout_PFC) is approximately 390 V, and the resistance value of R36-R38 is 150 kΩ, the resistance value of R39 is 130 kΩ, the resistance value of R40 is 120 kΩ, and the resistance value of R41 is 9.1 kΩ.

Next, consider the variation of the output voltage. Calculate the Vout_PFC $_{min}$ and Vout_PFC $_{max}$ using the variations of the parameters in the above output voltage calculation formulas as follows.

Vref_PFC :4.87 V (min) ,5.15 V (max)

Ibias_PFC :20 nA (min) ,250 nA (max)

R36-R40 : (D) Deviation, TCR = ±100 ppm/°C

R41 : (D) Deviation, TCR = ±50 ppm/°C

Operating temperature :0 ℃ (min), 55 ℃ (max)

Regarding the temperature change of R36-R41, the positive direction shall be +45℃ considering the difference of 30℃ from Ta = 25 ℃ to the upper operating temperature limit of 55℃ and the temperature rise of 15℃ inside the equipment, and the negative direction shall be-25℃ from Ta = 25 ℃ to the lower operating temperature limit of 0℃. When the square root is used to calculate the effect of the variations in the above parameters, the Vout_PFC $_{min}$ and the Vout_PFC $_{max}$ are as follows.

Vout_PFC$_{min}$ = 379.1 V

Vout_PFC$_{max}$ = 401.8 V

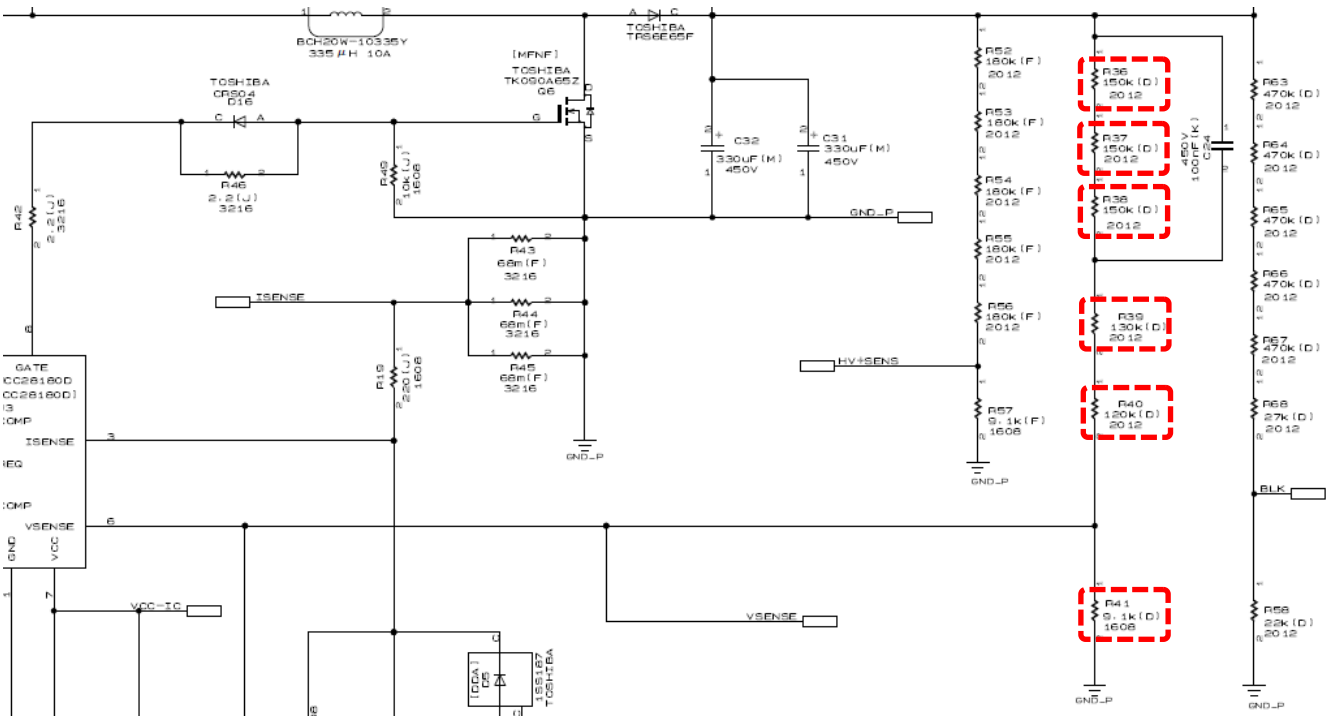

Fig. 2.3 Output Voltage Setting Circuit

Gate drive circuit

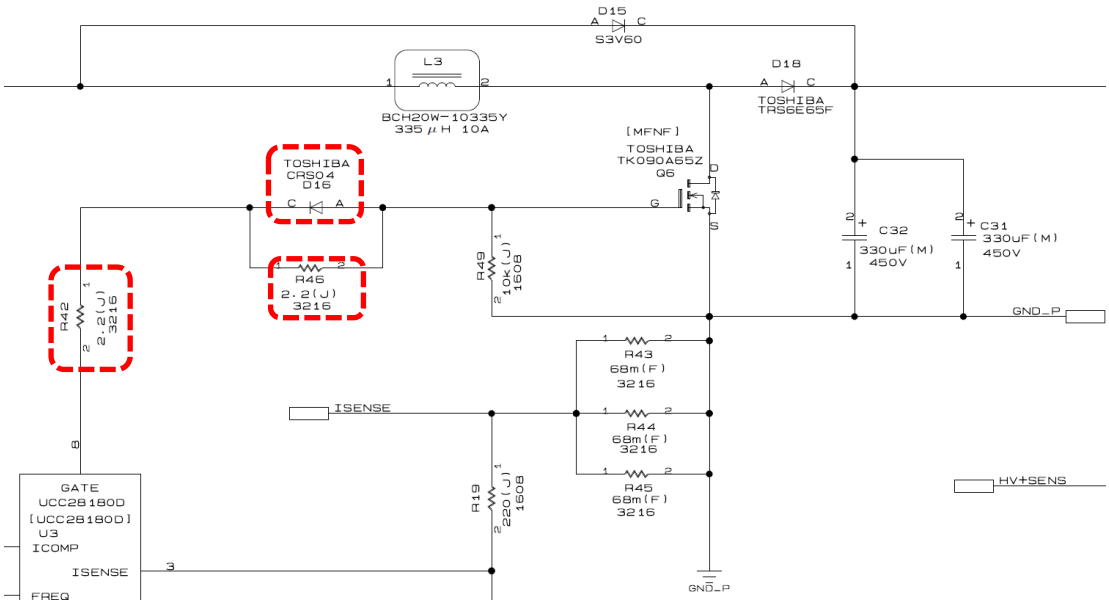

Fig. 2.4 Gate Drive Circuit

Fig. 2.4 shows the gate drive circuit. Gate drive design affects power supply efficiency and EMI (noise). Generally, there is a trade-off between power efficiency and EMI (noise), and a balanced design is required. To reduce EMI (noise), adjust the resistance value of the gate series resistors (R42, R46) and check it. In the gate drive circuit, turn-on speed and turn-off speed of MOSFET are adjustable individually. If EMI (noise) occurs both at turn-on and turn-off of MOSFET, increase the resistor R42. This allows you to reduce turn-on and turn-off speeds at the same time, reducing EMI (noise). If EMI (noise) is present when MOSFET turns on, increase the R46. This reduces the turn-on speed only and reduces EMI (noise).

Note that increasing the resistors (R42, R46) may reduce the switching speed of MOSFET, which may also reduce the power-supply efficiency. Check that the power supply efficiency specification and heat dissipation specification satisfy the required specification.

Switching frequency

Fig. 2.5 shows the switching frequency adjustment circuit. The switching frequency (fpwm1) of the PFC controller (UCC28180D) is calculated by the following equation.

$$fpwm1 = \frac{65kHz \times 32.7k\Omega \times 1M\Omega + 65kHz \times 32.7k\Omega \times R20}{R20 \times 1M\Omega + 65kHz \times 32.7k\Omega \times R20}$$

The setting of the switching frequency (fpwm1) is 78 3 kHz, and the resistance R20 is 27 kΩ.

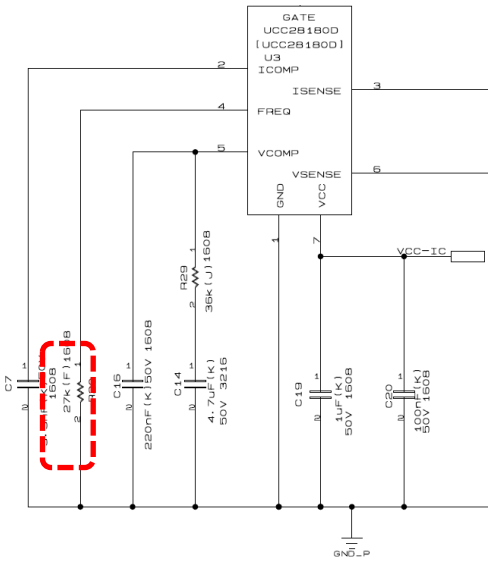

Fig. 2.5 Switching Frequency Adjustment Circuit

Inductor

Fig. 2.6 shows the inductor peripheral circuit. Set the inductance (L) of inductor L3 with the following items.

1. Max. Output Power (Pout)
2. RMS AC-Line Voltage (VinAC)
3. Total power conversion efficiency (η1 x η2) and power factor (PF) of this power supply
4. PFC output voltage (Vout_PFC)
5. Switching frequency(f_{PWM1})

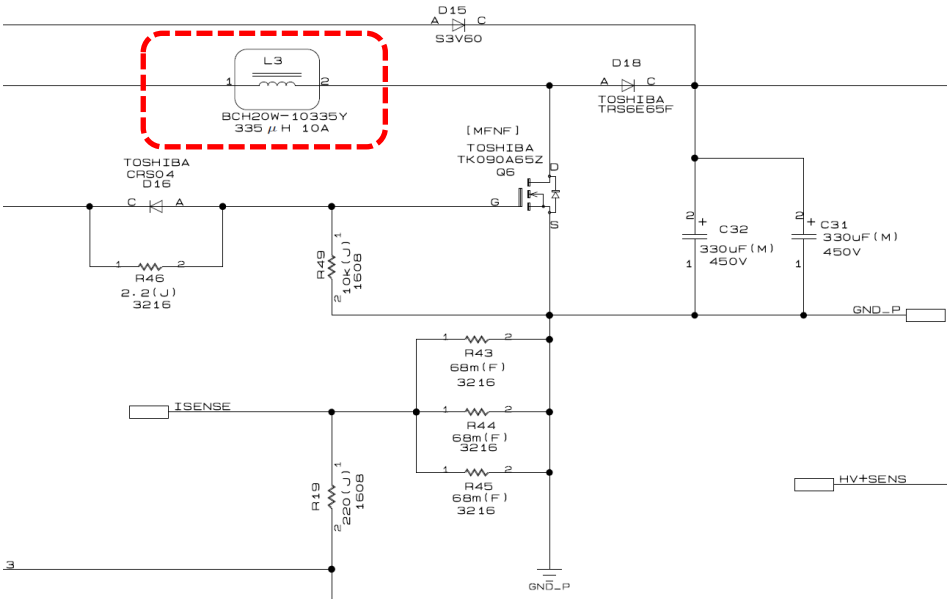

Fig. 2.6 Inductor Peripheral Circuit

Setting the Inductor Ripple Current (ΔI) to 33.5% of the AC Line's Peak Input Current Value (ACin) ($_{peak}$), the Inductance (L) value can be calculated by the following equation:

$$ACin_{peak} = \frac{Pout \times \sqrt{2}}{\eta 1 \times \eta 2 \times PF \times VinAC_{min}}$$

$$\Delta I = ACin_{peak} \times 33.5\%$$

$$L = \frac{\left(Vout\_PFC - \sqrt{2} \times VinAC_{min}\right) \times \eta 1 \times \eta 2 \times PF \times {VinAC_{min}}^2}{30\% \times f_{PWM1} \times Vout\_PFC \times P_{out}}$$

When the maximum output power (Pout) is 500 W, the RMS AC line voltage (VinAC) is 85V, the PFC power supply efficiency (η1) is 94 %, the LLC power supply efficiency (η2) is 94 %, the power factor (PF) is 0.99, the PFC output voltage (Vout_PFC) is 390 V, and the switching frequency (f_{PWM1}) is 78 3 kHz, the inductance (L) is calculated as 333 μH. Magnetic saturation due to load current must be considered when selecting an inductor. This power supply uses an inductgor with an inductance value of 335 μH at 10 A.

The peak current (IL_{peak}) flowing through the inductor is calculated by the following equation using the AC-line peak input current (ACin's $_{peak}$).

$$IL_{peak} = ACin_{peak} + \frac{\Delta I}{2}$$

Because the AC line peak input current (ACin) is 9.5 A, the peak current (IL_{peak}) that flows through the inductor is 11.1 A, and you must select an inductor that can pass 11.1 A or more.

Current limiter

Fig. 2.7 shows the current limiter circuit. The current limiter level of the PFC circuit is set by the current sense resistors (R43-R45) of the PFC circuit. The PFC controller (UCC28180D) controls the current limiter in two stages according to the voltage generated by the load current and the current sense resistor (R43-R45). The first stage current limiter is activated when the voltage value at ISENSE pin reaches the current limit threshold V_limit1. This causes the PFC controller (UCC28180D) to activate a circuitry that bypasses VCOMP pins to GND at 4 kΩ. Although this operation does not directly stop the gate drive signal, the output current is reduced equivalently. The current limiter of the second stage is activated when the voltage value at ISENSE pin reaches the current limit threshold V_limit2. In this situation, the PFC controller (UCC28180D) turns the gate drive signal (GATE) Disable on a pulse-by-pulse basis. Generally, the first stage current limiter is used as protection against excessive load current caused by some abnormality, and the second stage current limiter is used as protection against inductor saturation.

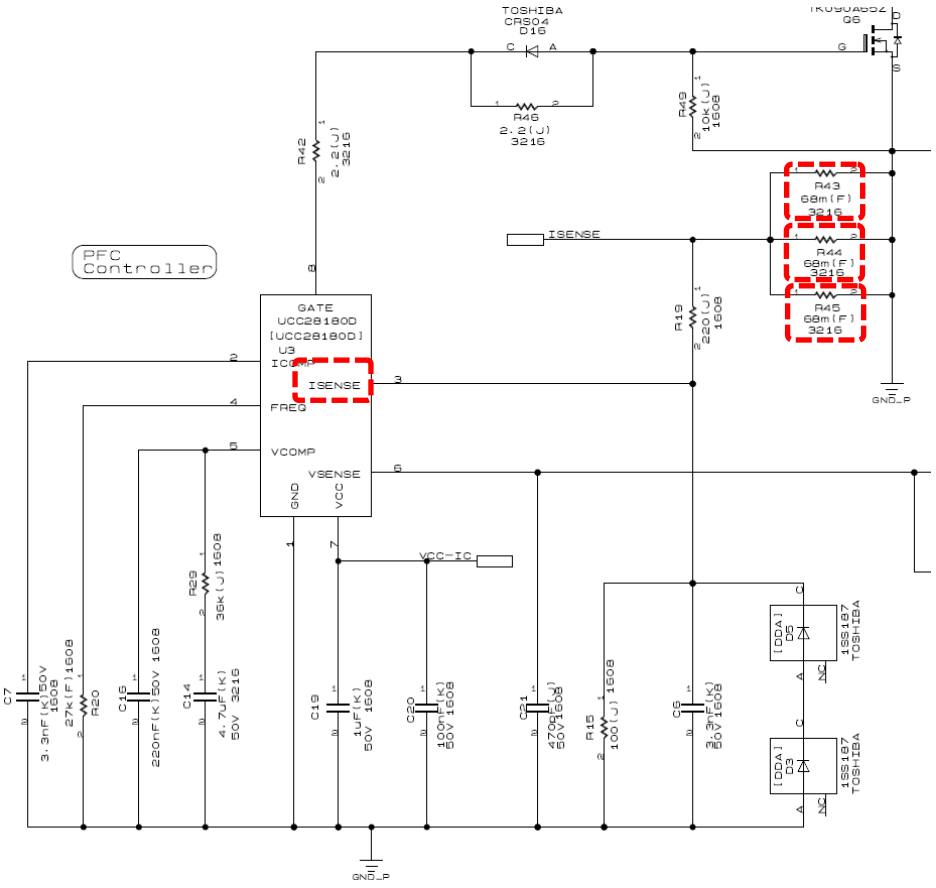

Fig. 2.7 Current Limiter Circuit

Calculate the setting value (I_limit1) of the current limiter level in the first stage using the following equation.

$$I\_limit1 = \frac{V\_limit1}{R43//R44//R45}$$

If the current limit threshold V_limit1 is 0.285 V and the current sense resistor (R43-R45) is 68 mΩ, the current limiter level setting is 12.6 A.

Calculate the setting value (I_limit2) of the current limiter level in the second stage using the following equation.

$$I\_limit2 = \frac{V\_limit2}{R43//R44//R45}$$

If the current limit threshold V_limit2 is 0.4 V and the current sense resistor (R43-R45) is 68 mΩ, the current limiter level setting is 17.7 A. The design of the current limiter circuit should take into account various variations.

As for the current detection resistor, it is necessary to select a product with rated power that does not pose a problem even if the maximum RMS current value of the AC line flows.$\mathrm{ACin}_{peakrms}$

Output capacitor

Fig. 2.8 shows the peripheral circuit of the output capacitor. For the capacitance of the output capacitors (C31, C32, Cout_PFC) is calculated based on hold-up time requirements.

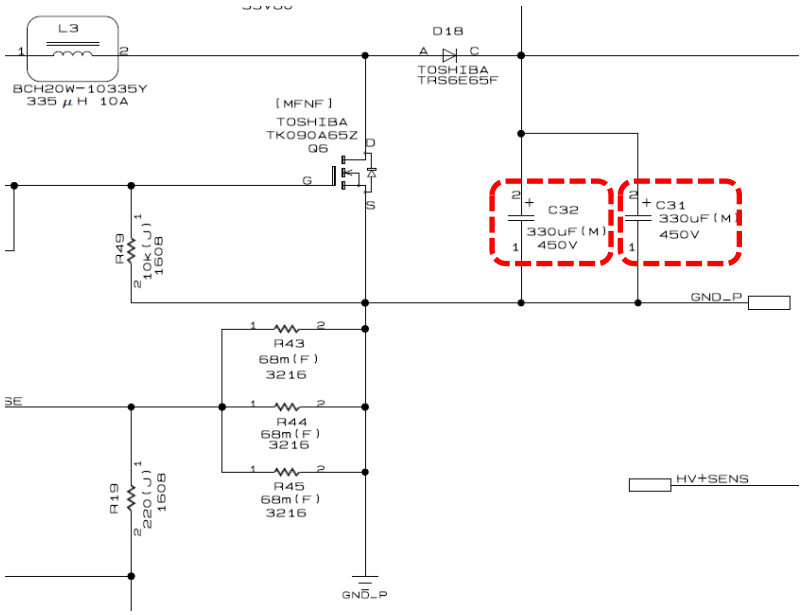

Fig. 2.8 Output Capacitor Peripheral Circuit

The hold-up time (Thold) is calculated by Cout_PFC and the output voltage (Vout_PFC), the output low limit voltage (Vout_PFC_hold), the maximum output power (Pout), and the LLC power supply efficiency (η2).

$$Thold = Cout\_PFC \times \frac{(Vout\_PFC^2 - Vout\_PFC\_hold^2) \times \eta 2}{2 \times Pout}$$

When the capacitance (Cout_PFC) setting is 660μF, the output voltage (Vout_PFC) is 390 V, the output low limit voltage (Vout_PFC_hold) is 330 V, the LLC power supply efficiency (η2) is 94 %, and the maximum output power (Pout) is 500 W, the hold-up time (Thold) is 26.8 ms.

In addition, when there is a required specification for the output ripple, set it by the following method.

1. Determine the capacitance value of the output capacitor (Cout_PFC) that satisfies the output ripple specification.
2. Calculate the capacitance value of the output capacitor (Cout_PFC) that satisfies the hold-up time.
3. Compare the capacitance values of both, and choose a large value.

Consider tolerances and aging degradation when selecting the output capacitor (Cout_PFC).

2.3. LLC Circuit Design

This power supply generates 500 W/12 V output in the LLC resonance circuit. The LLC-resonant circuitry alternately turns on/off the high-side MOSFET and low-side MOSFET of each arm on the input side at a duty of 50%, and adjusts the switching frequency according to the load to control the output voltage. When the high-side MOSFET and low-side MOSFET are switched, a dead-time is provided to prevent penetration. However, MOSFET is Zero Volt Switching (ZVS) due to co-oscillation operation during that period. ZVS reduces switching losses and enables a high-efficiency power supply. This power supply uses a controller UCC256303 manufactured by Texas Instruments (LLC controller) to form an LLC resonator. Fig. 2.9 shows the LLC power supply circuit (around the LLC controller) and explains the basic design method. Refer to the LLC Controller (UCC256303) datasheet and related documents for detailed designs of the surroundings.

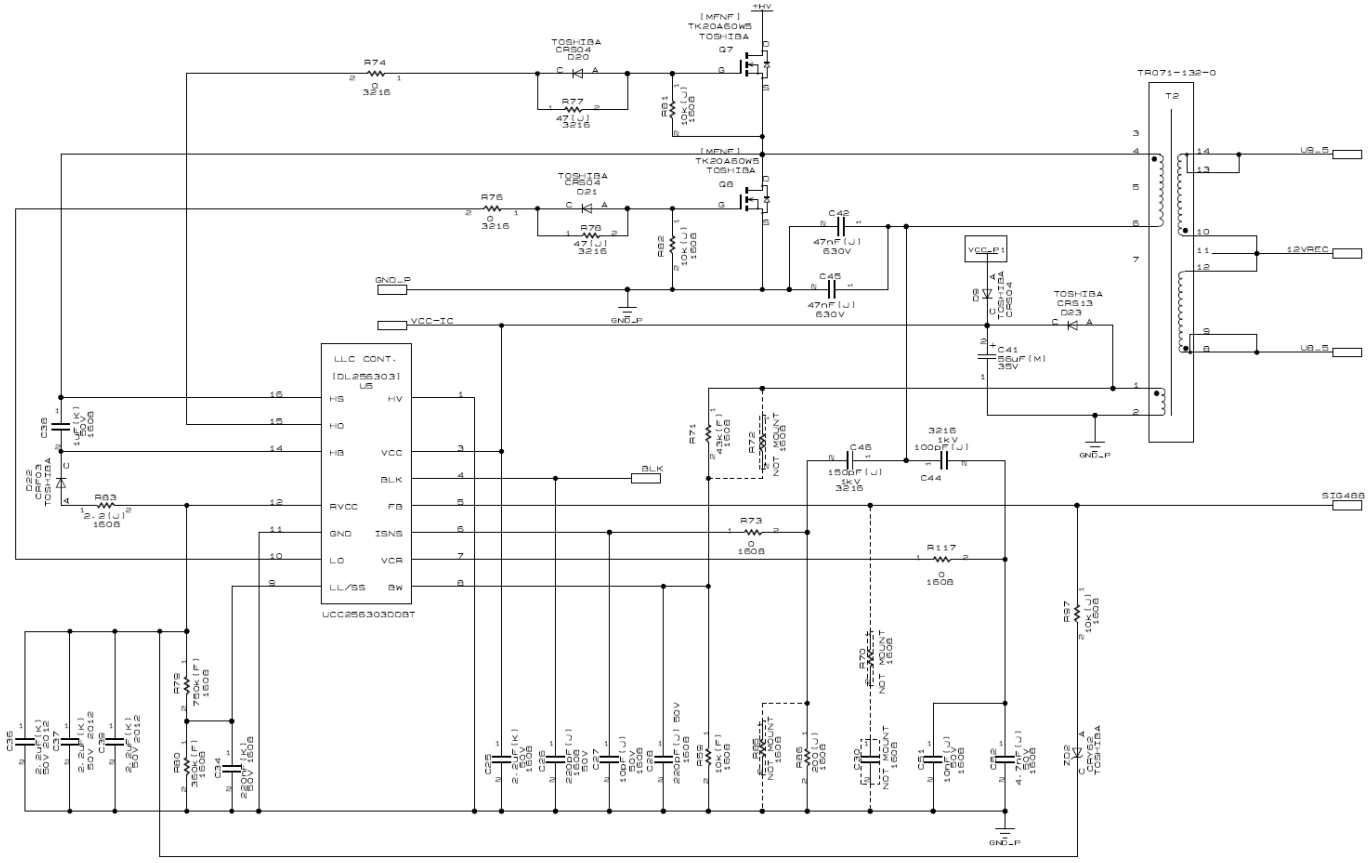

Fig. 2.9　LLC Circuit (Around the LLC Controller)

Setting operating input voltage range

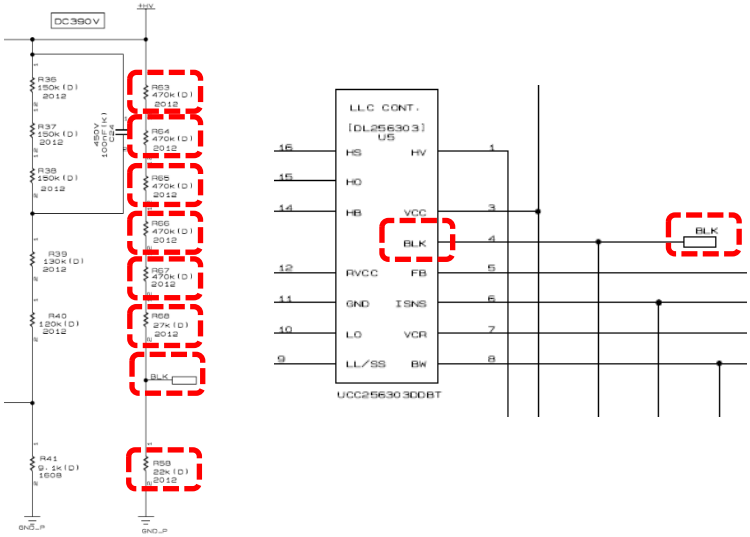

Fig. 2.10 LLC Operation Lower Limit Input Voltage Setting Circuit

Fig. 2.10 shows the LLC operation lower limit input voltage setting circuit. The LLC circuit operates on the output of the PFC circuit as an input power supply. The LLC controller detects the output voltage of the PFC circuit and starts operation. The operating voltage range of the LLC controller is set by the resistance value of the external resistors (R58, R63-R68). The operating voltage range ($V_{in\_min\_on}$, $V_{in\_min\_off}$) of the LLC circuit is set by dividing the output voltage Vout_PFC of the PFC circuit with resistors (R58, R63-R68) and inputting it to the BLK pin of the LLC controller (U5). The LLC controller (U5) starts switching when the BLK pin voltage generated by dividing these resistors exceeds the operation start threshold voltage (3.05V), and stops switching when it falls below the operation stop threshold voltage (2.17 V). Calculate the operating voltage lower limit ($V_{in\_min\_on}$, $V_{in\_min\_off}$) using the following equation.

$$V_{in\_min\_on}(V) = 3.05V \times \frac{(R58 + R63 + R64 + R65 + R66 + R67 + R68)}{R58}$$

$$V_{in\_min\_off}(V) = 2.17V \times \frac{(R58 + R63 + R64 + R65 + R66 + R67 + R68)}{R58}$$

In this power supply, the set value of the output voltage $V_{in\_min\_on}$ of the PFC where the LLC circuit starts operation is set to 333 V, and the set value of the output voltage $V_{in\_min\_off}$ of the PFC where the LLC circuit stops operation is set to 237 V. As shown in Fig. 2.9, 22 kΩ is selected for resistor (R58), 470 kΩ for resistor (R63-R67), and 27 kΩ for resistor (R68). Fig. 2.11 shows the relation between the input voltage (V_{in}) and the BLK pin voltage and the switching operation status.

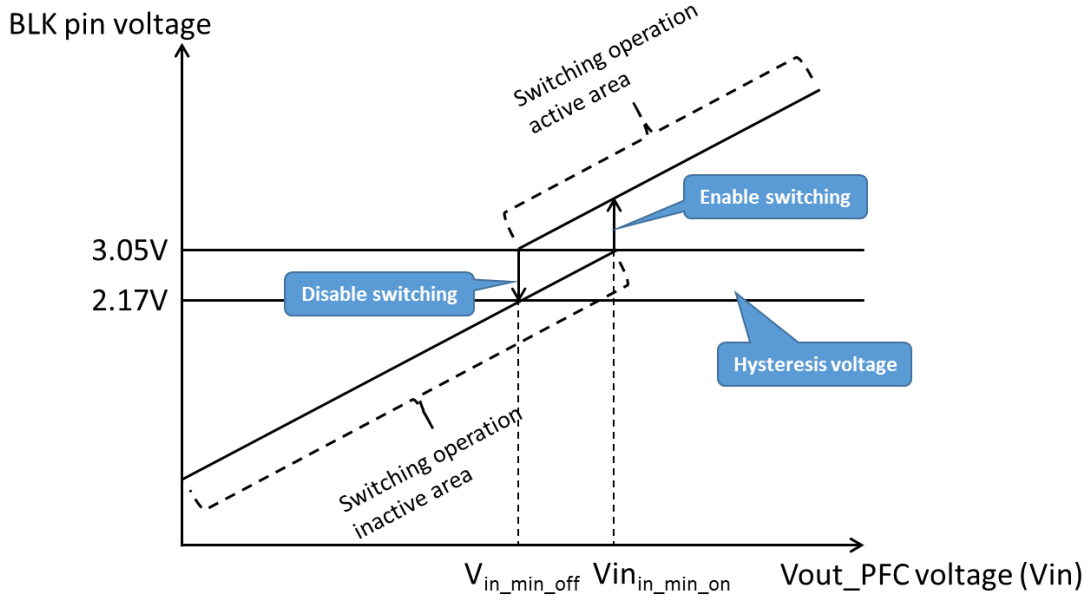

Fig. 2.11 Input Voltage vs BLK Pin Voltage, Switching Operation Status

Setting output voltage

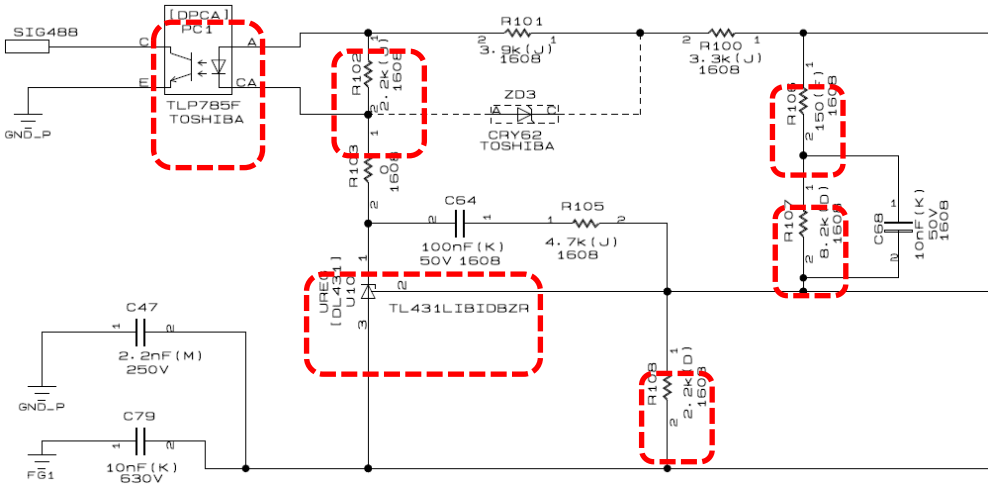

Fig. 2.12 Output Voltage Setting Circuit

Fig. 2.12 shows the output voltage setting circuit. Set the output voltage (Vout_LLC) of this power supply with the resistors (R106, R107, R108) and the shunt regulator (U10). The shunt regulator (TLVH431LIBIDBZR) controls the current of the photocoupler (PC1) so that the voltage obtained by dividing the output voltage of this power supply by the resistor (R106, R107, R108) matches the reference voltage Vref_LLC (2.495 V). The LLC controller operates to maintain a constant output-voltage (Vout_LLC) depending on the amount of current feedback from the photocoupler (PC1). Using the bias current to the REF pin voltage of the shunt regulator as Ibias_LLC (200 nA), calculate the output voltage (Vout_LLC) using the following equation.

$$Vout\_LLC \ = \frac{Vref\_LLC \times (R106 + R107 + R108)}{R108} + Ibias\_LLC \times (R106 + R107)$$

The output voltage (Vout_LLC) is set to 11.97 V with R106 = 150 Ω, R107 = 8.2 kΩ, and R108 = 2.2 kΩ.

Next, consider the variation of the output voltage. We calculate the minimum value of Vout_LLC and the maximum value of Vout_LLC by assuming that the variations in each parameter in the above output voltage calculation formula are as follows.

Vref_PFC :2.466 V (min), 2.524 V (max)

Ibias_LLC : 0A (min) and 400 nA (max) min. Because there is no minimum specification, 0A is used.

R106 :(F) Deviation, TCR = ±100 ppm/°C

R107 :(D) Deviation, TCR = ±100 ppm/°C

R108 :(D) Deviation, TCR = ±50 ppm/°C

Operating temperature :0 ℃ (min) ,55 ℃ (max)

Regarding the temperature change of R106-R108, the positive direction shall be +45 ℃ considering the difference of 30 ℃ from Ta = 25 ℃ to the upper limit of 55 ℃ and the temperature rise of 15 ℃ inside the equipment, and the negative direction shall be-25 ℃ from Ta = 25 ℃ to the lower limit of 0 ℃. When the square root is used to calculate the effect of variations in the above parameters, the Vout_LLC $_{min}$ and the Vout_LLC $_{max}$ are as follows.

Vout_LLC$_{min}$ = 11.80 V

Vout_LLC$_{max}$ = 12.14 V

The resistor (R102) connected in parallel to the photocoupler must be set to ensure the minimum cathode current of the shunt regulator, taking into account various variations in the photocoupler's conversion efficiency, aging, and feedback current on the primary side.

Transformer (Resonance Design)

We will proceed with the study using the fundamental approximation method (FHA). Fig. 2.13 shows the basic circuit of the LLC resonant circuit, and Fig. 2.14 shows a simple equivalent circuit.

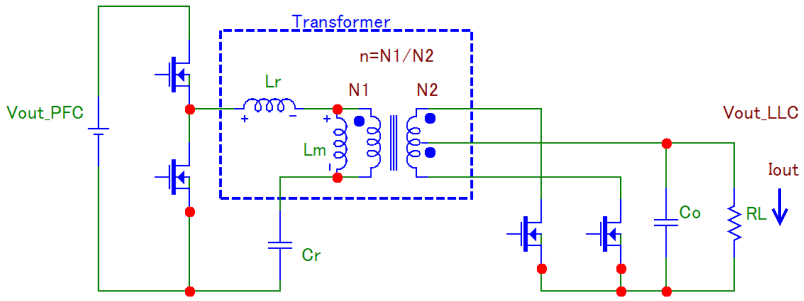

Fig. 2.13 LLC Resonant Basic Circuit

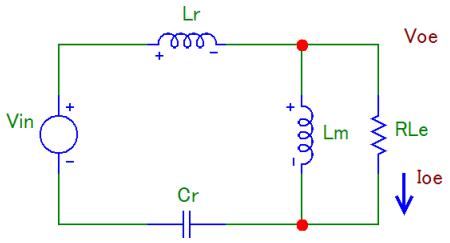

Fig. 2.14 Simple Equivalent Circuit

・Determination of turn ratio

Determine the turn ratio n. The turn ratio n is calculated by the following equation using the output voltage of PFC, Vout_PFC, and the output voltage of LLC, Vout_LLC.

$$n = \frac{Vout\_PFC}{2 \times Vout\_LLC}$$

n = 16.5 is set, because Vout_PFC is 390 V, Vout_LLC is 12 V, and n = 16.25.

・ Resonant Circuit Gain Determination

Calculate the required gain for the LLC resonant circuit. The maximum gain required by the LLC resonator in normal times, Mg_nom_{max}, is calculated by the following equation.

$$Mg\_nom_{max} = \frac{n \times Vout\_LLC_{max}}{Vout\_PFC_{min} /2}$$

Mg_nom_{max} = 1.06 because n is 16.5, the Vout_LLC $_{max}$ is 12.14 V, and the steady-state Vout_PFC $_{min}$ is 379.1 V. Allows gain to secure Mg_nom_{max} = 1.06 at 110% load including margins in max load.

Next, calculate the maximum gain required by the LLC-resonant circuitry in the event of an instantaneous power failure, Mg_hold $_{max}$. In the event of an instantaneous power failure, it is assumed that there is no problem if a gain that allows the output to secure a reduction value under the specification of the LLC output voltage at the maximum load is ensured, and the value is calculated using the following formula.

$$Mg\_hold_{max} = \frac{n \times Vout\_LLC\_Spec_{min}}{Vout\_PFC\_hold /2}$$

The Mg_hold_{max} is = 1.14 because n is 16.5, the output power supply voltage lower limit of this power supply, $Vout\_LLC\_Spec_{min}$, is 11.4 V, and output voltage at the instantaneous powe4r failure, Vout_PFC_hold, is 330 V.

From the above, the gain required for the LLC resonator is Mg_nom_{max} = 1.06 at 110% load and Mg_hold_{max} = 1.14 at 100% load. In the following calculations, we proceed with designing the resonant circuit with the required maximum gain, $Mg_{max,}$ = Mg_hold_{max} = 1.14 for the LLC resonant

circuit, and confirm that at the final stage of designing, the gain at 110 % loading can ensure Mg_nom_{max} = 1.06.

Calculate the minimum gain required by the LLC resonant circuit, Mg_{min}, using the following formula.

$$Mg_{min} = \frac{n \times Vout\_LLC_{min}}{Vout\_PFC_{max} / 2}$$

Mg_{min} = 0.97 because n is 16.5, the $Vout\_LLC_{min}$ is 11.80 V, and the steady-state $Vout\_PFC_{max}$ is 401.8 V.

・ Resonant circuit quality factor derivation

Fig. 2.15 shows the relationship between the maximum gain value of the LLC resonant circuit, Mg_{max} , in the fundamental approximation method (FHA) and the quality factor of the resonant circuit, Qe. Ln in the figure represents the ratio of the excitation inductance Lm of the transformer to the parasitic inductance Lr (Ln = Lm/Lr). If Ln = 5.5, then the quality factor Qe of the LLC-resonator is 0.53 when Mg_{max} = 1.14. The quality factor Qe is as follows:

$$Qe = \frac{\sqrt{Lr/Cr}}{RLe}$$

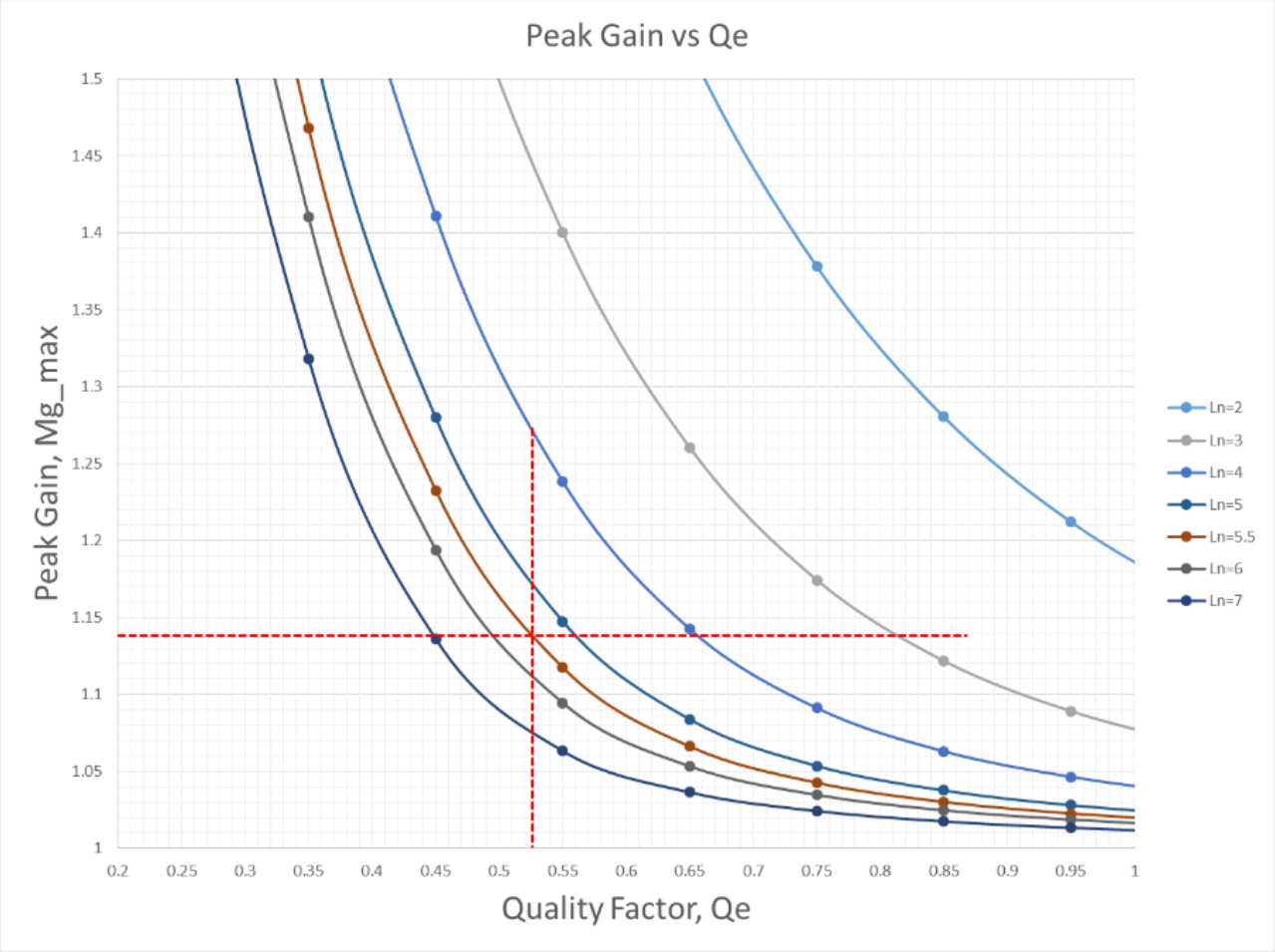

Fig. 2.15 Peak Gain vs Quality Factor

・Calculation of equivalent load resistance

The equivalent load-resistance R_{Le} in the simplified equivalent circuit of the LLC-resonant circuit is calculated by the following equation.

$$R_{Le} = \frac{8n^2}{\pi^2} R_L$$

Since R_L at the maximum load is 12 V/41.7 A = 0.288 ohms, R_{Le} at the maximum load is 63.56 ohms.

・ Calculation of Cr, Lr, Lm

When the resonance frequency of Lr and Cr is f0, Cr is as follows:

$$Cr = \frac{1}{2 \times \pi \times f0 \times R_{Le} \times Qe}$$

Here, if f0 is assumed to be 55 kHz, Cr is calculated as 86 nF because R_{Le} is 63.56 Ω and Qe is 0.53. In this case, two 47 nF units are used to set Cr = 94 nF.

Since Lr is the following equation, it is calculated to be 89 μH, and this time it is assumed to be 90 μH.

$$Lr = \frac{1}{(2 \times \pi \times f0)^2 \times Cr}$$

Lm is as shown in the following equation.

$Lm = Ln \times Lr$

Since Ln is 5.5, Lm is calculated as 495 μH, and this time it is assumed to be 500 μH.

・ Determination of Cr, Lr, Lm

The specifications of the transformer and resonant capacitor Cr created based on the above calculation results are as follows.

Turn ratio n = 16.5 (Np:Ns = 33:2)
Exciting Inductance Lm = 500 μH
Parasitic inductanceLr =90 μH
Resonant capacitor Cr = 94 nF

・ Resonant circuit gain check

Fig. 2.16 shows the relation between the switching frequency and Gain of the resonant circuit using the transformer and resonant capacitor specified above. It can be confirmed that the gain Mg_nom_{max} = 1.06 required at 110% load and the gain Mg_hold_{max} = 1.14 required at 100% load are secured.

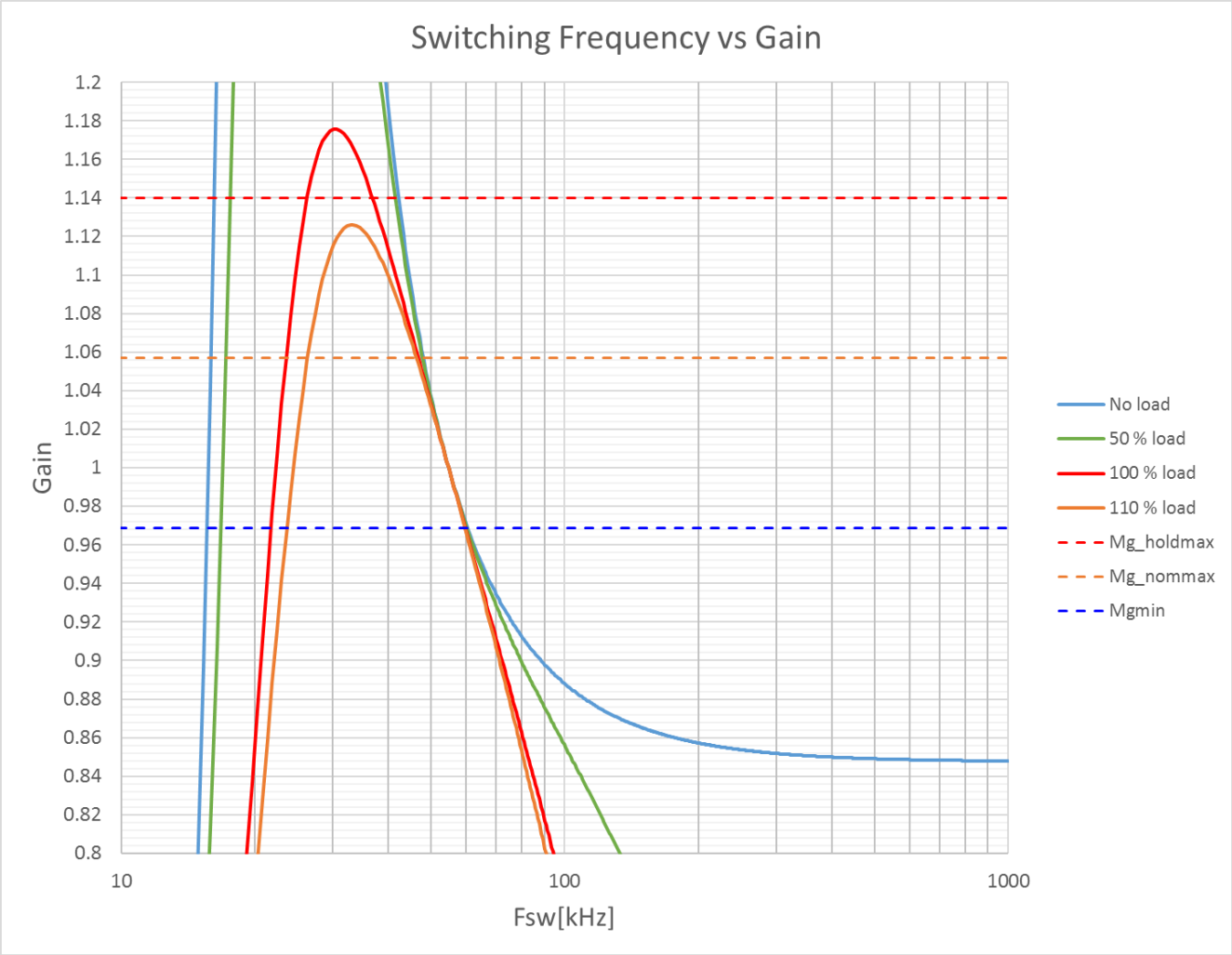

Fig. 2.16 Gain vs Switching Frequency

Checking the current value

Assuming that sinusoidal current flows through the secondary winding, determine the effective current flowing through the secondary winding. This time the transformer is at the center

Because of the tapped method, if the maximum load current is $Iout\_LLC_{max}$, the effective current Is_rms flowing through each wire of the secondary winding and the load current Ip_l flowing through the primary winding are respectively as follows.

$$Is\_rms = \frac{\pi \times Iout\_LLC_{max}}{2\sqrt{2}}$$

$$Ip\_l = \frac{\pi \times Iout\_LLC_{max}}{2\sqrt{2} \times n}$$

Since 41. 7 A is the $Iout\_LLC_{max}$, Is_rms is 46.3 A and Ip_l is 2.81 A. Excitation current Ip_m flowing in the primary winding is as follows.

$$Ip\_m = \frac{2\sqrt{2} \times n \times Vout\_LLC}{2\pi \times fsw \times Lm}$$

When the switching frequency is 37.2 kHz, the minimum value, the excitation current Ip_m becomes maximum value. Since Vout_LLC is 12 V and Lm is 500 μH, Ip_m is 1.53 A.

The total current Ip of the primary winding is 3.19 A as follows.

$$Ip = \sqrt{Ip\_l^2 + Ip\_m^2}$$

・ Checking Zero Volt Switching

The LLC power supply performs Zero Volt Switching (ZVS) by charging and discharging the output capacitance of the switching MOSFET with energy stored by the excitation current of the transformer, thereby achieving high-efficiency. To achieve ZVS in a wide range of load conditions, the ZVS condition must be satisfied even when the excitation current Ip_m is minimum. ZVS is established when the energy stored by the excitation current of the transformer exceeds the energy required to charge and discharge the output capacitance of MOSFET. The excitation current Ip_m is minimized when the switching frequency fsw is the largest value, 61. 8 kHz, and since Vout_LLC is 12 V, Lm is 500 μH, and Ip_m is 0.92 A. At this time, the energy stored in the transformer on the primary side is calculated as follows.

$$\frac{1}{2}(Lm + Lr) \times \{0.92(A)\}^2 = 249\mu J$$

ZVS can be realized if the output capacitance of the switching MOSFET can be charged and discharged with this energy. Since the effective capacitance of the switching MOSFET TK20A60W5 is 70 pF, the energy required for charging and discharging is calculated as follows.

$$\frac{1}{2}(2pcs \times 70pF) \times Vout\_PFC_{max}{}^2 = 11.3\mu J$$

From the above, the energy (249 μJ) stored in the transformer on the primary side is required to charge and discharge the output capacitance of MOSFET.

It can be seen that the condition of ZVS is satisfied even at the minimum excitation current condition because the stored energy, 249 μJ , is higher than the energy required for charging and discharging to the MOSFET, 11.3 μJ.

Soft-start setting

Fig. 2.17 shows the soft-start setting circuit. The soft-start time of the LLC power supply is set with an external capacitor (C34). The soft start time varies depending on the load conditions, but the maximum soft start time (Tss) can be calculated as follows.

$$Tss = \frac{7V \times C34}{25.8\mu A}$$

For this power supply, the maximum soft start time (Tss) is set to 56.7 ms, and 220 nF is selected for the external capacitor (C34). Adjust the soft start time by changing the capacity as necessary.

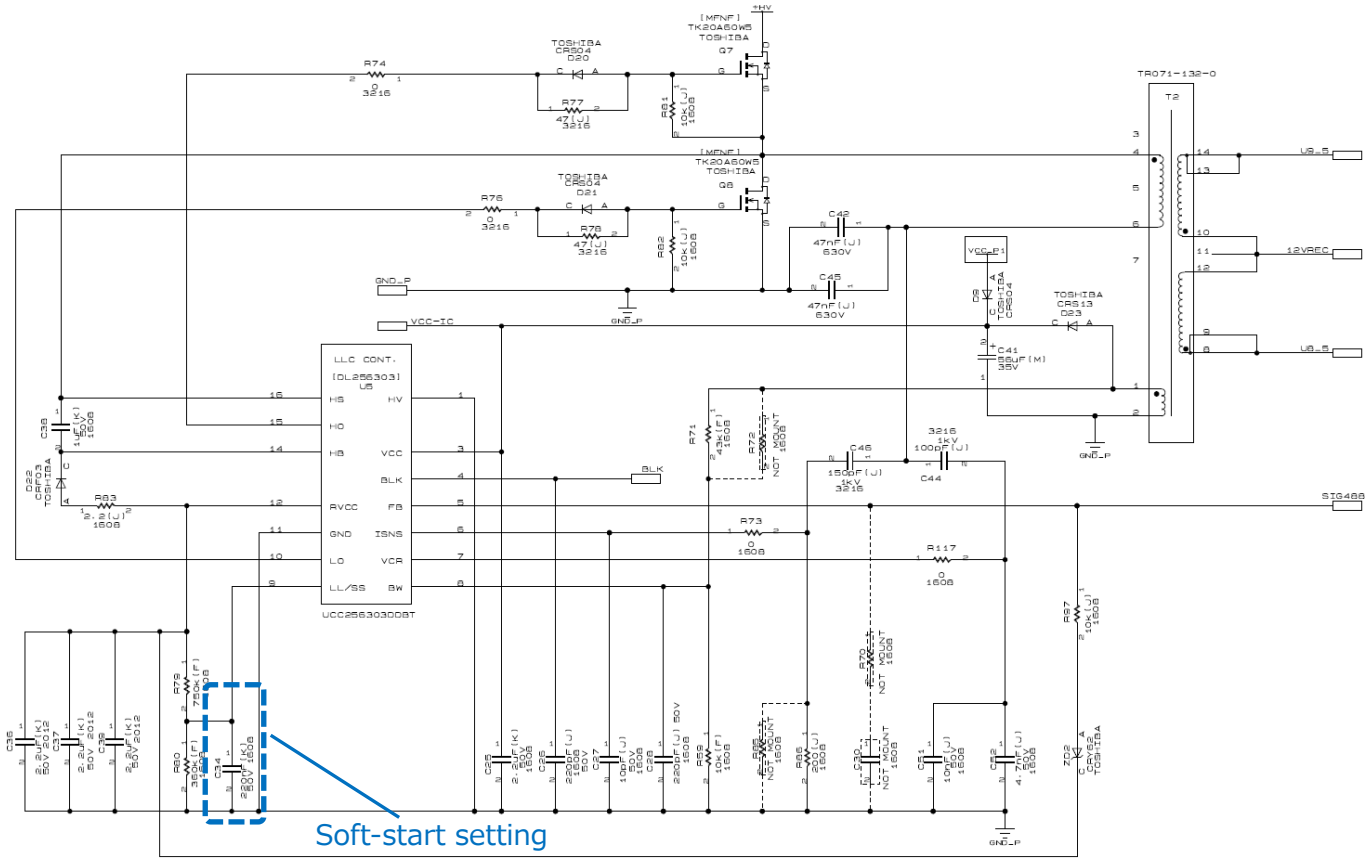

Fig. 2.17 Soft-Start Setting Circuit

Current limiter

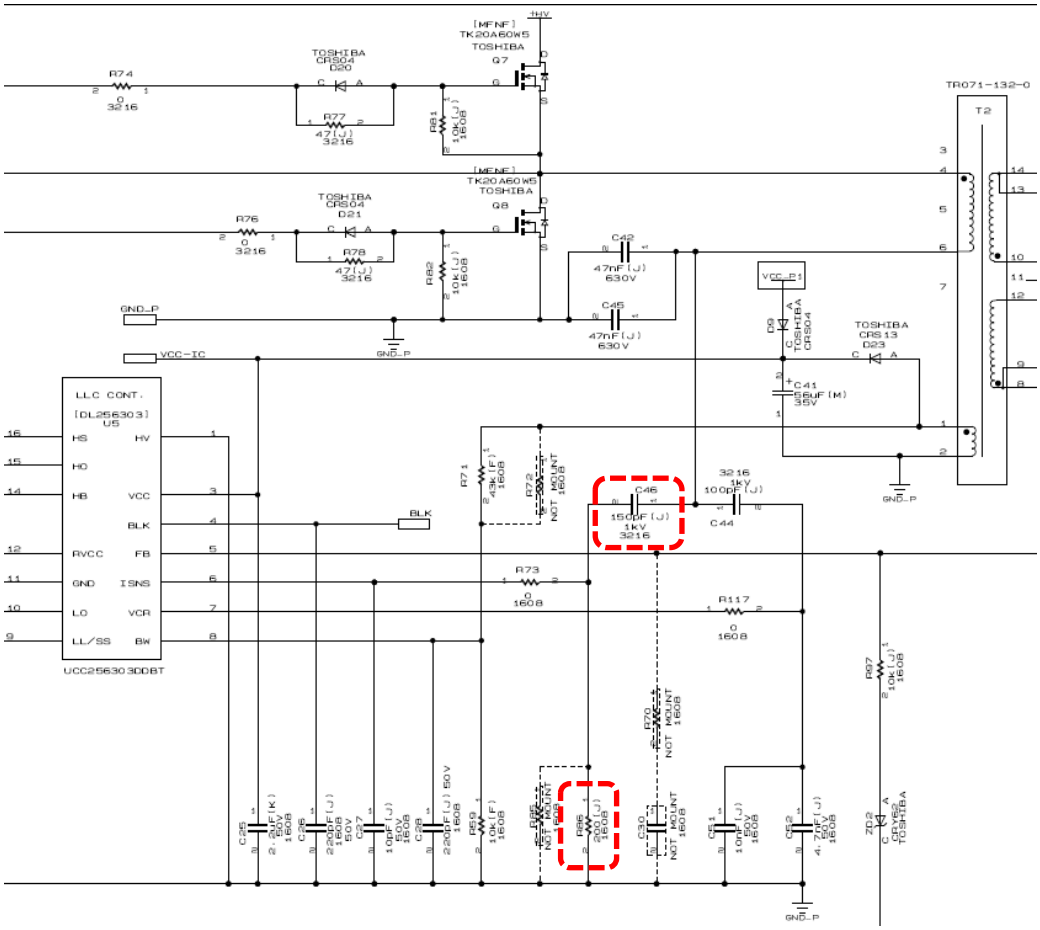

Fig. 2.18 Current Limiter

Fig. 2.18 shows the current limiter circuit. Set the current limiter level of the LLC with resistor (R86) and capacitance (C46). The LLC controller has a three-level current limiter (OCP1~OCP3). When the output load of the LLC power supply is increased, ISNS pin voltage rises, and the overcurrent limiter is activated when ISNSN pin voltage exceeds the threshold (OCP1~OCP3) for the specified duration. This power supply sets the load current at which OCP3 is activated to 150% of the maximum load ($Iout\_LLC_{max}$). At this time, the conditions for the current limiter to be activated (ISNS pin voltage threshold and duration) and the input current and output current at that time are shown in the tables below.

	OCP1	OCP2	OCP3
ISNS pin voltage thresholds	4.03 V (peak)	0.84 V (average)	0.64 V (average)
Duration	4 consecutive cycles	2 ms continuous	50 ms continuous
Input current	12.9 A (peak)	2.69 A (average)	2.05 A (average)
Output current	213 A (peak)	82.3 A (average)	62.7 A (average)

At this time, ISNS pin voltage at the maximum load, $VISNS\_Ioout\_LLC_{max}$, is calculated by the following equation.

$$VISNS\_Iout\_LLC_{max} = \frac{0.64V}{150\%} = 0.43V$$

The current sensing ratio K_{ISNS} is calculated as follows:

$$K_{ISNS} = \frac{VISNS\_Iout\_LLC_{max}}{\frac{Pout}{\eta 2} \times \frac{1}{PFC\_out}} = 0.31\Omega$$

Assuming that the capacitance value C46 is 150 pF and the capacitance value of the resonant capacitor Cr is 94 nF, R86 is calculated as follows.

$$R86 = \frac{K_{ISNS} \times Cr}{C46} = 195.9\Omega$$

Use 200 Ω as R86 here. The operating level of the current limiter must be checked on an actual device because it has an effect on the layout.

Gate drive circuit

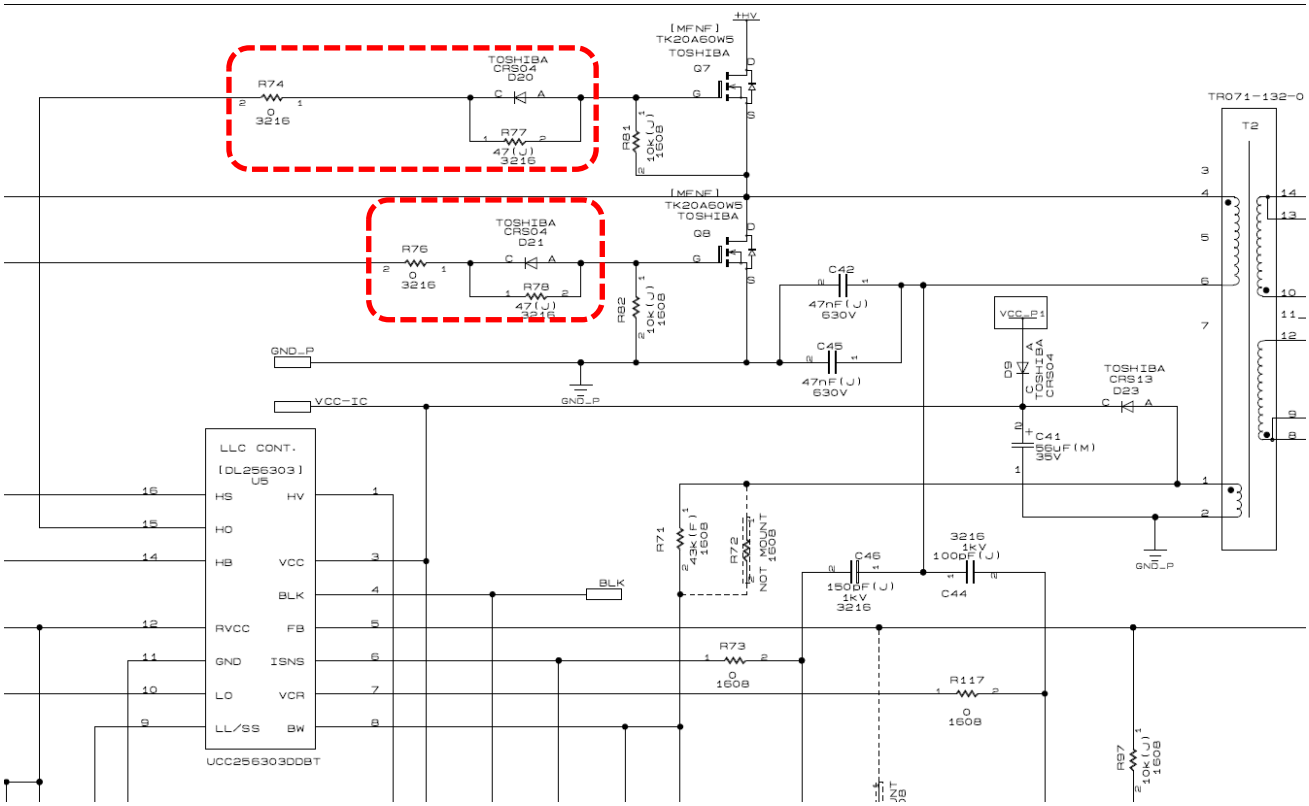

Fig. 2.19 Gate Drive Circuit

Fig. 2.19 shows the gate drive circuit. The design of the gate drive circuit affects power supply efficiency and EMI. Generally, there is a trade-off between power supply efficiency and EMI, and a balanced design is required for both. The LLC circuitry is low EMI due to ZVS operation, but if switching noise seems to be the source of EMI issues, adjust the value of the gate series resistors (R74, R76-R78) and check it. The gate drive circuit allows individual adjustments of MOSFET turn-on and turn-off speeds. If EMIs (noises) occur at both turn-on and turn-off of MOSFET (Q7),

increase the resistor R74. This allows you to reduce turn-on and turn-off speeds at the same time, and reduce EMIs (noises). If EMI (noise) is occurring when MOSFET turns on, increase the value of R77. This reduces the turn-on speed only and reduces EMI (noise). If you want to reduce the EMI (noise) generated by switching MOSFET (Q8), adjust resistors R76 and R78 in the same way as in the case of Q7.

Note that increasing the resistors (R74, R76-R78) may reduce the switching speed of MOSFET, which may also reduce the power-supply efficiency. Check that the power supply efficiency specification and heat dissipation specification satisfy the required specification.

Output capacitor

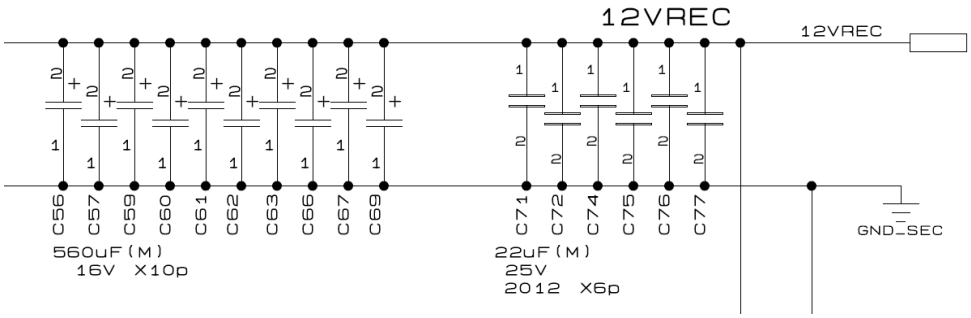

Fig. 2.20 Output Capacitor Circuit

Fig. 2.20 shows the peripheral circuits of the output capacitors. Set C_{out} of the output capacitance to meet the requirements of the output voltage ripple (V_{ripple}) and the requirements of the ripple current. The resulting combined ripple voltage is the output voltage ripple (V_{ripple}). If the output voltage ripple (V_{ripple}) is 120 mV and the maximum load is I_{max}, the ESR required for the output capacitors is calculated as follows:

$$ESR = \frac{V_{ripple}}{\frac{2 \times \pi}{4} \times I_{max}} = 1.8m\Omega$$

I_{max} is 41.7 A, so the ESR is 1.8 mΩ.

The effective I_{C_rms} of the ripple current flowing through the capacitors is calculated by the following equation.

$$I_{C\_rms} = \sqrt{\left(\frac{\pi}{2\sqrt{2}} I_{out}\right)^2 - {I_{out}}^2} = 20.2A$$

Output capacitors and quantity must be selected so that the above ESR and I_{C_rms} meet the specifications. In this power supply, ten capacitors (C56, C57, C59-C63, C66, C67, and C69) with an output capacitance of 560 μF, an ESR of 8 mΩ, and an allowable ripple current of 4.2 A (rated ripple current of 6.1 A at 100 kHz, and a frequency-correction factor of 10kHz≦f<100kHz of 0.7) are arranged in parallel. This results in a total ESR of 8 mΩ/10 = 0.8 mΩ, indicating that the above requirements are met. The ripple current per unit is also 20.2 A/10 = 2.02 A, which indicates that the specifications are satisfied.

Also make surek the following:

1. The undershoot and overshoot voltages of output terminal that occur when the load changes suddenly is within the specified voltage range.
2. The allowable ripple current of the output capacitor is ensured.
3. Consider tolerances and aging of output capacitors.

Synchronous rectifier MOSFET surge-voltage reduction circuit

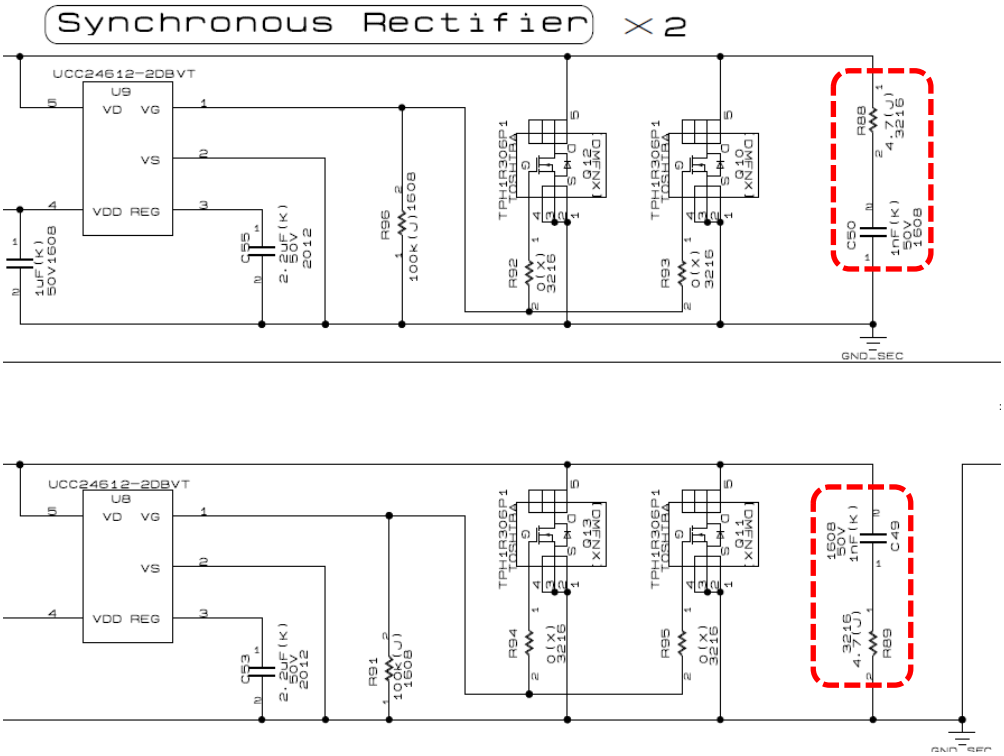

Fig. 2.21 Snubber Circuit

Fig. 2.21 shows snubber circuit. Snubber circuit consists of R89, C49, R88 and C50. Snubber circuit absorbs surge-voltage (V_{srg}) generated in Q10-Q13. At this time, the loss P_{d_Rsnb} generated by the resistors R89 and C49 are as follows.

$$P_{d\_Rsnb} = C49 \times (V_{srg})^2 \times \left(\frac{f_{PWM}}{2}\right)$$

When the surge voltage (V_{srg}) is 35 V, C49 is 1000 pF, and f_{PWM} is 61. 8 kHz, the loss P_{d_Rsnb} generated by the resistor R89 is 38 mW. Adjust the constants and ratings of each element according to the actual surge voltage level.

Terms of Use

This terms of use is made between Toshiba Electronic Devices and Storage Corporation (“We”) and customers who use documents and data that are consulted to design electronics applications on which our semiconductor devices are mounted (“this Reference Design”). Customers shall comply with this terms of use. Please note that it is assumed that customers agree to any and all this terms of use if customers download this Reference Design. We may, at its sole and exclusive discretion, change, alter, modify, add, and/or remove any part of this terms of use at any time without any prior notice. We may terminate this terms of use at any time and for any reason. Upon termination of this terms of use, customers shall destroy this Reference Design. In the event of any breach thereof by customers, customers shall destroy this Reference Design, and furnish us a written confirmation to prove such destruction.

1. Restrictions on usage

1. This Reference Design is provided solely as reference data for designing electronics applications. Customers shall not use this Reference Design for any other purpose, including without limitation, verification of reliability.
2. This Reference Design is for customer's own use and not for sale, lease or other transfer.
3. Customers shall not use this Reference Design for evaluation in high or low temperature, high humidity, or high electromagnetic environments.
4. This Reference Design shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable laws or regulations.

2. Limitations

1. We reserve the right to make changes to this Reference Design without notice.
2. This Reference Design should be treated as a reference only. We are not responsible for any incorrect or incomplete data and information.
3. Semiconductor devices can malfunction or fail. When designing electronics applications by referring to this Reference Design, customers are responsible for complying with safety standards and for providing adequate designs and safeguards for their hardware, software and systems which minimize risk and avoid situations in which a malfunction or failure of semiconductor devices could cause loss of human life, bodily injury or damage to property, including data loss or corruption. Customers must also refer to and comply with the latest versions of all relevant our information, including without limitation, specifications, data sheets and application notes for semiconductor devices, as well as the precautions and conditions set forth in the "Semiconductor Reliability Handbook".
4. When designing electronics applications by referring to this Reference Design, customers must evaluate the whole system adequately. Customers are solely responsible for all aspects of their own product design or applications. WE ASSUME NO LIABILITY FOR CUSTOMERS' PRODUCT DESIGN OR APPLICATIONS.
5. No responsibility is assumed by us for any infringement of patents or any other intellectual property rights of third parties that may result from the use of this Reference Design. No license to any intellectual property right is granted by this terms of use, whether express or implied, by estoppel or otherwise.
6. THIS REFERENCE DESIGN IS PROVIDED "AS IS". WE (a) ASSUME NO LIABILITY WHATSOEVER, INCLUDING WITHOUT LIMITATION, INDIRECT, CONSEQUENTIAL, SPECIAL, OR INCIDENTAL DAMAGES OR LOSS, INCLUDING WITHOUT LIMITATION, LOSS OF PROFITS, LOSS OF OPPORTUNITIES, BUSINESS INTERRUPTION AND LOSS OF DATA, AND (b) DISCLAIM ANY AND ALL EXPRESS OR IMPLIED WARRANTIES AND CONDITIONS RELATED TO THIS REFERENCE DESIGN, INCLUDING WARRANTIES OR CONDITIONS OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, ACCURACY OF INFORMATION, OR NONINFRINGEMENT.

3. Export Control

Customers shall not use or otherwise make available this Reference Design for any military purposes, including without limitation, for the design, development, use, stockpiling or manufacturing of nuclear, chemical, or biological weapons or missile technology products (mass destruction weapons). This Reference Design may be controlled under the applicable export laws and regulations including, without limitation, the Japanese Foreign Exchange and Foreign Trade Law and the U.S. Export Administration Regulations. Export and re-export of this Reference Design are strictly prohibited except in compliance with all applicable export laws and regulations.

4. Governing Laws

This terms of use shall be governed and construed by laws of Japan.