5 kW Isolated Bidirectional DC-DC Converter

Design Guide

RD167-DGUIDE-02

TOSHIBA ELECTRONIC DEVICES & STORAGE CORPORATION

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1. Introduction

This design guide describes how to design various circuitry for a 5 kW Isolated Bidirectional DC-DC Converter (hereafter referred to as this power supply). Refer to the reference guide for the specifications, usage, and characteristic data of this power supply.

Even if the part number is indicated in the circuit diagram, it is not mounted on PCBs if it is indicated as "Not Mounted" in the bill of materials. A mounting location is provided on the PCB for constant value adjustment at the time of circuit design.

1.1. Onboard Power MOSFET

This power supply adopts 1200 V withstanding SiC MOSFET (TW070J120B) for the high-voltage side bridge and 650 V withstanding MOSFET (TK49N65W5) for the low-voltage side bridge as switching elements.

TW070J120B

Mounted on the high-voltage side bridge.

V_{DSS} = 1200 V, $R_{DS(ON)}$@V_{GS} = 20 V (typ.) = 70 mΩ, TO-3P(N) package

Built-in SiC Schottky barrier diode reduces loss when reverse current is applied.

TK49N65W5

Mounted on the low-voltage side bridge.

V_{DSS} = 650 V, $R_{DS(ON)}$@V_{GS} = 10 V (typ.) = 51 mΩ, TO-247 package

High-speed built-in diode product reduces loss during reverse recovery operation.

2. Circuit Design

This section describes the points of circuit design of this power supply.

2.1. High-Voltage Side Circuit Design

This section describes the design of the high-voltage side circuit of this power supply.

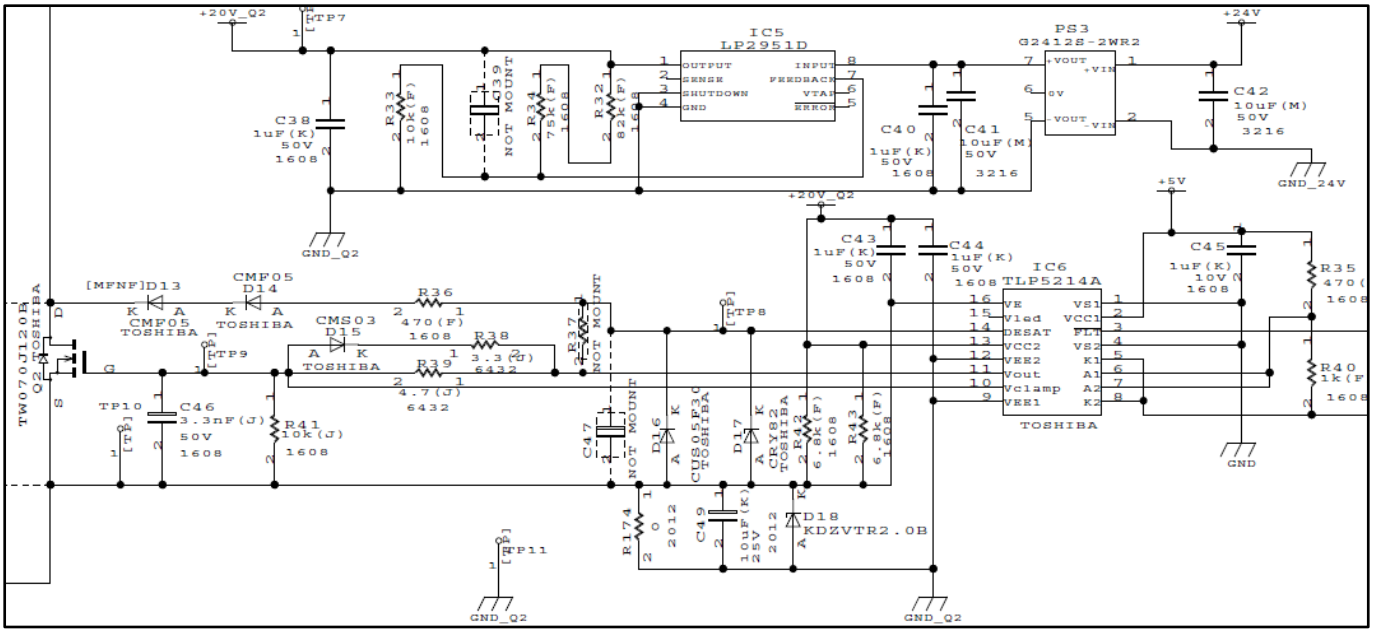

Fig. 2.1 Gate Drive Circuit (High-Voltage Side Lower Arm)

Gate Drive Circuit

One of the gate drive circuit of high-voltage side is described here. The gate drive circuit of the lower arm side MOSFET Q2 is shown in Fig. 2.1. The design of the gate drive circuit affects power supply efficiency and EMI noise. Generally, power supply efficiency and EMI noise have a trade-off relationship, so it is necessary to design both in a balanced manner. The gate-drive circuit of this power supply has a circuit configuration that can adjust the switching speed of MOSFET. If it is necessary to reduce the noise at turn-on of MOSFET, changing the gate series resistor (R39) to a large value may reduce EMI noise. Note that if the gate-series resistor is changed to a large value, not only the turn-on speed of MOSFET but also the turn-off speed will be reduced, which may result in worsening of the power supply efficiency. In this situation, in order to reduce power-efficiency degradation only the turn-off speed of MOSFET should be increased. Changing the gate-series resistor (R38) to a small value may only increase the turn-off speed of MOSFET and reduce the power-efficiency degradation of the system. When changing the gate series resistance, it is necessary to confirm that the EMI noise, power efficiency performance, and heat dissipation performance required for the system are satisfied.

Negative Bias Circuit

Negative-bias circuit is used if there is a risk of malfunction due to the parasitic mirror capacitance between the drain-gate of MOSFET. Fig. 2.1 shows the gate drive circuit used on the lower arm side. When the lower arm is turned off and the upper arm is turned on, the intermediate potential rises steeply and displacement current is generated through the mirror capacitance between the drain and gate of the lower arm, and flows toward VOUT terminal of the smart gate driver coupler (IC6). When this displacement current passes through the gate resistor of the circuit, a voltage drop occurs, and when the gate voltage rises, the lower arm may be erroneously turned on, resulting in a short circuit of the upper and lower arms. Such erroneous on occurrence was not confirmed with this power supply. However, measures must be taken when erroneous ON occurs due to the board layout or wiring in actual applications.

Generally, as a countermeasure against erroneous ON, it is effective to bias the voltage during gate-off to a negative voltage. Although this power supply does not bias the gate to a negative voltage, a negative bias circuit using a zener diode (D18) can be easily realized. By removing the 0 Ω resistor (R174) placed in parallel with the D18 and placing a capacitor of about 1 μF, a negative bias equivalent to the zener voltage is applied to the gate during gate-off. Although a 2 V zener diode is used for this power supply, select an appropriate element according to the actual operation.

Output Capacitor

When the power supply is operating with high-voltage side as power supply output, the capacitance value of the output capacitors (C62 to C69) is calculated based on the hold-up time requirement. The hold-up time $Thold_{high}$ is calculated by the following equation, where the combined capacitance of the output capacitors is $Cout_{high}$, the output voltage is $Vout_{high}$, the lower voltage of the output voltage is $Vout_{high\_min}$, and the maximum output power is Pout.

$$Thold_{high} = Cout_{high} \times \frac{(Vout_{high^2} - Vout_{high\_min^2})}{2 \times Pout}$$

The initial setting is $Cout_{high}$ = 705 μF (3 parallel of (2 serial 470 μF)), $Vout_{high}$ = 750 V, $Vout_{high\_min}$ = 700 V, Pout = 5 kW, and the hold-up time is 5.11 ms. Adjust the capacitance of the output capacitor to satisfy the hold-up time required for the system in practical applications. In addition, when the output ripple specification is defined, the capacitance required to satisfy the output ripple specification must be calculated and compared with the capacitance that satisfies the hold-up time, and the larger capacitance value must be used. In addition, tolerances and aging degradation must be considered when selecting a capacitor.

2.2. Selection of Transformer and Inductors

Transformer Selection

Set the ratio n = n1/n2 of high-voltage side winding n1 and low-voltage side winding n2 to be equal to the ratio of high-voltage side voltage 750 V and low-voltage side voltage 400 V (750/400 = 1.875). For this power supply, a transformer with n1/n2 = 28/15 (= 1.87) was selected.

Inductor Selection

This section explains how to select inductors (L11 and L12). Although the maximum output power of this power supply is 5 kW, an inductor capable of outputting up to 15 kW was adopted for expandability. Since the inductor is located on the low-voltage side, the approximate number of required inductance values (L) can be calculated using the following items, assuming that the low-voltage side is the input (V_{in}) and the high-voltage side is the output (V_{out}).

- Input voltage: V_{in} (V)
- Output Voltage: V_{out} (V)
- Output Power: P_{out} (W)
- Winding ratio: n
- Switching frequency: F_c (Hz)
- Phase difference between input and output sides (overlap angle): θ (degree)

The current I_L applied to the indictor is expressed by the following equation.

$$I_L = \frac{2 \times P_{out}}{V_{out}}$$

Assuming that P_{out} is 15 kW and V_{out} is 750 V, I_L is 40 A.

The inductance value L for outputting this I_L = 40 A when the phase difference θ is calculated by the following equation.

$$L = \left(V_{in} + V_{out} \times \frac{1}{n}\right) \times \frac{\theta}{180} \times \frac{1}{F_c \times 2} \times \frac{1}{4I_L}$$

Here, assuming that F_c is 50 kHz and θ is 25 degrees for controllability, the above inductance value L is calculated as 6.96 μH, so an inductor of 6 μH is selected for this power supply.

In the actual design, the inductance value of the inductor varies depending on the DC superimposition characteristics. Select a component that can secure the above calculated value while the inductance value is decreased due to DC superimposition characteristics.

2.3. Low-Voltage Side Circuit Design

This section describes the design of the low-voltage side circuit of this power supply.

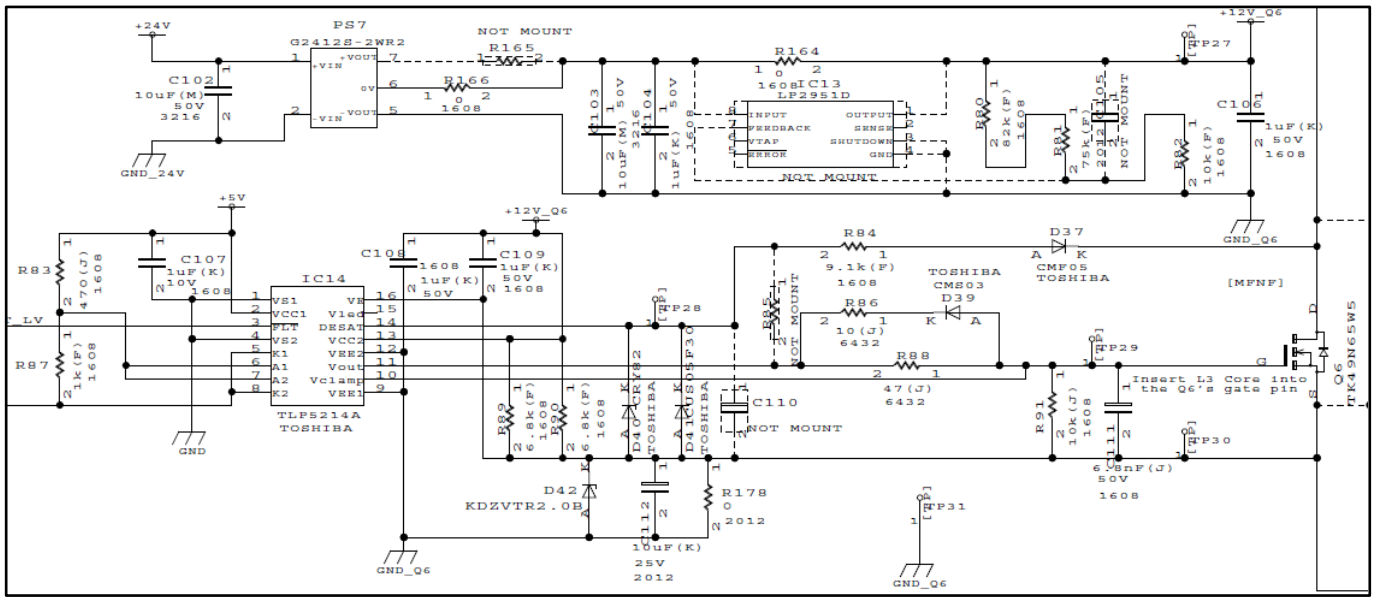

Fig. 2.2 Gate Drive Circuit (Low-Voltage Side Lower Arm)

Gate Drive Circuit

One of the gate drive circuit of Low-voltage side is described here. The gate drive circuit of the lower arm side MOSFET Q6 is shown in Fig. 2.2. The design of the gate drive circuit affects power supply efficiency and EMI noise. Generally, power supply efficiency and EMI noise have a trade-off relationship, so it is necessary to design both in a balanced manner. The gate-drive circuit of this power supply has a circuit configuration that can adjust the switching speed of MOSFET. If it is necessary to reduce the noise at turn-on of MOSFET, changing the gate series resistor (R88) to a large value may reduce EMI noise. Note that if the gate-series resistor is changed to a large value, not only the turn-on speed of MOSFET but also the turn-off speed will be reduced, which may result in worsening of the power supply efficiency. In this situation, in order to reduce power-efficiency degradation only MOSFET turn-off speed should be increased. Changing the gate-series resistor (R86) to a small value may only increase the turn-off speed of MOSFET and reduce the power-efficiency degradation of the system. When changing the gate series resistance, it is necessary to confirm that the EMI noise, power efficiency performance, and heat dissipation performance required for the system are satisfied.

Negative Bias Circuit

Use a negative-bias circuit if there is a risk of malfunction due to the parasitic mirror capacitance between the drain-gate of MOSFET. Fig. 2.2 shows the gate drive circuit used on the lower arm side. When the lower arm is turned off and the upper arm is turned on, the intermediate potential rises steeply and displacement current is generated through the mirror capacitance between the drain and gate of the lower arm, and flows toward VOUT terminal of the smart gate driver coupler

(IC14). When this displacement current passes through the gate resistor of the circuit, a voltage drop occurs, and when the gate voltage rises, the lower arm may be erroneously turned on, resulting in a short circuit of the upper and lower arms. This power supply did not confirm such erroneous ON. However, measures must be taken when erroneous ON occurs due to the board layout and wiring in actual applications.

Generally, as a countermeasure against erroneous ON, it is effective to bias the voltage at gate-off to the negative voltage. Although this power supply does not bias the gate to a negative voltage, a negative bias circuit using a zener diode (D42) is easily realized. By removing the 0 Ω resistor (R178) placed in parallel with the D42 and placing a capacitor of about 1μF, a negative bias equivalent to the zener voltage is applied to the gate during gate-off. Although a 2 V zener diode is used for this power supply, select an appropriate element according to the actual operation.

Output Capacitor

When the power supply is operating with low-voltage side as power supply output, the capacitance value of the output capacitors (C146 to C152) is calculated based on the hold-up time requirement. The hold-up time $Thold_{low}$ is calculated by the following equation, where the combined capacitance of the output capacitors is $Cout_{low}$, the output voltage is $Vout_{low}$, the lower voltage of the output voltage is $Vout_{low\_min}$, and the maximum output power is Pout.

$$Thold_{low} = Cout_{low} \times \frac{(Vout_{low^2} - Vout_{low\_min^2})}{2 \times Pout}$$

The initial setting is $Cout_{low}$ = 2820 μF (6 parallel of 470 μF), $Vout_{low}$ = 400 V, $Vout_{low\_min}$ = 370 V, Pout = 5 kW, and the hold-up time is 6.51 ms. Adjust the capacitance of the output capacitor to satisfy the hold-up time required for the system in practical applications. In addition, when the output ripple specification is defined, the capacitance required to satisfy the output ripple specification must be calculated and compared with the capacitance that satisfies the hold-up time, and the larger capacitance value must be used. In addition, tolerances and aging degradation must be considered when selecting a capacitor.

This power supply uses Texas Instruments's TMS320F28377SPTP as a PWM controller and uses a software library manufactured by Headspring to create control software. For more information about controllers and software libraries, please refer to the manufacturer's product data sheet and related documents. Please refer to "Sample Software" for the software used with this power supply and its outline.

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