500 W Server Power Supply using TOLL Package DTMOS

Design Guide

RD169-DGUIDE-01

TOSHIBA ELECTRONIC DEVICES & STORAGE CORPORATION

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1. Introduction

This Design Guide describes how to design various circuits and layouts of the 500 W Server Power Supply using TOLL package DTMOS (hereafter referred to as "this power supply"). Refer to the reference guide for the specifications, usage, and characteristic data of this power supply.

If a component is indicated as "Not Mounted" in the bill of materials, then it is not mounted on the PCB even if its part number is indicated in the circuit diagram. A mounting location is provided on the PCB for constant value adjustment at the time of circuit design.

1.1. Onboard Power MOSFET

We have commercialized the 600/650 V DTMOS series, which is suitable for the primary side (PFC/main switch) of AC-DC converters, and the low-voltage U-MOS series, which is suitable for the secondary side (synchronous rectifier and ORing). Both series offer an extensive lineup, allowing the designer to select the most suitable product according to the design specifications. The following is an introduction to the products used in this power supply.

TK090U65Z

Mounted on PFC circuit.

V_{DSS} = 650 V, $R_{DS(ON)}$ (Max) = 90 mΩ@V_{GS} = 10 V, TOLL package.

Modern DTMOSVI process product capable of high-speed switching and reduced switching loss.

TK20A60W5

Mounted on the primary side of LLC circuit.

V_{DSS} = 600 V, $R_{DS(ON)}$ (Max) = 175 mΩ@V_{GS} = 10 V, TO-220SIS package.

Product with built-in high-speed diode and reduced loss during reverse recovery operation.

TPH1R306P1

Mounted on the secondary-side synchronous rectifier of LLC circuit.

V_{DSS} = 60 V, $R_{DS(ON)}$ (Max) = 1.28 mΩ@V_{GS} = 10 V, SOP Advance package.

U-MOSIX-H process products suitable for switching applications, as it suppresses surge voltage during switching by optimizing the cell structure.

TPHR9203PL

Mounted on ORing circuitry of the output unit.

V_{DSS} = 30 V, $R_{DS(ON)}$ (Max) = 0.92 mΩ@V_{GS} = 10 V, SOP Advance package.

Modern U-MOSIX-H process products with low on-resistance reduces power dissipation in ORing circuitry.

2. Circuit Design

This section describes the points of circuit design of this power supply.

2.1. AC Line Circuit Design

Fig. 2.1 shows the AC line circuit and explains the basic design method.

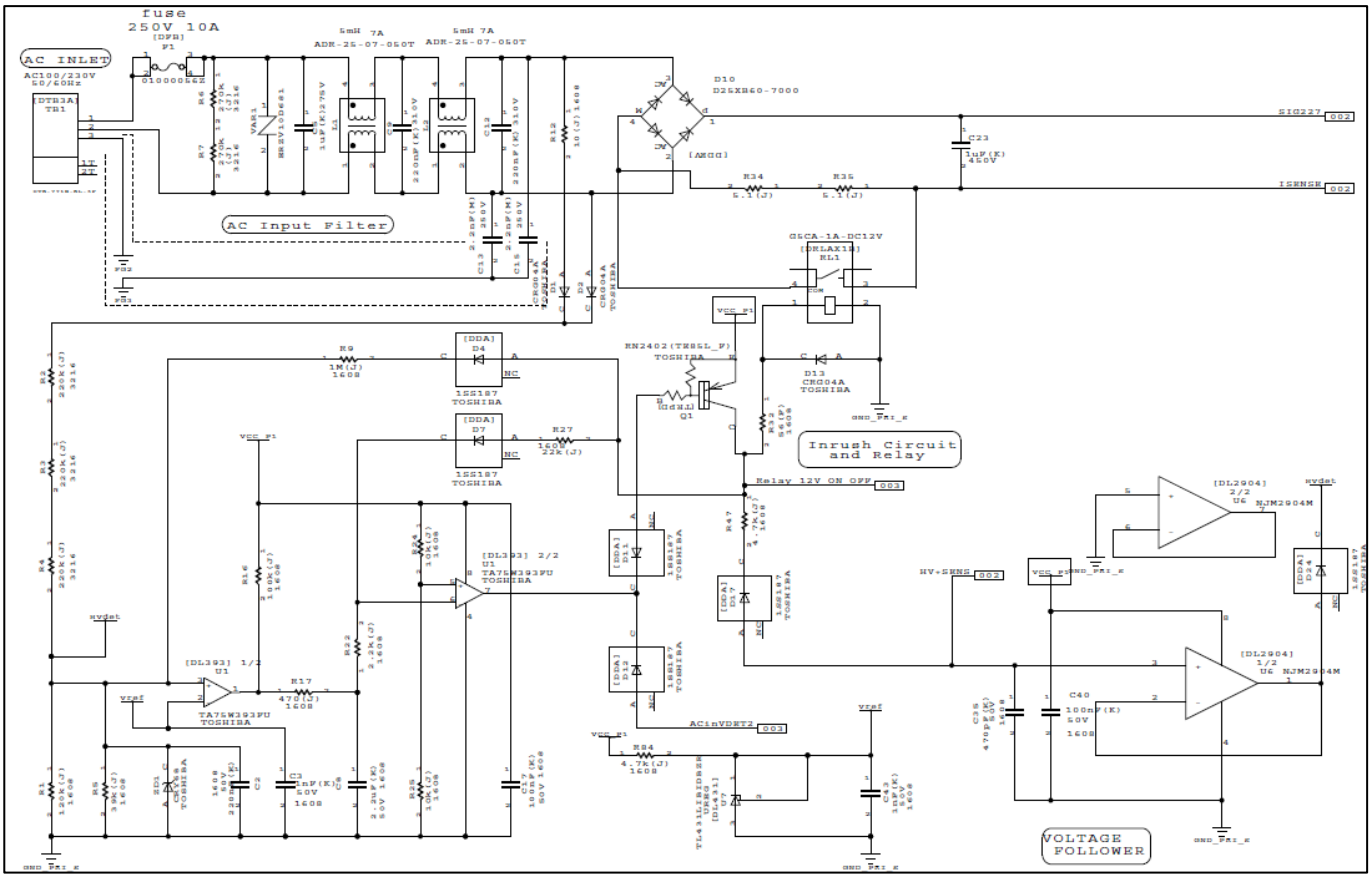

Fig. 2.1 AC Line Circuit

Fuse

A fuse (F1) is used to cut off the AC line when an excessive current flows through the AC line. Select a fuse using the maximum current rms value $ACin_{peakrms}$ of the AC line. Using the maximum power Pout, PFC power supply efficiency η1, LLC power supply efficiency η2, power factor PF, and AC line voltage rms value $VinAC_{min}$, the maximum current rms value $ACin_{peakrms}$ of the AC line can be calculated using the following equation.

$$ACin_{peakrms} = \frac{Pout}{\eta 1 \times \eta 2 \times PF \times VinAC_{min}}$$

The output specification of this power supply is 500 W. Since the power supply efficiency of the PFC decreases when the AC line voltage is low, the AC line current rms value (max) is calculated by setting the AC line voltage rms value (min) to 90 V, which is the minimum value of the 100 V system.

Assuming that the input voltage (min rms value) = 90 V, the maximum power = 500 W, the PFC power supply efficiency (η1) = 94 %, the LLC power supply efficiency (η2) = 94 %, and the power factor = 0.99, the maximum AC line current value of this power supply is approximately 6.4 A. Therefore, a 10 A fuse is used with margins added. When selecting a fuse, in addition to the above maximum current it is necessary to consider the inrush current that flows when the AC power is turned on, and whether the fuse is in accordance with the safety standards to be supported.

Varistor

A metal oxide varistor (VAR1) is used to protect the circuitry when surge voltages due to inductive lightning, etc., occurs on the AC line. Select a varistor using the voltage value of the AC line. Since the maximum AC line voltage of this power supply is 264 V for the rms value and 373 V for the instantaneous value, and after adding margin the maximum allowable circuit voltage of becomes 420 V (AC rms value), therefore a varistor with varistor voltage of 680 V is used.

Select the product considering not only the maximum allowable circuit voltage and varistor voltage, but also the surge current withstand capacity and energy withstand capacity. In addition, since the varistor failure mode has many short modes, insert a fuse to the front stage (input side of the AC line) of the varistor.

X Capacitor Discharge Resistance

X capacitor Cx (C5, C9, C12) Use resistor Rdis (R6, R7) for discharging. Set the resistance value to meet the safety standards. For example, if the safety standard that the system should comply with requires that the safety voltage (Vsafe) be less than or equal to t seconds after the AC plug is unplugged, to meet the standard even if the AC plug is unplugged at the peak AC line voltage, set the discharge resistance value that satisfies the following equation.

$$Rdis \leq \frac{t}{Cx \times ln\left(\frac{VinAC \times \sqrt{2}}{Vsafe}\right)}$$

When t is set to 2 seconds and Vsafe is set to 60 V, Rdis is 759 kΩ or less when Cx is 1.44 μF and VinAC is the largest 264 V. Rdis is taken to be 540 kΩ (R6 and R7 are 270 kΩ) considering variations in capacitance and resistance values and design margins. In addition, the loss of resistance is as follows.

$$Rloss = \frac{VinAC^2}{Rdis}$$

The total power loss (Rloss) in the discharge-resistor Rdis is 129 mW when VinAC is up to 264 V. Reducing the resistance of the discharging resistor makes it easier to satisfy the safety standards, but care must be taken because the power loss (Rloss) of the resistor increases. If power loss due to resistance is unacceptable for the system, use an IC for X-CON discharge that connects the discharge path of the X-CON only when AC power is lost.

EMI Countermeasure Parts

Y capacitors (C13, C15) and common mode chokes (L1, L2) are used to suppress common mode noise. In addition, an X capacitor (C5, C9, C12) is used to suppress differential noise. Since each noise level is affected by the PCB layout and the enclosure structure, change, delete, or add the aforementioned components as necessary. Note that this power supply does not have a sufficient Y-capacitor because it does not have an enclosure. When designing a system with an enclosure, install a Y capacitor sufficient to prevent common mode noise. Note that when installing a Y capacitor, if the capacitance value is increased, the leakage current will increase. Therefore, confirm that safety standards are satisfied.

Inrush Current Suppressing Components

Resistors (R34, R35) and relays (RL1) are used to suppress inrush current when AC power is turned on. When the AC power is turned on, the relay (RL1) opens and AC-line current flows through the resistors (R34 and R35), thereby suppressing inrush current. After the AC power supply is turned on, when the specified conditions are satisfied, the (RL1) conducts. When the relay (RL1) conducts, the resistors (R34 and R35) that were suppressing the AC-line current are short-circuited, reducing power dissipation during operation. Resistors (R34 and R35) must be selected to withstand inrush current. Also, check that the conditions and timing for opening and continuity of the relay (RL1) satisfy the required specifications.

Bridge Diode

Bridge diode (D10) is used as rectifying diode. Match the product ratings with the inrush current value and the maximum applied voltage.

2.2. Power Factor Collection (PFC) Circuit Design

To improve the power factor, a PFC circuit using a CCM mode PFC controller UCC28180D (hereinafter referred to as the PFC controller) manufactured by Texas Instruments is used. Fig. 2.2 shows the PFC circuit 1 (around the PFC controller) and explains the basic design method. For detailed designs of the controller peripherals, refer to UCC28180D datasheets and related documents.

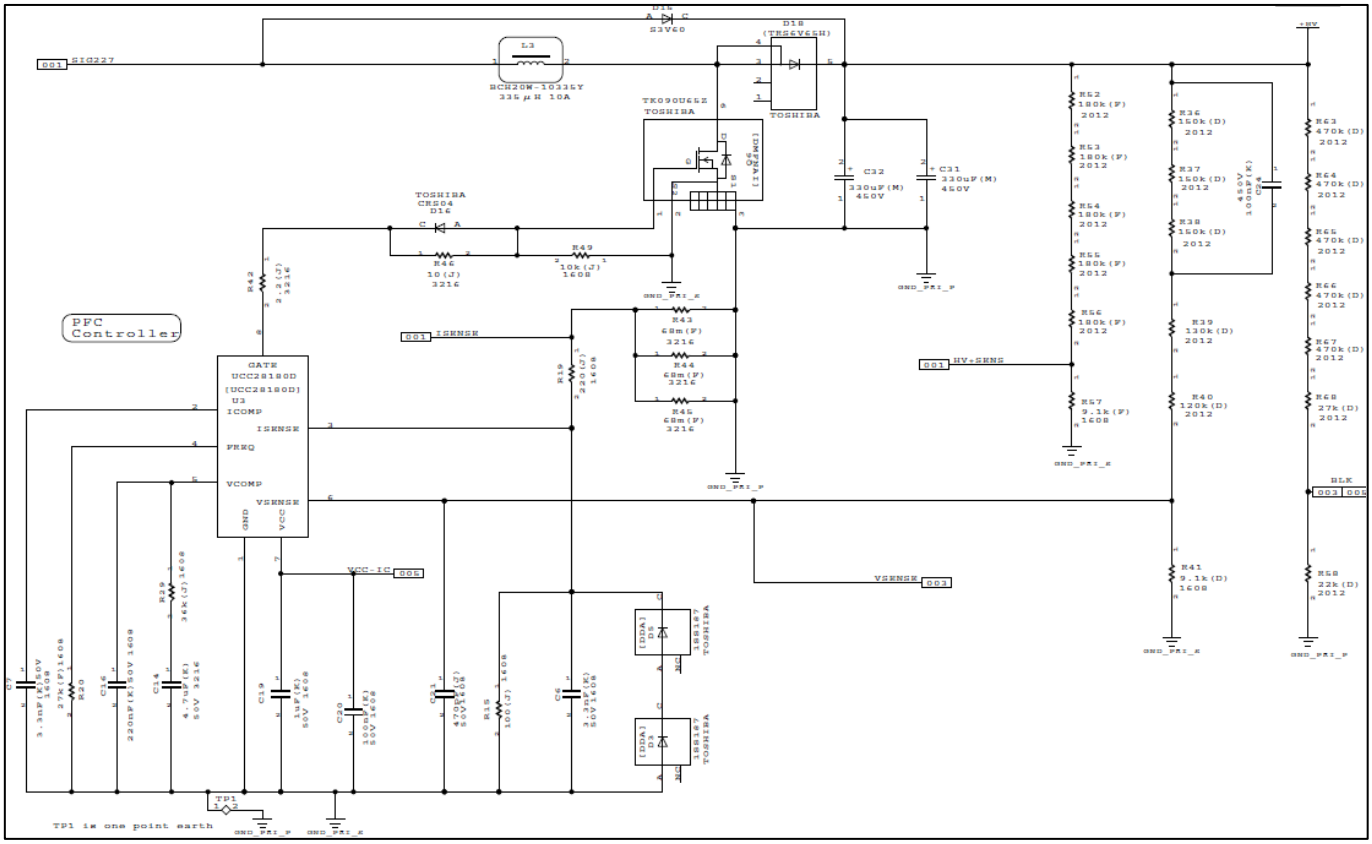

Fig. 2.2 PFC Circuit 1 (PFC Controller and Peripherals)

Output Voltage

Fig. 2.3 shows the output voltage setting circuit. Set the output-voltage (Vout_PFC) using resistances (R36-R41). PFC controller controls the output voltage (Vout_PFC) so that the output terminal sense voltage (VSENSE) divided by these resistors matches the internal reference voltage Vref_PFC (5 V) of the PFC controller. Calculate the output voltage (Vout_PFC) at Ta = 25 °C using the following equation with Ibias_PFC (100 nA) as the bias current for VSENSE pin voltage.

$$Vout\_PFC = \frac{Vref\_PFC \times (R36+R37+R38+R39+R40+R41)}{R41} + Ibias\_PFC \times (R36+R37+R38+R39+R40)$$

The setting of the output voltage (Vout_PFC) is approximately 390 V, and for this the resistance value of R36-R38 is 150 kΩ, the resistance value of R39 is 130 kΩ, the resistance value R40 is 120 kΩ, and the resistance value of R41 is 9.1 kΩ.

Next, perform the variation calculation of the output voltage. Calculate $Vout\_PFC_{min}$ and $Vout\_PFC_{max}$ using the variations of the parameters in the above equation as follows.

Vref_PFC :4.87 V (min), 5.15 V (max)

Ibias_PFC :20 nA (min), 250 nA (max)
R36-R40 : (D) Deviation, TCR = ±100 ppm/°C
R41 : (D) Deviation, TCR = ±50 ppm/°C
Operating temperature: 0 ℃ (min), 55 ℃ (max)

Regarding the temperature change of R36-R41, the positive direction change shall be +45 ℃ considering the difference of 30 ℃ from Ta = 25 ℃ to the upper operating temperature limit of 55 ℃ and the temperature rise of 15 ℃ inside the equipment, and the negative direction change shall be -25 ℃ from Ta = 25 ℃ to the lower operating temperature limit of 0 ℃. If the effects of the variations in the above parameters are calculated using the sum of square roots, then $Vout\_PFC_{min}$ and $Vout\_PFC_{max}$ are as follows:

$Vout\_PFC_{min}$ = 379.1 V
$Vout\_PFC_{max}$ = 401.8 V

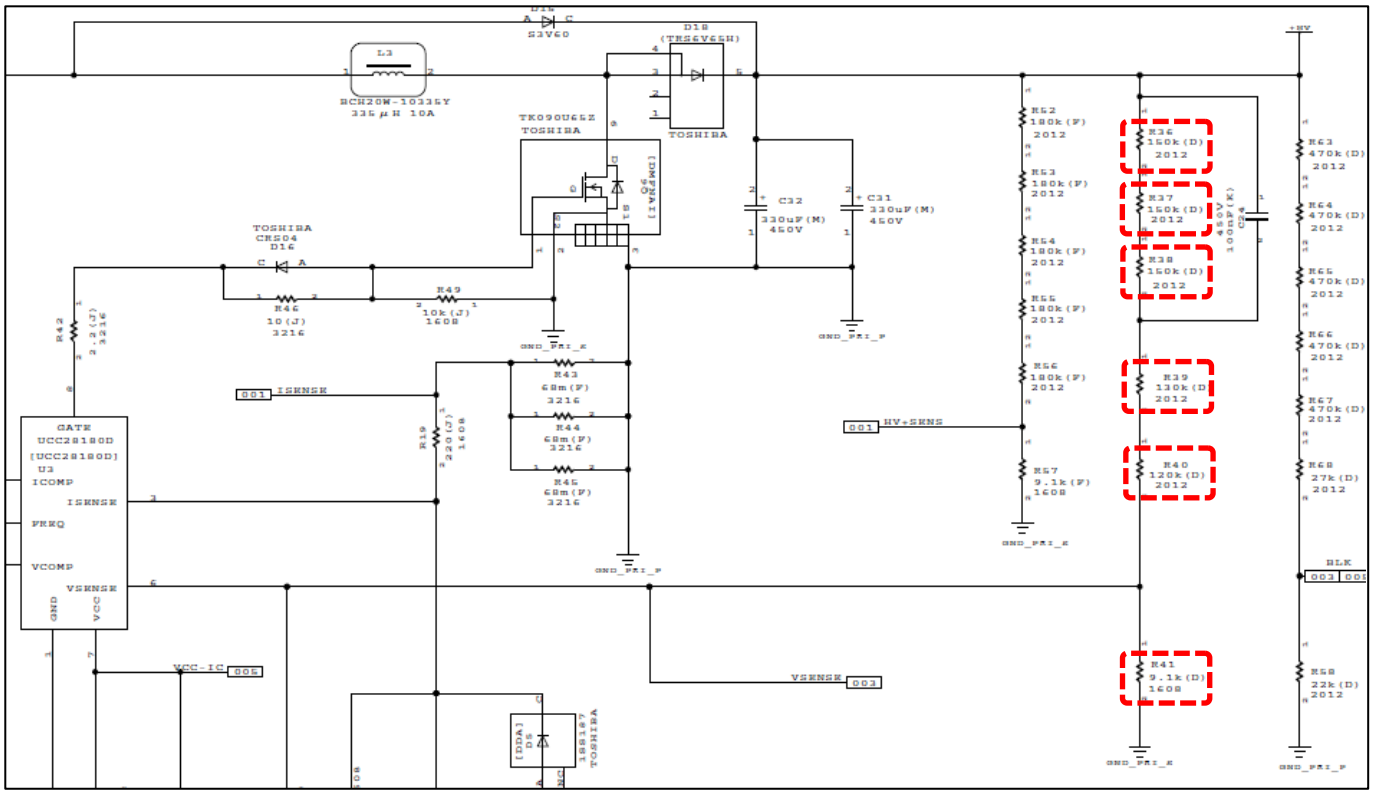

Fig. 2.3 Output Voltage Setting Circuit

Gate Drive Circuit

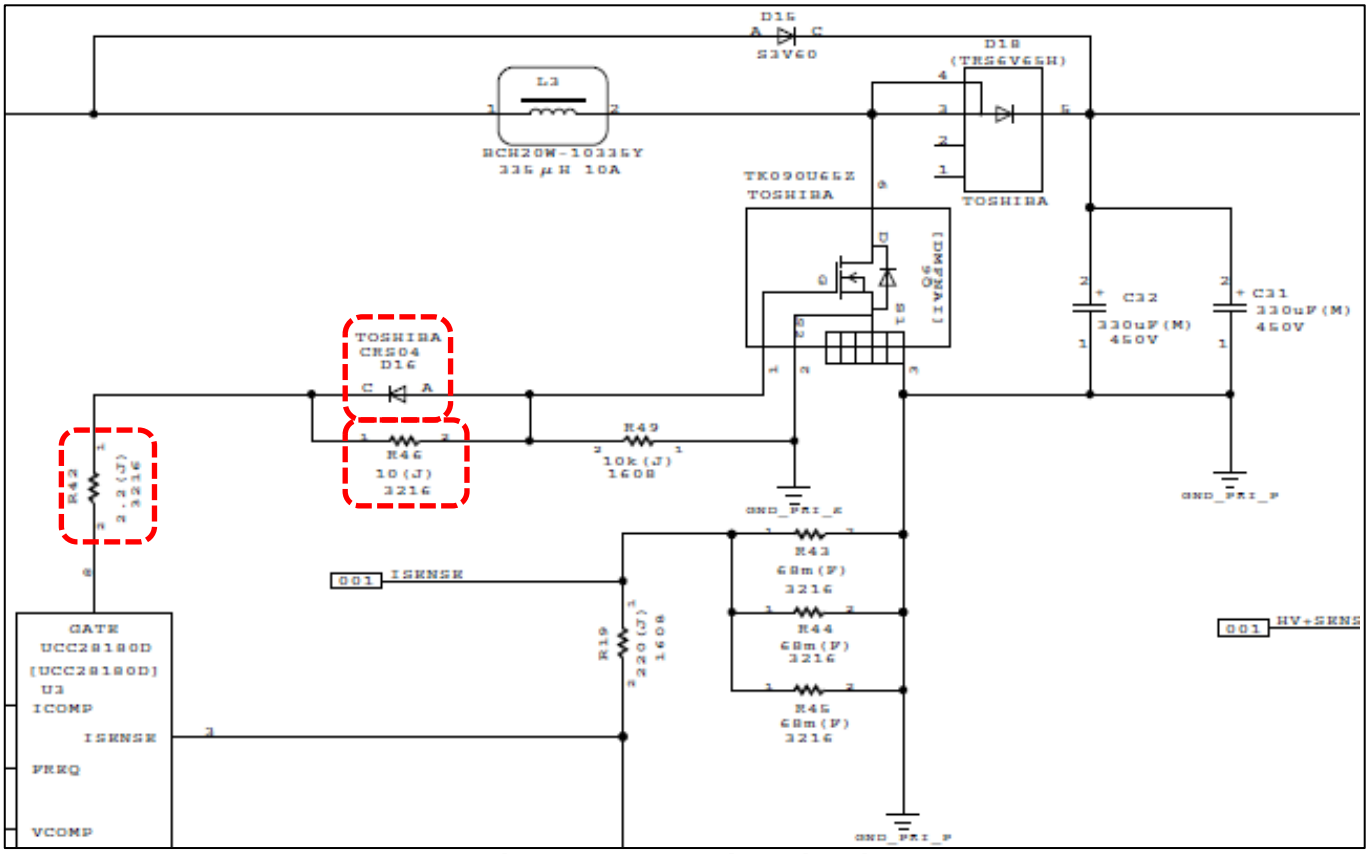

Fig. 2.4 Gate Drive Circuit

Fig. 2.4 shows the gate drive circuit. Gate drive design affects power supply efficiency and EMI (noise). Generally, there is a trade-off between power efficiency and EMI (noise), and a balanced design is required. To reduce EMI (noise), adjust the resistance value of the gate series resistors (R42, R46) and check result. Individual adjustments of turn-on speed and turn-off speed of MOSFET gate-drive circuitry are possible. If EMIs (noises) occur both at turn-on and turn-off of MOSFET, increase the value of resistor R42. This allows you to reduce turn-on and turn-off speeds at the same time, and thus reducing EMI (noise). If EMIs (noises) are present when MOSFET turns on, increase the value of resistor R46. Due to D16, the value of R46 does not participate in the turn-off speed. This only reduces the turn-on speed and thus reduces EMI (noise) during turn-on.

Note that increasing the resistor (R42, R46) may reduce the switching speed of MOSFET, which may also reduce the power-supply efficiency. Check that the power supply efficiency specification and heat dissipation specification satisfy the required specification.

Switching Frequency

Fig. 2.5 shows the switching frequency adjustment circuit. The switching frequency (fpwm1) of the PFC controller is calculated by the following equation.

$$fpwm1 = \frac{65kHz \times 32.7k\Omega \times 1M\Omega + 65kHz \times 32.7k\Omega \times R20}{R20 \times 1M\Omega + 65kHz \times 32.7k\Omega \times R20}$$

The switching frequency (fpwm1) setting is 78.3 kHz, where R20 is 27 kΩ.

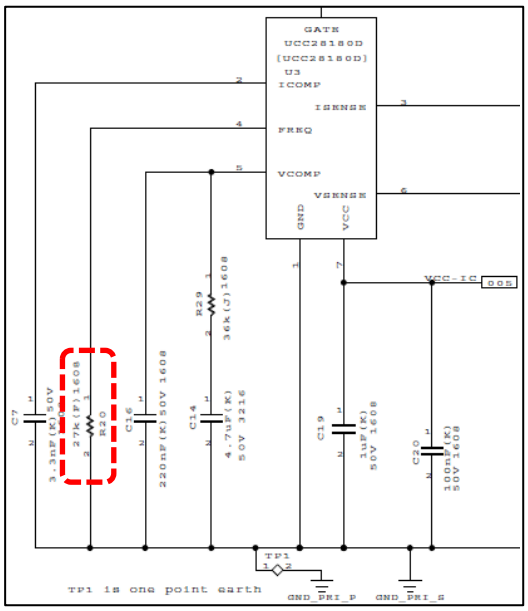

Fig. 2.5 Switching Frequency Adjustment Circuit

Inductor

Fig. 2.6 shows the inductor peripheral circuit. Set the inductance (L) of inductor L3 using the following items.

1. Max. Output Power (Pout)
2. AC-Line Voltage RMS (VinAC)
3. Total power conversion efficiency (η1 x η2) and power factor (PF) of this power supply
4. PFC output voltage (Vout_PFC)
5. Switching frequency(f_{PWM1})

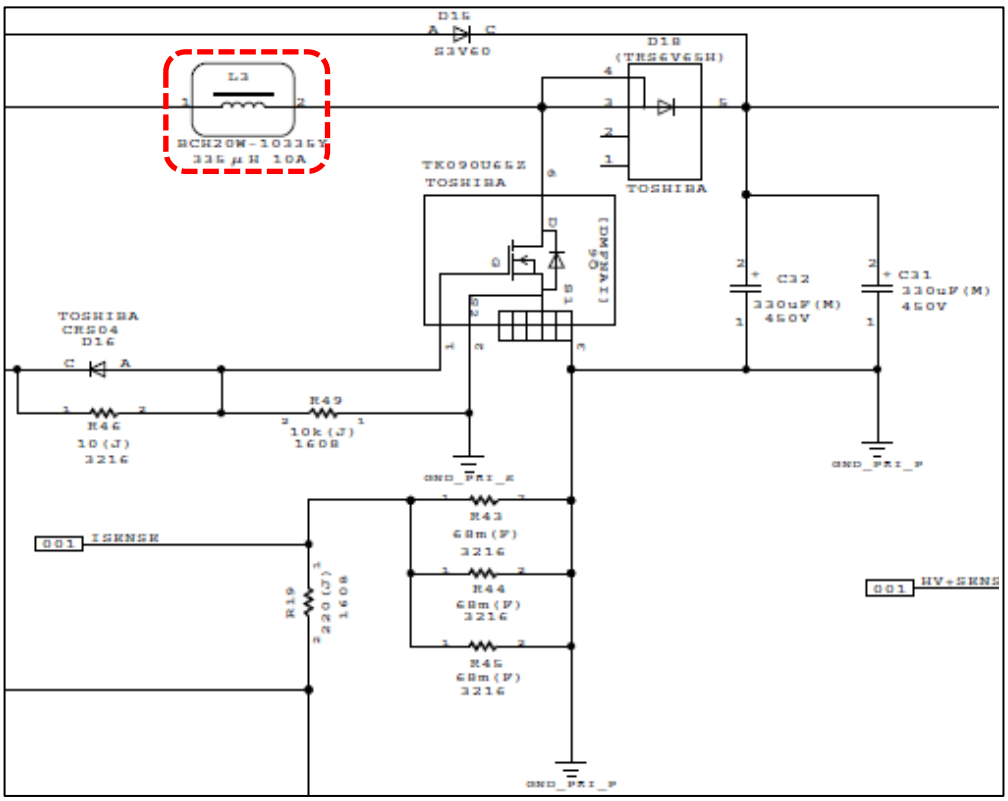

Fig. 2.6 Inductor Peripheral Circuits

When the ripple current (ΔI) of the inductor is set to 33.5 % of the peak input current value ($ACin_{peak}$) of the AC line, the inductance (L) value can be calculated by the following equation.

$$ACin_{peak} = \frac{Pout \times \sqrt{2}}{\eta 1 \times \eta 2 \times PF \times VinAC_{min}}$$

$$\Delta I = ACin_{peak} \times 33.5\%$$

$$L = \frac{\left(Vout\_PFC - \sqrt{2} \times VinAC_{min}\right) \times \eta 1 \times \eta 2 \times PF \times VinAC_{min}{}^{2}}{33.5\% \times f_{PWM1} \times Vout\_PFC \times P_{out}}$$

When the maximum output power (Pout) is 500 W, the AC line voltage rms ($VinAC_{min}$) is 85 V, the PFC power supply efficiency (η1) is 94%, the LLC power supply efficiency (η2) is 94%, the power factor (PF) is 0.99, the PFC output voltage (Vout_PFC) is 390 V, and the switching frequency (f_{PWM1}) is 78.3 kHz, the inductance (L) is calculated to be 333 μH. Magnetic saturation due to load current must be considered when selecting an inductor. This power supply uses a coil with an inductance value of 335 μH at 10 A.
In addition, the peak current (IL_{peak}) that flows through the inductor is calculated using the AC line peak input current ($ACin_{peak}$) using the following equation.

$$IL_{peak} = ACin_{peak} + \frac{\Delta I}{2}$$

Because the AC line peak input current ($ACin_{peak}$) is 9.5 A, the peak current (IL_{peak}) that flows through the inductor is 11.1 A, therefore a coil that can pass 11.1 A or more must be selected.

Output Capacitor

Fig. 2.7 shows the peripheral circuits of the output capacitor. Capacitance of output capacitor (C31, C32, hereafter referred as Cout_PFC) is calculated based on hold-up time requirements.

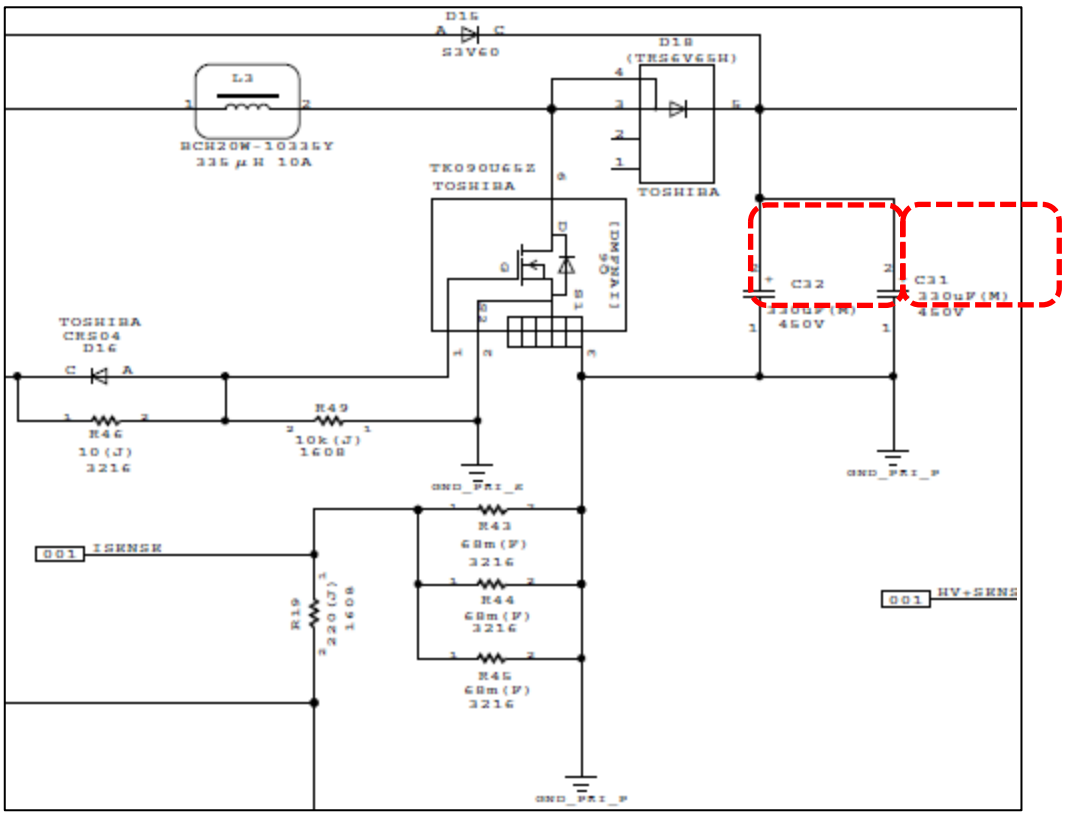

Fig. 2.7 Output Capacitor Peripheral Circuit

The hold-up time (Thold) is calculated using Cout_PFC, the output voltage (Vout_PFC), the output low limit voltage (Vout_PFC_hold), the maximum output power (Pout), and the LLC power supply efficiency (η2).

$$Thold = Cout\_PFC \times \frac{(Vout\_PFC^2 - Vout\_PFC\_hold^2) \times \eta 2}{2 \times Pout}$$

When the capacitance (Cout_PFC) setting is 660μF, the output voltage (Vout_PFC) is 390 V, the output low limit voltage (Vout_PFC_hold) is 330 V, the LLC power supply efficiency (η2) is 94 %, and the maximum output power (Pout) is 500 W, the hold-up time (Thold) becomes 26.8 ms.

In addition, when there is a required specification for the output ripple, set it by the following method.

1. Determine the capacitance value of the output capacitor (Cout_PFC) that satisfies the output ripple specification.
2. Calculate the capacitance value of the output capacitor (Cout_PFC) that satisfies the hold-up time.
3. Compare the capacitance values of both, and use the larger value.

Consider tolerances and aging degradation when selecting the output capacitor (Cout_PFC).

2.3. LLC Circuit Design

This power supply generates 500 W/12 V with an LLC-resonator. The LLC-resonant circuitry alternately turns on/off the high-side MOSFET and low-side MOSFET of each arm on the input side at a duty of 50%, and adjusts the frequency to turn on/off according to the load to control the output voltage. When the high-side MOSFET and low-side MOSFET are switched, a dead-time is provided to prevent penetration. However, MOSFET performs Zero Volt Switching (ZVS) due to resonance operation during that period. ZVS reduces switching losses and enables a high-efficiency power supply. This power supply uses a controller UCC256303 manufactured by Texas Instruments (hereinafter referred to as the LLC controller) to form an LLC resonator. Fig. 2.8 shows the LLC power supply circuit (around the LLC controller) and explains the basic design process. For detailed design of the surrounding circuit, refer to the datasheet and related documents of UCC256303.

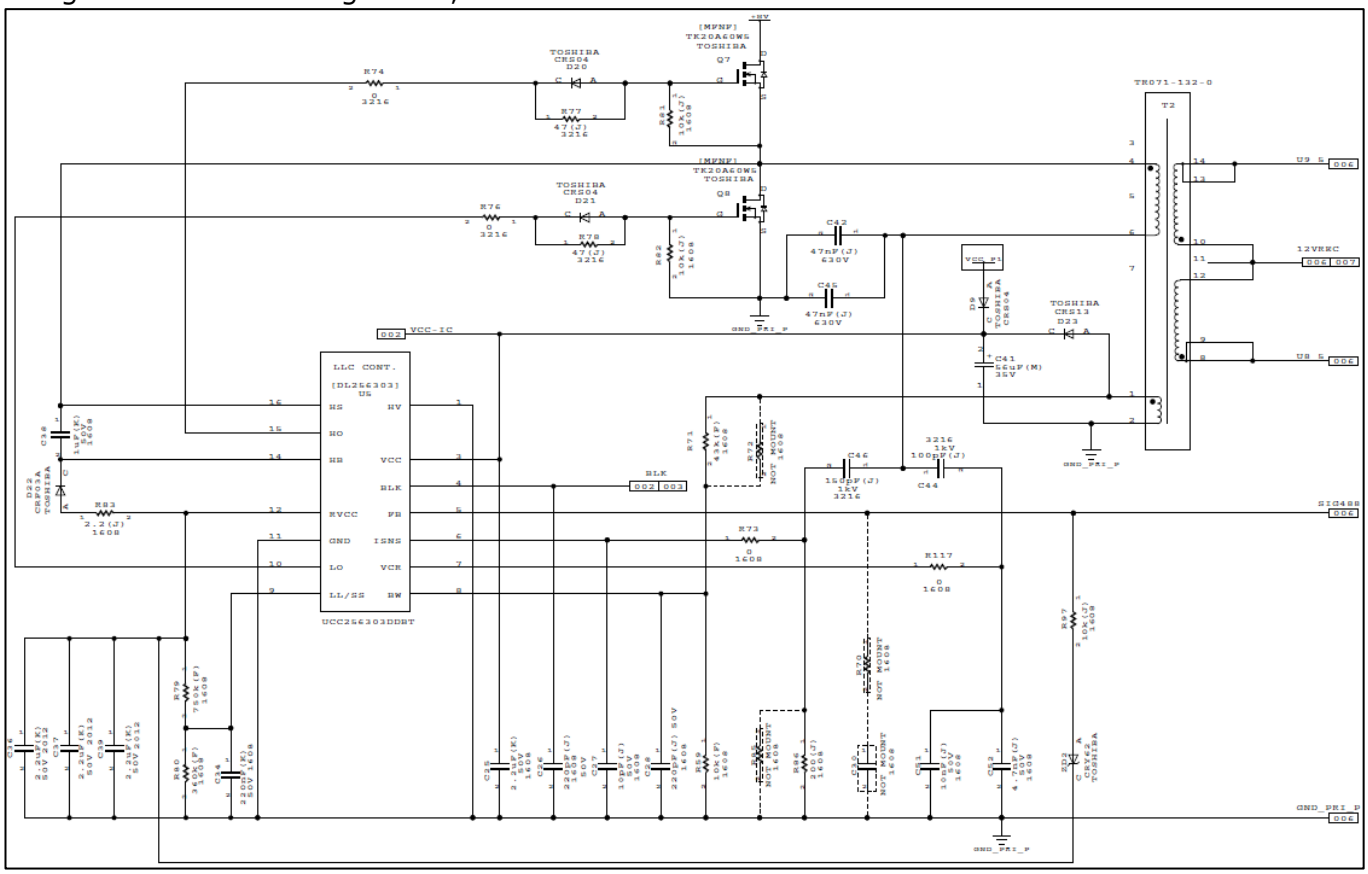

Fig. 2.8 LLC Power Supply Circuit (Circuit around LLC Controller)

Setting the Input Voltage Operating Range

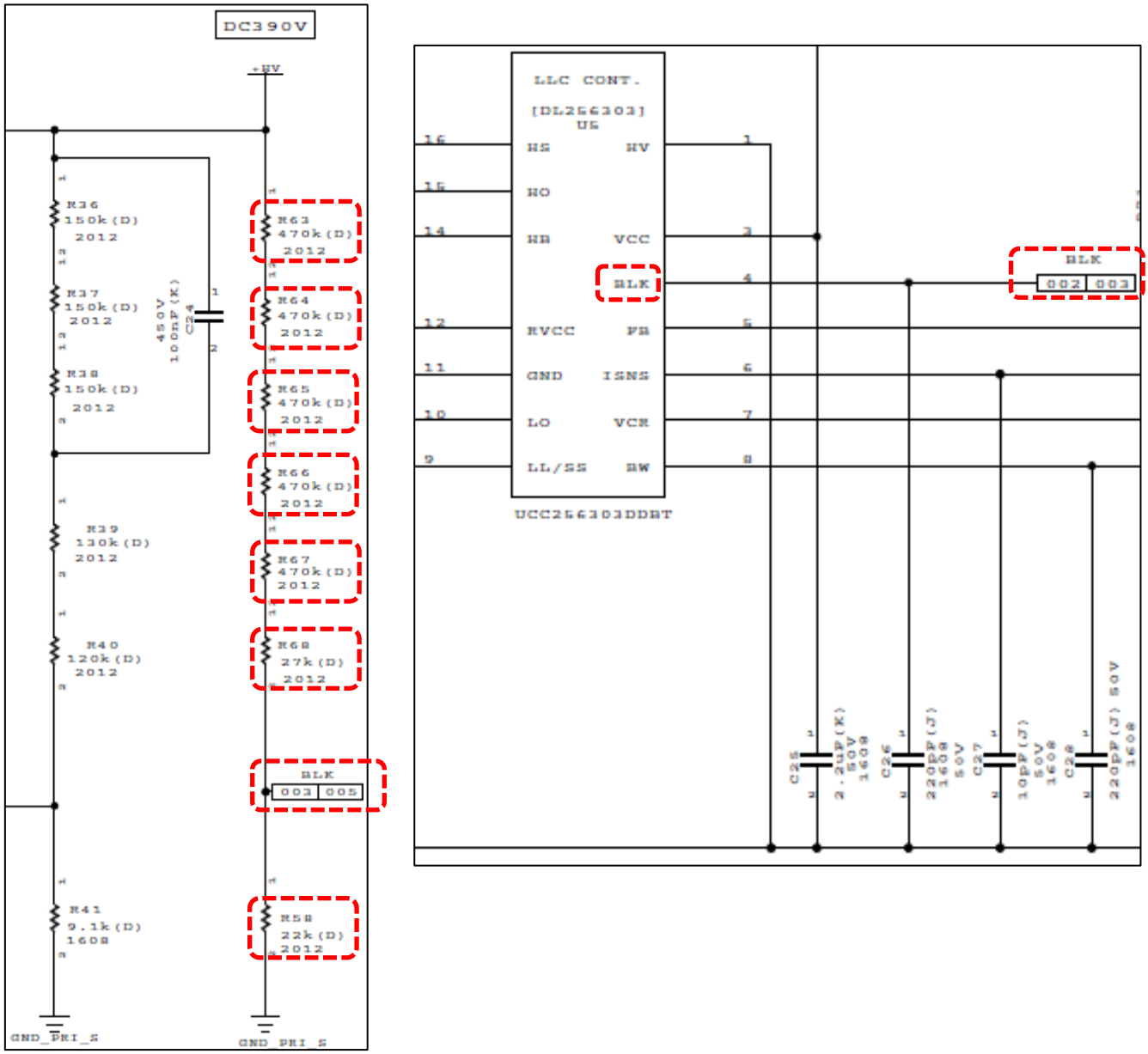

Fig. 2.9 LLC Operation Lower Limit Setting Circuit

Fig. 2.9 shows the LLC operation lower limit setting circuit. The LLC circuit operates on the output of the PFC circuit as an input power supply. The LLC controller detects the output voltage of the PFC circuit and starts operation. The operating voltage range of the LLC controller is set by the resistance value of the external resistors (R58, R63-R68). The operating voltage range ($V_{in\_min\_on}$, $V_{in\_min\_off}$) of the LLC circuit is set by dividing the output voltage Vout_PFC of the PFC circuit with the resistors (R58, R63-R68) and inputting it to the BLK pin of the LLC controller (U5). The LLC controller (U5) starts switching when the BLK pin voltage (generated by dividing with these resistors) exceeds the operation start threshold voltage (3.05 V), and stops switching when it falls below the operation stop threshold voltage (2.17 V). Calculate the operating voltage lower limit ($V_{in\_min\_on}$, $V_{in\_min\_off}$) using the following equation.

$$V_{in\_min\_on}(V) = 3.05V \times \frac{(R58 + R63 + R64 + R65 + R66 + R67 + R68)}{R58}$$

$$V_{in\_min\_off}(V) = 2.17V \times \frac{(R58 + R63 + R64 + R65 + R66 + R67 + R68)}{R58}$$

In this power supply, the set value of the output voltage $V_{in\_min\_on}$ of the PFC where the LLC circuit starts operation is set to 333 V, and the set value of the output voltage $V_{in\_min\_off}$ of the PFC where the LLC circuit stops operation is set to 237 V. As shown in Fig. 2.9, 22 kΩ is selected for resistor (R58), 470 kΩ for resistor (R63-R67), and 27 kΩ for resistor (R68). Fig. 2.10 shows the relation between the input voltage (V_{in}) and the EN pin voltage and the switching operation status.

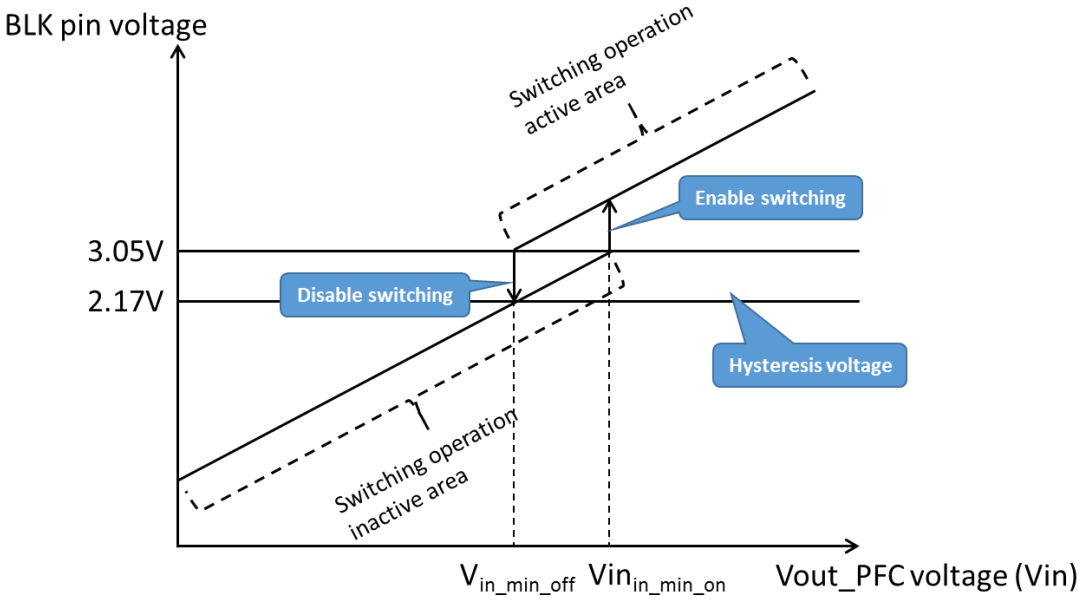

Fig. 2.10 Input Voltage vs UVLO Pin Voltage, Switching Operation Status

Output Voltage Setting

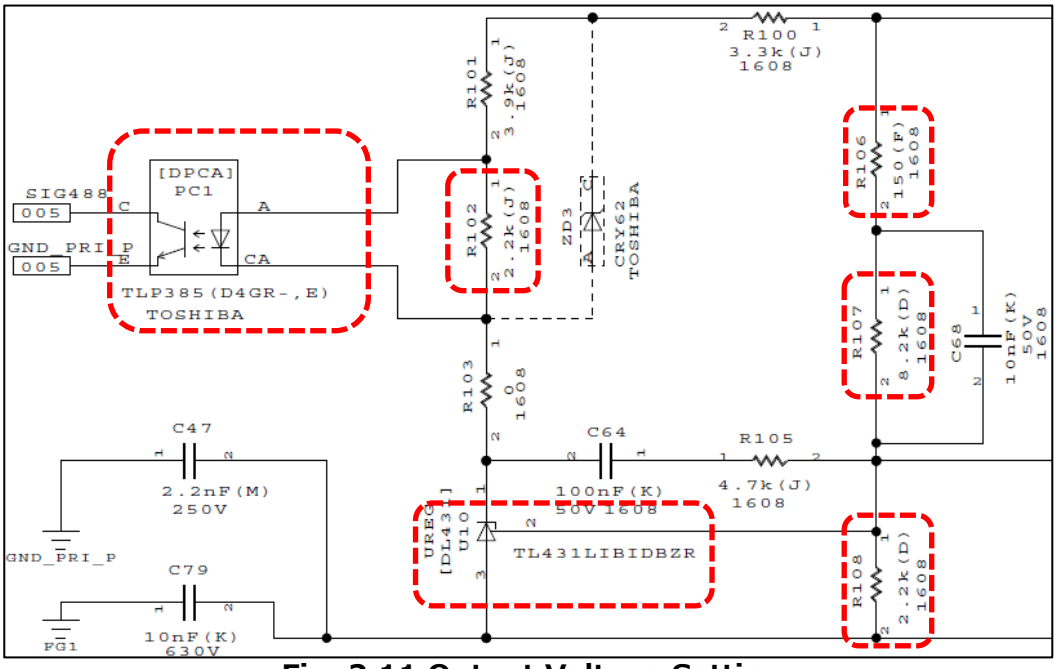

Fig. 2.11 Output Voltage Setting

Fig. 2.11 shows the output voltage setting circuit. Set the output voltage (Vout_LLC) of this power supply with the external resistors (R106, R107, R108) and the shunt regulator (U10). The shunt regulator (TL431LIBIDBZR) controls the current of the photocoupler (PC1) so that the voltage obtained by dividing the output voltage of this power supply by the resistor (R106, R107, R108) matches the reference voltage Vref_LLC (2.495 V). The LLC controller operates to maintain a constant output-voltage (Vout_LLC) depending on the amount of current fed back from the photocoupler (PC1). Using the bias current to the REF pin voltage of the shunt regulator as Ibias_LLC (200 nA), calculate the output voltage (Vout_LLC) using the following equation.

$$Vout\_LLC = \frac{Vref\_LLC \times (R106 + R107 + R108)}{R108} + Ibias\_LLC \times (R106 + R107)$$

The output voltage (Vout_LLC) is set to 11.97 V with a resistance (R106) of 150 Ω, a resistance (R107) of 8.2 kΩ, and a resistance (R108) of 2.2 kΩ.

Next, perform the variation calculation of the output voltage. Calculate $Vout\_LLC_{min}$ and $Vout\_LLC_{max}$ using the variations of the parameters used in the above equation as shown below.

Vref_LLC :2.466 V (min), 2.524 V (max)
Ibias_LLC : 0 A (min) and 400 nA (max) min. Because there is no specification, 0A is used.
R106 :(F) Deviation, TCR = ±100 ppm/°C
R107 :(D) Deviation, TCR = ±100 ppm/°C
R108 :(D) Deviation, TCR = ±50 ppm/°C
Operating temperature :0 ℃ (min), 55 ℃ (max)

Regarding the temperature change of R106-R108, the positive direction change can be +45℃ considering the difference of 30℃ from Ta = 25 ℃ to the upper limit of 55℃ and the temperature rise of 15℃ inside the equipment, and the negative direction can be-25℃ from Ta = 25 ℃ to the lower limit of 0℃. If the effects of the variations in the above parameters are calculated using the sum of square roots, then $Vout\_LLC_{min}$ and $Vout\_LLC_{max}$ are as follows:

$Vout\_LLC_{min}$ = 11.80 V
$Vout\_LLC_{max}$ = 12.14 V

The resistor (R102) connected in parallel to the photocoupler must be set to ensure the minimum cathode current of the shunt regulator, after taking into account various variations in the photocoupler's conversion efficiency, aging, and feedback current on the primary side.

Transformer (Resonance Design)

We will proceed with the study using the Fundamental Approximation Method (FHA). Fig. 2.12 shows the basic circuit of the LLC resonant circuit, and Fig. 2.13 shows a simple equivalent circuit.

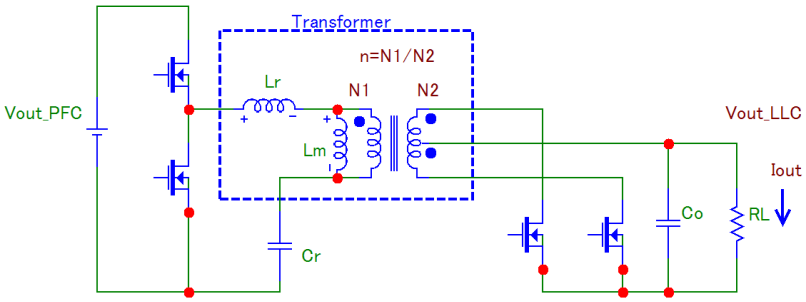

Fig. 2.12 Basic Circuit of LLC Resonant Circuit

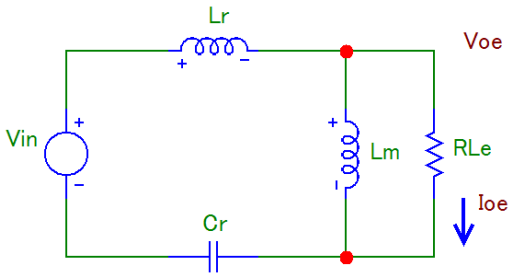

Fig. 2.13 Simple Equivalent Circuit of LLC Resonant Circuit

・Determination of turn ratio

The turn ratio n is calculated by the following equation using the output voltage Vout_PFC of the PFC and the output voltage Vout_LLC of the LLC.

$$n = \frac{Vout\_PFC}{2 \times Vout\_LLC}$$

n = 16.5 because Vout_PFC is 390 V, Vout_LLC is 12 V, and n = 16.25.

・Resonant circuit voltage gain determination

In the Fundamental Approximation Method (FHA), the design is developed based on the voltage gain between the input and output of the LLC circuit. The voltage gain required for LLC resonant circuit needs to be calculated. The maximum voltage gain Mg_nom_{max} required by the LLC-resonator under normal conditions is calculated using the following equation.

$$Mg\_\mathrm{nom}_{max} = \frac{n \times\ Vout\_LLC_{max}}{Vout\_PFC_{min}\ /2}$$

Mg_nom_{max} becomes 1.06 because n is 16.5, $Vout\_LLC_{max}$ is 12.14 V, and the steady-state $Vout\_PFC_{min}$ is 379.1 V. This allows voltage gain of Mg_nom_{max} = 1.06 even at 110% load which includes 10% margin from maximum load.

Next, calculate the maximum voltage gain Mg_hold_{max} required by the LLC-resonant circuitry in the event of an instantaneous power failure. In the event of an instantaneous power failure, it is assumed that there is no problem if a voltage gain that allows the output to secure a minimum value under the specification of the LLC output voltage at the maximum load is ensured, and the value is calculated using the following formula.

$$Mg\_\mathrm{hold}_{max} = \frac{n \times\ Vout\_LLC\_Spec_{min}}{Vout\_PFC\_hold\ /2}$$

The Mg_hold_{max} is = 1.14 because n is 16.5, the output power supply voltage lower limit $Vout\_LLC\_Spec_{min}$ of this power supply is 11.4 V, and the instantaneous stop Vout_PFC_hold is 330 V.

From the above, the voltage gain required for the LLC resonant circuit is Mg_nom_{max} = 1.06 at 110 % load and Mg_hold_{max} = 1.14 at 100 % load. In the following calculations, we proceed with designing the resonant circuit with the voltage gain maximum Mg_{max} = Mg_hold_{max} = 1.14 required for the LLC resonant circuit, and confirm that at the final stage of designing, the voltage gain at 110 % load can ensure Mg_nom_{max} = 1.06.

Calculate the minimum voltage gain Mg_min required by the LLC resonant circuit using the following formula.

$$Mg_{\_min} = \frac{n \times Vout\_LLC_{min}}{Vout\_PFC_{max} /2}$$

Because n is 16.5, $Vout\_LLC_{min}$ is 11.80 V, and the steady-state $Vout\_PFC_{max}$ is 401.8 V, therefore Mg_min becomes 0.97.

・Resonant circuit quality factor derivation

Fig. 2.14 shows a graph showing the relationship between the gain maximum value Mg_max of the LLC resonant circuit in the Fundamental Approximation Method (FHA) and the quality factor Qe of the resonant circuit. Ln in the figure represents the ratio of the excitation inductance Lm of the transformer to the parasitic inductance Lr (Ln = Lm/Lr). If Ln = 5.5, and when Mg_max = 1.14, then the quality factor Qe of the LLC resonant circuit is 0.53. The quality factor Qe is as follows:

$$Qe = \frac{\sqrt{Lr/Cr}}{RLe}$$

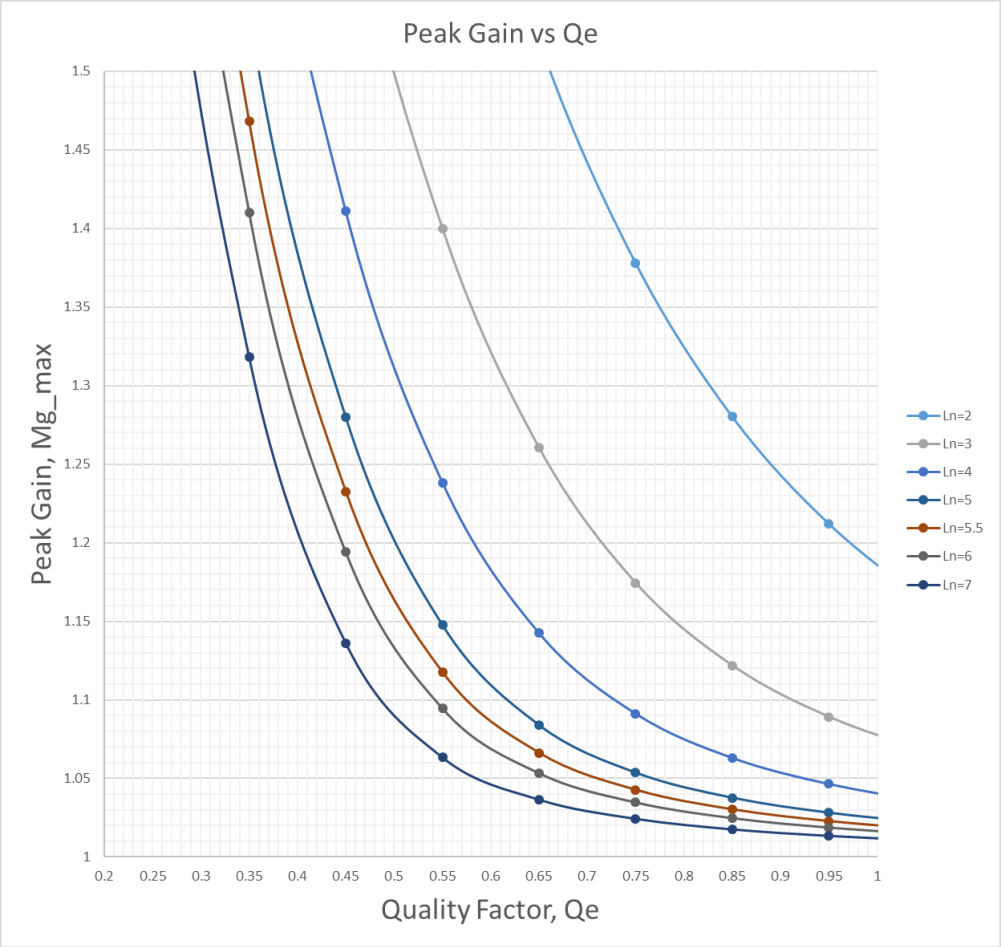

Fig. 2.14 LLC Resonant Circuit Voltage: Maximum Gain and Quality Factor Relationship Diagram

・Calculation of equivalent load resistance

The equivalent load-resistance R_{Le} in the simplified equivalent circuit of the LLC-resonant circuit is calculated by the following equation.

$$R_{Le} = \frac{8n^2}{\pi^2} R_L$$

Since R_L at the maximum load is 12 V/41.7 A = 0.288 Ω, R_{Le} at the maximum load is 63.56 Ω.

・Calculation of Cr, Lr, Lm

When the resonance frequency of Lr and Cr is f0, Cr is as follows:

$$Cr = \frac{1}{2 \times \pi \times f0 \times R_{Le} \times Qe}$$

Here, if f0 is assumed to be 55 kHz, Cr is calculated as 86 nF because R_{Le} is 63.56 Ω and Qe is 0.53. In this case, two 47 nF are used to set Cr = 94 nF.
Since Lr has the following equation, it is calculated to be 89 μH, therefore 90μH is used.

$$Lr = \frac{1}{(2 \times \pi \times f0)^2 \times Cr}$$

Lm is as shown in the following equation.

$$Lm = Ln \times Lr$$

Since Ln is 5.5, Lm is calculated to be 495 μH, and therefore 500 μH is used.

・Determination of Cr, Lr, Lm

The specifications of the transformer and resonant capacitor Cr created based on the above calculation results are as follows.

Turn ratio n = 16.5 (Np:Ns = 33:2)
Excitation inductance Lm = 500 μH
Parasitic inductance Lr =90 μH
Resonant capacitor Cr = 94 nF

Thus, the resonant frequency of the parasitic inductance Lr and the resonant capacitor Cr is f0.
The ratio of the excitation inductance Lm and the parasitic inductance Lr is Ln, which is as follows.

Resonance frequency f0 of Lr and resonant capacitor Cr is 54.72 kHz.
Ratio of Lm and Lr is Ln = 5.56.

・Resonant circuit voltage gain check

Fig. 2.15 shows a graph of relationship between the switching frequency and the voltage gain of a resonant circuit using a transformer and a resonant capacitor of the above specifications. The voltage gain Mg_nom_{max} = 1.06 required at 110 % load and the voltage gain Mg_hold_{max} = 1.14 required at 100 % load can be confirmed.

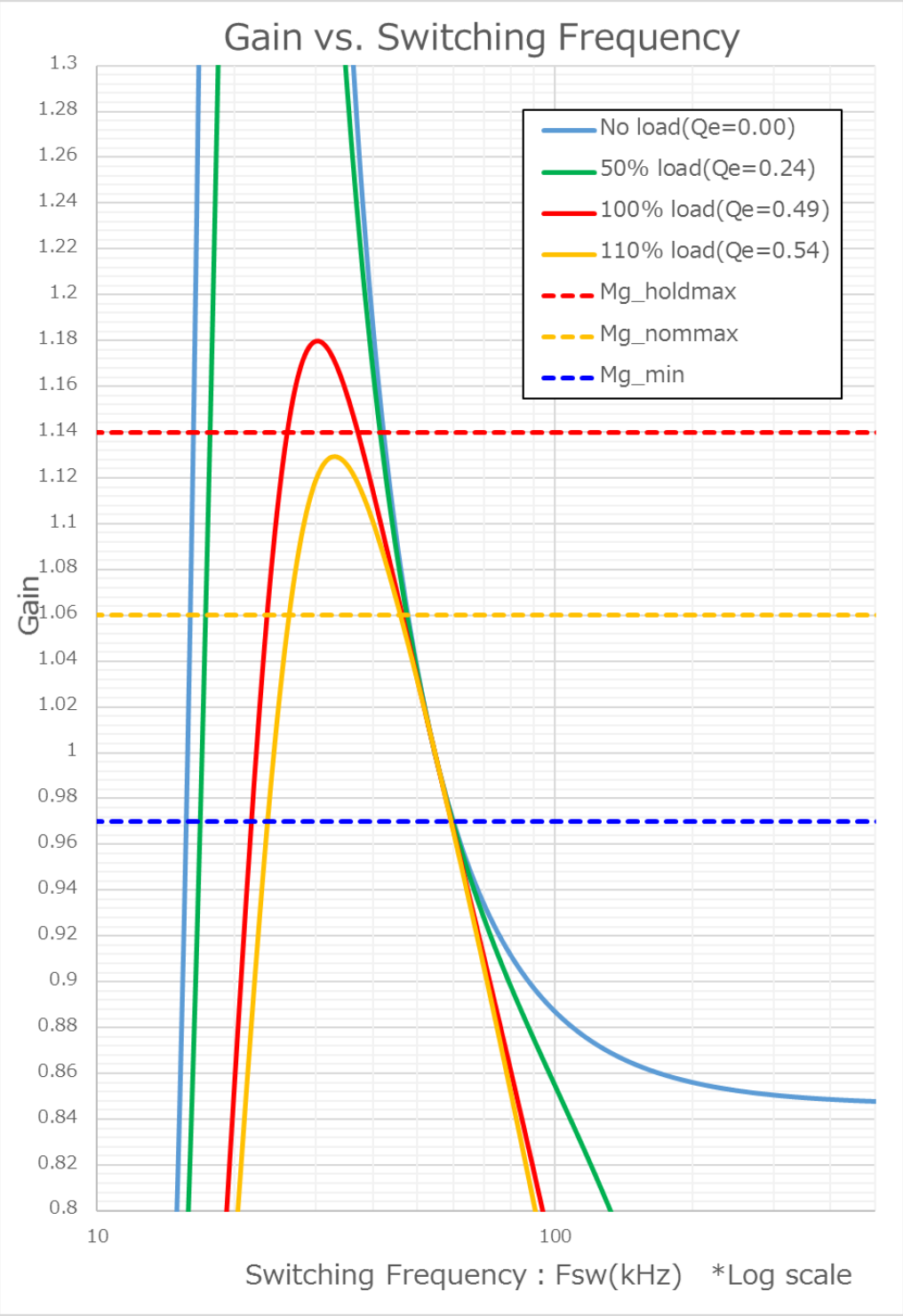

Fig. 2.15 LLC Resonant Circuit: Voltage Gain and Switching Frequency Relationship Diagram

・Switching frequency fluctuation range check

Fig. 2.16 shows a graph in which Fig. 2.15 is partially enlarged and the frequency axis is converted to a linear scale. From the graph, the minimum switching frequency Fsw_min is where the maximum voltage gain Mg_hold_{max} = 1.14 is secured at a load of 100%, and the maximum switching frequency Fsw_max is where the minimum voltage gain Mg_min = 0.97 is secured at no load. The calculation results are as follows.

Switching frequency minimum value Fsw_min = 37.21 kHz

Switching frequency maximum value Fsw_max = 60.19 kHz

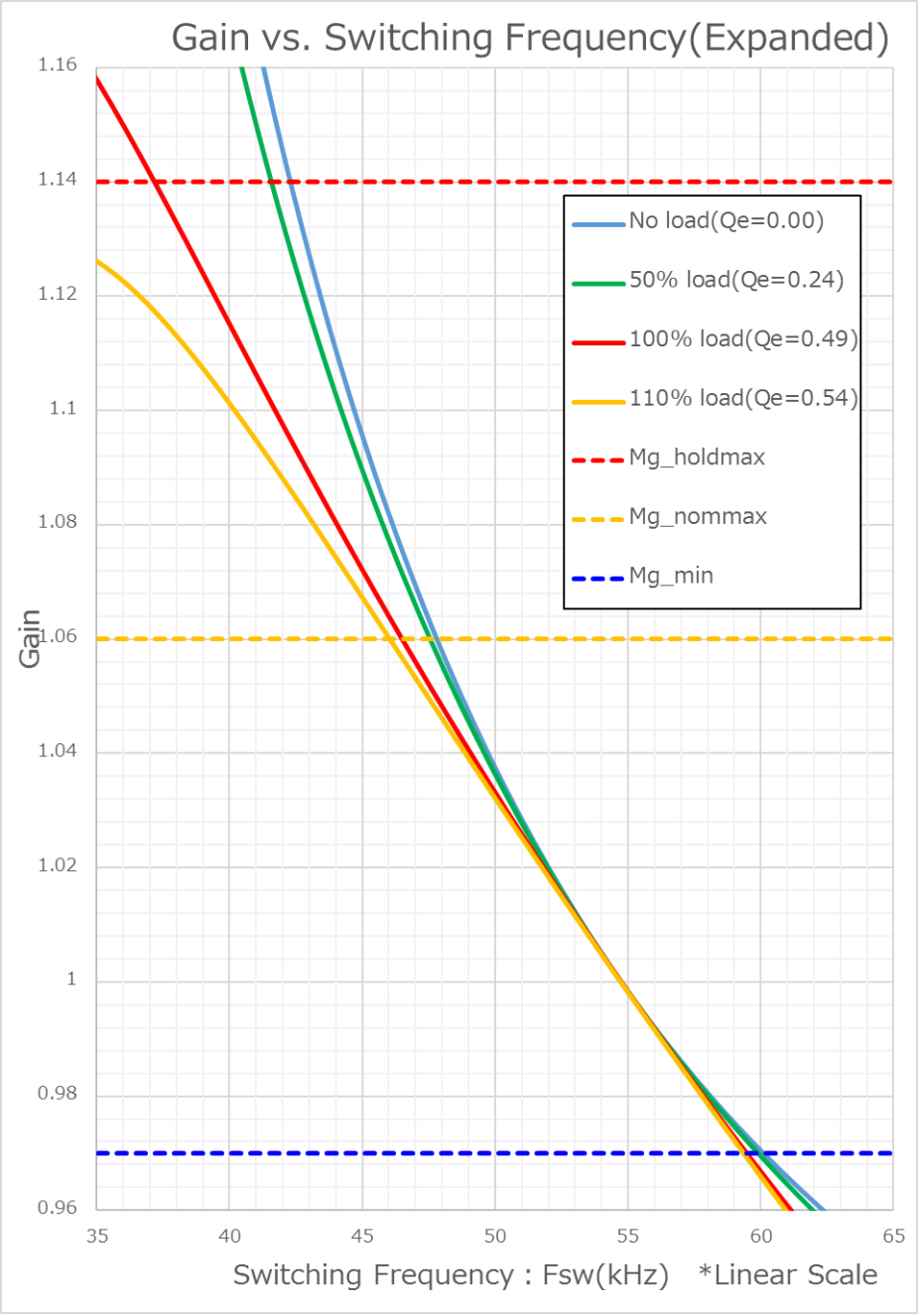

Fig. 2.16 LLC Resonant Circuit: Voltage Gain vs. Switching Frequency Relationship (Expanded, Frequency Axis Linear Scaling)

・Checking the current value

The effective current flowing through the secondary winding is determined assuming that sinusoidal current flows through the secondary winding. Since a center tapped type transformer is used, when the maximum load current is taken as $Iout\_LLC_{max}$, the current rms value Is_rms flowing through each wire of the secondary winding and the load current Ip_l flowing through the primary winding are as follows.

$$Is\_rms = \frac{\pi \times Iout\_LLC_{max}}{2\sqrt{2}}$$

$$Ip\_l = \frac{\pi \times Iout\_LLC_{max}}{2\sqrt{2} \times n}$$

Since $Iout\_LLC_{max}$ is 41.7 A and n is 16.5, the value of Is_rms becomes 46.3 A and Ip_l becomes 2.80 A. The Excitation current Ip_m flowing in the primary winding is as follows.

$$Ip\_m = \frac{2\sqrt{2} \times n \times Vout\_LLC}{2\pi^2 \times fsw \times Lm}$$

The excitation current Ip_m is maximum when the switching frequency minimum Fsw_min=37.21 kHz. Since Vout_LLC is 12 V and Lm is 500 μH, therefore Ip_m becomes 1.52 A.
Total primary winding current Ip is calculated by using the following formula. Therefore, Ip becomes 3.19 A.

$$Ip = \sqrt{Ip\_l^2 + Ip\_m^2}$$

・Checking Zero Volt Switching

The LLC power supply performs Zero Volt Switching (ZVSs) by charging and discharging the output capacitance of the switching MOSFET with energy stored by the exciting current of the transformer, thereby achieving high-efficiency. To achieve ZVS in a wide range of load conditions, the ZVS condition must be satisfied even when the excitation current Ip_m is minimum. ZVS is established when the energy stored by the excitation current of the transformer exceeds the energy required to charge and discharge the output capacitance of MOSFET. The minimum excitation current Ip_m is at the maximum switching frequency Fsw_max=60.19 kHz. Since Vout_LLC is 12 V and Lm is 500 μH, Ip_m becomes 0.94 A. At this time, the energy stored in the primary side of transformer is calculated as shown below.

$$\frac{1}{2}(Lm + Lr) \times \{0.94(A)\}^2 = 262\ \mu J$$

ZVSs can be realized if the output capacitance of the switching MOSFET can be charged and discharged with this energy. Since the effective capacitance of the switching MOSFET TK20A60W5 is 70 pF, the energy required for charging and discharging is calculated as shown below.

$$\frac{1}{2}(2pcs \times 70pF) \times {Vout\_PFC_{max}}^2 = 11.3\ \mu J$$

From the above, the energy (262 μJ) stored in the primary side the transformer is required to charge and discharge the output capacitance of the MOSFET (11.3 μJ).
It can be seen that the ZVS condition is satisfied even when the excitation current is minimum.

Soft Start Setting

Fig. 2.17 shows the soft start setting circuit. The soft-start time of the LLC power supply is set with an external capacitor (C34). The soft start time varies depending on the load conditions, but the maximum soft start time (Tss) can be calculated as follows.

$$Tss = \frac{7V \times C34}{25.8\ \mu A}$$

For this power supply, the maximum soft start time (Tss) is set to 56.7 ms, and 220 nF is selected for the external capacitor (C34). Adjust the soft start time by changing the capacitance as necessary.

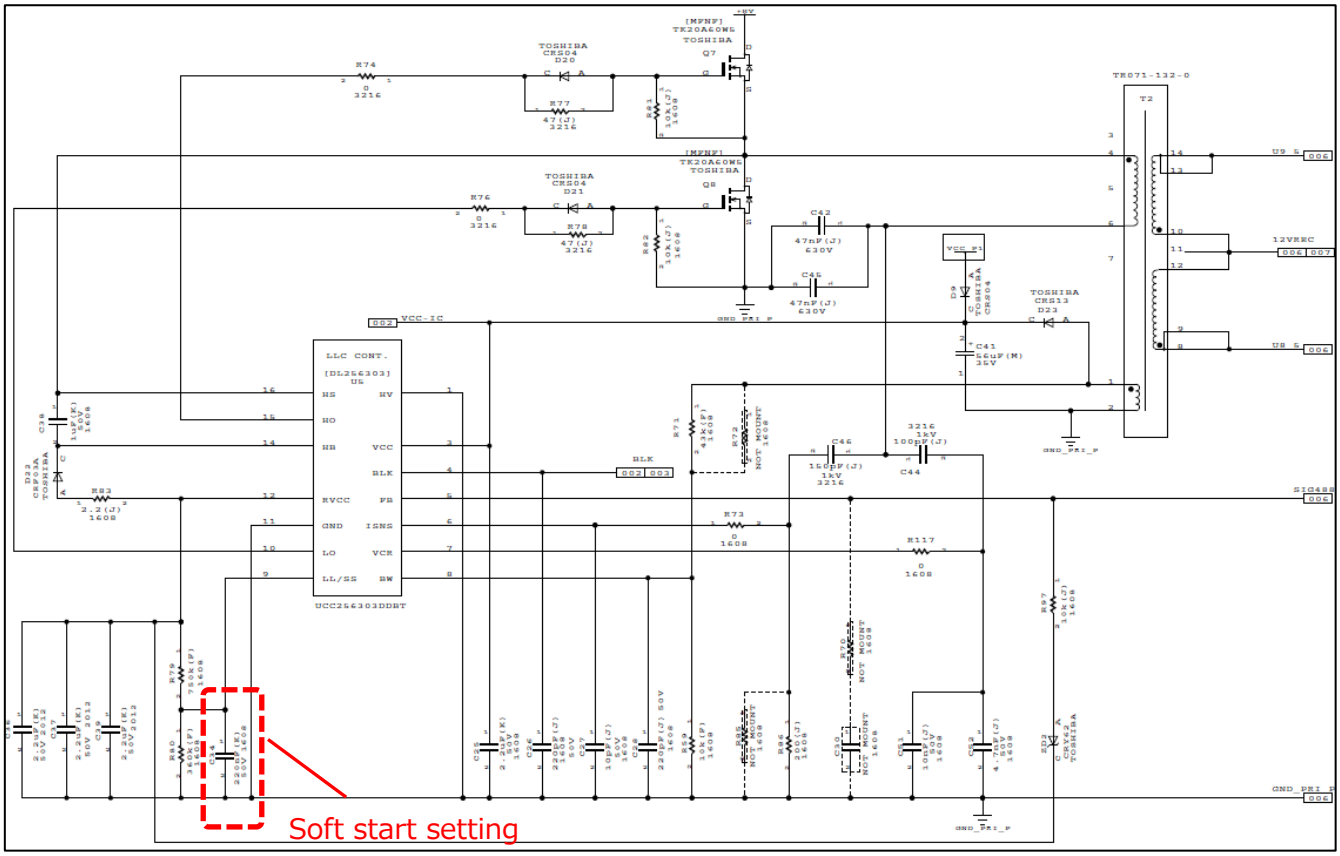

Fig. 2.17 Soft Start Setting Circuit

Current Limiter

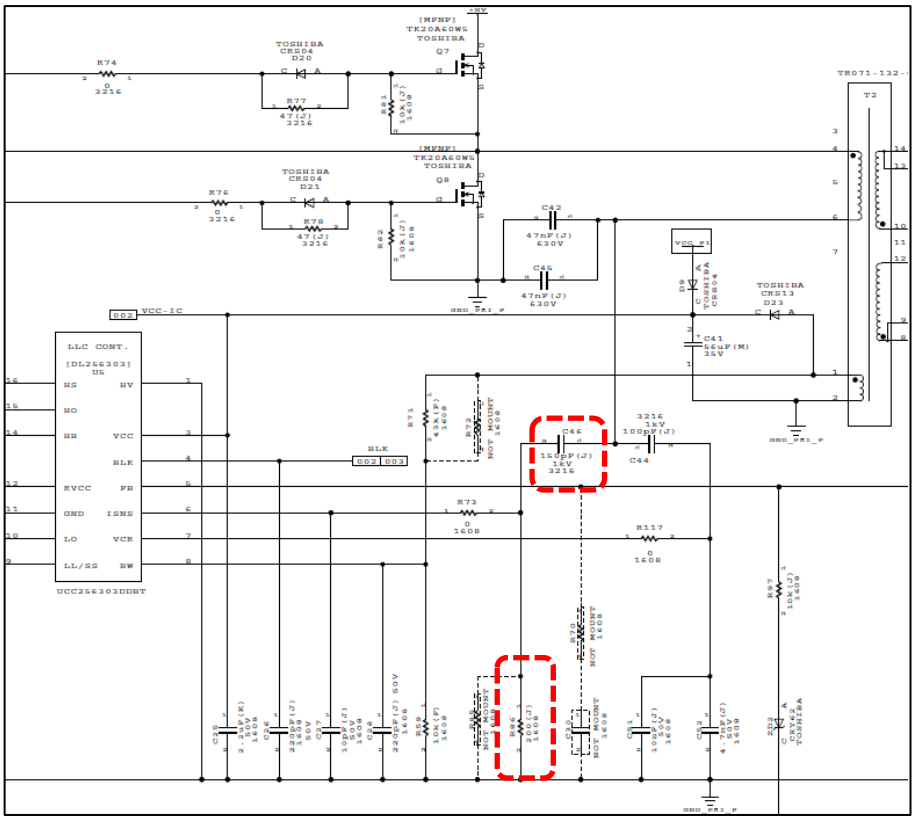

Fig. 2.18 Current Limiter Circuit

Fig. 2.18 shows the current limiter circuit. Set the current limiter level of the LLC with resistance (R86) and capacitance (C46). The LLC controller has a three-level current limiter (OCP1~OCP3). When the output load of the LLC power supply is increased, ISNS terminal voltage rises, but the overcurrent limiter is activated when ISNS pin voltage exceeds the threshold (OCP1~OCP3) for the specified period. This power supply sets the load current at which OCP3 operates to 150% of the maximum load ($Iout\_LLC_{max}$).

At this time, the conditions for the current limiter to be activated (ISNS terminal voltage threshold and duration) and the input current and output current at that time are shown in the table below.

	OCP1	OCP2	OCP3
ISNS terminal voltage thresholds	4.03 V (peak)	0.84 V (average)	0.64 V (average)
Duration	4 consecutive cycles	2 ms continuous	50 ms continuous
Input current	12.9 A (peak)	2.69 A (average)	2.05 A (average)
Output current	213 A (peak)	82.3 A (average)	62.7 A (average)

At this time, ISNS terminal voltage VISNS_Iout_LLC$_{max}$ at maximum load can be calculated by the following equation.

$$VISNS\_Iout\_LLC_{max} = \frac{VISNS\_OCP3}{150\%} = \frac{0.64V}{150\%} = 0.43\ V$$

From the maximum output power (Pout) of 500 W, the PFC output voltage (Vout_PFC) of 390 V, and the LLC power supply efficiency (η2) of 94%, the current sensing ratio K_{ISNS} is calculated as follows:

$$K_{ISNS} = \frac{VISNS\_Iout\_LLC_{max}}{\frac{Pout}{\eta 2} \times \frac{1}{PFC\_out}} = 0.31\ \Omega$$

Assuming that the capacitance value of C46 is 150 pF and the capacitance value of the resonant capacitor is Cr (94nF), R86 is calculated as follows.

$$R86 = \frac{K_{ISNS} \times Cr}{C46} = 196.0\ \Omega$$

Here 200 Ω is used as R86. The operation level of the current limiter must be checked on an actual device because it is affected by the layout.

Gate Drive Circuit

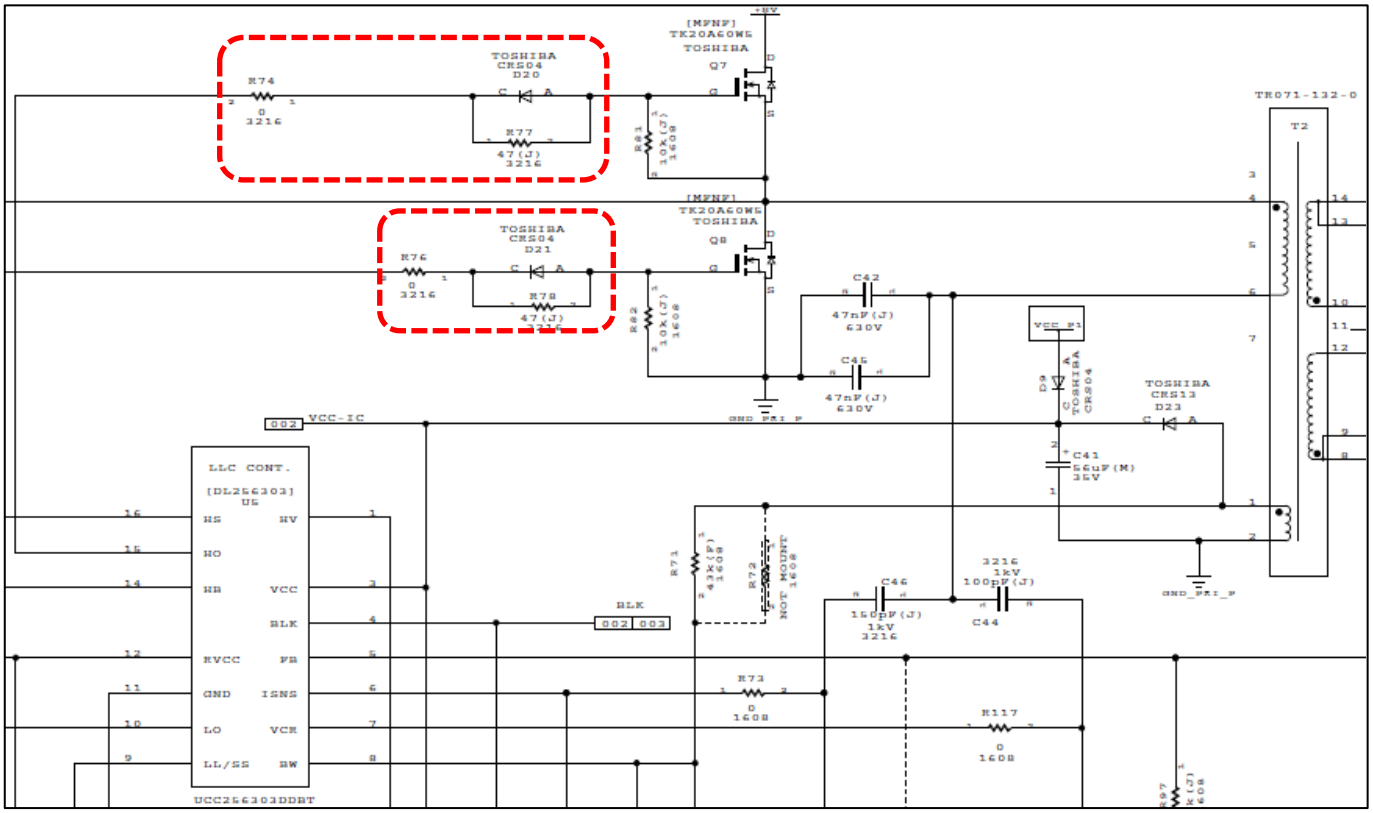

Fig. 2.19 Gate Drive Circuit

Fig. 2.19 shows the gate drive circuit. The design of the gate drive circuit affects power supply efficiency and EMI. Generally, there is a trade-off between power supply efficiency and EMI, and a

balanced design is required for both. The LLC circuitry has low EMI due to ZVS operation, but if switching noise seems to be the source of EMI issues, adjust the value of the gated series resistor (R74, R76-R78) and check it. The gate drive allows individual adjustments of MOSFET turn-on and turn-off speeds. If EMI (noise) occur at both turn-on and turn-off of MOSFET (Q7), increase the resistor R74. This allows you to reduce turn-on and turn-off speeds at the same time, reducing EMI (noise). If EMIs (noises) are occurring when MOSFET turns on, increase the resistor R77 . This reduces the turn-on speed only and reduces EMI (noise). If you want to reduce the EMI (noise) generated by switching MOSFET (Q8), adjust resistors R76 and R78 in the same way as in the case of Q7.

Note that increasing the resistor (R74, R76-R78) may reduce the switching speed of MOSFET, which may also reduce the power-supply efficiency. Check that the power supply efficiency specification and heat dissipation specification satisfy the required specification.

Output Capacitor

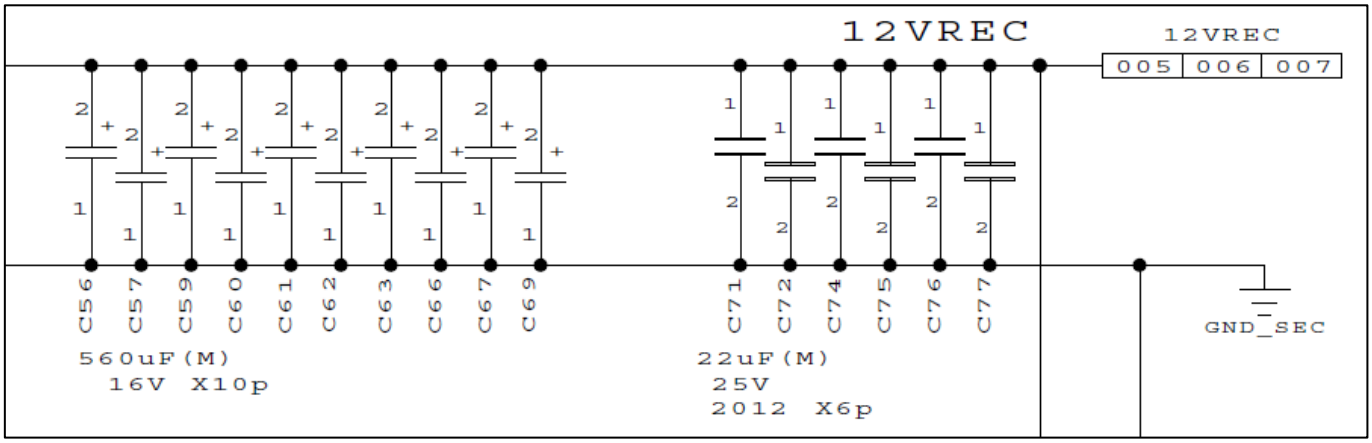

Fig. 2.20 Output Capacitor Peripheral Circuit

Fig. 2.20 shows the peripheral circuit of the output capacitor. Set the output capacitance value C_{out} to meet the requirements of the output voltage ripple (V_{ripple}) and the requirements of the ripple current. If the output voltage ripple (V_{ripple}) is 120 mV and the maximum load is I_{max}, the ESR required for the output capacitors is calculated as follows:

$$ESR = \frac{V_{ripple}}{\frac{2 \times \pi}{4} \times I_{max}} = 1.8 \ m\Omega$$

I_{max} is 41.7 A, so the ESR is 1.8 mΩ.

The RMS I_{C_rms} of the ripple current that flows through the output capacitors is calculated by the following equation.

$$I_{C\_rms} = \sqrt{\left(\frac{\pi}{2\sqrt{2}} I_{max}\right)^2 - {I_{max}}^2} = 20.2 \ A$$

Output capacitor quantity must be selected so that the above ESR and I_{C_rms} meet the specifications. This power supply has ten capacitors (C56, C57, C59-C63, C66, C67, C69) in parallel with an output capacity of 560 µF, an ESR of 8 mΩ, and an allowable ripple current of 4.2 A (rated ripple current of 6.1 A at 100 kHz, and a frequency correction factor of 0.7 for 10 kHz ≦ f < 100 kHz). This results in a total ESR of 8 mΩ/10 = 0.8 mΩ, indicating that the above requirements are met. The ripple current per unit is also 20.2 A/10 = 2.02 A, which indicates that the specifications are satisfied.

Also, check the following:

1. Output terminal undershoot and overshoot that occur when the load changes suddenly fall within the specified voltage range.
2. The allowable ripple current of the output capacitor is ensured.
3. Consider tolerances and aging of output capacitors.

Synchronous Rectifier MOSFET Surge-Voltage Reduction Circuit

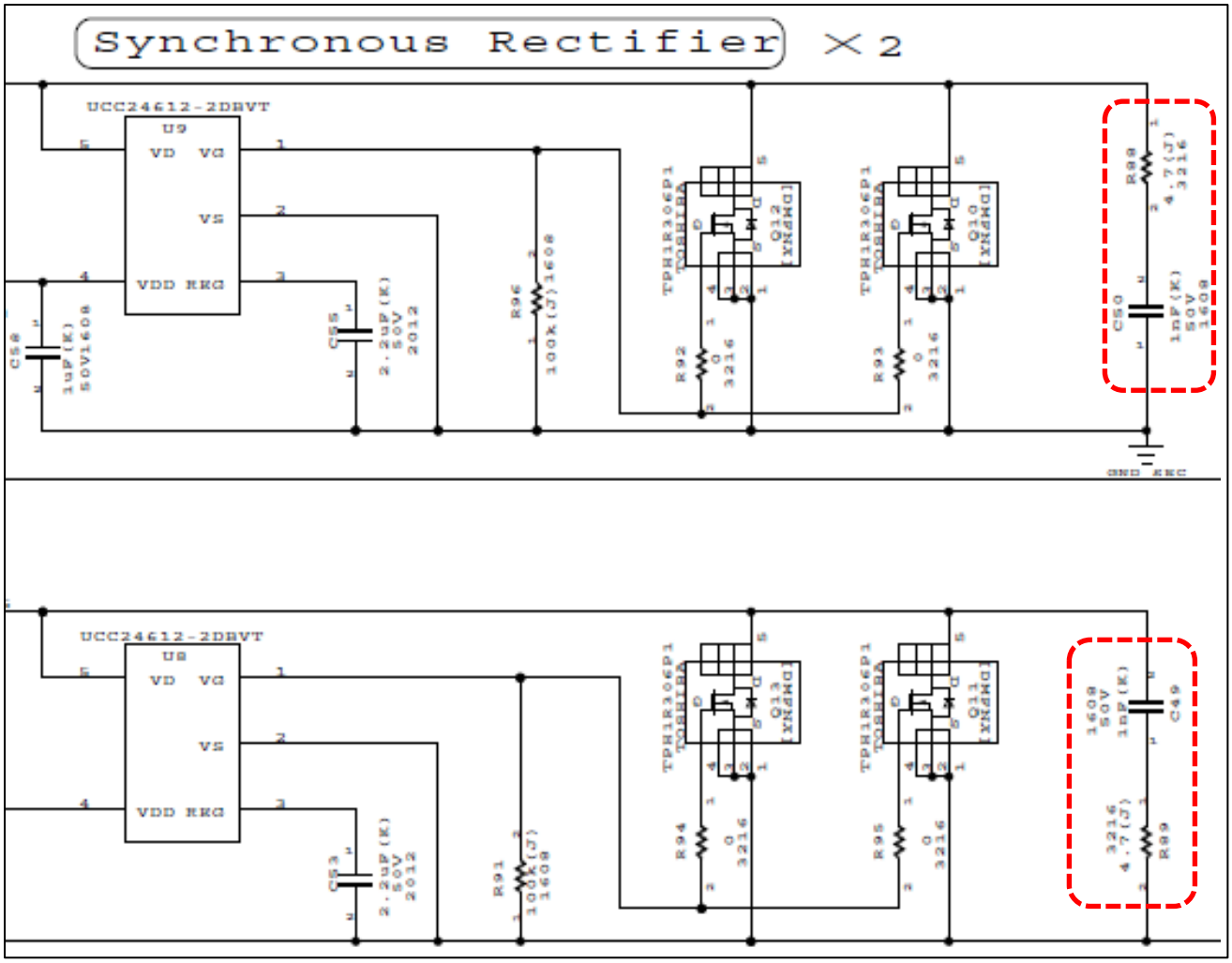

Fig. 2.21 Snubber Circuitry

Fig. 2.21 shows Snubber circuitry. Snubber circuitry consists of R89, C49, R88 and C50. Snubber circuitry absorbs surge-voltage (V_{srg}) generated in Q10-Q13. At this time, the loss P_{d_Rsnb} generated by the resistors R89 and C49 are as follows.

$$P_{d\_Rsnb} = C49 \times (V_{srg})^2 \times \left(\frac{f_{PWM}}{2}\right) = 36.87\ mW$$

If the surge voltage (V_{srg}) is 35 V, the C49 is 1000 pF, and f_{PWM} is the maximum switching frequency Fsw_max = 60.19 kHz, then the loss P_{d_Rsnb} generated by resistor R89 is 36.87mW. Adjust the constants and ratings of each element according to the actual surge voltage level.

3. Reduction in Size by Adopting TOLL Package

Fig. 3.1 shows the block diagram of the circuit. By adopting TOLL package product for MOSFET installed in PFC circuit, we have achieved a size reduction in power supply that uses TO-220SIS package.

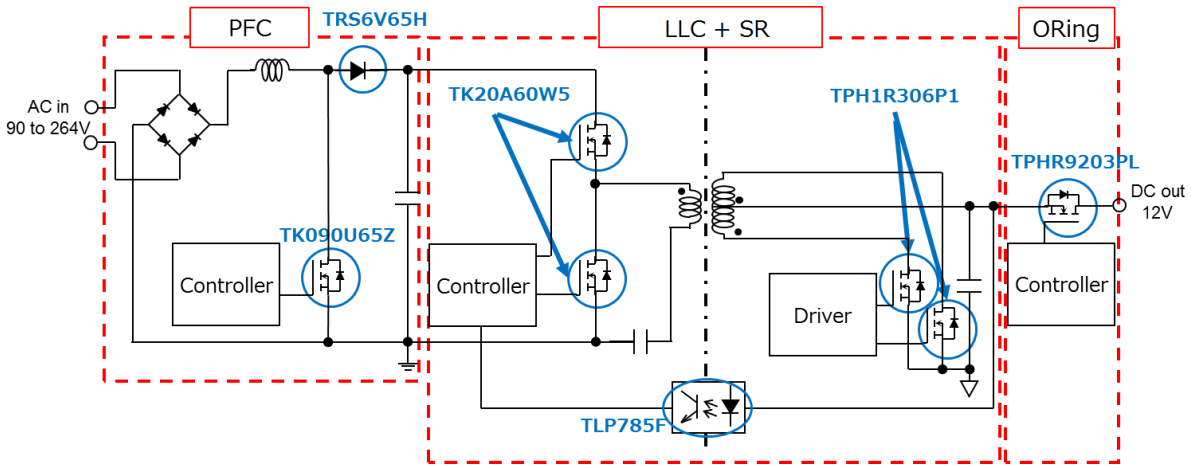

Fig. 3.1 Circuit Block Diagram

TOLL package is a surface-mounted type package. The signal source terminal for the gate drive can be kelvin-connected. This reduces the impact on switching caused by the inductance of the source wire inside the package, which leads to high-speed switching performance of MOSFET and reduces switching losses. The thermal resistance of the device is as low as 1/5 that of TO-220SIS packaged product, and the heat dissipation through the board is designed to reduce the switching loss. In addition, the heat dissipation of the device contributes to a reduction in the size of the heat sink. Miniaturization of the heat sink, which is a large component, increases the freedom of placement of other components, and helps in reducing the board area more than the size of the heat sink.

Mounting of TOLL Package on PCB and Mounting of Heat Sink

Mounting of TOLL package is important for heat dissipation. TOLL package is surface-mounted on the board, and heat is dissipated through the insulating sheet with a heat sink mounted on the front of the board through the thermal vias provided on the board. Therefore, not only heat sink but also substrate layout is greatly related to the heat dissipation effect. The PFC diode is placed next to the PFC circuit board and mounted on the same heat dissipation board, resulting in a higher mounting density. Fig. 3.2 shows the mounting diagram.

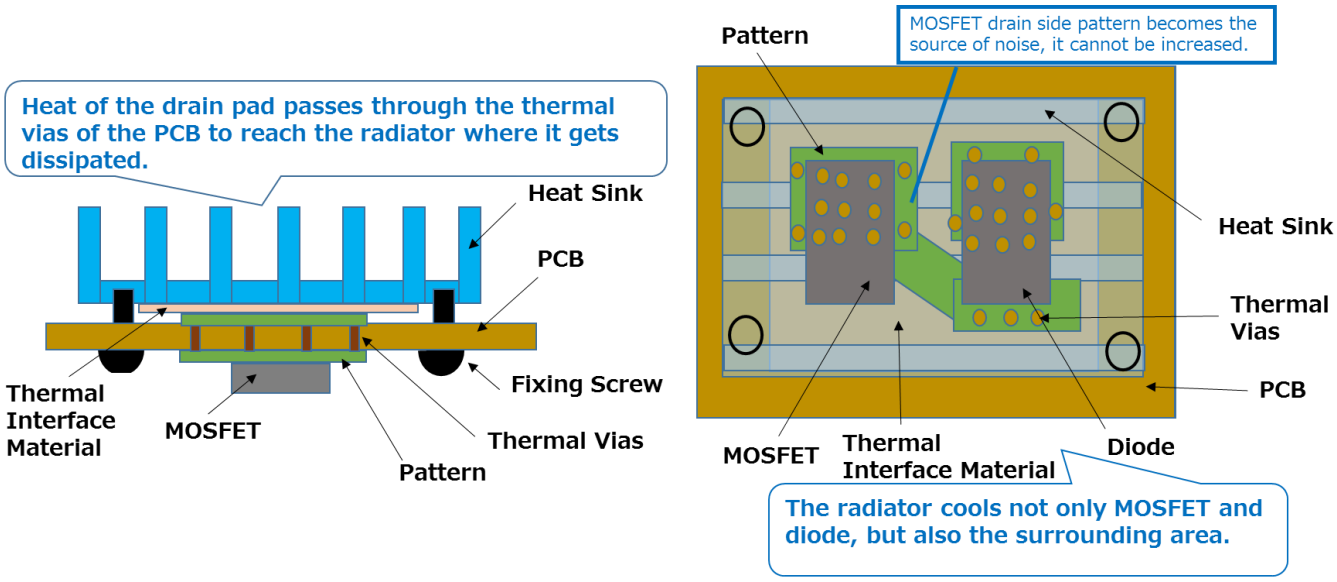

Fig. 3.2 TOLL Package Mounting Diagram

Comparison of Heat Sinks for TO-220SIS and TOLL Package

Fig. 3.3 shows a thermal simulation model of a TO-220SIS package product, TK090A65Z, and TOLL package product, TK090U65Z. As shown in Fig. 3.4, a heat sink is attached to the package model, and the chip temperature is confirmed by simulation (natural air cooling) by changing the heat sink size. Based on this result, the thermal resistance from the chip to the surrounding area (@Ta=25°C) according to the heat sink size is calculated and shown in Fig. 3.5.
Fig. 3.5 shows that TOLL packaging can reduce the overall thermal resistance including that of the heat sink compared to TO-220SIS, thus contributing to a reduction in the size of the heat sink.

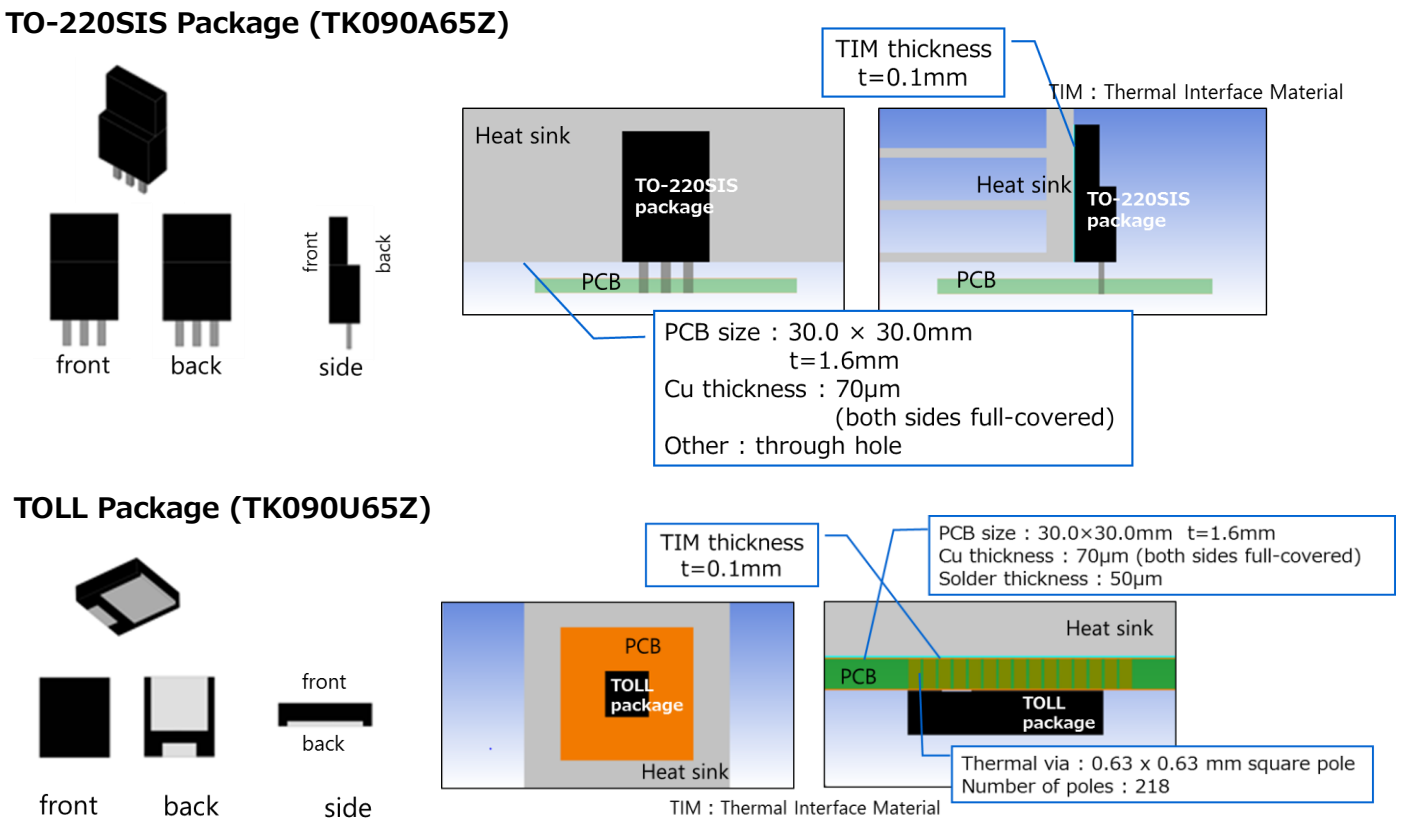

Fig. 3.3 TO220SIS and TOLL Package Thermal Simulation Models

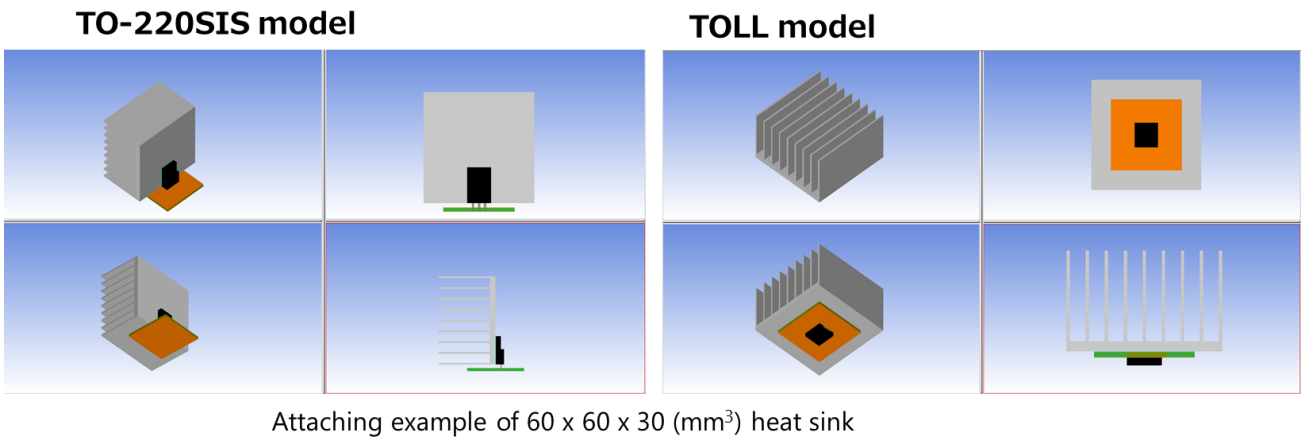

Fig.3.4 TO220SIS and TOLL Package Simulated Heat Sink Model

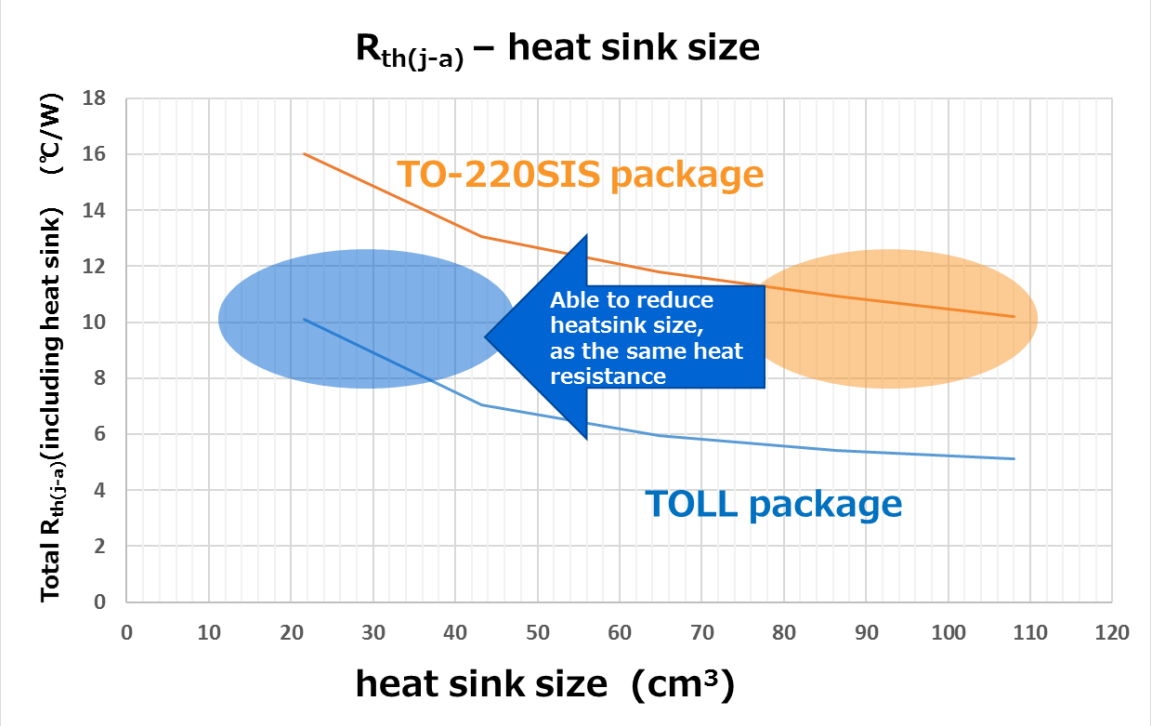

Fig. 3.5 Thermal Resistance Comparison

Miniaturization of Power Supply by Adopting TOLL Package (in PFC circuitry)

The use of TOLL package has reduced the size of the heat sink, which is a large component, and with the increased flexibility of arranging other components, the area of the power supply board has been reduced. (Fig. 3.5 shows the reduction of board area by 20%.)

NOTE) The power supply using TO-220IS was designed previously.

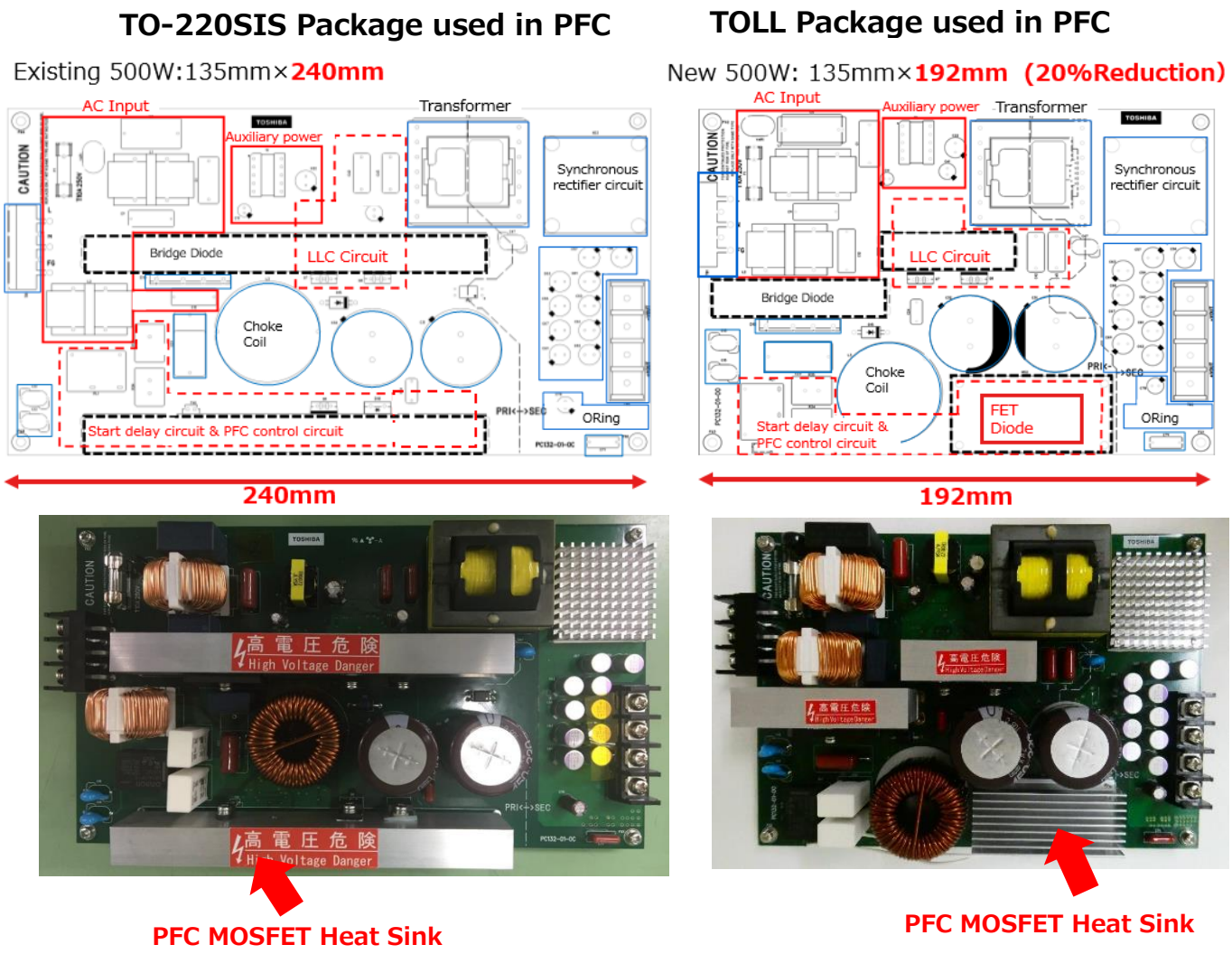

Fig. 3.6 Reduction of Board Area by 20%

Simulated Temperature Comparison of MOSFET for PFC

Fig. 3.6 shows the comparison of temperature simulation of the power supply using TO-220SIS package PFC MOSFET and of the power supply that is miniaturized by adopting TOLL package PFC MOSFET. The heat sink and board of power supply with TOLL package are miniaturized as shown in Fig. 3.5, and the temperature of MOSFET is lower than that of the power supply using TO-220SIS.

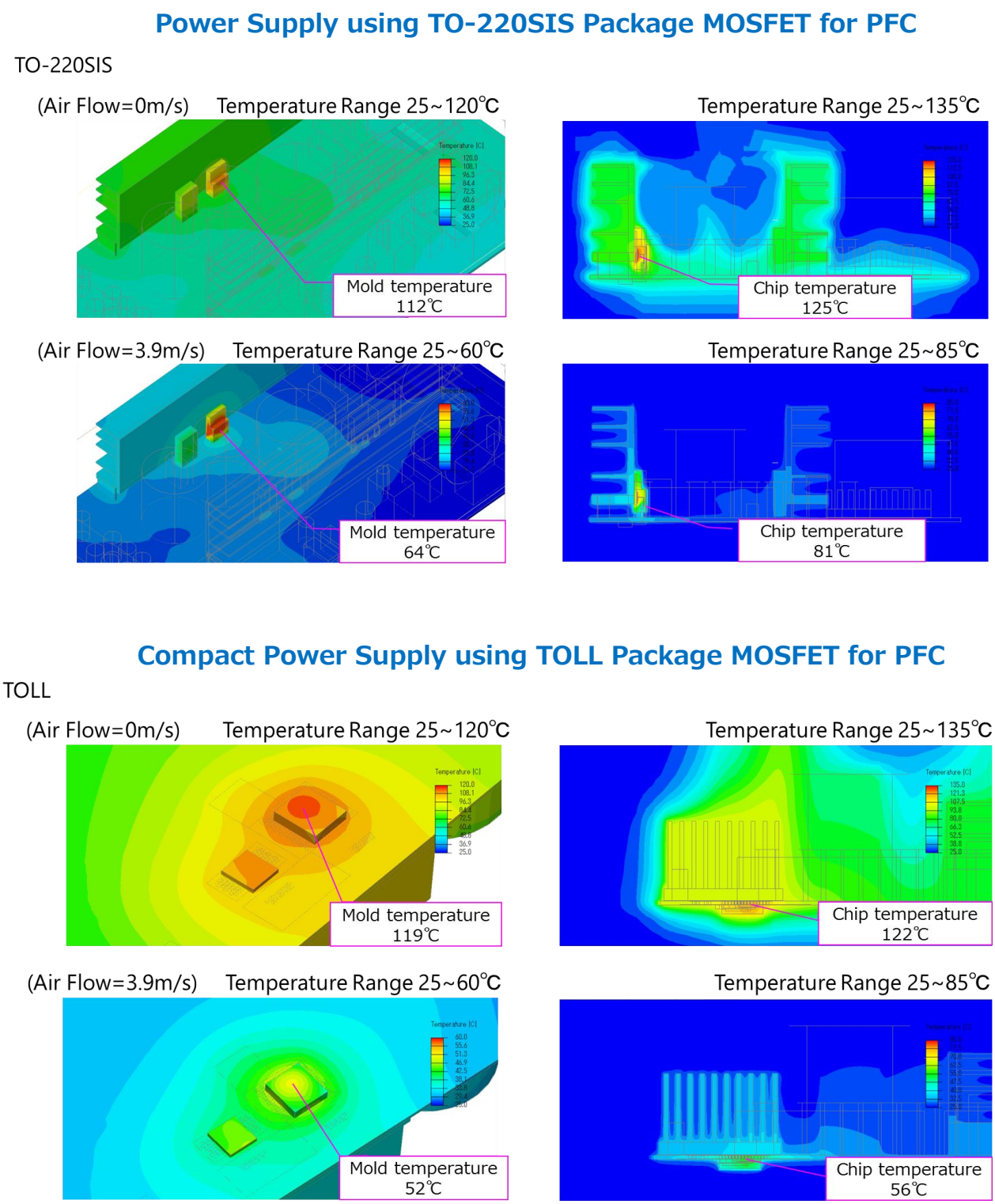

Fig. 3.7 Temperature Comparison of TO-220IS and TOLL Package

[Note]

・Thermal simulations are carried out by using the designed power of each device.

・The data of air flow speed 3.9 m/s is shown, however the wind speed is calculated from the catalogue value of the fan using the reference model. Fig. 3.7 shows the direction of the air input to the power supply.

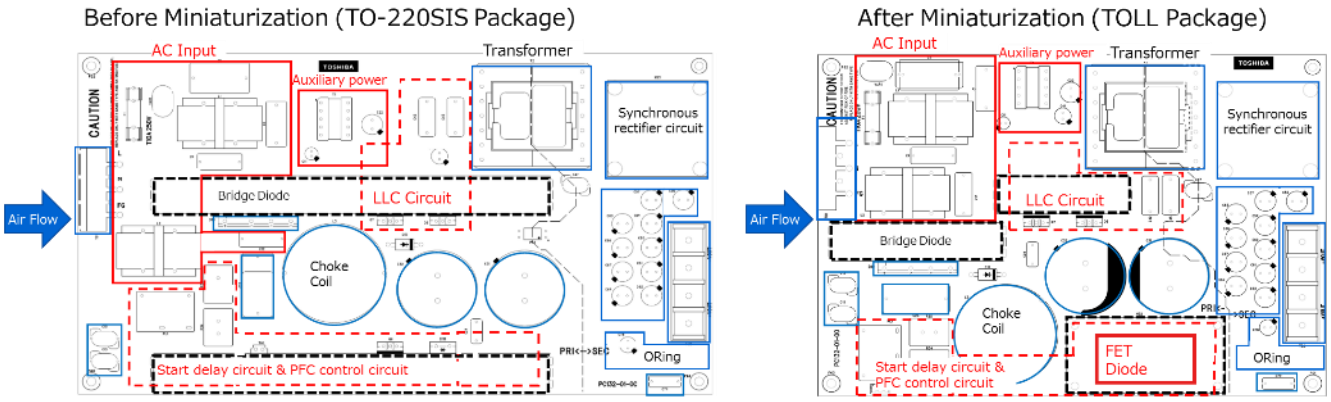

Fig. 3.8 Air Flow Direction of Power Supply

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