200 W Active Clamp Forward DC-DC Converter

Design Guide

RD175-DGUIDE-01

TOSHIBA ELECTRONIC DEVICES & STORAGE CORPORATION

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1. Introduction

This Design Guide provides instructions on how to design the various circuits and layout of the 200 W Active Clamp Forward DC-DC Converter (hereafter referred to as the Power Supply). Refer to the reference guide for the specifications, usage, and characteristic data of this power supply.

If a component is indicated as "Not Mounted" in the bill of materials, then it is not mounted on the PCB even if its part number is indicated in the circuit diagram. Mounting locations are provided on the PCB for constant value adjustment at the time of circuit design.

1.1. Onboard Power MOSFET

TPH3300CNH

Mounted on primary side main switch section.

V_{DSS} = 150 V, $R_{DS(ON)}$ (Max) = 33 mΩ@V_{GS} = 10 V, SOP Advance package

U-MOSVIII-H process product suitable for switching applications with reduced switching loss.

TPN5900CNH

Mounted on primary side clamp switch section.

V_{DSS} = 150 V, $R_{DS(ON)}$ (Max) = 59 mΩ@V_{GS} = 10 V, TSON Advance package

U-MOSVIII-H process product suitable for switching applications.

Its small capacitance reduces drive losses.

TPH9R00CQH

Mounted on secondary synchronous rectifier section

V_{DSS} = 150 V, $R_{DS(ON)}$ (Max) = 9.0 mΩ@V_{GS} = 10 V, SOP Advance package

Latest U-MOSX-H process product with low on-resistance to reduce continuity loss.

2. Circuit Design

This section describes the circuit design of this power supply.

2.1. Active Clamp Circuit Design

This power supply is a 200 W /24 V power supply of the active clamp type forward converter. The active clamping method alternately turns on/off the main switching MOSFET and clamping MOSFET on the input side. The on Duty is adjusted according to the load to control the output voltage. A magnetic reset circuit, which is usually one of the causes of loss in the forward power supply, can be realized without loss in an active circuit, thereby reducing loss and realizing a high-efficiency power supply. This power supply uses Texas Instruments's controller LM5025CMTC (hereinafter referred to as "active clamp controller") to achieve active clamping method. Fig. 2.1 shows the peripheral circuit of the active clamp controller and explains the basic design method. For detailed designs of the peripherals, refer to LM5025CMTC datasheet and related documents.

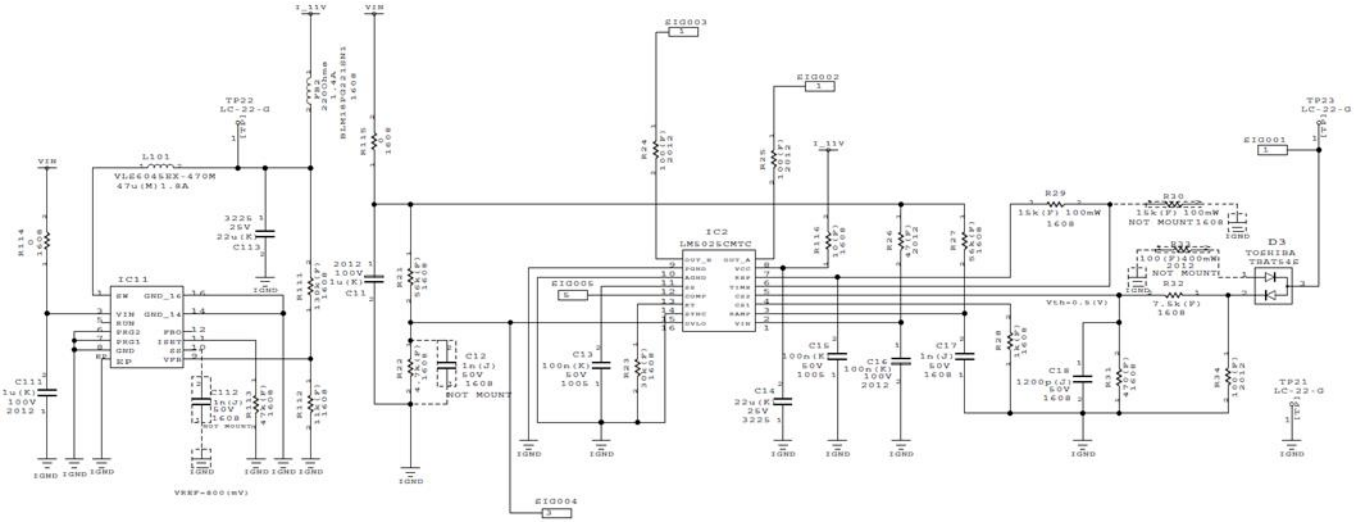

Fig. 2.1 Active Clamp Controller Peripheral Circuit

Input Voltage Operating Range Setting

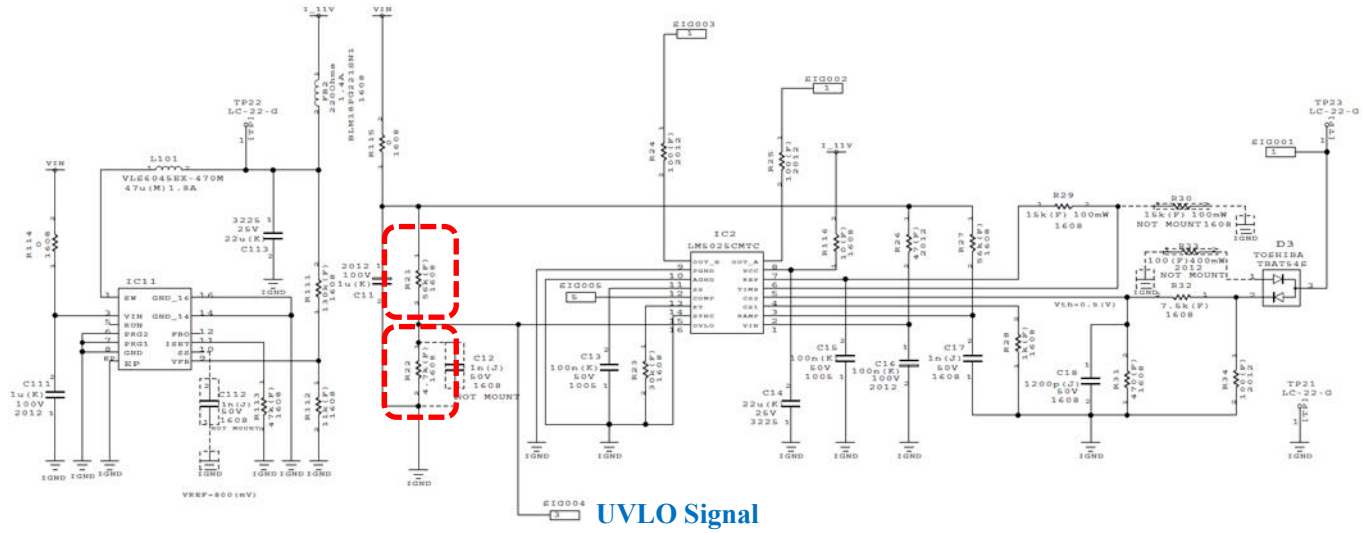

Fig. 2.2 Normal UVLO Circuit

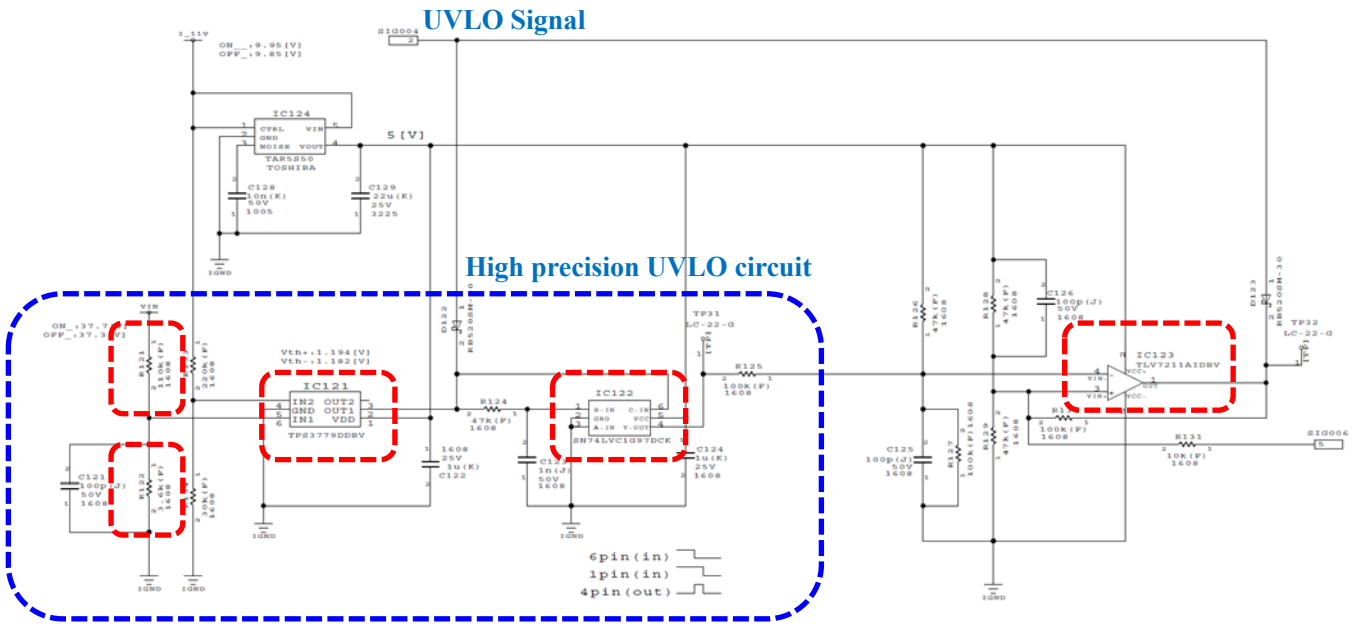

Fig. 2.3 High Precision UVLO Circuit

Fig. 2.2 and Fig. 2.3 show the power supply operation lower limit setting circuit (UVLO circuit). The active clamp circuit operates using the external DC power supply voltage as the input power supply. The active clamp controller detects the voltage at UVLO terminal and starts operation. In the normal UVLO circuit (Fig. 2.2), a signal obtained by dividing the external DC power supply voltage by resistors is input to UVLO terminal. However, in this power supply, a high precision UVLO circuit (Fig. 2.3) that controls the voltage at UVLO terminal is added in addition to the normal UVLO circuit to detect the power supply voltage with higher accuracy.

The operating voltage of the active clamp controller is set by an external high precision UVLO circuit. The threshold value of UVLO is set by the resistance value of the external resistor (R121, R122). The operating voltage range ($V_{in\_min\_on}$, $V_{in\_min\_off}$) of the active clamp circuit is set by dividing the external DC power supply voltage Vin by a resistor (R121, R122) and inputting it to IN1 pin of the voltage detection IC (IC121). When IN1 pin voltage of the voltage detection IC (IC121) exceeds the threshold voltage (1.194 V), the active clamp controller starts switching operation and stops switching operation when it falls below the operation stop threshold voltage (1.182 V). The operating voltage lower limit ($V_{in\_min\_on}$, $V_{in\_min\_off}$) is calculated using the following equation.

$$V_{in\_min\_on}(V) = \ 1.194 \ V \times \frac{(R121 + R122)}{R122}$$

$$V_{in\_min\_off}(V) = 1.182 \ V \times \frac{(R121 + R122)}{R122}$$

Assuming that the setting value of the DC power supply voltage $V_{in\_min\_on}$ at which the active clamp circuit starts operation is 37.7 V and the setting value of the DC power supply voltage $V_{in\_min\_off}$ at which the active clamp circuit stops operation is 37.3 V, 110 kΩ is selected for the resistor (R121) and 3.6 kΩ for the resistor (R122) as shown in Fig. 2.3. In order to prioritize the operation of the high precision UVLO circuit in this power supply, the threshold value of the normal UVLO circuit should be set lower than the threshold value of the high precision UVLO. Assuming that the operating voltage of the normal UVLO circuit is 31.2 V, 56 kΩ is selected for the resistor (R21) and 4.7 kΩ for the resistor (R22) as shown in Fig. 2.2.

In external high precision UVLO circuit, after IC121, IC122, IC123 causes the DC power supply voltage to drop below $V_{in\_min\_off}$, UVLO is activated and switching stops, a latch-off function is provided to prevent the switching operation from restarting again even if the DC power supply voltage temporarily rises due to load derating. Fig. 2.4 shows the relation between the input-voltage (V_{in}), the main signals of the high precision UVLO circuit, and the switching operation status. If high precision UVLO is not required, remove the part in blue dotted line in Fig. 2.3. If this happens, the thresholds of the normal UVLO circuit must be adjusted with resistors (R21) and resistors (R22).

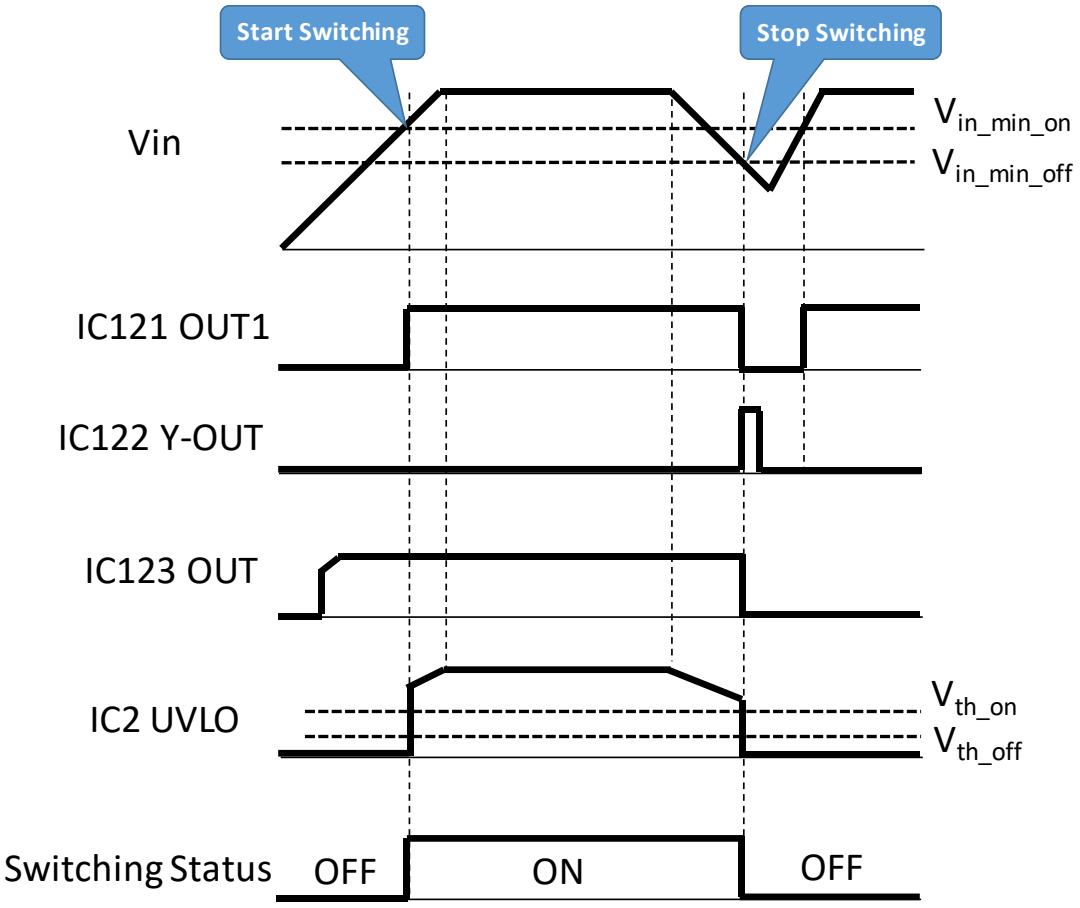

Fig. 2.4 High precision UVLO circuit and switching operation status

Output Voltage Setting

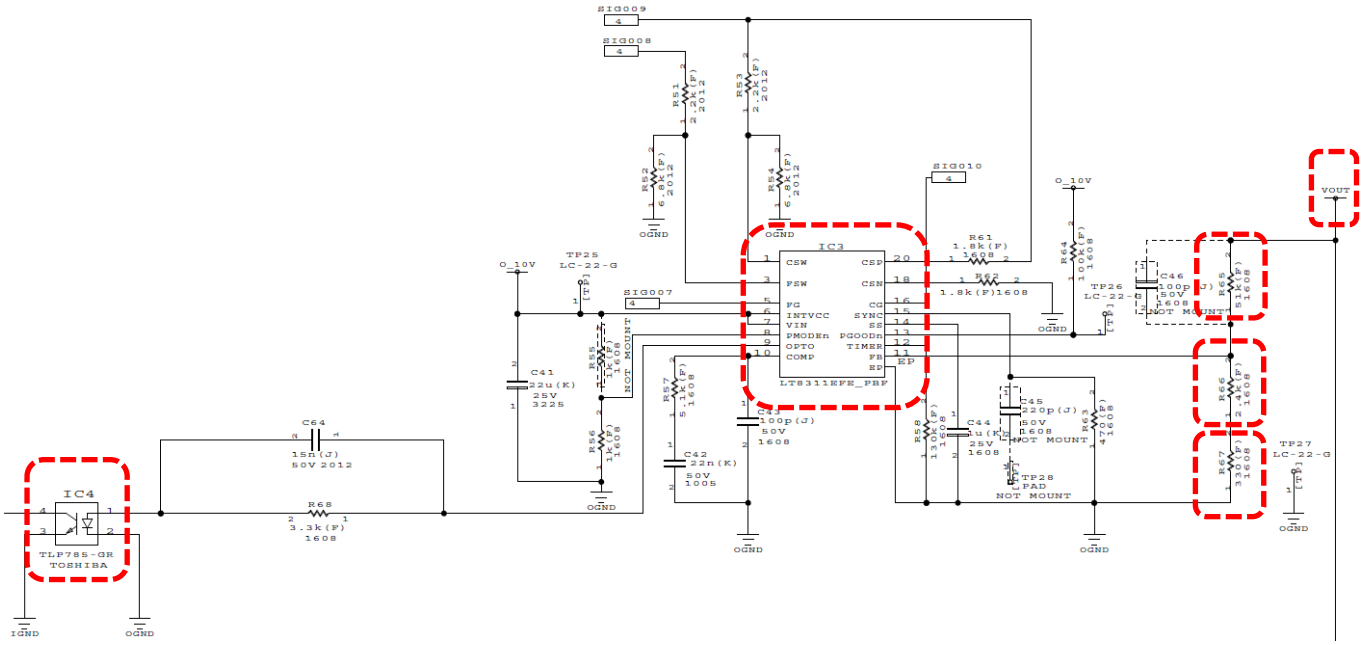

Fig. 2.5 Output Voltage Setting Circuit

Fig. 2.5 shows the output voltage setting circuit. The output-voltage (V_{out}) of this power supply is set using external resistors (R65, R66, R67). The synchronous rectifier controller (LT8311EFE) controls the current of the photocoupler (IC4) so that the voltage obtained by dividing the output voltage of this power supply by the resistors (R65, R66, R67) matches the internal feedback reference voltage Vref_ACF (1.227 V). The active clamp controller operates to maintain a constant output-voltage (V_{out}) depending on the amount of current fed back from the photocoupler (IC4). The Output voltage (V_{out}) is calculated using the following equation.

$$V_{out} = \frac{Vref\_ACF \times (R65 + R66 + R67)}{(R66 + R67)} + Ibias\_ACF \times R65$$

The output-voltage (V_{out}) is set to 24.16 V, with a resistance (R65) of 51 kΩ, a resistance (R66) of 2.4 kΩ, and a resistance (R67) of 330 kΩ.

Switching Frequency Setting

The switching frequency (f_{PWM}) of the active clamp circuit is set using the resistance of the external resistor (R23). The external resistor (R23) is calculated using the following equation.

$$R23(k\Omega) = \left(\frac{6002}{f_{PWM}(kHz)}\right)^{1.0192}$$

In this power supply, the switching frequency (f_{PWM}) is set to 213 kHz; therefore (R23) is selected to be 30 kΩ as shown in Fig. 2.6.

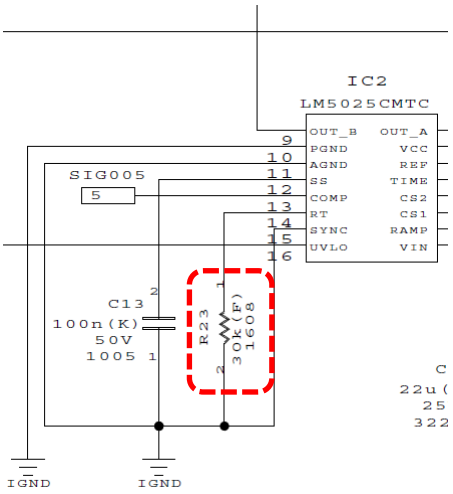

Fig. 2.6 Switching Frequency Setting Circuit

Soft Start Setting

Fig. 2.7 shows the soft start setting circuit. The soft-start time of the active clamp power supply is set by the external capacitor (C44) of the synchronous rectifier controller. The soft start time (Tss) is calculated as follows:

$$Tss = \frac{C44 \times Vref\_ACF}{10\mu A}$$

For this power supply, the maximum soft start time (Tss) is set to 123 ms, and therefore 1 μF is selected for the external capacitor (C44). Soft start time can be adjusted by changing the capacitance as necessary.

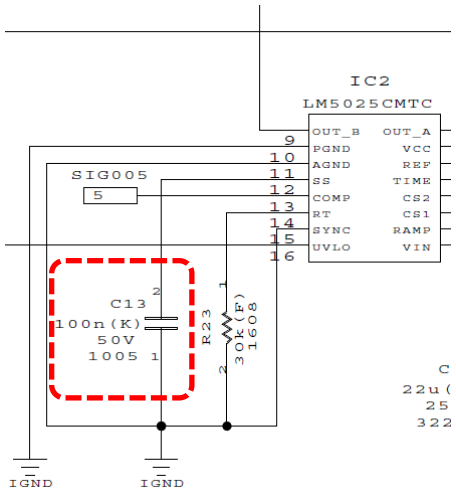

Fig. 2.7 Soft Start Setting Circuit

Gate Drive Circuit

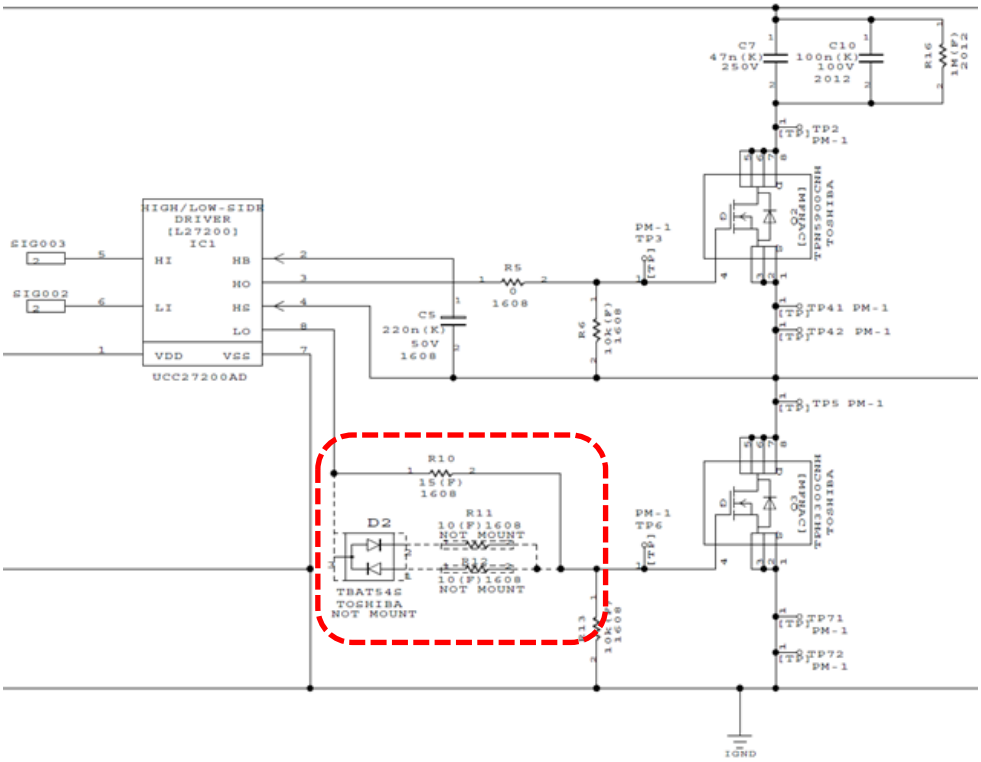

Fig. 2.8 Gate Drive Circuit

Fig. 2.8 shows the gate drive circuit. The design of the gate drive circuit affects power supply efficiency and EMI. Generally, there is a trade-off between power supply efficiency and EMI, and a balanced design is required for both. The active clamping circuit is low EMI, but if switching noise seems to cause EMI problems, adjust the values of the gate series resistors (R10, R11, R12) and check again. The gate drive allows individual adjustments of MOSFET turn-on and turn-off speeds. If EMIs (noises) occur both when MOSFET (Q3) is turned on and turned off, increase the resistor (R10). This reduces turn-on and turn-off speeds at the same time, and thus reducing EMI (noise). If EMI (noise) occurs only when MOSFET is turned on or turned off, increase resistor (R11) or resistor (R12). This allows the reduction of either turn-on speed or turn-off speed only, and thus reducing EMI (noise). Note that increasing the resistors (R10, R11, R12) will reduce the switching speed of MOSFET, which may also reduce the power-supply efficiency. Check that the power supply efficiency specification and heat dissipation specification satisfy the required specification.

Transformer

The number of turns of the transformer is calculated by setting the on-duty of the main switching MOSFET at 45 % in the steady-state of the active clamping circuit. Assuming that the number of windings on primary side of Transformer as Np, and on secondary side as Ns, and the sum of voltage drop across winding resistance of transformer and the secondary side rectifier circuit is 2 V, then the turn ratio (Ns/Np) of Transformer is calculated as follows:

$$\frac{Ns}{Np} = \frac{V_{out} + 2\ V}{V_{in} \times 0.45}$$

If the input voltage (V_{in}) is 48 V and the output voltage (V_{out}) is 24.2 V, then the turn ratio (Ns/Np) of the transformer (T1) is 1.21, so 7:9 is selected as the number of turns. In addition, since 9 V is required for the secondary auxiliary power supply, assuming that the number of turns of the auxiliary winding is Ns', the ratio of turns (Ns'/Np) of the transformer is calculated as follows.

$$\frac{Ns'}{Np} = \frac{9\ V}{V_{in} \times 0.45}$$

If the input voltage (V_{in}) is 48 V, Ns' is 2.91 because Np is 7. Therefore, 3 is selected as the number of turns Ns'. As a result, the number of turns of the transformer used is 7:9:3.
This results in a square wave of 61.7 V on the secondary side. In addition, primary-secondary dielectric strength, winding temperature rise, magnetic flux saturation, core loss, etc. must be considered sufficiently. Refer to the Bill of Materials (RD175-BOM-01) for the specifications of the transformer used in this power supply. In addition, this power supply uses the leakage inductance of the transformer to perform active clamping operation. If the resonance due to the leakage inductance is insufficient, problems such as decrease in power supply efficiency and increase in EMI may occur.

Output Capacitor

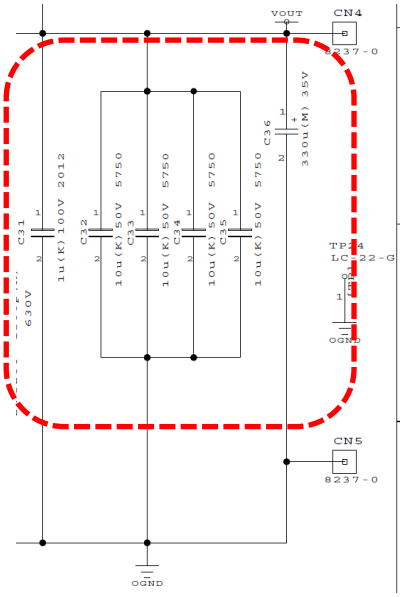

Fig. 2.9 Output Capacitor-Peripheral Circuit

Set the output capacitor (C_{out}) so that the output ripple voltage (V_{ripple}) falls within the required range. The output ripple voltage (V_{ripple}) is the combination of following ripple voltages.

1. Ripple voltage (V_{ripple_ESR}) generated by the ripple current (ΔI) and the equivalent series resistance (ESR) of the output capacitor.
2. Ripple voltage (V_{ripple_Cap}) generated by the ripple current (ΔI), the capacitance (C_{out}) of the output capacitor, and switching frequency (f_{PWM}).
3. Ripple voltage (V_{ripple_ESL}) generated by the switching voltage (V_{SW}), the equivalent series inductance value (ESL) of the output capacitor, and inductance (L) of the inductor.

For simplicity, assume that the above ripple occurs only with a large-capacity aluminum polymer capacitor (C36), and calculate the ripple voltage as shown in the following equation.

$$V_{ripple\_ESR}(V) = \Delta I \times ESR$$

$$V_{ripple\_Cap}(V) = \frac{\Delta I}{8 \times C_{out} \times f_{PWM}}$$

$$V_{ripple\_ESL}(V) = \frac{V_{SW} \times ESL}{L}$$

Here,

$$\Delta I(A) = \frac{(V_{SW} - V_{out}) \times V_{out}}{V_{SW} \times f_{PWM} \times L}$$

If the switching voltage (V_{SW}) is 61.7 V, the output voltage (V_{out}) is 24.16 V, the switching frequency (f_{PWM}) is 213 kHz, and the duty (L) is 47 μH, the ripple current (ΔI) is 1.47 A.

If the equivalent series resistance (ESR) is 16 mΩ (16 mΩ @ 100 kHz), the capacitance (C_{out}) of the output capacitor is 330.0 μF (330 μF x 1 pcs @ 120 Hz), the equivalent series inductance (ESL) of the output capacitor is 6 nH, and the inductance (L) is 47 μH, the ripple voltages that

occur are V_{ripple_ESR} = 23.5 mV, V_{ripple_Cap} = 2.6 mV, and V_{ripple_ESL} = 7.9 mV. The ripple voltage generated by V_{ripple_Cap} cannot be simply added because it is out of phase with V_{ripple_ESR} and V_{ripple_ESL}, but because the ripple voltage generated by V_{ripple_Cap} is small, the simplified sum can be used as a reference for the output voltage ripple.

The output capacitors (C_{OUT}), (ESR), and (ESL) needs to be adjusted so that the output voltage ripple (V_{ripple}) satisfies the required specifications. And, following points must also be considered:

1. The output terminal undershoot and overshoot which occur when the load changes suddenly is within the specified voltage range.
2. The allowable ripple current of the output capacitor is ensured.
3. Tolerances and aging of output capacitors are considered.

Synchronous Rectifier MOSFET Surge Voltage Reduction Circuit

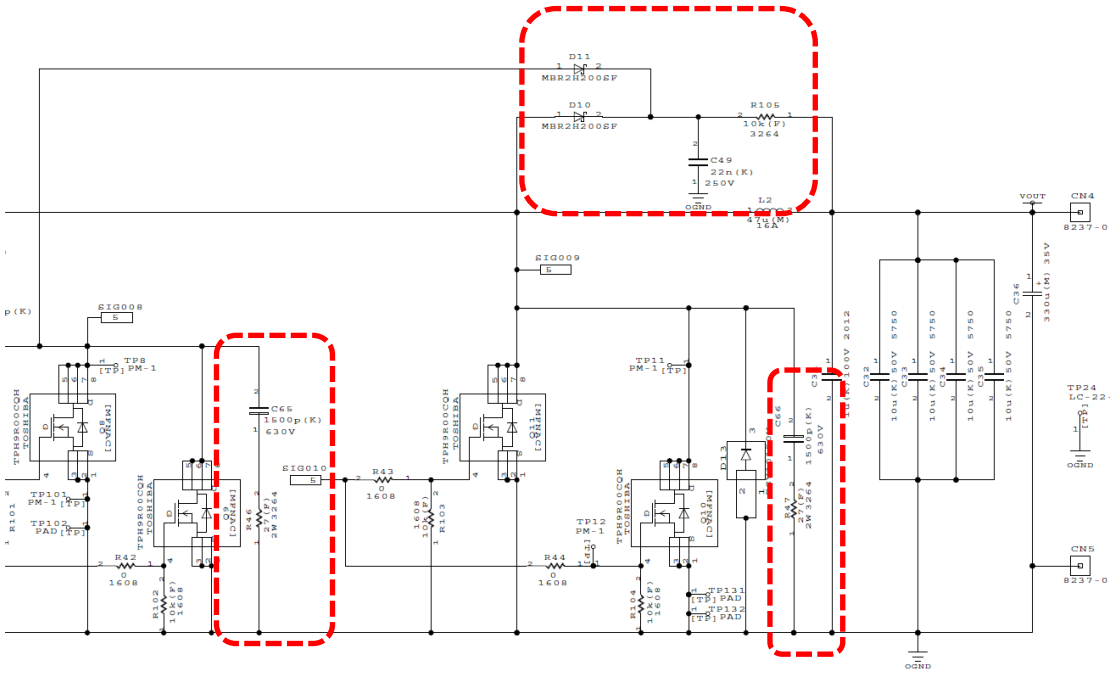

Fig. 2.10 Snubber Circuit

Fig. 2.10 shows the Snubber circuit. The resistor (R46) and capacitor (C65), resistor (R47) and capacitor (C66) constitute RC Snubber circuit, and the diode (D10, D11), resistor (R105) and capacitor (C49) constitute RCD Snubber circuit. Both Snubber circuit absorb surge voltage (V_{srg}) generated in the FETs (Q8-Q11). At this time, the loss (P_{d_Rsnb1}) generated by the resistor (R46) depends on the rise of the surge voltage, but assuming that it is 30% of the loss when a square-wave voltage is generated in the main power supply, the following results are obtained.

$$P_{d\_Rsnb1} = C65 \times (V_{srg})^2 \times (f_{PWM}) \times 30\% = 0.78\ W$$

If the surge voltage (V_{srg}) is 90 V, the resistor (R46) is 27 Ω, the capacitor (C65) is 1500 pF, and the (f_{PWM}) is 213 kHz, the loss (P_{d_Rsnb1}) generated by the resistor (R46) is 0.78 W. Value and rating of each element needs to be adjusted according to the actual surge voltage level.

The loss (P_{d_Rsnb2}) generated by the resistor (R105) is as follows.

$$P_{d\_Rsnb2} = \left(\frac{V_{srg} - V_{out}}{R105}\right)^2 = 0.43\ W$$

If the (V_{out}) is 24.16 V, the surge voltage (V_{srg}) is 90 V, and the resistance (R105) is 10 kΩ, the loss (P_{d_Rsnb2}) generated by the resistance (R105) is 0.43 W. Value and rating of each element needs to be adjusted according to the actual surge voltage level.

Output Overvoltage Detection Circuit

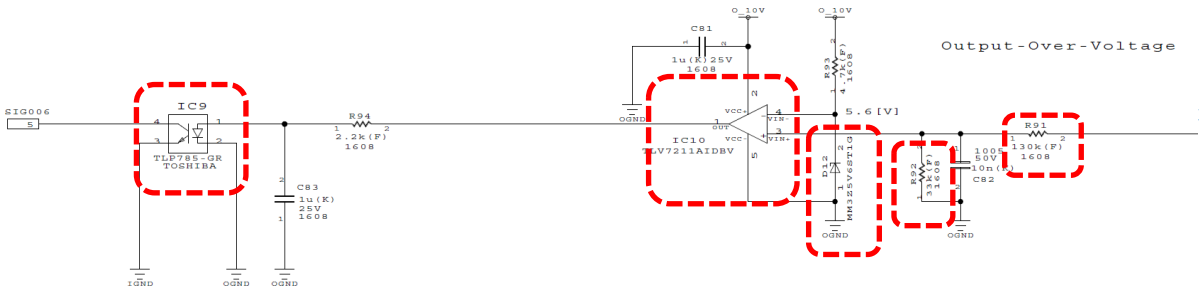

Fig. 2.11 Output Overvoltage Detection Circuit

The overvoltage detection value (V_{ovp}) of the output is set using the comparator (TLV7211A), zener diode (MM3Z5V6S), and external resistors (R91, R92). When the output voltage reaches the overvoltage detection value (V_{ovp}), the photocoupler (IC9) is activated to latch UVLO pin of the active clamp controller to LOW, and thus stopping the switching operation. Using the zener voltage of the zener diode as (V_{Zener}), the output overvoltage detection value (V_{ovp}) is calculated using the following equation.

$$V_{ovp} = \frac{R91 + R92}{R92} \times V_{Zener}$$

In this power supply, the overvoltage detection value (V_{ovp}) is set to 27.7 V, by selecting 130 kΩ for R91 and 33 kΩ for R92 as shown in Fig. 2.11. To restart the switching operation stopped by overvoltage detection, it is necessary to either shut off the input power and input it again, or perform the power-off/on control using Enable pin.

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