Power Multiplexer Circuit

Design Guide

RD221-DGUIDE-02

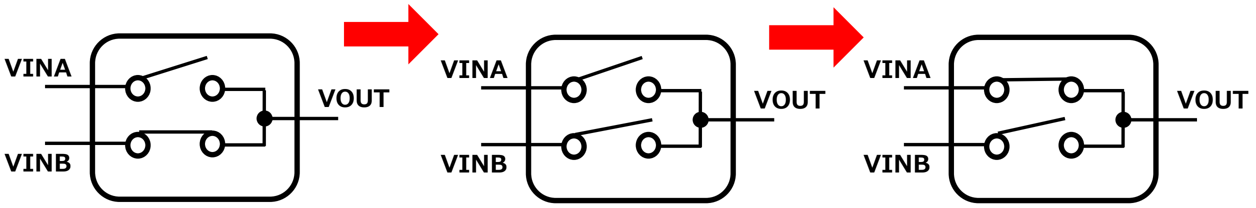
TOSHIBA ELECTRONIC DEVICES & STORAGE CORPORATION

Table of Contents

1. Introduction

This Design Guide provides an overview of the power multiplexer circuit design, PCB design, and product usage.

Demand for power multiplexer circuits used for switching and supply power from multiple sources such as USB terminal, a non-contact power supply terminal, and a built-in battery such as a lithium-ion battery is increasing in consumer applications such as mobile devices like smartphones, PCs, tablets, and wearable devices as well as game devices and charging devices for various types of batteries. In addition, high-current battery recharging, such as USB Power Delivery and quick recharging, requires a low-loss MOSFET to provide power. In addition, it is necessary to prevent reverse current flow to the input side when switching the power supply source and seamlessly switch the output voltage (ideal diode characteristic). This requires a BBM (Break-Before-Make) or MBB (Make-Before-Break) operation to achieve these characteristics.

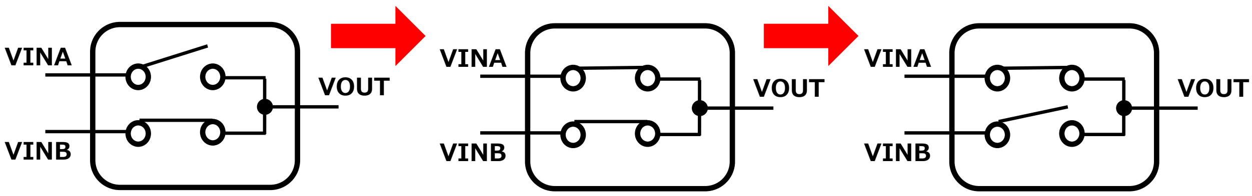


① Status before switching: VINB and VOUT are connected.

② Status during switching: VINB and VINA are disconnected from VOUT

③ Status after switching: VINA and VOUT are connected.

Fig. 1.1 BBM (Break-Before-Make)



①Status before switching: VINB and VOUT are connected.

② Status during switching: VINB and VINA are connected to VOUT

③ Status after switching: VINA and VOUT are connected.

Fig. 1.2 MBB (Make-Before-Break)

2. Specifications and Block Diagram

2.1. Specifications

Table 2.1 and Table 2.2 list the main specifications of this circuit.

Table 2.1 Module Board Specifications

Board Name	Board Type	Input Voltage VINA/VINB	Maximum Output Current *	BBM Operation Support	MBB Operation Support	Switching Element		For Output MOSFET
MUX1	Standard 1	20 V 5 V	3 A	Yes	Yes	Gate Driver IC	TCK421G TCK425G	TPHR6503PL1
MUX2	Standard 2	12 V 5 V	3 A	Yes	Yes	Gate Driver IC	TCK423G TCK425G	TPN1R603PL
MUX3	High Power 1	20 V 9 V	5 A	Yes	Yes	Gate Driver IC	TCK421G TCK424G	TPN1R603PL
MUX4	eFuse IC	12 V 5 V	3 A	Yes	-	eFuse IC	TCKE812NA TCKE712BNL	SSM6K513NU -
MUX5	High Power 2	24 V 12 V	5 A	Yes	Yes	Gate Driver IC	TCK420G TCK422G	TPHR8504PL1

* The product can carry a current exceeding the specified value. However, the board should be used within the range not exceeding the specified value due to heat dissipation design.

Table 2.2 Base Board Specifications

Input	VINA input (VINA 5 to 24 V) VINB input (VINB 5 to 12 V) Drive power supply (VDD 5 to 12 V)
Output	Output load A to D (LOAD-A~LOAD-D, each Load can have both resistive load and capacitive load, Max current 3 A or 5 A depending on module board) FLAG output (H-level (approx. 3.3 V) is output when VINA is input)

2.2. Block Diagram

Fig. 2.1 and Fig. 2.2 show the block diagrams of this circuit.

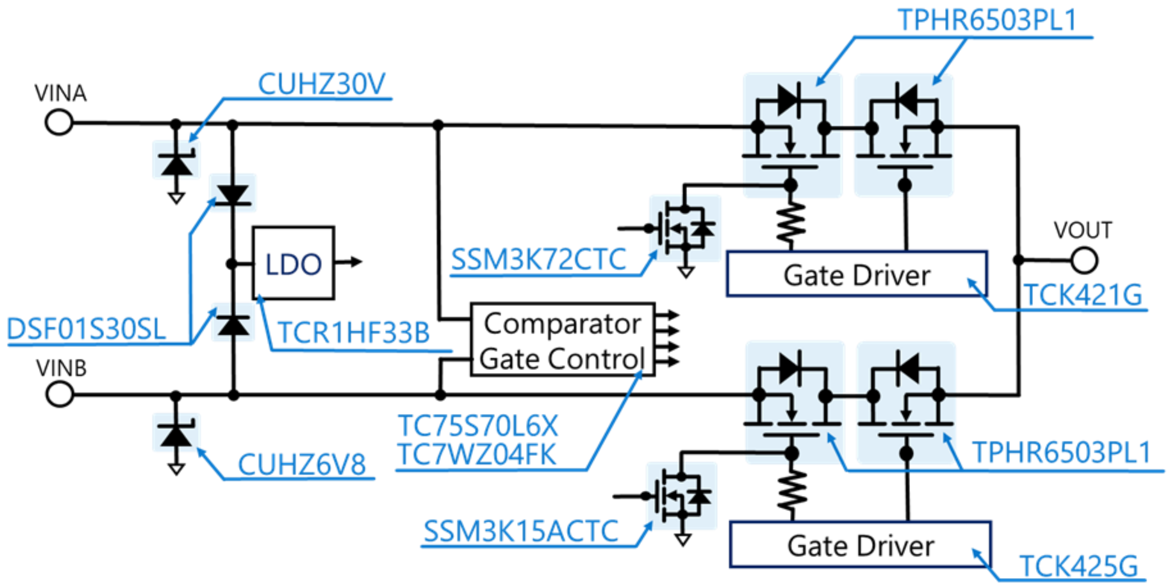


Fig. 2.1 Block Diagram (Module Board – Example MUX1)

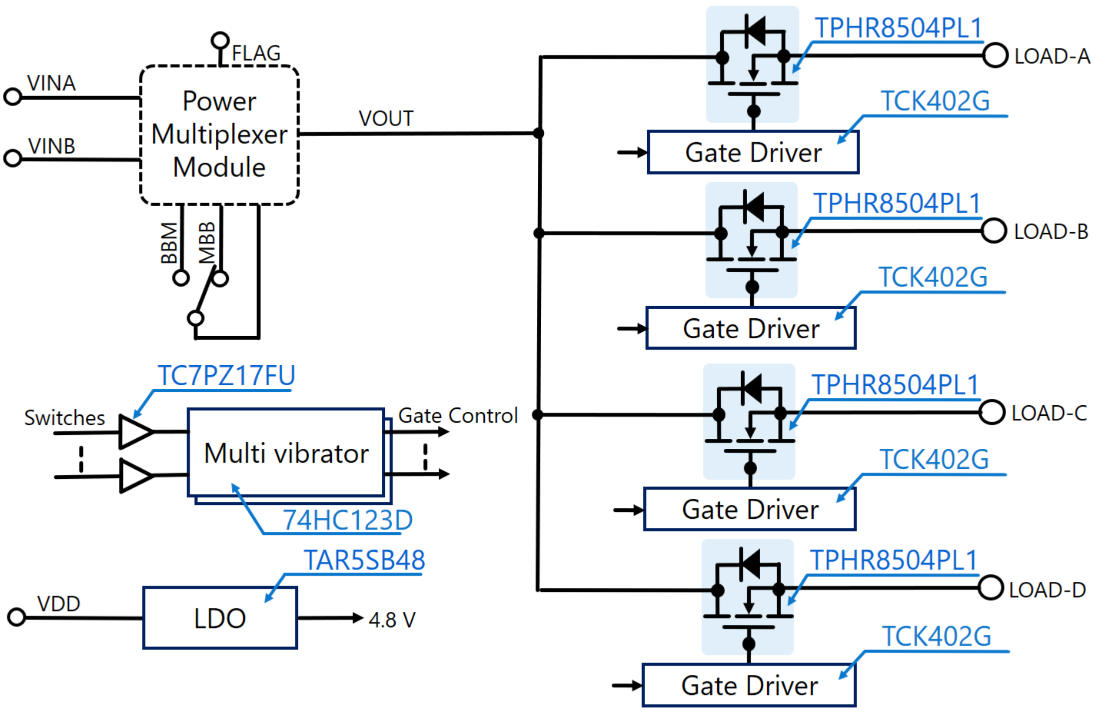


Fig. 2.2 Block Diagram (Base Board)

3. Circuit Design

3.1. Module Board

3.1.1. BBM Operation

Fig. 3.1 shows the waveform when the module board MUX1 is operated in the BBM mode.

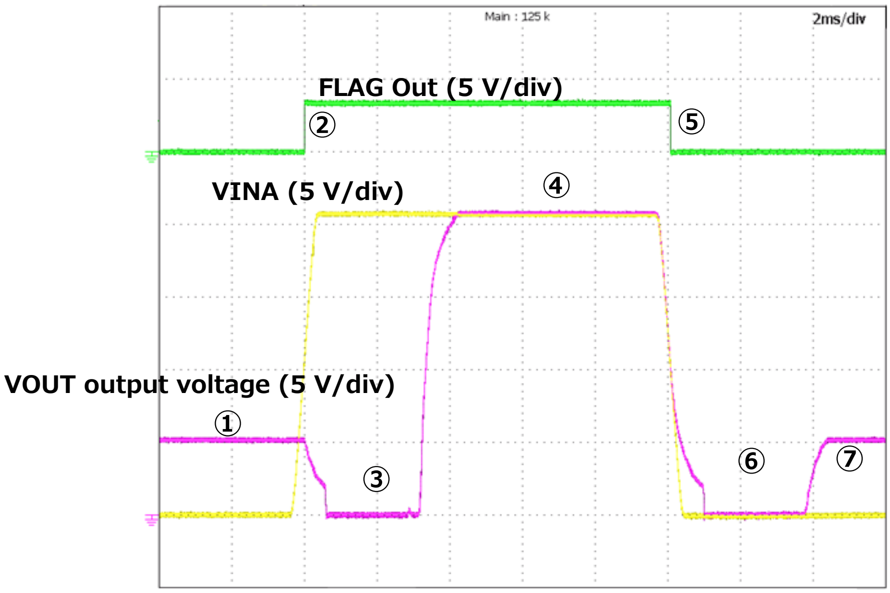


Fig. 3.1 Waveform during BBM Operation (2 ms/div)
VINA = 20 V, VINB = 5 V, RL = 300 Ω, CL = None

VINB is continuously energized with 5 V, and 20 V voltage pulses of 10 ms are applied to VINA. When 20 V is applied to VINA and the output voltage switches from 5 V to 20 V, there is a start-up-time t_{ON} of approximately 3 ms when MOSFET driver IC TCK421G that controls VINA voltage is turned on, and the output voltage during this time is 0 V. Also, when VINA pin becomes 0 V and the output voltage switches from 20 V to 5 V, there is a start-up time t_{ON} of about 3 ms when MOSFET driver IC TCK425G that controls VINB voltage is turned on in the same way, and the output voltage during this time becomes 0 V. FLAG output is High (approx. 3.3 V) while VINA is applied.

Details of each operation in the waveform are as follows.

① 5 V is applied to VINB, and VINB voltage (approx. 5 V) is output.

② When 20 V is applied to VINA, FLAG output becomes High (approx. 3.3 V). VINA driver (TCK421G) starts operating at this timing.

③ 0 V is output because of VINB driver (TCK425G) is off.

④ VINA voltage (about 20 V) is generated after t_{ON} of VINA driver (TCK421G).

⑤ When the voltage at VINA becomes 0 V, FLAG output becomes Low (0 V). VINB driver (TCK425G) starts operating at this timing.

⑥ 0 V is output because VINA driver (TCK421G) is off.

⑦ VINB voltage (approximately 5 V) is output after t_{ON} of VINB driver (TCK425G).

3.1.2. MBB Operation

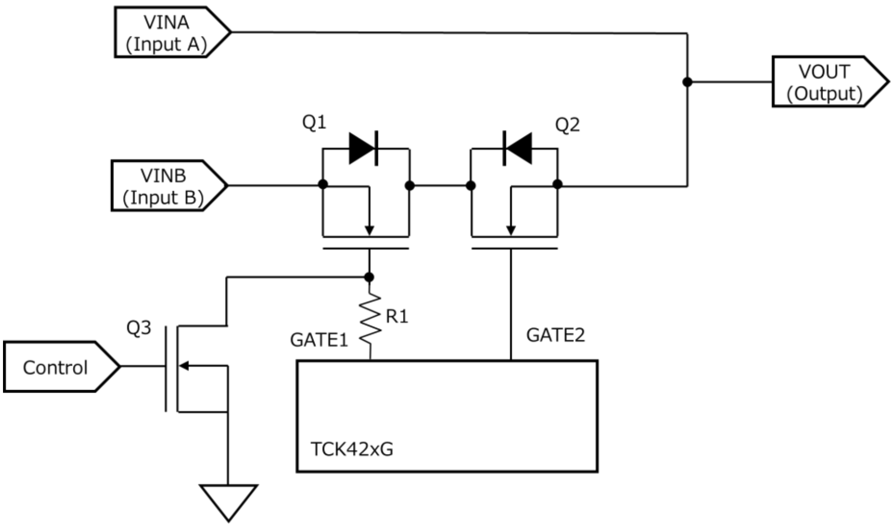


Fig. 3.2 MBB Operation Circuit

The MBB operation outline of this circuit is described below. The MBB operation circuit shown in Fig. 3.2 assumes that VINA voltage > VINB voltage and VINB is continuously energized.

① Apply voltage to VINB (VINA voltage is off). Common drain connected MOSFET Q1 and Q2 are turned on by MOSFET driver IC TCK42xG, and VINB voltage is output to VOUT .

② When VINA is detected, the Gate Shut-off MOSFET Q3 is turned on. This causes the voltage at the gate of MOSFET Q1 to become 0 V and Q1 is turned off. Therefore the voltage dropped by the forward voltage of the body diode of Q1 from VINB voltage is output to VOUT.

③ Even when voltage is applied from VINA, reverse current does not flow to VINB because of the body diode of Q1.

The above operation allows seamless voltage-output switching from VINB to VINA by MBB operation.

In addition, the following operations enable seamless voltage-output switching to VINB from VINA by MBB operation.

① VINA is turned off (0 V) while VINA is being supplied.

② The voltage dropped by the forward voltage of the body diode of Q1 from VINB voltage is output to VOUT.

③ Q3 turns off. Thus Q1 is turned ON. VINB voltage is output to VOUT.

Table 3.1 shows the timing transition table of MBB operation, and Fig. 3.3 shows the timing chart of MBB operation. The operation assumes that VINA voltage > VINB voltage.

Table 3.1 Timing Transitions of MBB Operation (Input VINA Voltage > VINB Voltage)

Time (state)	t1	t2	t3	t4	t5	t6
VINA In	0 V	0 V	ON	ON	0 V	0 V
VINB In	0 V	ON	ON	ON	ON	ON
FLAG Out*	L	L	H	H	L	L
Q1 Gate	OFF	ON	OFF	OFF	OFF	ON
Q2 Gate	OFF	ON	ON	ON	ON	ON
Q3 Gate Shut-off	OFF	OFF	ON	ON	ON	OFF
VOUT	0 V	VINB end	**	VINA end ***	**	VINB end

* H output (approx. 3.3 V) when there is VINA input, and L output (0 V) when there is no VINA input

** The voltage dropped by the forward voltage of the body diode of Q1 from VINB voltage is output to VOUT.

*** VINA voltage is reached after t_{ON} of TCK42xG (about 3 ms). It holds the voltage of the previous timing until then

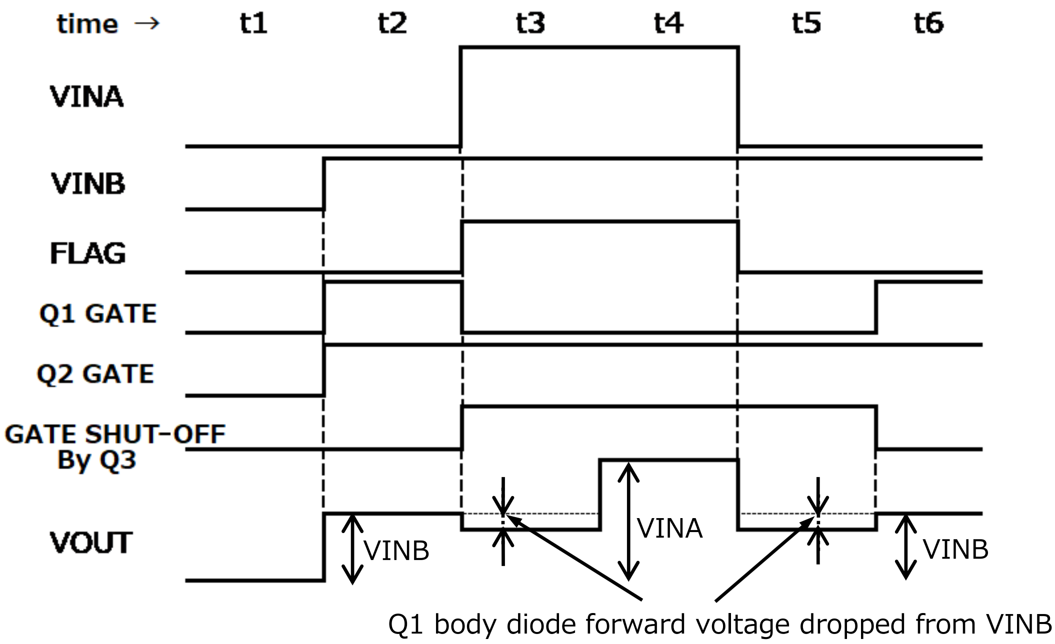


Fig. 3.3 MBB Operation Timing Chart

Fig. 3.4 shows the waveforms during actual MBB operation (of MUX1 as an example).

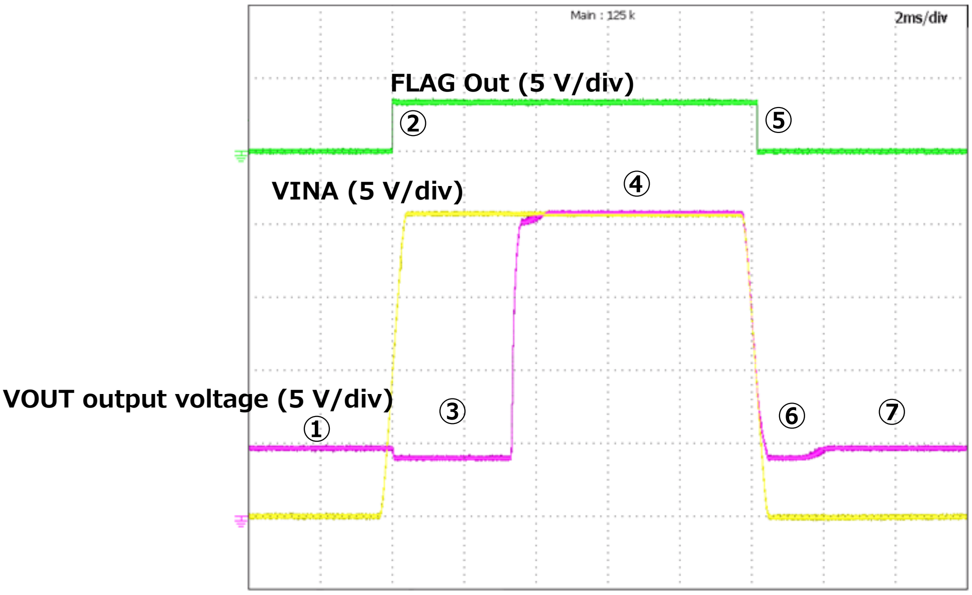


Fig. 3.4 MBB Operation Waveform (2 ms/div)
VINA = 20 V, VINB = 5 V, RL = 300 Ω, CL = None

This section describes the operation of seamlessly switching the voltage without dropping to 0 V when VINB is continuously energized as 5 V and 20 V pulses of 10 ms are applied to VINA.

① 5 V is applied to VINB, and VINB voltage (about 5 V) is sent to the output.

② When 20 V is applied to VINA, the FLAG output becomes High (approx. 3.3 V). And VINA driver (TCK421G) starts operating at this timing.

③ In VINB driver circuit, the gate shut-off MOSFET SSM3K15ACTC corresponding to Q3 in Fig. 3.2 is turned on, and MOSFET TPHR6503PL1 corresponding to Q1 is turned off. During the start-up time t_{ON} after TCK421G is turned on in ② (about 3 ms), the voltage dropped by the forward voltage of the body diode of Q1 from VINB voltage is output to VOUT.

④ VINA voltage (about 20 V) is output after t_{ON} period of TCK421G from the time it turned on in step ③.

⑤ When the applied voltage of VINA becomes 0 V, FLAG output becomes Low (0 V).

⑥ Since VINA voltage became 0 V, the Gate Shut-off MOSFET corresponding to Q3 in Fig. 3.2 is turned off, and TPH6503PL1 corresponding to Q1 starts turn-on operation. During this time, voltage dropped by the forward voltage of the body diode of Q1 from VINB voltage is output to VOUT.

⑦ TPH6503PL1 corresponding to Q1 is turned on. VINB voltage (approx. 5 V) is output.

3.1.3. Circuit for MOSFET Gate Driver IC

MUX1 circuit is shown below as an example circuit for the module board (MUX1, MUX2, MUX3, MUX5) using MOSFET gate driver ICs.

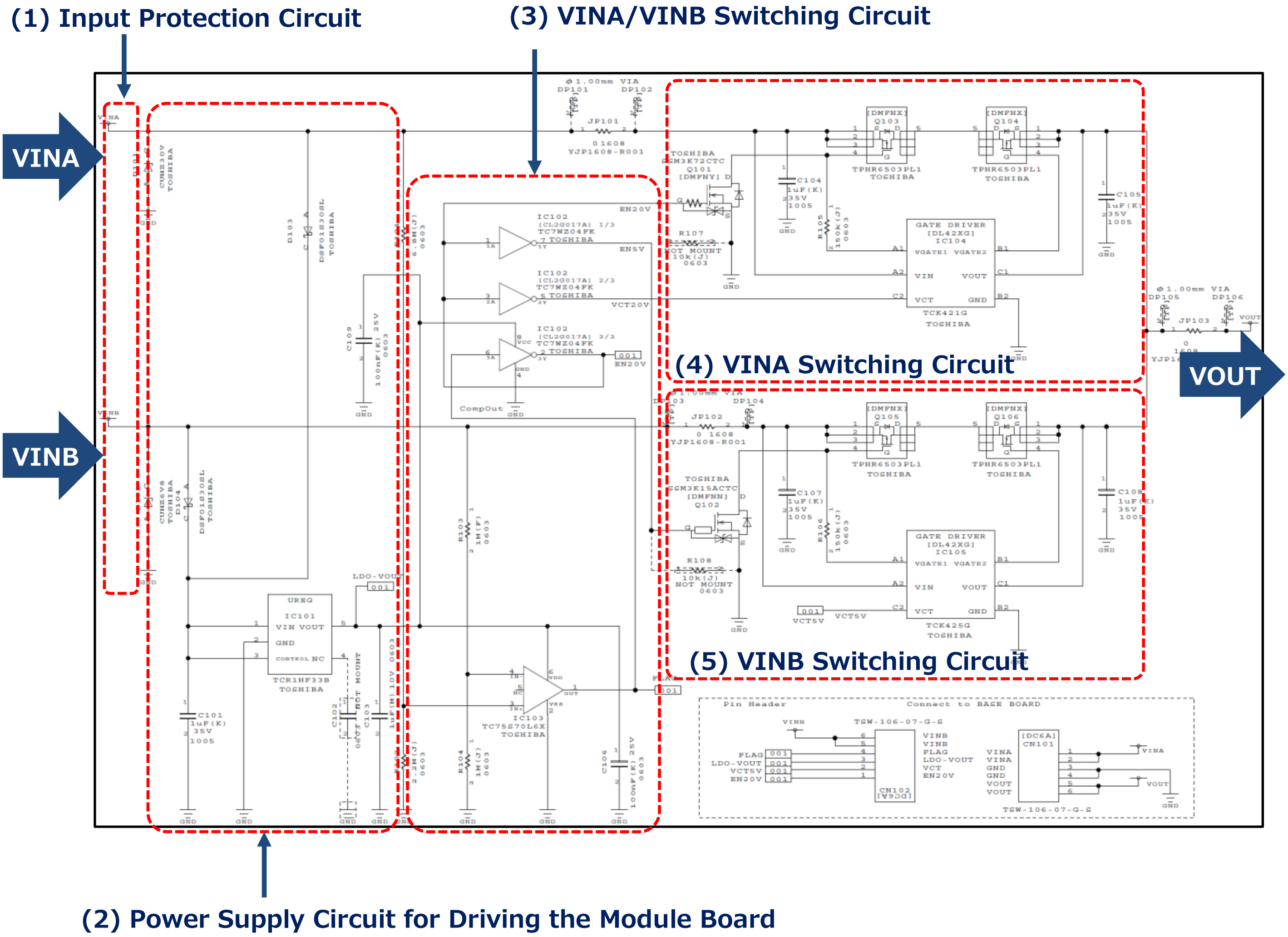


Fig. 3.5 Module Board (MUX1) Circuit

The module board consists of the following circuits:

(1) Input protection circuit

There are two power inputs for the power multiplexer: VINA and VINB, and MUX1 supports 20 V (VINA) and 5 V (VINB) inputs. A zener diode CUHZ30V with a zener voltage of 30 V is used on VINA side and a zener diode CUHZ6V8 with a zener voltage of 6.8 V is used on VINB side to protect the circuit from overvoltage surges, etc. from the input.

(2) Power supply circuit for driving the module board

A 3.3 V output LDO TCR1HF33B is used as the power supply for ICs used in VINA/VINB switching circuit described below. VINA and VINB are connected to the power inputs of the LDOs via Schottky barrier diode DSF01S30SL. If either power supply VINA or VINB is applied, the power supply for driving the module board is supplied.

(3) VINA/VINB switching circuit

A comparator TC75S70L6X is used to detect the voltages of VINA and VINB and to output the H-level (approx. 3.3 V) to FLAG output when the voltage is input to VINA, and a CMOS logic IC TC7WZ04FK is used to generate a switching control signal between VINA and VINB from the output of the comparator.

(4) VINA switching circuit

To switch to the output of VINA power supply (20 V, max. 3 A), two MOSFETs TPHR6503PL1 in common drain configuration are used. And to control the gate signals of these MOSFETs a 20 V bus compatible MOSFET gate driver IC TCK421G is used. SSM3K72CTC is used as a gate shut-off MOSFET for the input-side MOSFET of the common-drain configuration.

(5) VINB switching circuit

To control the output of VINB power supply (5 V, max. 3 A), two MOSFETs TPHR6503PL1 in common drain configuration are used. And to control gate signals of these MOSFETs a 5 V bus compatible MOSFET gate driver IC TCK425G is used. SSM3K15ACTC is used as a gate shut-off MOSFET for the input-side MOSFET of the common-drain configuration.

The power supplied from VINA (20 V, max. 3 A) and VINB (5 V, max. 3 A) is output from VOUT as shown below.

・If the power is input only to either VINA (20 V) or VINB (5 V) connector, the input power is output to VOUT.

・If power is input to both VINA and VINB, the power of VINA (20 V) is output to VOUT.

3.1.4. BBM/MBB Switching Operation

Module board (MUX1, MUX2, MUX3, MUX5) using MOSFET gate driver IC can switch between BBM operation or MBB operation.

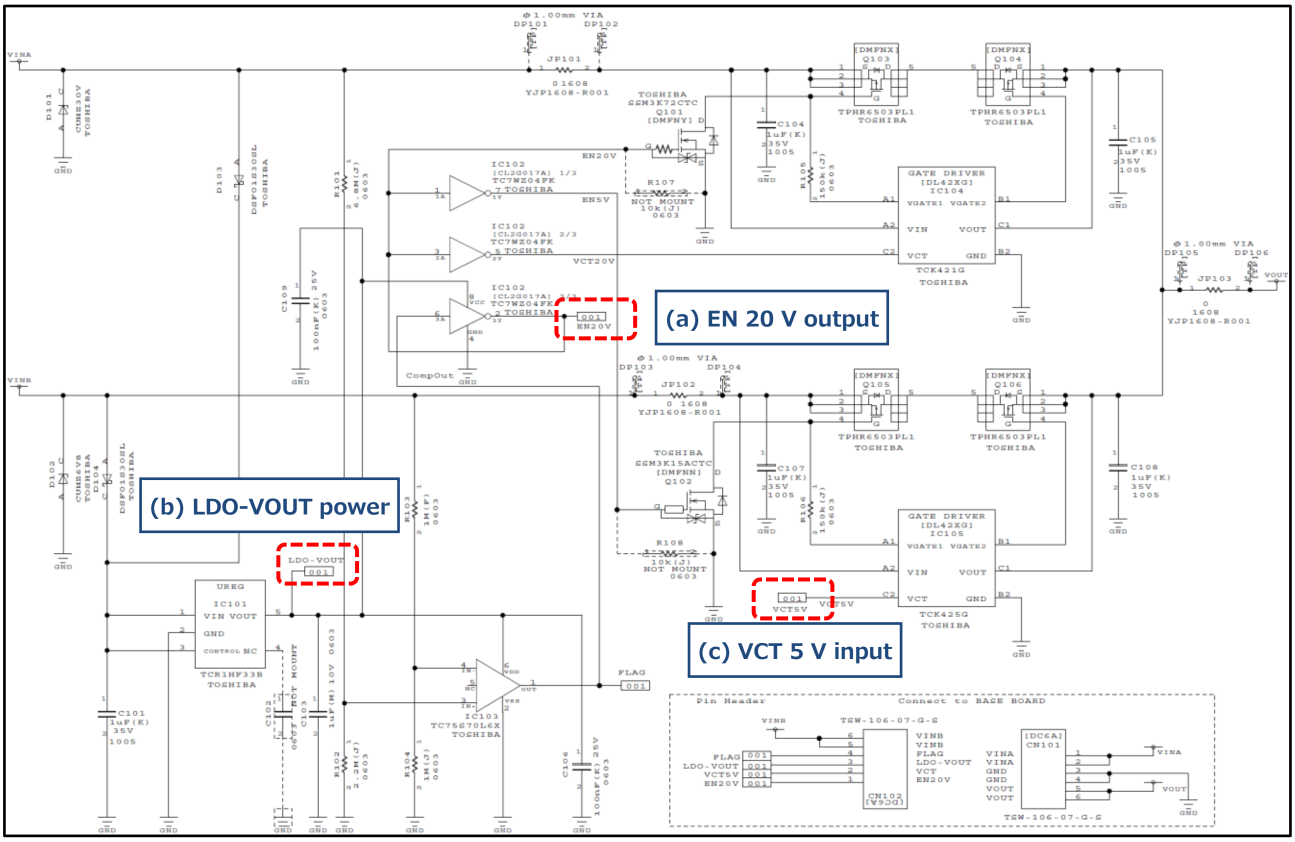


Fig. 3.6 BBM/MBB Switching on the Module-Board (MUX1)

BBM/MBB operation switching is achieved switching the signals of the module board connector with a toggle switch on the base board. The input voltages of VINA and VINB are compared using a comparator and if the voltage is input to VINA, High level (approx. 3.3 V) is output to the FLAG, and if the voltage is not input to VINA, Low level (0 V) is output to the FLAG.

(a) EN20V output (Inverted output of FLAG signal, High level output when no voltage is input to VINA)

(b) LDO-VOUT output (High level output if voltage is input to either of VINA, VINB)

(c) VCT5V input (control pin of VINB side MOSFET gate driver IC, gate on with H level input)

In BBM mode, (a) EN20V output is connected to (c) VCT5V input. Thus, MOSFET gate driver IC TCK425G on VINB side is gated off when voltage is input to VINA and gated on when voltage is not input to VINA to achieve BBM operation.

In MBB mode, (b) LDO-VOUT output is connected to (c) VCT5V input. As a result, VINB side MOSFET gate driver IC TCK425G is constantly turned on if the voltage is input to VINB, and MBB operation is realized by operating the gate cut-off MOSFET.

3.1.5. Circuit of eFuse IC Version Board

Circuit of the Module Board (MUX4) using eFuse IC is shown below.

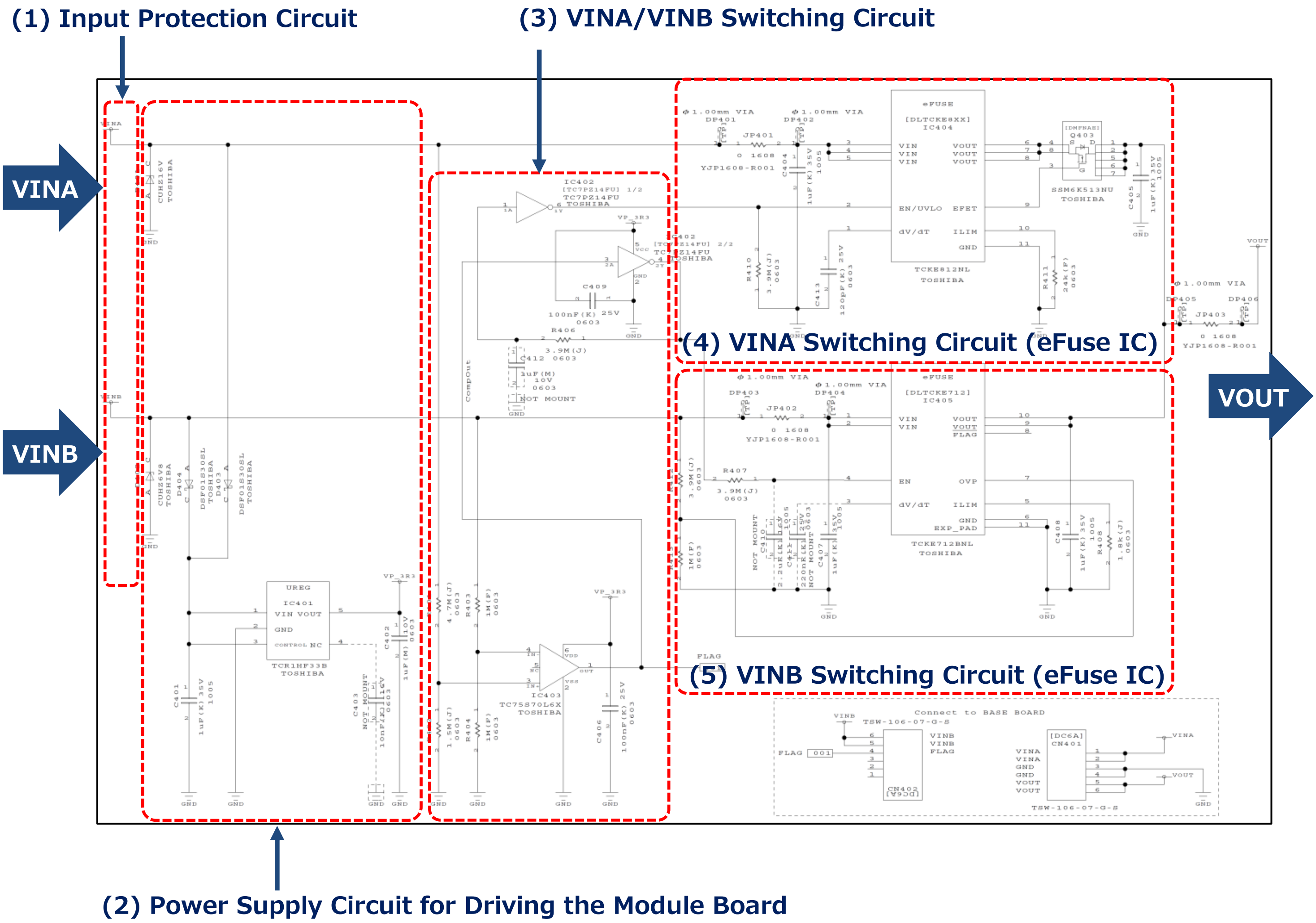


Fig. 3.7 Module Board (MUX4) Circuit

MUX4 module board uses eFuse IC instead of MOSFET gate driver ICs for the switching of inputs. A semiconductor fuse, eFuse IC is equipped with a variety of protective functions such as a high-speed current interrupt function and a short-circuit protection function when overcurrent is detected. Unlike circuits with MOSFET gate driver ICs, they do not drive external common-drain or common-source-connected MOSFET, so they only support BBM operation, but power multiplexer circuits can be realized with a simple configuration.

VINA (12 V) switch uses eFuse IC TCKE812NL, MOSFET SSM6K513NU externally to prevent current backflow, and VINB (5 V) switch uses eFuse IC TCKE712BNL.

3.2. Base Board

3.2.1. Circuit of the Base Board

Each circuit on the base board is shown below.

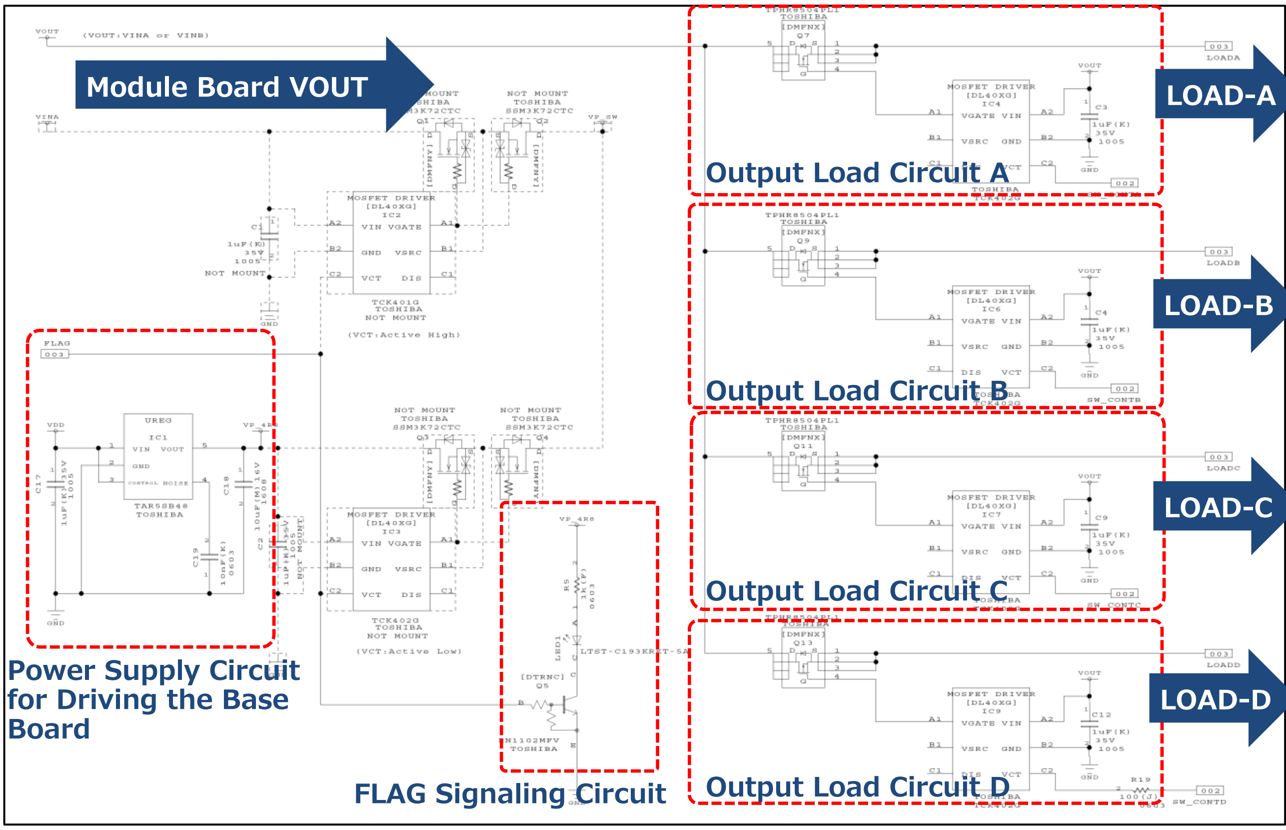


Fig. 3.8 Base Board Circuit (1)

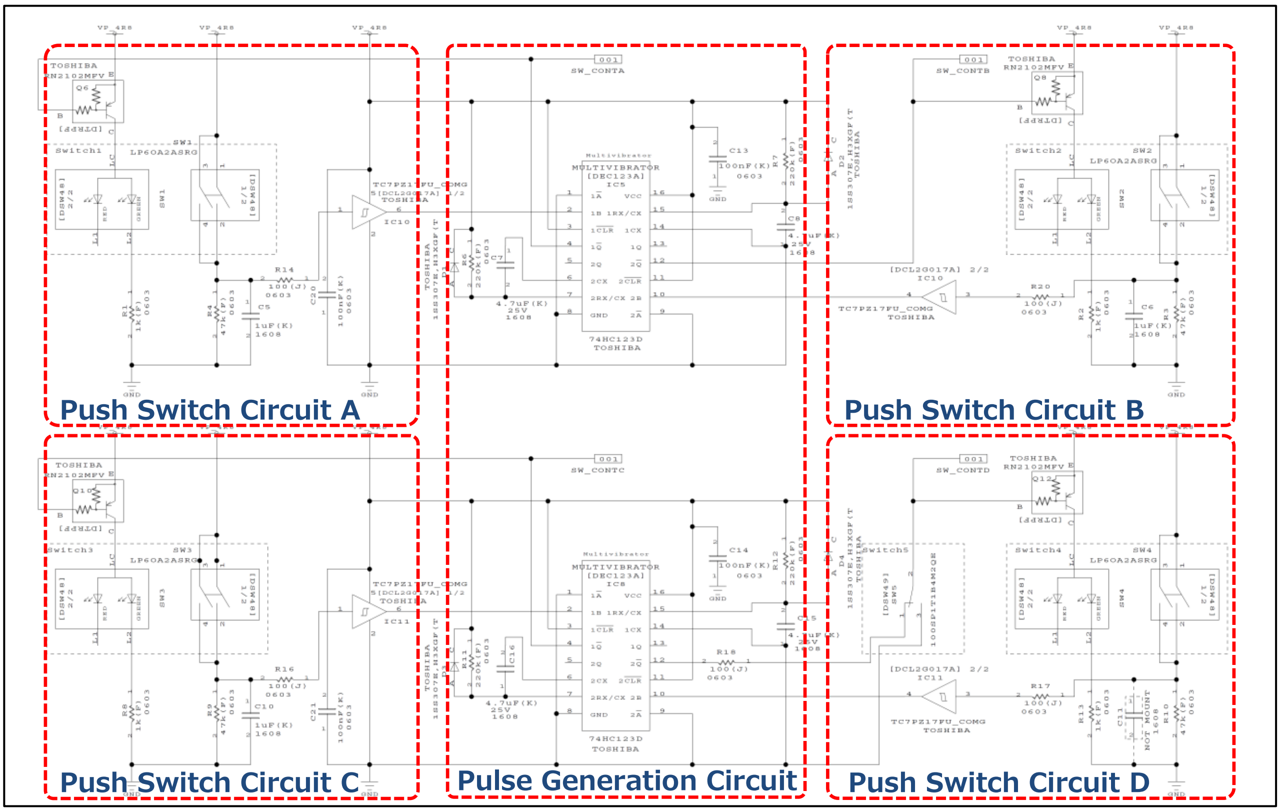


Fig. 3.9 Base Board Circuit (2)

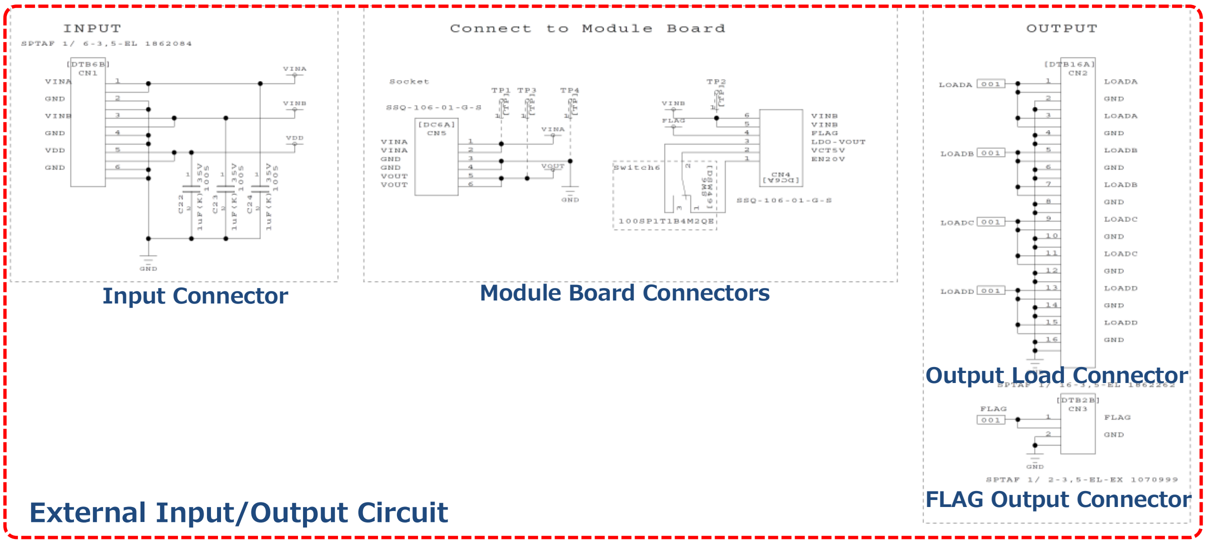


Fig. 3.10 Base board circuit (3)

The base board consists of the following circuits:

(1) Power supply circuit for driving the base board

It generates the power required to operate each circuit on the base board. The drive power supply VDD (5 to 12 V) supplied to the input connector (CN1). It also generates the internal power supply VP_4R8 (approx. 4.8 V) by LDO TAR5SB48.

(2) FLAG signalling circuit

The built-in resistor transistor (BRT) RN1102MFV lights the LED when FLAG output signal from the module board is High level (approx. 3.3 V).

(3) Output load circuit (A to D)

High-side switches are configured with power MOSFET TPHR8504PL1 and MOSFET gate driver IC TCK402G. The power-out VOUT of the module board is used to power TCK402G.

(4) Push switch circuit (A to D)

Four push switches are used to generate the trigger signals for pulse signal generation circuit. Resistor, capacitor and schmitt trigger input buffer TC7PZ17FU are used for removing fluctuations. While the pulse signal generated by the pulse generator is at H level, the LED in the key switch is lit and driven by the transistor RN2102MFV with built-in resistor.

(5) Pulse generation circuit

Monostable multi-vibrator 74HC123D uses the trigger signals from four push switches to generate a single-shot pulse of approximately 1 second for that system.

(6) External input/output circuit

Following connectors are used during the evaluation of power multiplexer module board. The input connector (CN1) takes VINA input, VINB input, and VDD input. The output load connector (CN2) output four loads (LOAD-A, LOAD-B, LOAD-C, LOAD-D). The connector (CN3) output FLAG signal. And connectors (CN4, CN5) are used for connecting the module board to base board.

3.2.2. Output Load Energization Method

Four pulse energization switches that output current to the load for approximately 1 second after pressing the switch and one DC energization/pulse energization switch are mounted on the base board.

There are four output loads (LOAD-A, LOAD-B, LOAD-C, LOAD-D) on the base board. When the corresponding pulse energization switch is pressed, one-shot pulse of the following duration is generated by the monostable multi-vibrator 74HC123D, and the high-side switch of the output load circuit is turned on and current flows to the output load while this pulse is at the High level.

t_{wout} = 1 x Cx x Rx = 1 x 4.7 μF x 220 kΩ (approximately 1.03 sec)

As for LOAD-D output, if DC energization/pulse energization switch is switched to DC energization, DC energization takes precedence over pulse energization, and current is continuously output. Therefore, be careful not to overheat or burn the load when DC energization is enabled.

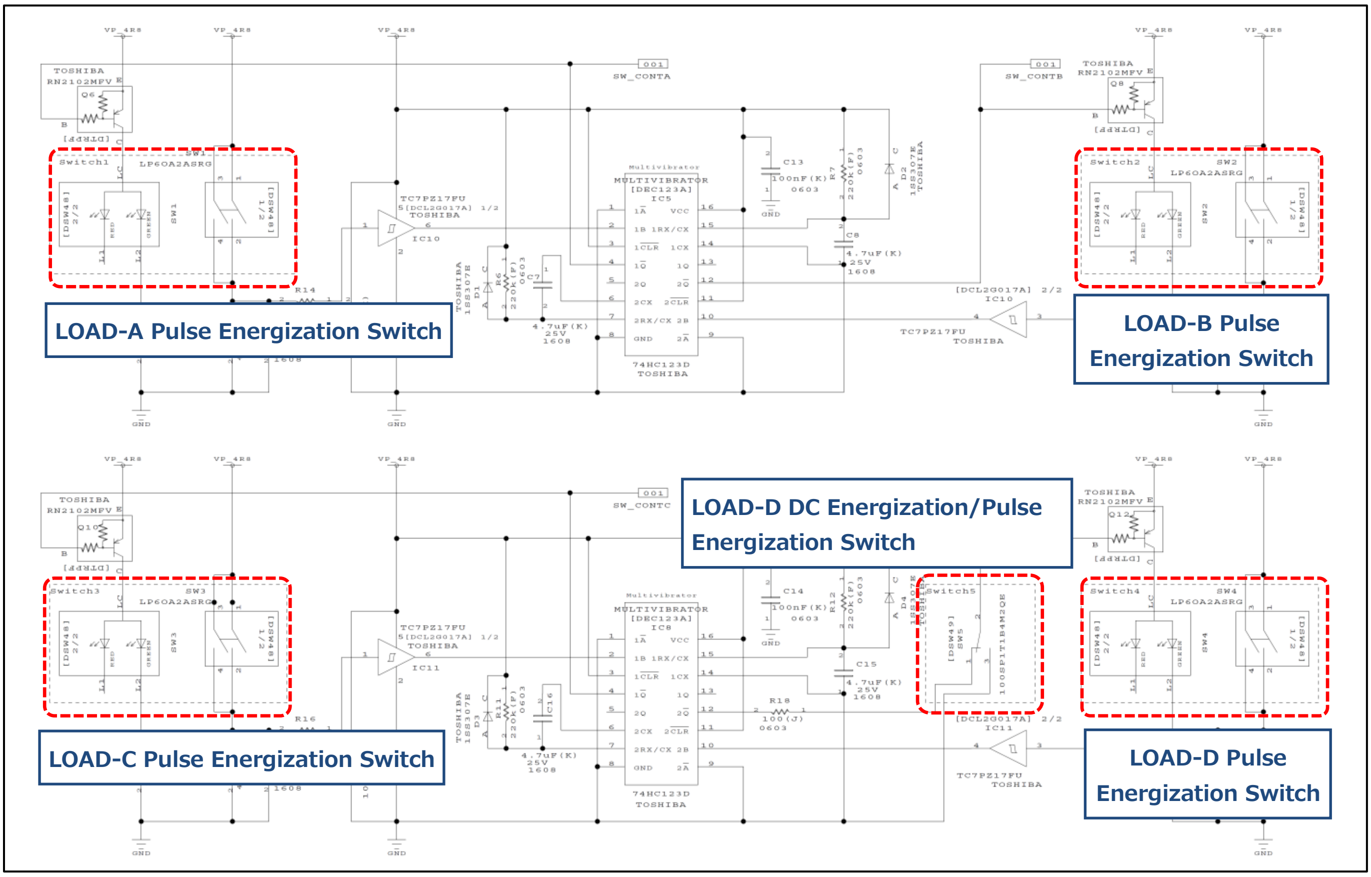


Fig. 3.11 Switches for Output Load Energization on Base Board Circuit

4. PCB Design

4.1. Component Layout Example

Fig. 4.1, Fig. 4.2, and Fig. 4.3 show the component layout of module board and base board.

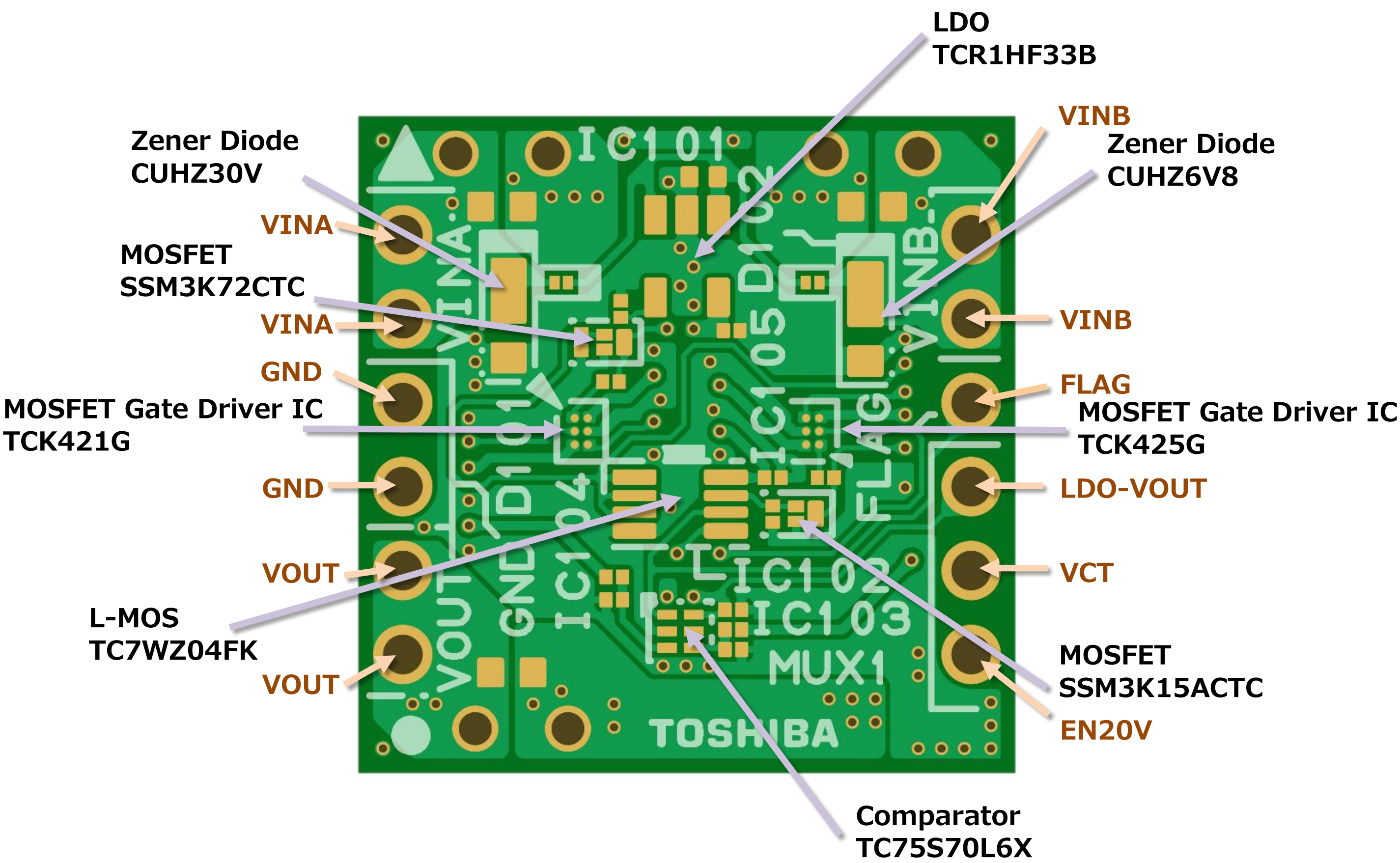


Fig. 4.1 Module Board Main Component Layout (Front Side – Example MUX1)

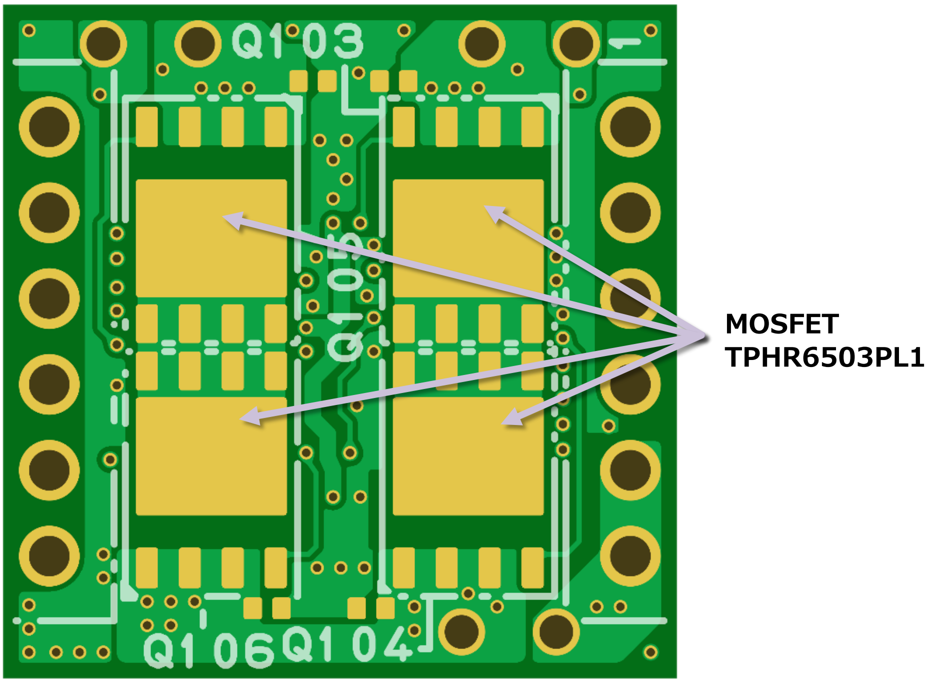


Fig. 4.2 Module Board Main Component Layout (Back Side – Example MUX1)

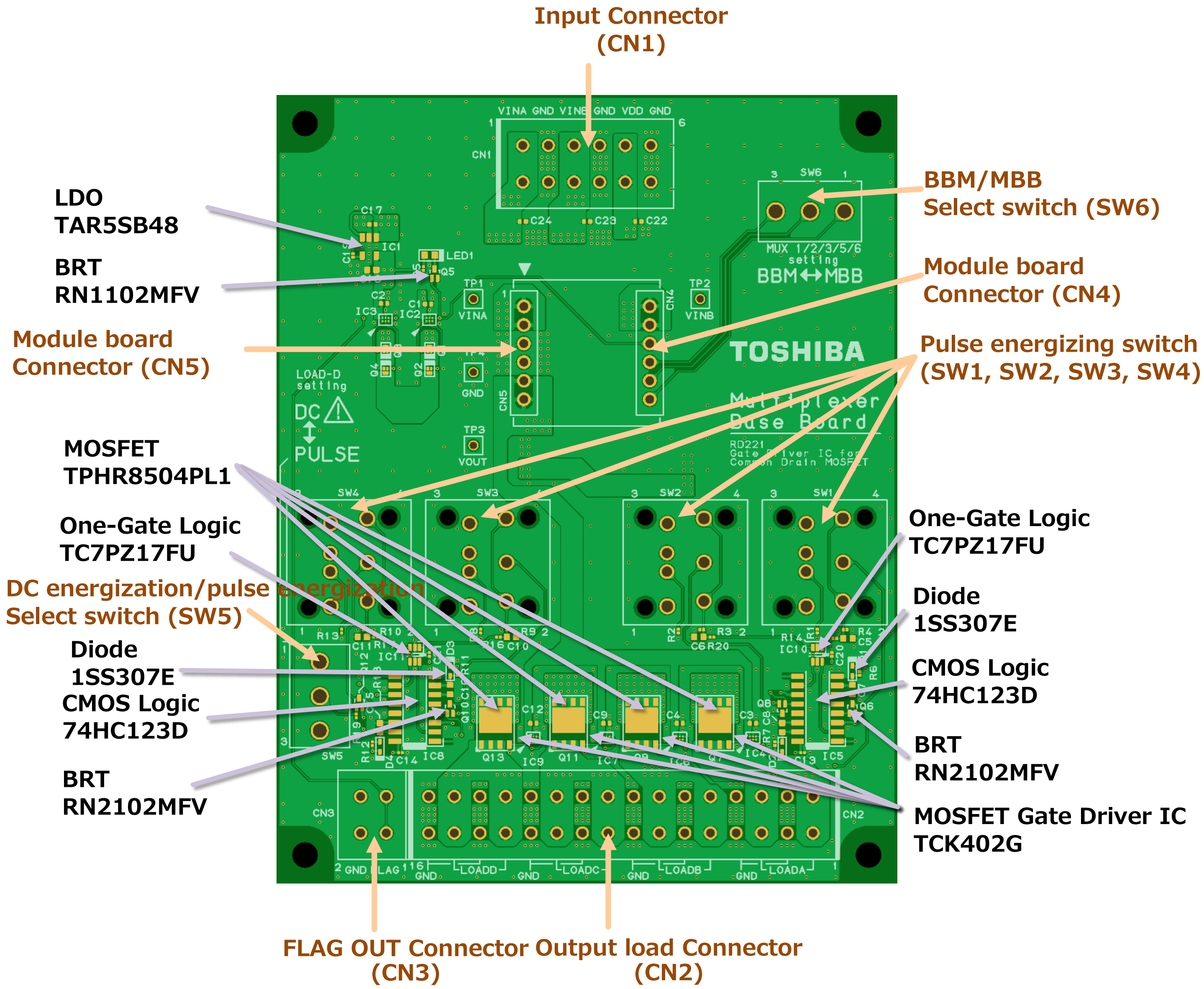


Fig. 4.3 Base Board Main Component Layout

4.2. Design Precautions

Consider the following when designing the PCB pattern.

- Pattern Design Considering Current

  Since the base board and the module board have circuits in which large currents flow, a sufficient pattern width must be ensured in designing the pattern to prevent problems due to temperature rise or voltage drop caused by the pattern when the maximum current with added margin is applied.

- Ground peripheral pattern design

  In order to suppress the voltage drop when current flows, it is necessary to consider the GND wiring, such as providing a ground plane or the shortest distance.

5. Component Overview

The components used in this circuit are described here.

5.1. MOSFET Gate Driver IC

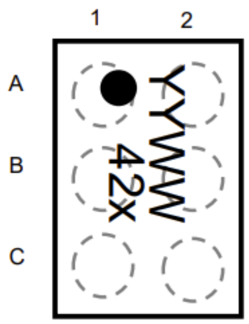
TCK42xG

In this design, these are used to drive the load switch MOSFET of VINA, VINB on the module board. Please click here for more information.

Features

- Gate driver for N-channel Common Drain MOSFET
- Gate driver for N-channel Single High side MOSFET
- High maximum input voltage: $V_{IN\ max}$ = 40 V
- Wide input voltage operation: V_{IN} = 2.7 to 28 V
- Gate-Source protection circuit
- Over Voltage Lock Out : V_{IN_OVLO} = 6.31 V, 10.83 V, 14.29 V, 23.26 V and 27.73 V typ
- Under Voltage Lock Out : V_{IN_UVLO} = 2.0 V typ
- Built in Charge pump circuit: Gate source voltage V_{GS} = 5.6 V and 10 V typ
- Low standby current : $I_{Q(OFF)}$ = 0.9 μA max at V_{IN} = 12 V (Except TCK424G, TCK425G)

External View, Pin Assignment



A1: VGATE1
B1: VGATE2
C1: VOUT
A2: VIN
B2: GND
C2: VCT

YYWW: Lot No.

42x: Device name code
420: TCK420G
421: TCK421G
422: TCK422G
423: TCK423G
424: TCK424G
425: TCK425G

List of Products Number, OVLO and VGS

Part Number	OVLO Threshold, Falling Typ. (V)	External MOSFET Gate Source Voltage (Control ON) Typ. (V)
TCK420G	27.73	10
TCK421G	23.26	10
TCK422G	14.29	10
TCK423G	14.29	5.6
TCK424G	10.83	5.6
TCK425G	6.31	5.6

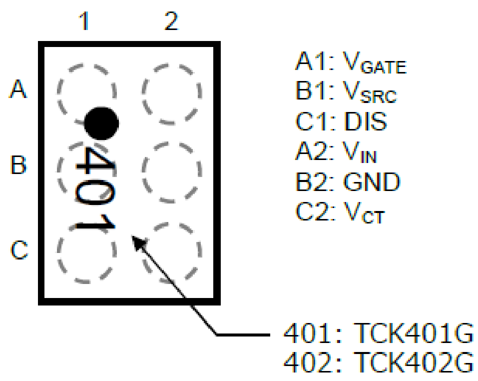
TCK402G

In this design, it is used to drive the load switch application MOSFET on the base board. Click here for more information.

Features

- High maximum input voltage: $V_{IN\ max}$ = 40 V
- Wide input voltage range: V_{IN} = 2.7 to 28 V
- Auto output discharge
- Charge pump circuit
- Inrush current reducing circuit.
- Over voltage lock out (Over 28 V)
- Under voltage lock out (Under 2.7 V)

External View, Pin Assignment



5.2. MOSFET

The following MOSFETs are used in this design. Click the part number for more details.

Location		Part Number	Package	V_{DSS}	V_{GSS}	$R_{DS(ON)}$ Max
Module Board	For output	TPHR6503PL1	SOP Advance (N)	30 V	+/-20 V	0.65 mΩ @10 V
	For output	TPN1R603PL	TSON Advance	30 V	+/-20 V	1.6 mΩ @10 V
	For output	SSM6K513NU	UDFN6B	30 V	+/-20 V	8.9 mΩ @10 V
	For output	TPHR8504PL1	SOP Advance (N)	40 V	+/-20 V	0.85 mΩ @10 V
	For control	SSM3K72CTC	CST3C	30 V	+/-20 V	4.7 Ω @4.5 V
	For control	SSM3K15ACTC	CST3C	30 V	+/-20 V	6.0 Ω @2.5 V
Base Board	For output	TPHR8504PL1	SOP Advance (N)	40 V	+/-20 V	0.85 mΩ @10 V

5.3. eFuse IC

TCKE812NA

In this design, it is used as a VINA load switch on the module board. Please click here for more information.

Features

- High input voltage: $V_{IN\ max}$ = 18.0 V
- High output current: $I_{OUT\ (DC)}$ = 5.0 A
- Low ON resistance : R_{ON} = 28 mΩ (typ.)
- Adjustable overcurrent limit : up to 5.0 A
- Fixed over voltage clamp
  - 5 V power rail TCKE805 : V_{OVC} = 6.04 V (typ.)
  - 12 V power rail TCKE812 : V_{OVC} = 15.1 V (typ.)
  - TCKE800 : No over voltage clamp
- Programmable slew rate control by external capacitance for inrush current reduction
- Programmable under voltage lockout by external resistor
- Reverse current blocking support by built in MOSFET driver
- Thermal shutdown
- Auto-discharge
- Small package: WSON10B (3.0 mm x 3.0 mm, t: 0.7 mm (typ.))
- IEC62368-1 Certified

External View, Pin Assignment

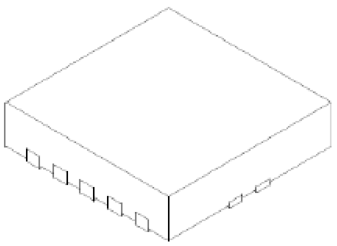
TCKE712BNL

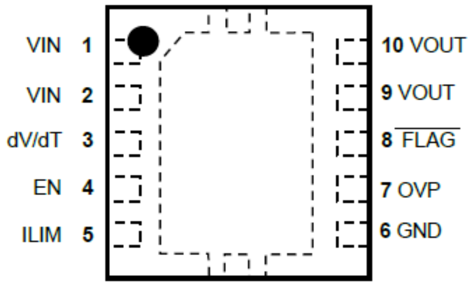
In this design, it is used as a VINB load switch on the module board. Please click here for more information.

Features

- High input voltage: $V_{IN\ max}$ = 13.2 V
- Low ON resistance : R_{ON} = 53 mΩ (typ.)
- Adjustable over current protection
- Adjustable over voltage protection
- Programmable Slew rate control by External Capacitance for Inrush current reduction
- FLAG indicates
- Reverse current blocking (SW OFF state)
- Thermal Shutdown
- Small package:WSON10 (3.0 mm x 3.0 mm, t: 0.7 mm (typ))

External View, Pin Assignment


WSON10



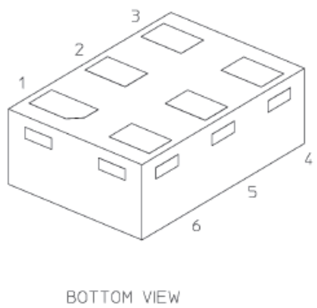
5.4. Comparator IC (TC75S70L6X)

In this design, it is used for controlling the module board. Please click here for more information.

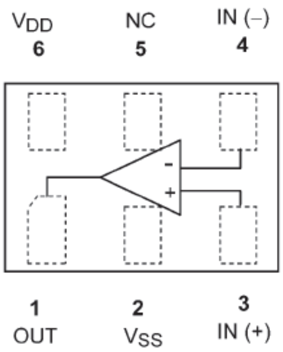
Features

- Single circuit, Input/Output full swing comparator
- Low operating voltage: V_{DD} = 1.3 to 5.5 V
- Low supply current: I_{DD} = 18 μA (typ.) (@V_{DD} = 1.5 V)
- Ultra Small package: MP6C (1.0 mm × 1.45 mm, t = 0.55 mmMAX)
- Low input bias current: 1 pA (typ.)
- Push-pull output circuit
- Single power supply operation

External View, Pin Assignment



MP6C



(Top View)

5.5. LDO Regulator

In this design, these are used for controlling the module board and base board. Click the part number for details.

Board	Part Number	Package	V_{IN} Max	V_{OUT}	I_{OUT} Max
Module Board	TCR1HF33B	SMV	40 V	3.3 V	150 mA
	TCR1HF50B	SMV	40 V	5.0 V	150 mA
Base Board	TAR5SB48	SMV	15 V	4.8 V	200 mA

5.6. L-MOS, Standardized CMOS Logic IC

In this design, these are used for controlling the module board and base board. Click the part number for details.

Board	Part Number	Package	Function	V_{CC}
Module Board	TC7WZ04FK	SM8	Triple Inverter	1.65 to 5.5 V
	TC7PZ14FU	US6	Dual Schmitt Inverter	1.65 to 5.5 V
Base Board	TC7PZ17FU	US6	Dual Schmitt Buffer	1.65 to 5.5 V
	74HC123D	SOIC16	Dual Monostable Multi-vibrator	2.0 to 6.0 V

5.7. Zener Diode

In this design, these are used for overvoltage protection of the input voltage of the module board. Click the part number for details.

Part Number	Package	V_Z (V) Typ.	VESD
CUHZ6V8	US2H	6.8 V @I_Z = 10 mA	±30 kV
CUHZ12V	US2H	12 V @I_Z = 10 mA	±30 kV
CUHZ16V	US2H	16 V @I_Z = 10 mA	±30 kV
CUHZ30V	US2H	30 V @I_Z = 10 mA	±30 kV

5.8. Diode

In this design, these are used for controlling the module board and base board. Click the part number for details.

Board	Part Number	Package	V_R	I_O	V_F Max	I_R Max
Module Board	DSF01S30SL	SL2	30 V	100 mA	0.3 V @I_F = 10 mA	50 μA @V_R = 30 V
Base Board	1SS307E	ESC	80 V	100 mA	1.3 V @I_F = 100 mA	10 nA @V_R = 80 V

5.9. Transistor with Built-in Resistor

In this design, these are used for controlling the base board. Click the part number for details.

Part Number	Package	Polarity	V_{CBO}	I_C	R1/R2
RN1114MFV	VESM	NPN	50 V	100 mA	1 kΩ/10 kΩ
RN2102MFV	VESM	PNP	-50 V	-100 mA	10 kΩ/10 kΩ

Terms of Use

This terms of use is made between Toshiba Electronic Devices and Storage Corporation (“We”) and customers who use documents and data that are consulted to design electronics applications on which our semiconductor devices are mounted (“this Reference Design”). Customers shall comply with this terms of use. Please note that it is assumed that customers agree to any and all this terms of use if customers download this Reference Design. We may, at its sole and exclusive discretion, change, alter, modify, add, and/or remove any part of this terms of use at any time without any prior notice. We may terminate this terms of use at any time and for any reason. Upon termination of this terms of use, customers shall destroy this Reference Design. In the event of any breach thereof by customers, customers shall destroy this Reference Design, and furnish us a written confirmation to prove such destruction.

1. Restrictions on usage

1. This Reference Design is provided solely as reference data for designing electronics applications. Customers shall not use this Reference Design for any other purpose, including without limitation, verification of reliability.
2. This Reference Design is for customer's own use and not for sale, lease or other transfer.
3. Customers shall not use this Reference Design for evaluation in high or low temperature, high humidity, or high electromagnetic environments.
4. This Reference Design shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable laws or regulations.

2. Limitations

1. We reserve the right to make changes to this Reference Design without notice.
2. This Reference Design should be treated as a reference only. We are not responsible for any incorrect or incomplete data and information.
3. Semiconductor devices can malfunction or fail. When designing electronics applications by referring to this Reference Design, customers are responsible for complying with safety standards and for providing adequate designs and safeguards for their hardware, software and systems which minimize risk and avoid situations in which a malfunction or failure of semiconductor devices could cause loss of human life, bodily injury or damage to property, including data loss or corruption. Customers must also refer to and comply with the latest versions of all relevant our information, including without limitation, specifications, data sheets and application notes for semiconductor devices, as well as the precautions and conditions set forth in the "Semiconductor Reliability Handbook".
4. When designing electronics applications by referring to this Reference Design, customers must evaluate the whole system adequately. Customers are solely responsible for all aspects of their own product design or applications. WE ASSUME NO LIABILITY FOR CUSTOMERS' PRODUCT DESIGN OR APPLICATIONS.
5. No responsibility is assumed by us for any infringement of patents or any other intellectual property rights of third parties that may result from the use of this Reference Design. No license to any intellectual property right is granted by this terms of use, whether express or implied, by estoppel or otherwise.
6. THIS REFERENCE DESIGN IS PROVIDED "AS IS". WE (a) ASSUME NO LIABILITY WHATSOEVER, INCLUDING WITHOUT LIMITATION, INDIRECT, CONSEQUENTIAL, SPECIAL, OR INCIDENTAL DAMAGES OR LOSS, INCLUDING WITHOUT LIMITATION, LOSS OF PROFITS, LOSS OF OPPORTUNITIES, BUSINESS INTERRUPTION AND LOSS OF DATA, AND (b) DISCLAIM ANY AND ALL EXPRESS OR IMPLIED WARRANTIES AND CONDITIONS RELATED TO THIS REFERENCE DESIGN, INCLUDING WARRANTIES OR CONDITIONS OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, ACCURACY OF INFORMATION, OR NONINFRINGEMENT.

3. Export Control

Customers shall not use or otherwise make available this Reference Design for any military purposes, including without limitation, for the design, development, use, stockpiling or manufacturing of nuclear, chemical, or biological weapons or missile technology products (mass destruction weapons). This Reference Design may be controlled under the applicable export laws and regulations including, without limitation, the Japanese Foreign Exchange and Foreign Trade Law and the U.S. Export Administration Regulations. Export and re-export of this Reference Design are strictly prohibited except in compliance with all applicable export laws and regulations.

4. Governing Laws

This terms of use shall be governed and construed by laws of Japan.