TOSHIBA

Smart Gate Driver Coupler Evaluation Board

Reference Guide

RD224-RGUIDE-01

1. Outline of TLP5214/TLP5214A, (TLP5212) Evaluation Board

This evaluation board facilitates the characteristic evaluation of the Smart Gate Driver Coupler (SGD).

- Peripheral circuit consisting of resistors, capacitors, and ICs required for evaluation is implemented.
- Buffer circuit and output buffer transistors for LED drive are also implemented, eliminating the need to connect these circuits externally.
- Blanking capacitors, DESAT voltages, and output-peak currents are adjustable,
  Active mirror clamp, gate negative power supply, and external blanking circuit can be enabled/disabled.

Blanking capacitor:
The blanking capacitance C_{BLANK} adjusts the amount of time (blanking time t_{BLANK}) before overcurrent protection is enabled.

DESAT Voltage:
DESAT voltage is the voltage threshold at which the overcurrent protection operation is activated. When the collector voltage of IGBT rises due to abnormal overcurrent, the DESAT terminal voltage also rises accordingly. When the DESAT terminal voltage reaches DESAT voltage, the overcurrent protection operation is enabled.

Active mirror clamp (AMC):
IGBT may malfunction when turned off due to a steep voltage change in the mirror capacitance between the gate and collector. The active mirror clamp function forcibly bypasses and clamps the gate and emitter to prevent this malfunction.

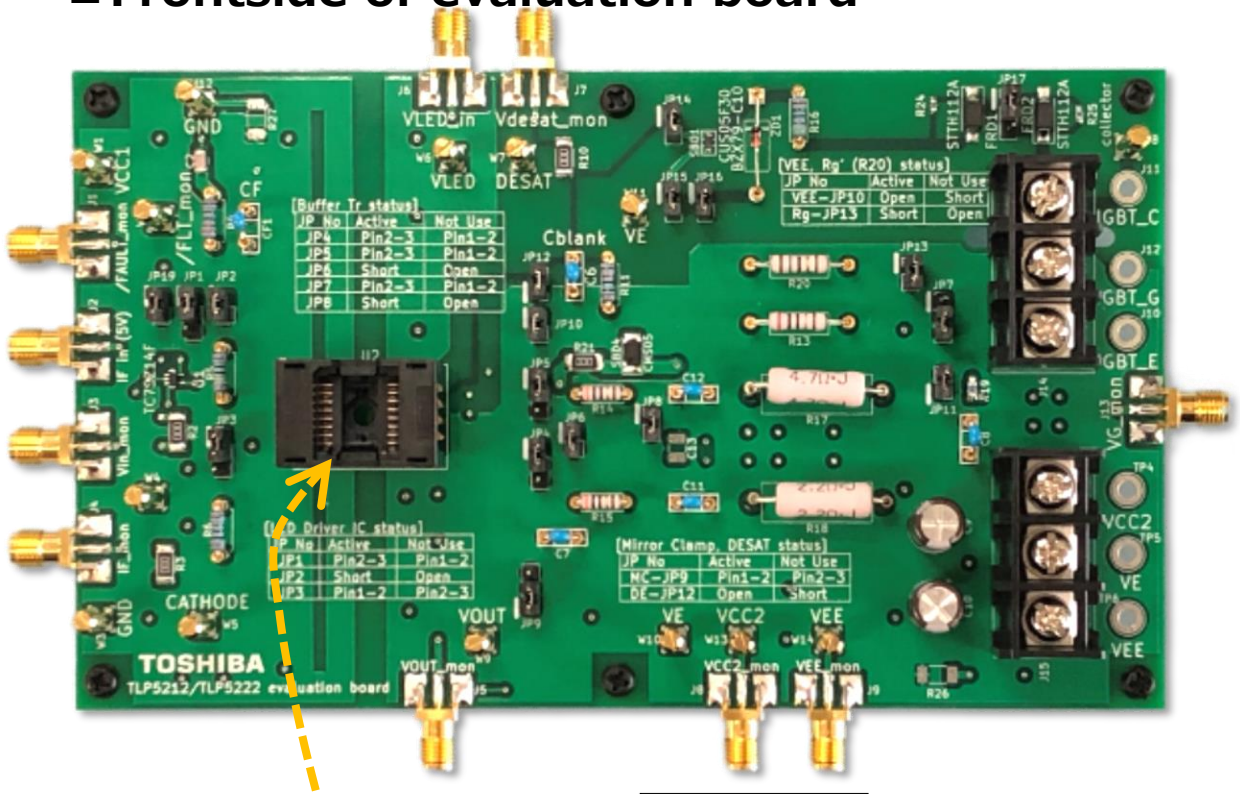
External blanking circuit:
When the blanking time becomes longer due to increase in blanking capacitance, the external blanking circuit charges the blanking capacitance of SGD by supplying current (I_{CHARGE}) to shorten the blanking time.

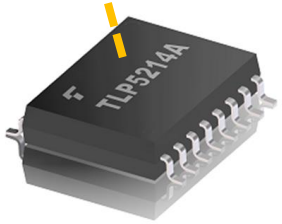
Gate negative power supply:
By using a negative power supply, the gate potential becomes a negative when IGBT is turned off. This prevents malfunction due to mirror capacitance.

■Caution ■	Circuit on this evaluation board is designed for the evaluation of the characteristics of smart gate driver couplers. This circuit specification does not guarantee the characteristics and reliability of the set. Thank you for your understanding.

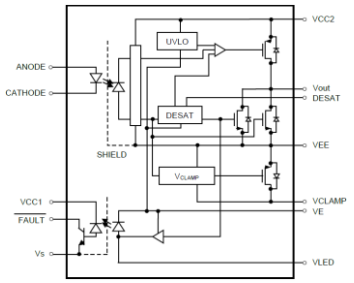
2. External View of Evaluation Board and Internal Circuit Diagram of TLP5214A

■ Frontside of evaluation board



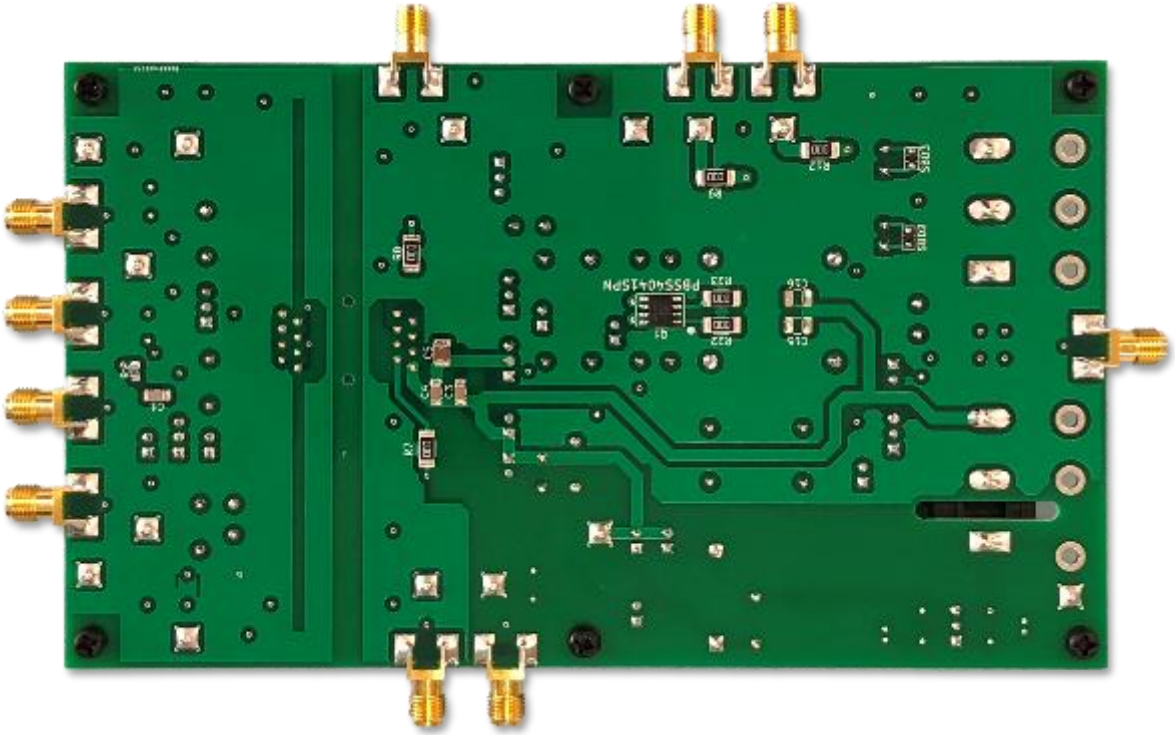


TLP5214A
TLP5214
(TLP5212)



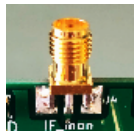
TLP 5214A Internal circuit

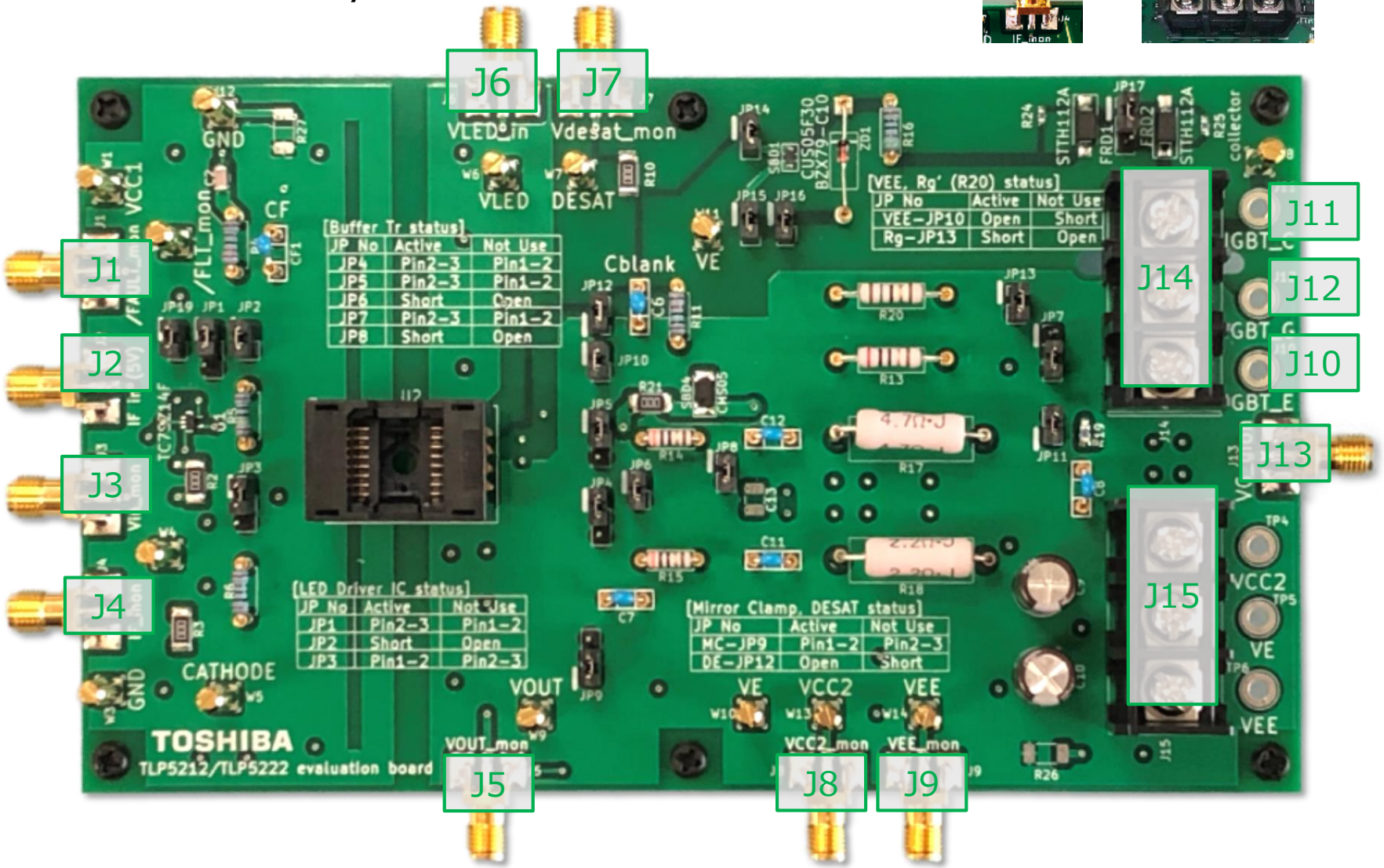
■ Backside of the evaluation board



2. Evaluation Board Terminal Layout

■ Terminals layout- **Junction connector**

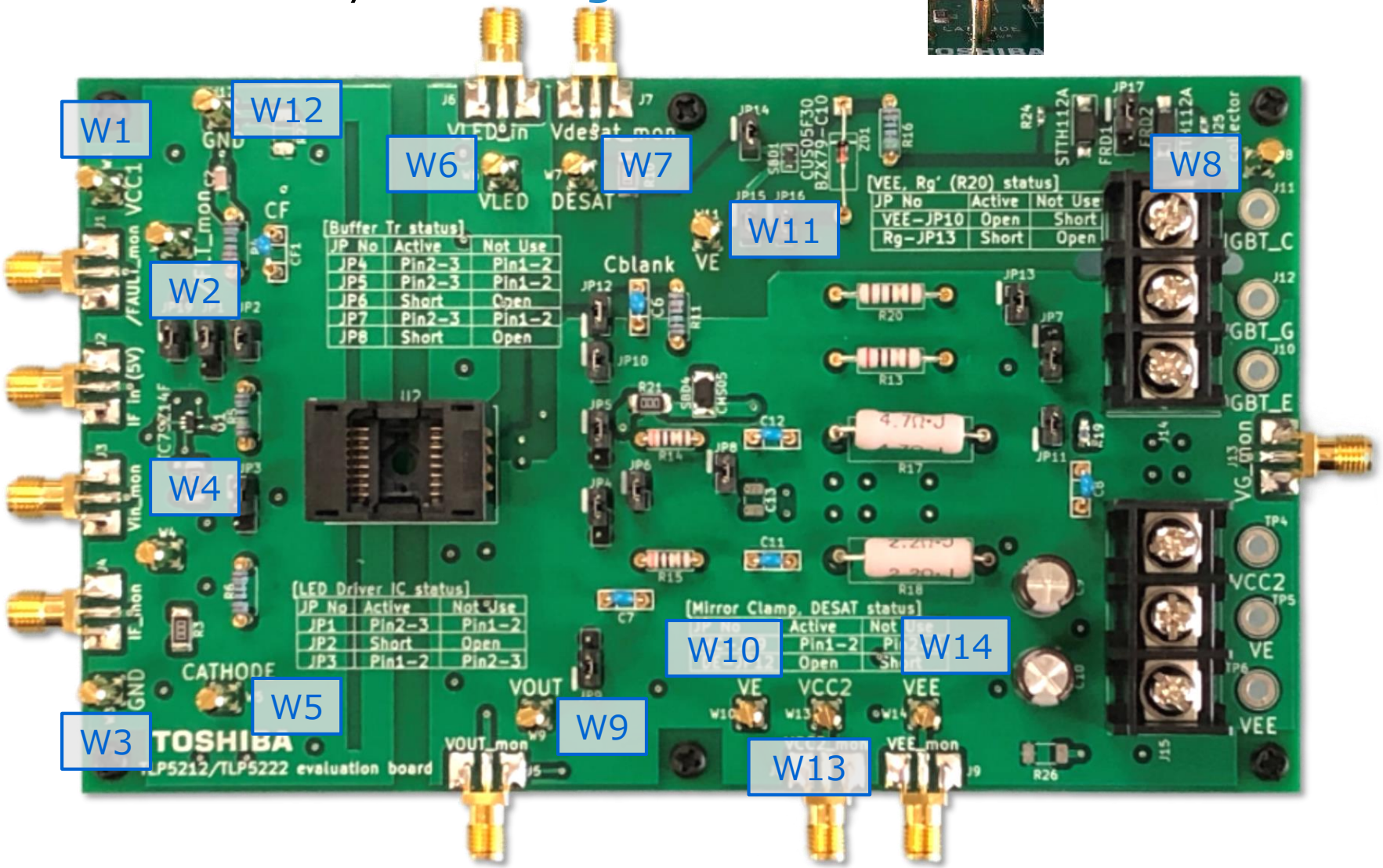




Symbol	Terminal Name
J1	FAULT Monitor
J2	$I_{F_}$in / V_{IN}
J3	V_{IN} Monitor
J4	I_F Monitor
J5	V_{OUT} Monitor
J6	V_{LED} in
J7	V_{DESAT} Monitor
J8	V_{CC2} Monitor
J9	V_{EE} Monitor
J10	IGBT_E
J11	IGBT_C
J12	IGBT_G
J13	IGBT_G Monitor
J14	IGBT E, C, G
J15	V_{CC2}, V_E, V_{EE}

2. Evaluation Board Terminal Layout

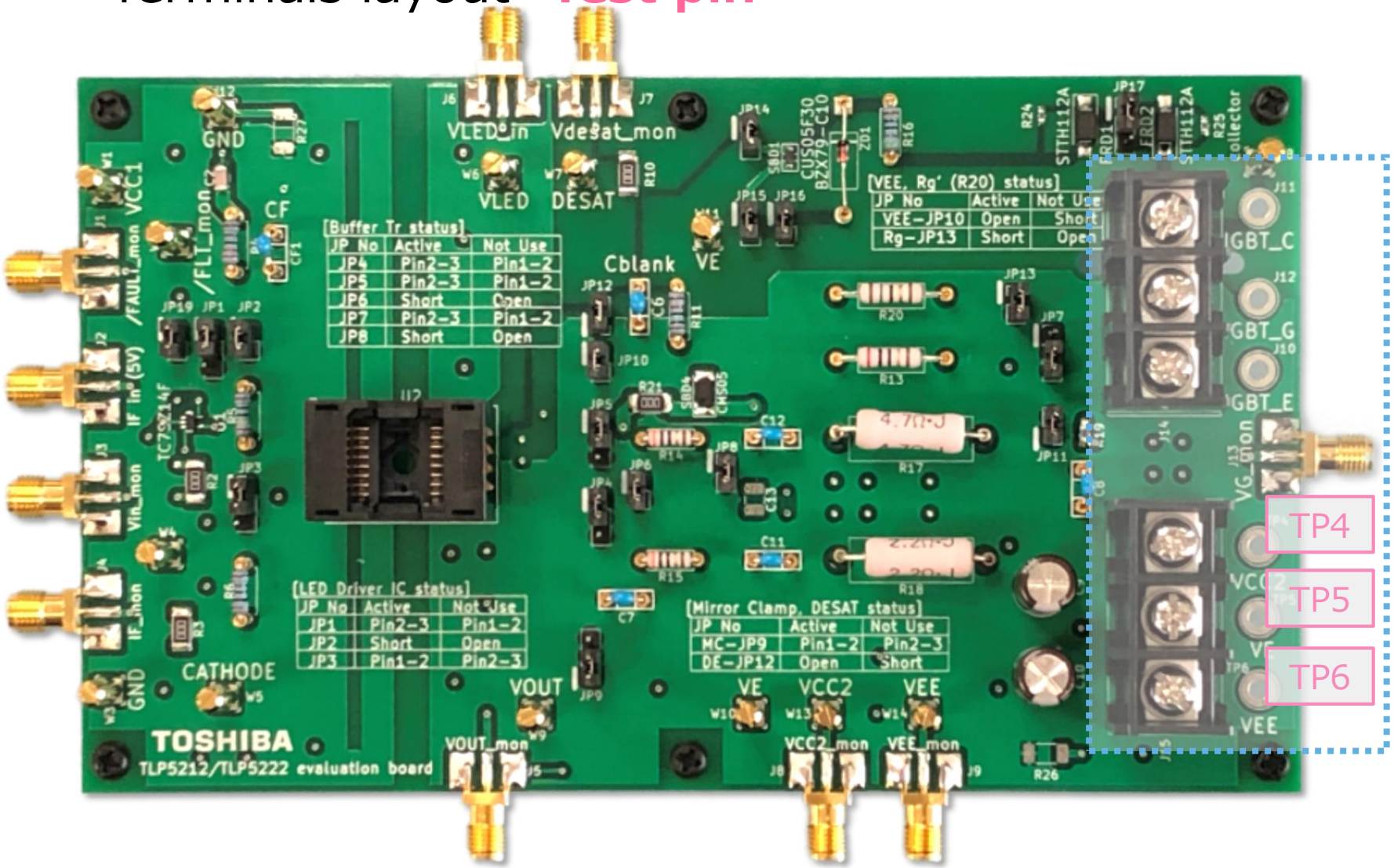
■ Terminals layout- **Wiring Terminal**



Symbol	Terminal Name
W1	V_{CC1}
W2	FAULT Monitor
W3	GND
W4	V_{IN} Monitor
W5	CATHODE
W6	V_{LED}
W7	DESAT
W8	COLLECTOR
W9	V_{OUT}
W10	V_E
W11	V_E
W12	GND (V_S)
W13	V_{CC2}
W14	V_{EE}

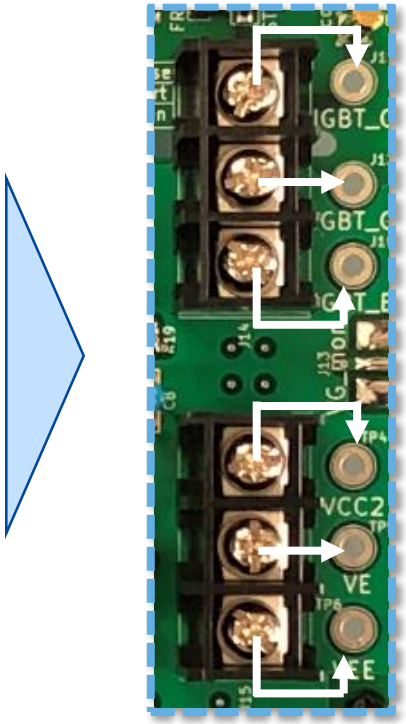
2. Evaluation Board Terminal Layout

■ Terminals layout- Test pin

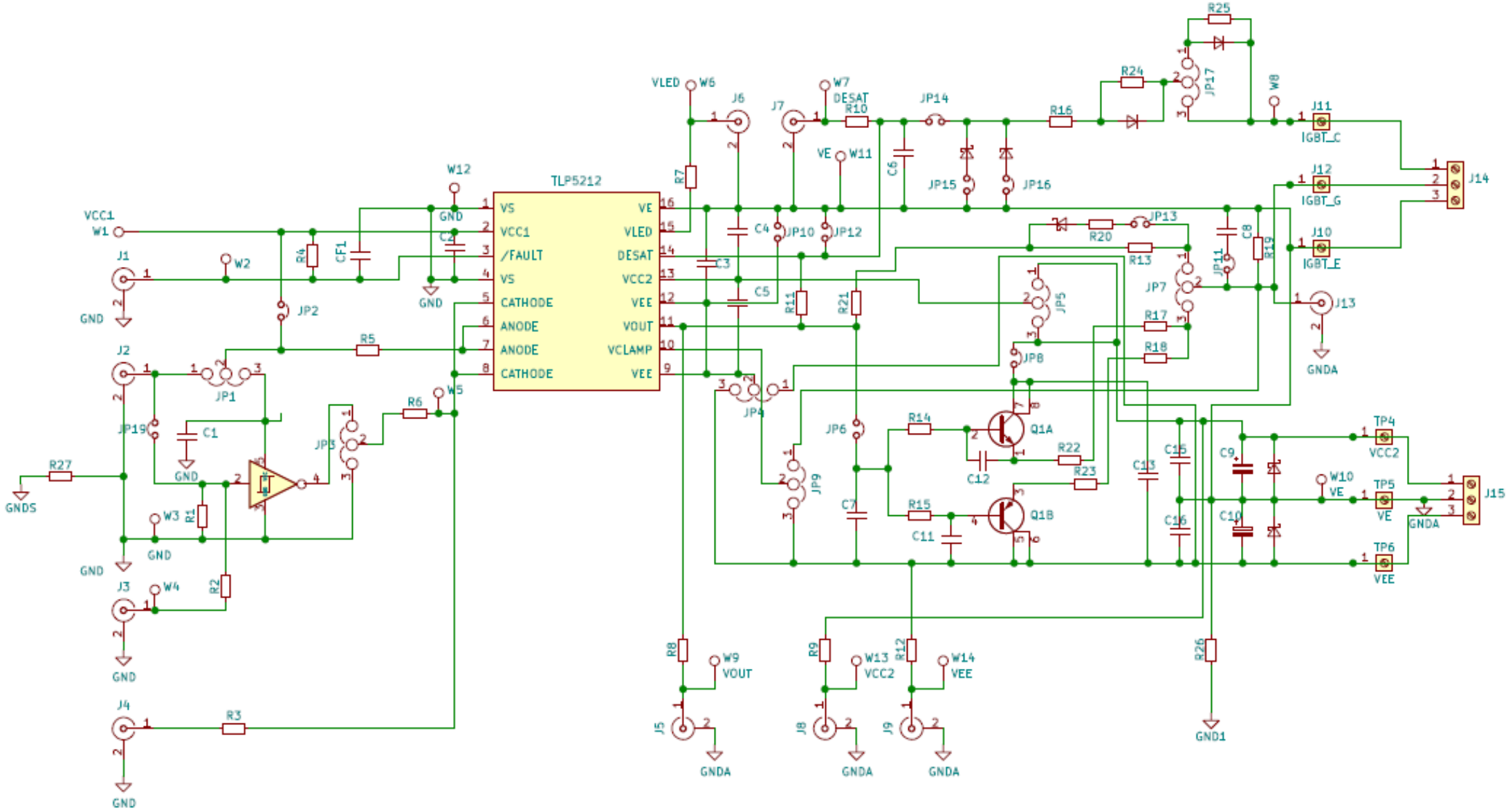


Symbol	Terminal Name
TP4	V_{CC2}
TP5	V_E
TP6	V_{EE}

Terminal blocks on the board, are connected as indicated by the arrows in the figure below.
Use the connection method suitable for your environment.

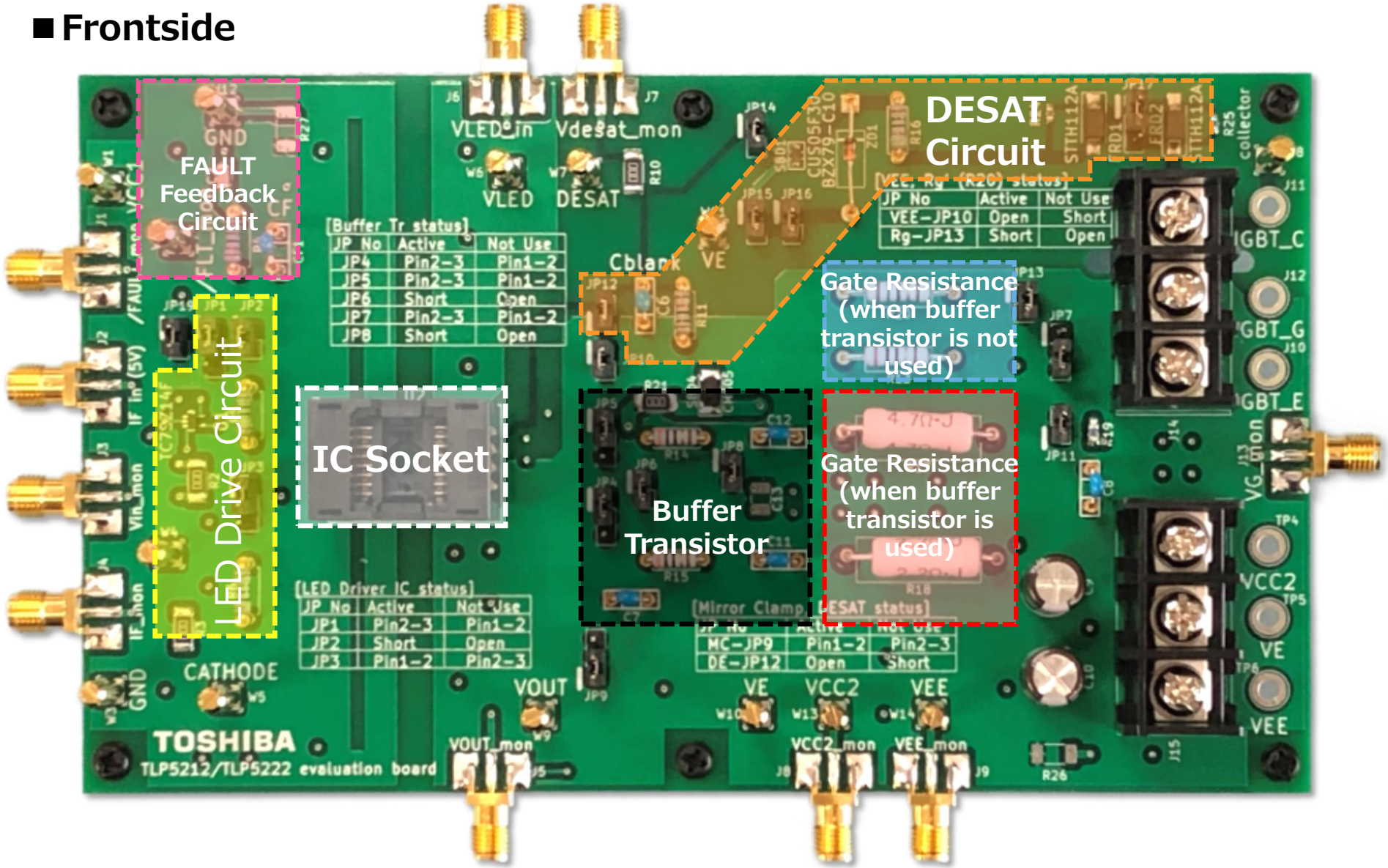


3. Evaluation Board Connection Diagram



4. Appearance and Main Functions of the Evaluation Board

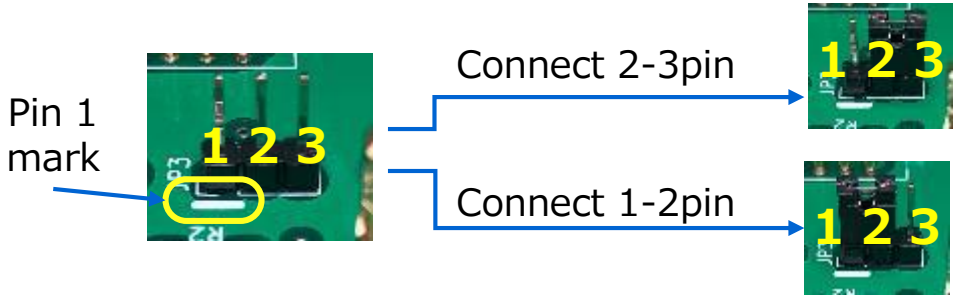
■ **Frontside**



List of Mounting Facility on Evaluation Board ①

Function	Jumper No.	Function selection		Detail
●LED drive circuit		When using	When not using	P.11
	JP1	Connect 2-3pin	Connect 1-2pin	
	JP2	Short	Open	
	JP3	Connect 1-2pin	Connect 2-3pin	
●Buffer transistor drive circuit		When using	When not using	P.12
	JP4	Connect 2-3pin	Connect 1-2pin	
	JP5	Connect 2-3pin	Connect 1-2pin	
	JP6	Short	Open	
	JP7	Connect 2-3pin	Connect 1-2pin	
	JP8	Short	Open	
●Active mirror clamp		When using	When not using	P.13
	JP9	Connect 1-2pin	Connect 2-3pin	
●Gate negative voltage power supply		When using	When not using	P.13
	JP10	Open	Short	

■ Jumper pin connection example: 3pin type

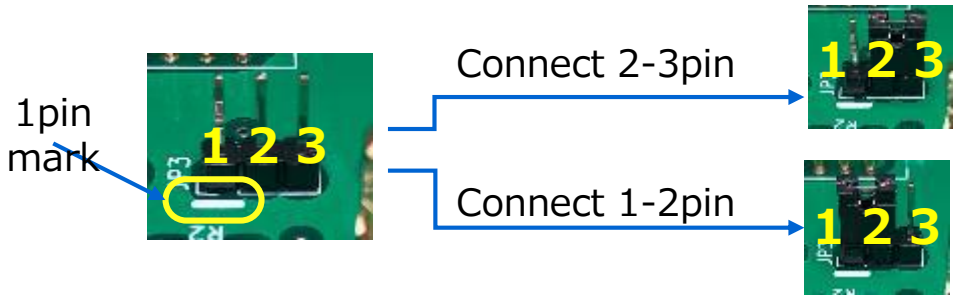


■ Jumper pin connection example: 2pin type

List of Mounting Facility on Evaluation Board ②

Function	Jumper No.	Function selection		Detail
●Externally connected Cg		When using	When not using	P.13
	JP11	Short	Open	
●DESAT function		When using	When not using	P.15
	JP12	Open	Short	
●DESAT protective device		When using	When not using	P.15
	JP15	Short	Open	
	JP16	Short	Open	
		FRD1 only	**FRD1 + FRD2**	
	JP17	Connect 2-3pin	Connect 1-2pin	
●Gate Resistor Separation Function for On/Off		When using	When not using	P.14
	JP13	Short	Open	
●Power device collector/drain terminal connection		When using	When not using	P.14
	JP14	Short	Open	

■ Jumper pin connection example: 3pin type



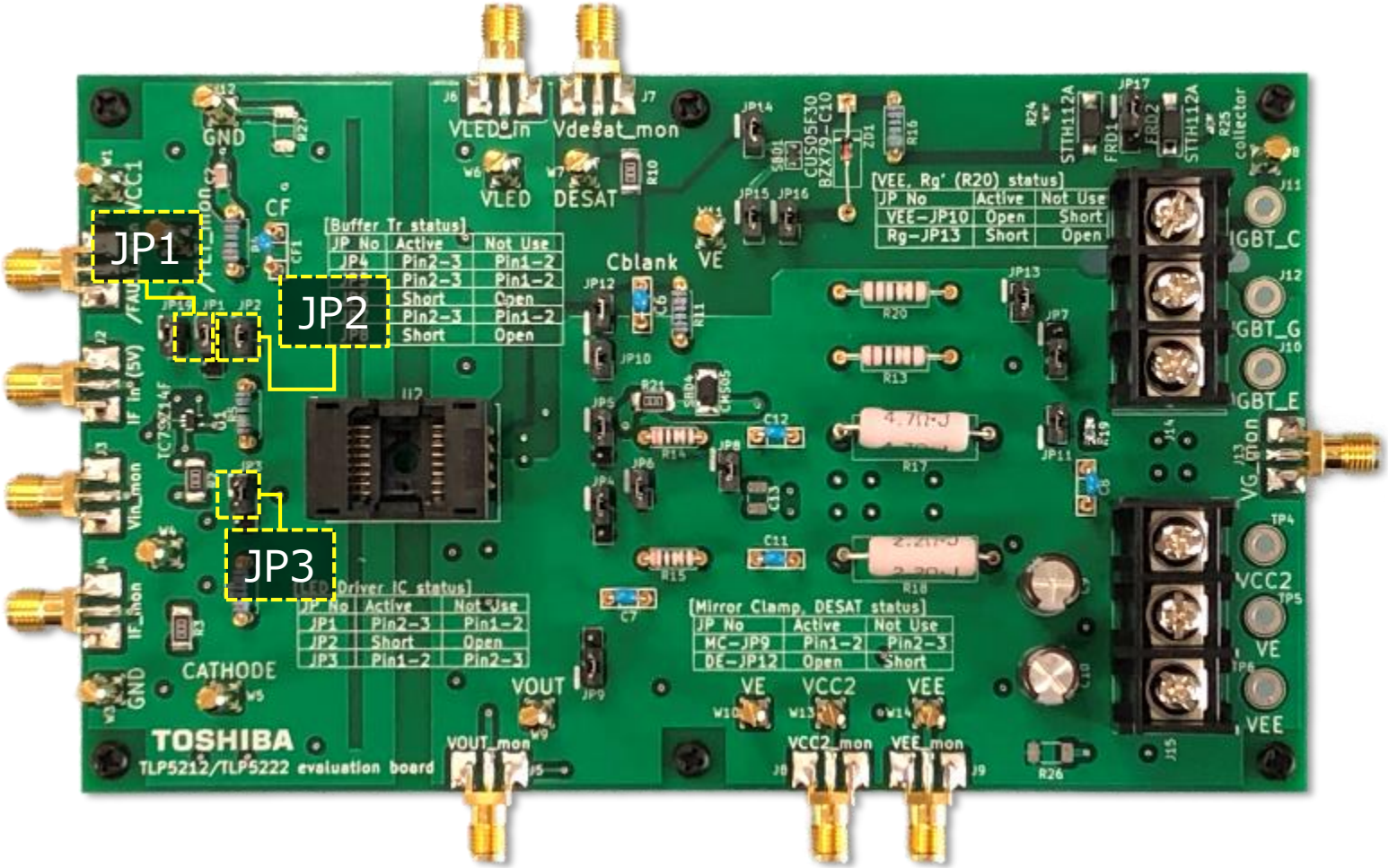
■ Jumper pin connection example: 2pin type

Open

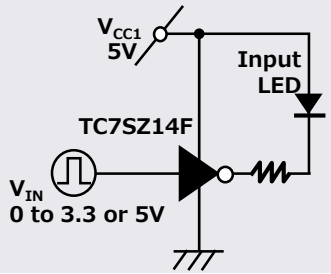
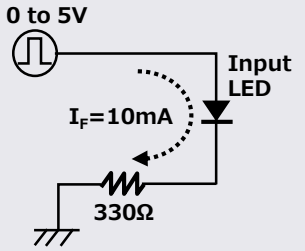
Short

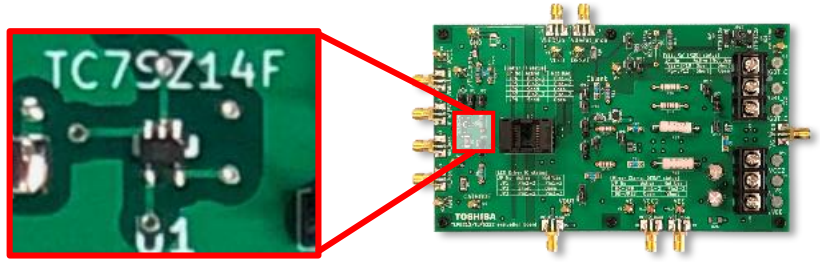
4. Appearance and Main Functions of Evaluation Board ①
LED Drive Circuit

Allows selection of using/not-using of logic IC driving input LED.
When using, the gate driving of the power device can be performed with 5V CMOS signal input rather than the current input.



LED drive circuit while using/not using

JP No.	When using driver IC (Voltage signal input)	When not using driver IC (Current signal input)
Schematic		
JP1	Connect 2-3pin	Connect 1-2pin
JP2	Short	Open
JP3	Connect 1-2pin	Connect 2-3pin

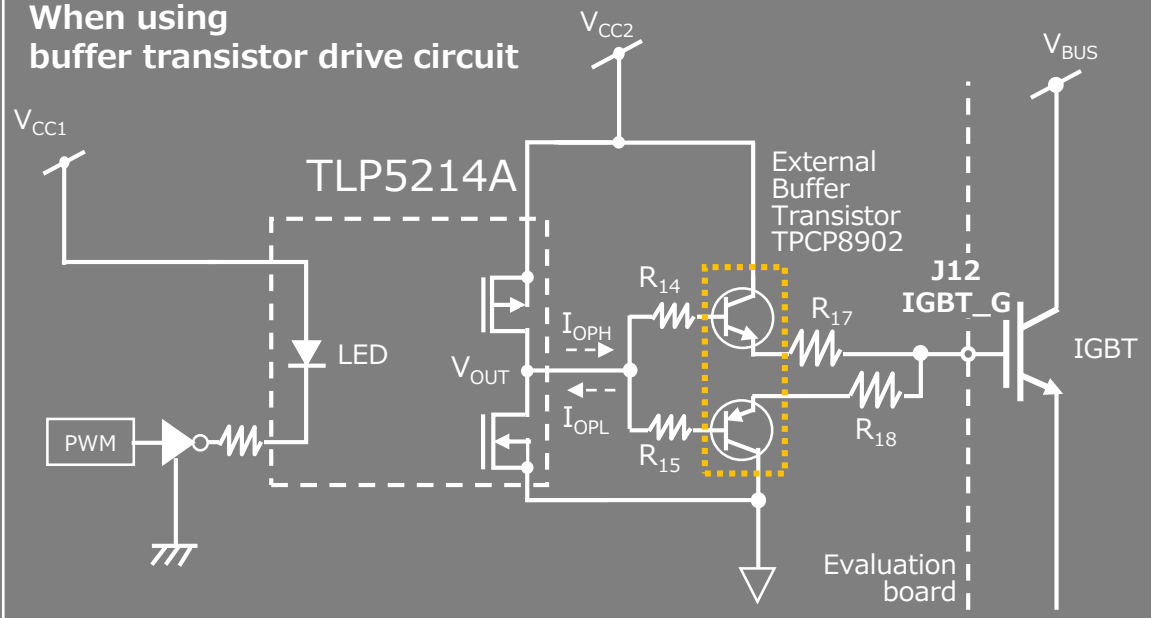


4. Appearance and Main Functions of Evaluation Board ②
Buffer Transistor Drive Circuit

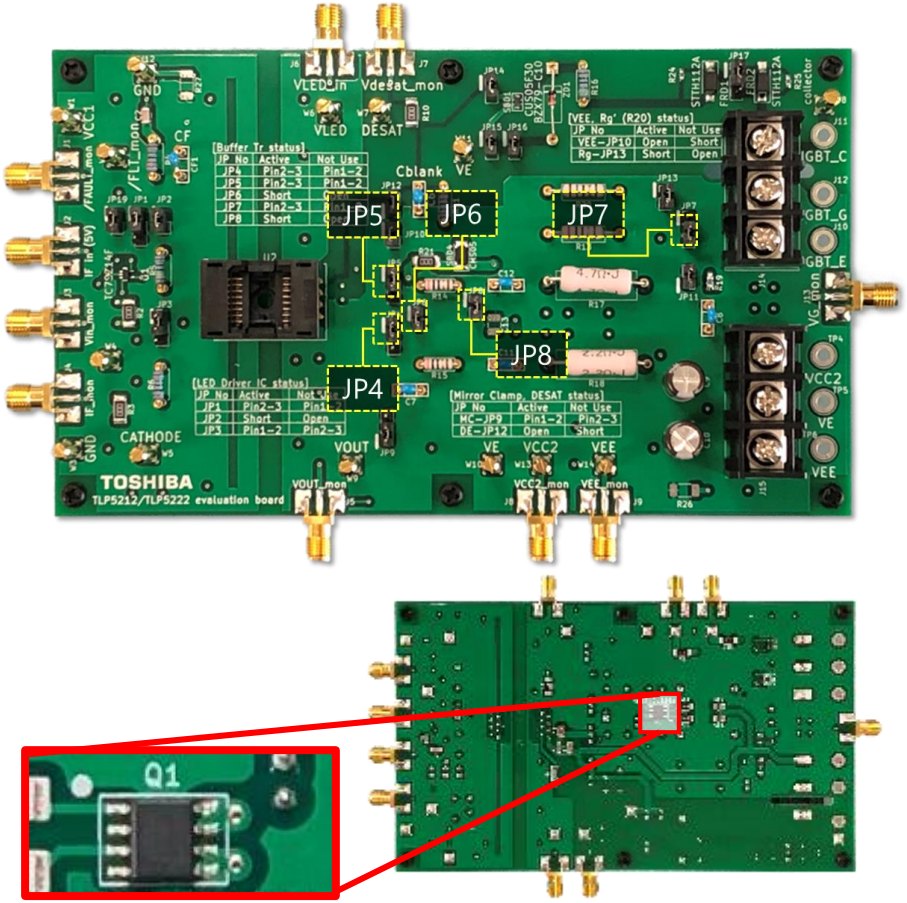
If the output current of the installed smart gate driver coupler does not provide enough gate drive capability for the subsequent power device, a buffer transistor (TPCP8902) is used to amplify the current.
When used, the base resistance/gate resistance, and capacitor constant are set according to the voltage conditions and output current.

Schematic

When using buffer transistor drive circuit

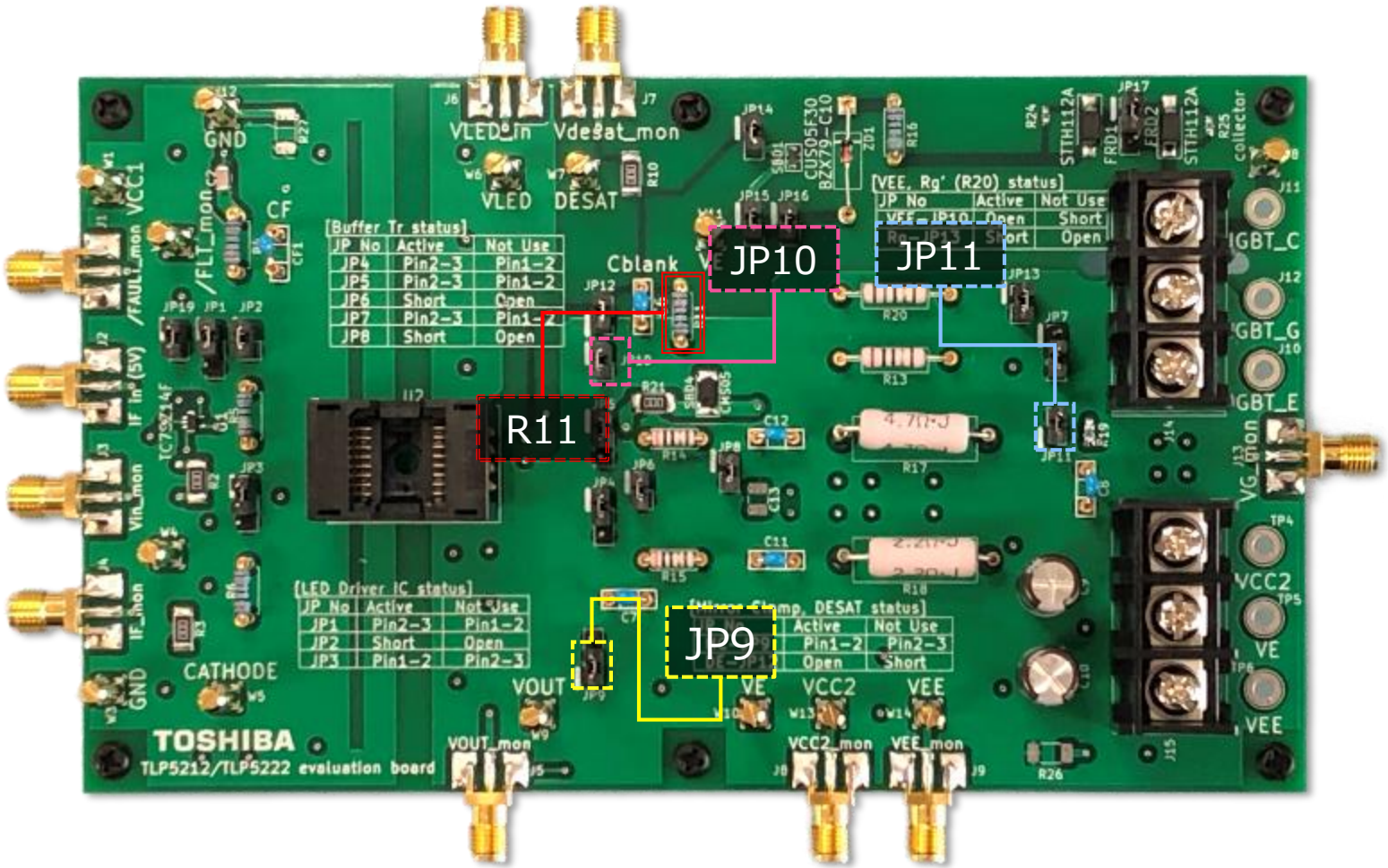


JP No.	When using	When not using
JP4	Connect 2-3pin	Connect 1-2pin
JP5	Connect 2-3pin	Connect 1-2pin
JP6	Short	Open
JP7	Connect 2-3pin	Connect 1-2pin
JP8	Short	Open



Backside of the board

4. Appearance and Main Functions of Evaluation Board ③



Active mirror clamp

Used to suppress malfunction caused by the mirror capacitance of the power device using the AMC function of the installed SGD.

JP No.	When using AMC	When not using AMC
JP9	Connect 1-2pin	Connect 2-3pin

Gate negative voltage power supply

When the power device is turned off, the gate potential is set negative to prevent false turn ON.
When a negative power supply is used, VE and VEE are separated and VEE is set to a negative potential.

JP No.	When using negative power supply	When using only positive power supply
JP10	Open	Short

External Cg

While adjusting the gate input capacitance, an external capacitive load Cg can used Instead of the gate input capacitance of the power device.

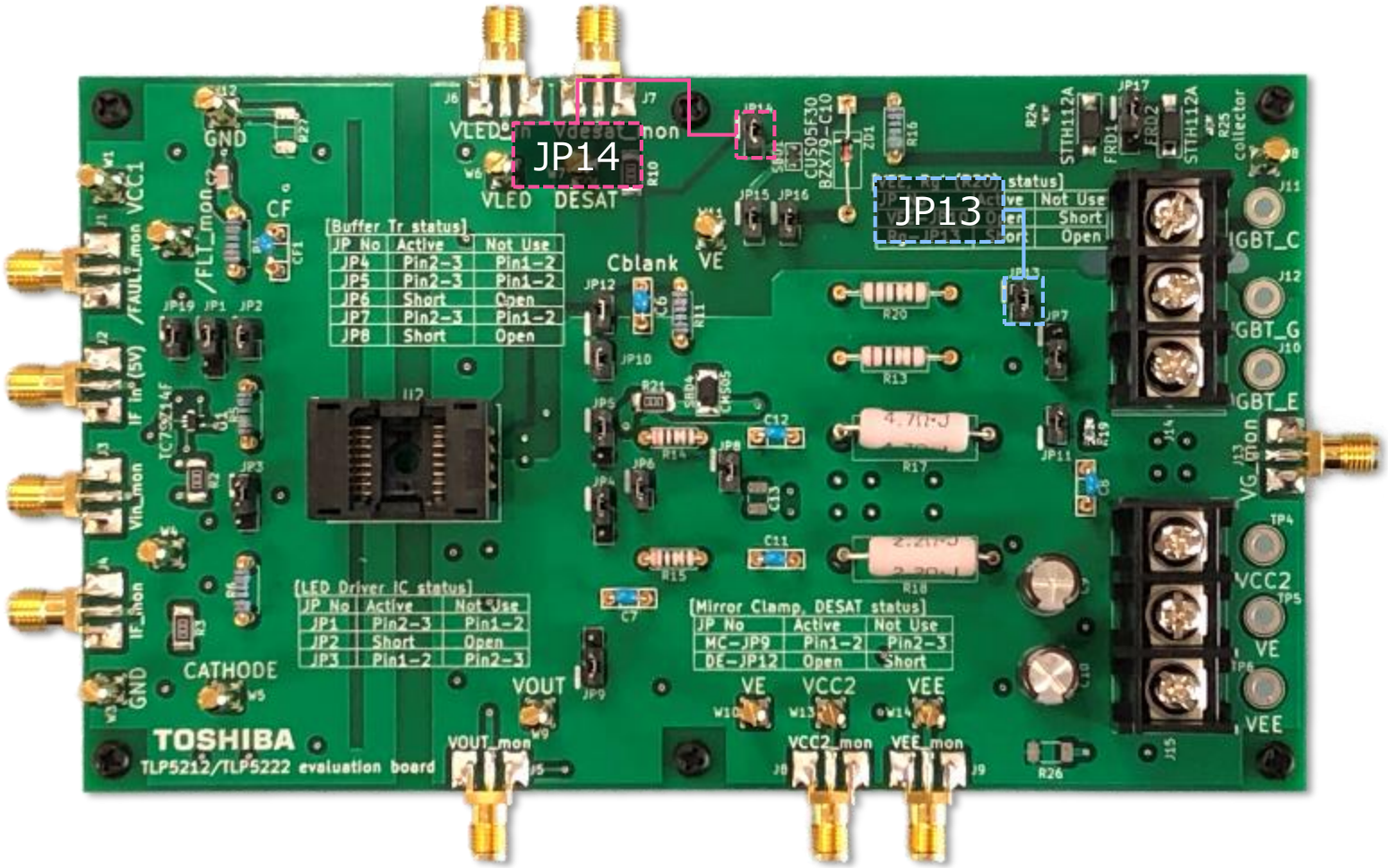
JP No.	When using external Cg	When not using external Cg
JP11	Short	Open

External blanking circuit

If the blanking capacitor is increased to prevent DESAT false detection due to noise, the detection of a short circuit by only ICHARGE of SGD gets delayed, so the current is supplied from this circuit to keep the blanking time within the short circuit tolerance of the power device.

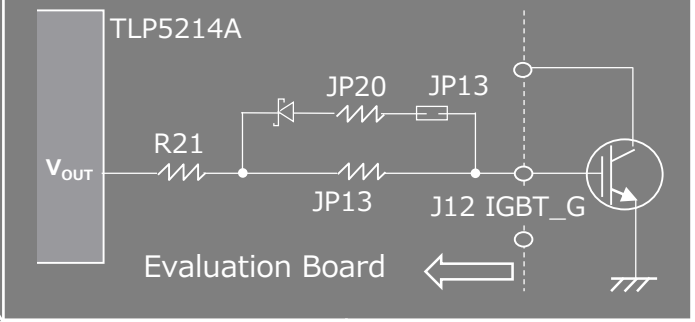
Part No.	Icharge enhancement	Without Icharge enhancement
R11	Resistance insertion (Default is 10 kΩ)	Open

4. Appearance and Main Functions of Evaluation Board ④



Gate resistor isolation function for on/off

This function is used when the user needs to set the gate resistor Rg independently for gate charging and discharging, respectively.

	Gate resistor isolation function for on/off is used/not used
Schematic	

JP No.	Independent use of Rg	When using a single Rg
JP13	Short	Open

Power device collector/drain terminal connection

Set to open when the collector / drain terminals of the power element are separated and evaluation and adjustment are performed using only the blanking capacitor.

JP No.	Power device connection enabled	Power device connection disabled
JP14	Short	Open

4. Appearance and Main Functions of the Evaluated Board ⑤
DESAT Function

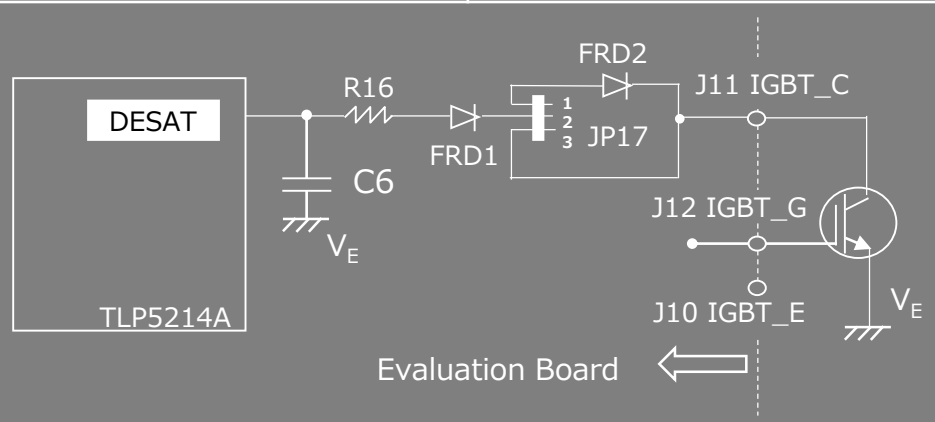
DESAT function
If SGD-protection feature is not required, short-circuit JP12 to deactivate DESAT detection feature.

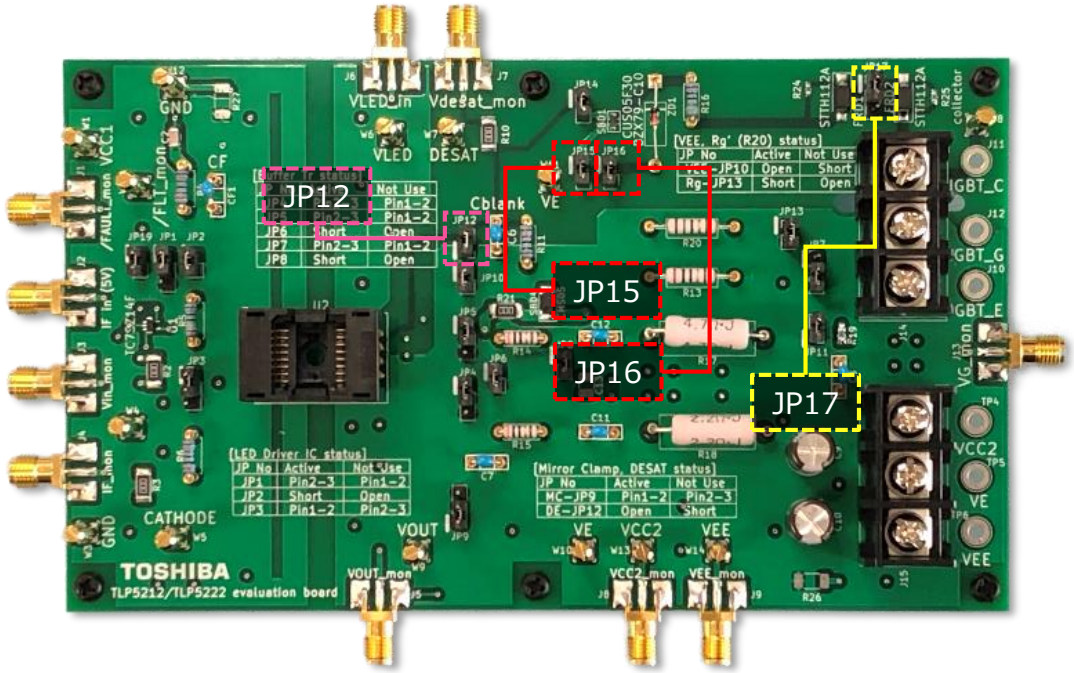
JP No.	When using DESAT	When not using DESAT
JP12	Open	Short

DESAT circuit protection device
They are basically short-circuited to protect DESAT terminal of SGD.

JP No.	When using protection device	When not using protection device
JP15	Short	Open
JP16	Short	Open

High Voltage Fast Recovery Diode (FRD)
The inverse withstand voltage of FRD1 is 1200 V, but if it is insufficient, add a FRD2 with a 1200 V inverse withstand voltage as well.

DESAT function	FRD1 only	FRD1 + FRD2
Schematic / JP No.		
JP17	Connect 2-3pin	Connect 1-2pin



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