32-bit RISC Microcontroller

TXZ+ Family
TMPM3H Group(2)

Reference Manual
Clock Control and Operation Mode
(CG-M3H(2)-D)

Revision 1.1

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Conventions

- Numeric formats follow the rules as shown below:
  Hexadecimal: 0xABC
  Decimal: 123 or 0d123 - Only when it needs to be explicitly shown that they are decimal numbers.
  Binary: 0b111 - It is possible to omit the "0b" when the number of bits can be distinctly understood from a sentence.
- "_N" is added to the end of signal names to indicate low active signals.
- It is called "assert" that a signal moves to its active level, "deassert" to its inactive level.
- When two or more signal names are referred, they are described like as [m:n].
  Example: S[3:0] shows four signal names S3, S2, S1 and S0 together.
- The characters surrounded by ***[ ]*** defines the register.
  Example: ***[ABCD]***
- "N" substitutes suffix number of two or more same kind of registers, fields, and bit names.
  Example: ***[XYZ1]***, ***[XYZ2]***, ***[XYZ3]*** → ***[XYZn]***
- "x" substitutes suffix number or character of units and channels in the register list.
- In case of unit, "x" means A, B, and C, ...
  Example: ***[ADACR0]***, ***[ADBCR0]***, ***[ADCCR0]*** → ***[ADxCR0]***
- In case of channel, "x" means 0, 1, and 2, ...
  Example: ***[T32A0RUNA]***, ***[T32A1RUNA]***, ***[T32A2RUNA]*** → ***[T32AxRUNA]***
- The bit range of a register is written like as [m: n].
  Example: Bit[3: 0] expresses the range of bit 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.
  Example: ***[ABCD]***<EFG> = 0x01 (hexadecimal), ***[XYZn]***<VW> = 1 (binary)
- Word and byte represent the following bit length.
  Byte: 8 bits
  Half word: 16 bits
  Word: 32 bits
  Double word: 64 bits
- Properties of each bit in a register are expressed as follows:
  R: Read only
  W: Write only
  R/W: Read and write are possible.
- Unless otherwise specified, register access supports only word access.
- The register defined as "Reserved" must not be rewritten. Moreover, do not use the read value.
- The value read from the bit having default value of "-" is unknown.
- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value, In the cases that default is "-", follow the definition of each register.
- Reserved bits of the write-only register should be written with their default value. In the cases that default is "-", follow the definition of each register.
- Do not use read-modified-write processing to the register of a definition which is different by writing and read out.

Terms and Abbreviations

Some of abbreviations used in this document are as follows:

ADC	Analog to Digital Converter
A-ENC32	Advanced Encoder Input Circuit (32bit)
APB	Advanced Peripheral Bus
A-PMD	Advanced Programmable Motor Control Circuit
CG	Clock Control and Operation Mode
COMP	Comparator
CRC	Cyclic Redundancy Check
DAC	Digital to Analog Converter
DMAC	Direct Memory Access Controller
DNF	Digital Noise Filter
ELOSC	External Low-speed Oscillator
EHOSC	External High-speed Oscillator
EI2C	I^2C Interface Version A
fsys	Frequency of SYSTEM Clock
I2C	Inter-integrated Circuit
I2CS	Wake-up Function by Address Matching
IHOSC	Internal High-speed Oscillator
IA(INTIF)	Interrupt Control Register A
IB(INTIF)	Interrupt Control Register B
I-Bus	Icode Memory Interface
IMN	Interrupt Monitor
INT	Interrupt
IO	IO Bus (32-bit Peripheral Bus)
DLCD	LCD Display Control Circuit
LVD	Voltage Detection Circuit
NMI	Non-Maskable Interrupt
OFD	Oscillation Frequency Detector
POR	Power-on Reset Circuit
PORF	Power-on Reset Circuit for FLASH and Debug
RAMP	RAM Parity Circuit
RLM	Low-speed Oscillation/Power Supply Control/reset
RMC	Remote Control Signal Preprocessor
RTC	Real Time Clock
S-Bus	System Interface
SCOUT	Source Clock Output
SIWDT	Clock Selective Watchdog Timer
TPIU	Trace Port Interface Unit
TRGSEL	Trigger Selection Circuit
TRM	Trimming Circuit
TSPI	Serial Peripheral Interface
T32A	32-Bit Timer Event Counter
UART	Universal Asynchronous Receiver Transmitter

1. Clock Control and Operation Mode

1.1. Outlines

The clock/mode control block can select a clock gear and prescaler clock and set the warmup of oscillator and so on.

Furthermore, it has NORMAL mode and a low-power consumption mode in order to reduce power consumption using mode transition.

Functions related to a clock are as follows.

- System clock control
- Prescaler clock control

1.2. Clock Control

1.2.1. Clock Type

This section shows a list of clocks.

EHCLKIN:	The clock input from the external.
fosc:	A clock generated in the internal oscillation circuit or input from the X1 and X2 pins
f_{PLL}:	A clock multiplied by PLL
fc:	A clock selected by ***[CGPLL0SEL]***<PLL0SEL> (high-speed clock)
fs:	A clock output from an external low-speed oscillator
fsys:	A system clock selected by ***[CGSYSCR]***<GEAR[2:0]>
ΦT0:	A clock selected by ***[CGSYSCR]***<PRCK[3:0]> (prescaler clock)
f_{IHOSC1}:	A clock generated with the internal high-speed oscillator 1
f_{IHOSC2}:	A clock generated with the internal high-speed oscillator 2
ADCLK:	A conversion clock for AD converter
TRCLKIN:	A clock for tracing facilities of a debugging circuit (Trace/SWV)

1.2.2. Initial Value by Reset Operation

A clock setting is initialized to the following states by a reset operation.

External high-speed oscillator:	Stop
Internal high-speed oscillator 1:	Oscillation
Internal high-speed oscillator 2:	Stop
External low-speed oscillator:	Stop
PLL (multiplying circuit):	Stop
Gear clock:	fc (no frequency dividing)

1.2.3. Clock System Diagram

The figure below shows a clock system diagram.

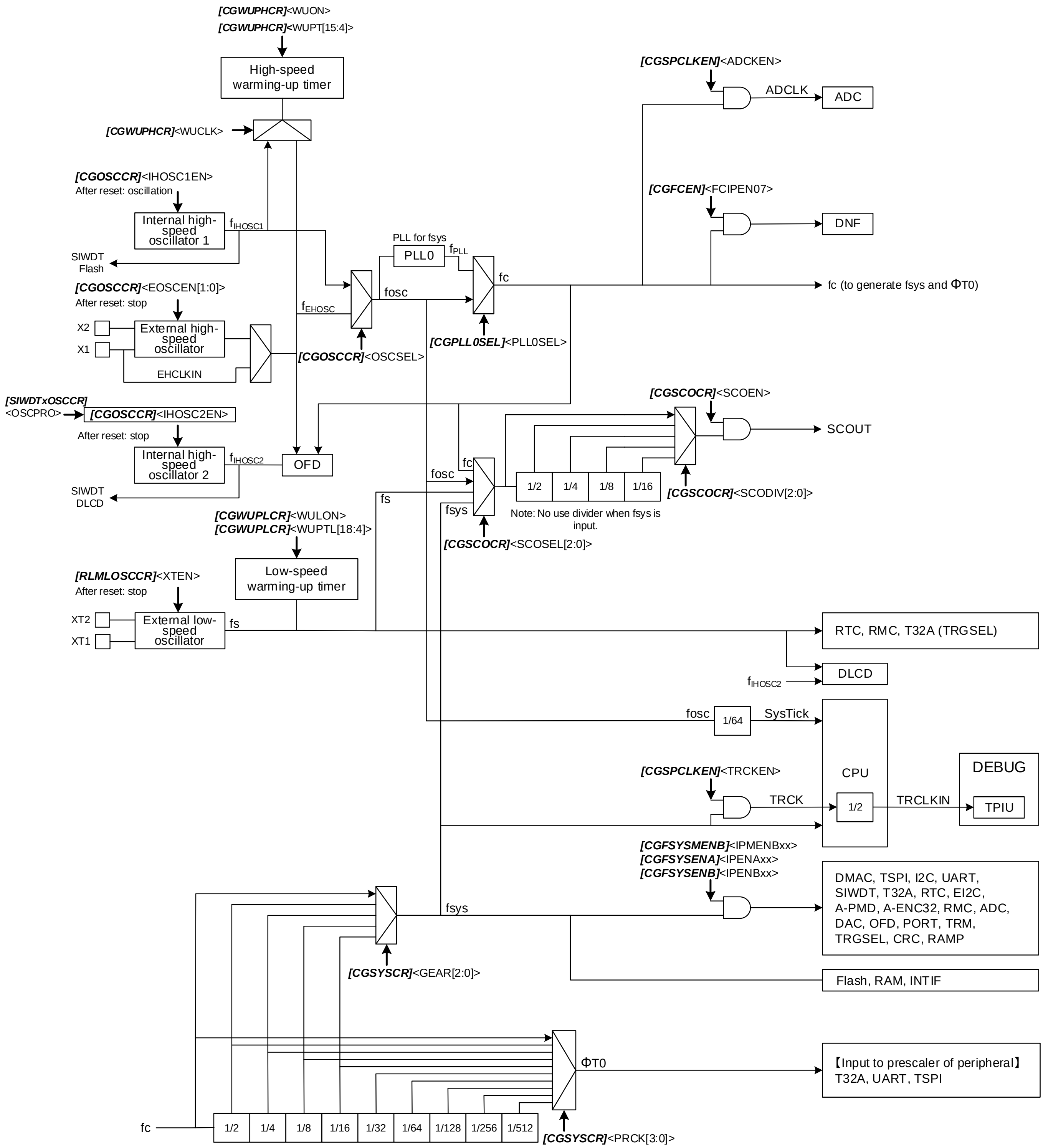

Figure 1.1 Clock System Diagram

1.2.4. Warming-up Function

A warming-up function is used to secure the oscillation stable time at the time of the STOP1 mode release which starts the warming-up timer for high-speed oscillation automatically.

It is available also as a count up timer which uses the exclusive warming-up timer of high-speed clock /each low-speed clock for the waiting for the stability of an external oscillator or an internal oscillator.

This chapter explains the setting method to the register for warming-up timers, and the case where it is used as a count up timer. The detailed explanation at the time of STOP1 mode release, refer to "1.3.3.2 Warming Up at Release of Low-power Consumption Mode".

1.2.4.1. Warming-up Timer for High-speed Oscillation

A 16-bit up counter is built in as a warming-up timer only for a high-speed oscillation. Also, when setting before changing to the STOP1 mode, the setting value is calculated in the following formula, set ***[CGWUPHCR]***<WUPT[15:4]> to the upper 12 bits of the setting value. Lower 4 bits are ignored.

＜Formula＞

(When using external high-speed oscillator)

Warming-up timer setting value (16 bits) = (warming-up time (s) / clock period (s)) -16

(Example) When 5 ms of warming-up time is set up with 10MHz (100ns of clock periods) of oscillators

Warming-up timer setting value (16 bits) = (5ms / 100ns) - 16
= 50000 - 16
= 49984
= 0xC340

Since upper 12 bits are set to a register, they are set as follows.

[CGWUPHCR]<WUPT[15:4]> = 0xC34

(When using internal oscillator 1)

Warming-up timer setting value (16 bits) = ((warming-up time (s) -63.3 (μs)) / clock period (s)) -41

(Example) When 163.4μs of warming-up time is set up with 10MHz (100ns of clock periods) of oscillators

Warming-up timer setting value (16 bits) = ((163.4-63.3) / 100ns) - 41
= (100.1μs / 100ns) - 41
= 960
= 0x03C0

Since upper 12 bits are set to register, they are set as follows.

[CGWUPHCR]<WUPT[15:4]> = 0x03C

In the case of 10MHz, the setting range is 0x03C ≤ <WUPT[15:4]> ≤ 0xFFF, the warming-up time is set from 163.4μs to 6.6194ms.

1.2.4.2. Warming-up Timer for Low-speed Oscillation

A 19-bit up-timer is built in as a warming-up timer only for a low-speed oscillation. The setting value is calculated in the following formula, set ***[CGWUPLCR]***<WUPT[18:4]> to the upper 15 bits of the setting value. Lower 4 bits are ignored. 16 is subtracted in order to perform the count for 4 bits of low ranks, even when a set point is "0".

＜Formula＞

Warming-up timer setting value (19 bits)
= (warming-up time (s) / clock period (s)) - 16

(Example) When 50ms of warming-up time is set up with 32kHz (clock period 31.25μs) of oscillators

Warming-up timer setting value (19 bits) = (50ms / 31.25μs) - 16
= 1600 - 16
= 1584
= 0x00630

Since upper 15 bits are set to a register, they are set as follows.

[CGWUPLCR]<WUPTL[18:4]> = 0x0063

In the case of 32kHz, the setting range is 0 ≤ <WUPTL[18:4]> ≤ 0x7FFF, the warming-up time is set from 500μs to 16.384s.

1.2.4.3. Directions for Warming-up Timer

The directions for a warming-up function are explained.

(1) Selection of a clock
In a high-speed oscillation, the clock classification (internal oscillation/external oscillation) counted with a warming-up timer is selected by ***[CGWUPHCR]***<WUCLK>.

(2) Calculation of warming-up timer setting value
The warming-up time can set any value to the timer for a high-speed oscillation/for a low-speed oscillation. Please compute and set up from each formula.

(3) The start of warming-up, and termination confirmation
When software (instruction) performs to start warming-up and to confirms termination of warming-up, a warming-up timer starts by setting ***[CGWUPHCR]***<WUON> (or ***[CGWUPLCR]***<WULON>) to "1". Termination is confirmed with ***[CGWUPHCR]***<WUEF> (or ***[CGWUPLCR]***<WULEF>) that becomes from "1" to "0". "1" indicates under warming-up and "0" indicates termination. After a counting end, a timer is reset and returns to an initial state.
It is not forced to terminate, although "0" is written to [CGWUPHCR]<WUON> (or ***[CGWUPLCR]***<WULON>) during timer operation. Writing "0" is ignored.

Note: Since it is operating with the oscillating clock, a warming-up timer includes an error, when Oscillation frequency has fluctuation. Therefore, it should be taken as an approximate time.

1.2.5. Clock Multiplying Circuit (PLL) for fsys

The clock multiplying circuit outputs the fPLL clock (up to 120MHz) multiplied by the optimum condition for the frequency (6MHz to 12MHz) of the output clock fosc of the high-speed oscillator.

So, it is possible to make the input frequency to an oscillator low-speed and to make an internal clock high-speed by this circuit.

1.2.5.1. PLL Setup after Reset Release

The PLL is disabled after reset release.

In order to use the PLL, set ***[CGPLL0SEL]***<PLL0SET> to a multiplication value while ***[CGPLL0SEL]*** <PLL0ON> is "0". Then wait until approximately 100 µs has elapsed as a PLL initial stabilization time, and set <PLL0ON> to "1" to start PLL operation.

After that, to use f_{PLL} clock which is multiplied fosc, wait until approximately 400 µs has elapsed as a lock up time. Then set "1" to ***[CGPLL0SEL]***<PLL0SEL>.

Note that a warming-up time is required until PLL operation becomes stable using the warming-up function, etc.

1.2.5.2. Formula and Example of Setting of PLL Multiplication Value

The details of the items of ***[CGPLL0SEL]***<PLL0SET[23:0]> which set up a PLL multiplication value are shown below.

Table 1.1 Details of *[CGPLL0SEL]*<PLL0SET[23:0]> Setup

Items of PLL0SET	Function	
[23:17]	Correction value setting	The quotient of fosc/450k (integer). For detail refer to Table 1.2
[16:14]	fosc setting	000: 6 ≤ fosc ≤ 7 001: 7 < fosc ≤ 8 010: 8 < fosc ≤ 10 011: 10 < fosc ≤ 12 100: 12 < fosc ≤ 15 101: 15 < fosc ≤ 19 110: 19 < fosc ≤ 24 111: Reserved (Unit: MHz)
[13:12]	Dividing setting	00: Reserved 01: 2 dividing (× 1 / 2) 10: 4 dividing (× 1 / 4) 11: 8 dividing (× 1 / 8)
[11:8]	Fraction part of multiplication setting	0000: 0.0000 0001: 0.0625 0010: 0.1250 0011: 0.1875 0100: 0.2500 0101: 0.3125 0110: 0.3750 0111: 0.4375 1000: 0.5000 1001: 0.5625 1010: 0.6250 1011: 0.6875 1100: 0.7500 1101: 0.8125 1110: 0.8750 1111: 0.9375
[7:0]	Integer part of multiplication setting	0x00: 0 0x01: 1 0x02: 2 : 0xFD: 253 0xFE: 254 0xFF: 255

Note: A multiplication value is the total of <PLL0SET[7:0]> (integer part) and <PLL0SET[11:8]> (fraction part).

f_{PLL} is denoted by the following formulas.

f_{PLL} = fosc× (***[CGPLL0SEL]***<PLL0SET[7:0]> + ***[CGPLL0SEL]***<PLL0SET[11:8]>) ×
(***[CGPLL0SEL]*** <PLL0SET[13:12]>)

Note1. The absolute value of frequency accuracy is not guaranteed.
Note2. There is no Linearity in the frequency by the fractional part of multiplication setting.
Note3: $f_{PLL} \leq$ Maximum operating frequency

Table 1.2 PLL Correction Value (example)

fosc (MHz)	<PLL0SET[23:17]> (decimal, integral value)
6.00	14
8.00	18
10.00	23
12.00	27

A PLL correction value can be calculated below.

When fosc = 6.0MHz, 6.0 / 0.45 = 13.33 ≈ 14 ; fractional part is rounded up.

The main examples of a setting of ***[CGPLL0SEL]***<PLL0SET[23:0]> are shown below.

(1) It multiplies by PLL, and dividing is carried out and the target Clock frequency (f_{PLL}) is generated for input frequency (fosc).
(2) A dividing value is chosen from 1 / 2, 1 / 4, and 1 / 8.
(3) Moreover, set up the frequency after multiplication in the following ranges.
200MHz ≤ (fosc × multiplication value) ≤ 320MHz

Table 1.3 PLL0SET Setting Value (example)

fosc (MHz)	Multiplication value	Dividing value	f_{PLL} (MHz)	<PLL0SET[23:0]>
6.00	40.0000	1/2	120.00	0x1C1028
8.00	30.0000	1/2	120.00	0x24501E
10.00	24.0000	1/2	120.00	0x2E9018
12.00	20.0000	1/2	120.00	0x36D014
6.00	53.3125	1/4	79.97	0x1C2535
8.00	40.0000	1/4	80.00	0x246028
10.00	32.0000	1/4	80.00	0x2EA020
12.00	26.6250	1/4	79.88	0x36EA1A
6.00	53.3125	1/8	39.98	0x1C3535
8.00	40.0000	1/8	40.00	0x247028
10.00	32.0000	1/8	40.00	0x2EB020
12.00	26.6250	1/8	39.94	0x36FA1A

1.2.5.3. Change of PLL Multiplication Value under Operation

It changes to a setup which sets "0" to ***[CGPLL0SEL]***<PLL0SEL> first, and does not use a PLL multiplication clock during PLL multiplication clock operation when changing a multiplication value. And ***[CGPLL0SEL]*** <PLL0ST> = 0 is read, after checking having changed to a setup which does not use a multiplication clock, ***[CGPLL0SEL]***<PLL0ON> is set to "0", and PLL is stopped.

Then, the multiplication value of ***[CGPLL0SEL]***<PLL0SET> is changed, as reset time of PLL, after about 100µs progress, ***[CGPLL0SEL]***<PLL0ON> is set to "1", and operation of PLL is started.

Then, ***[CGPLL0SEL]***<PLL0SEL> is set to "1" after locking up time (about 400µs) has elapsed.

Finally, ***[CGPLL0SEL]***<PLL0ST> is read and it checks having changed.

1.2.5.4. PLL Operation Start/stop/switching Procedure

(1) fc setup (PLL stop → PLL start)
As an fc setup, the example of switching procedure from the PLL stop state to the PLL operation state is as follows.

<<State before switching>>	
[CGPLL0SEL]<PLL0ON> = 0	Stop the PLL operation for fsys.
[CGPLL0SEL]<PLL0SEL> = 0	Select the setting of the PLL for fsys to "PLL is unused (fosc)".
[CGPLL0SEL]<PLL0ST> = 0	Indicate the status of the PLL for fsys to "PLL is unused (fosc)".

<<Example of switching procedure>>		
1	***[CGPLL0SEL]***<PLL0SET> = 0xX	A PLL multiplication value setup is chosen.
2	Wait 100µs or more	Latency time after a multiplication setup
3	***[CGPLL0SEL]***<PLL0ON> = 1	PLL operation for fsys is carried out to an oscillation.
4	Wait 400µs or more	PLL output clock stable latency time
5	***[CGPLL0SEL]***<PLL0SEL> = 1	PLL selection for fsys is carried out to PLL use (f_{PLL}).
6	Read ***[CGPLL0SEL]***<PLL0ST>	It waits until the PLL selection status for fsys becomes "PLL use (f_{PLL}) (= 1)".

Note: 1 to 4 is unnecessary when the state before switching is ***[CGPLL0SEL]***<PLL0ON> = 1. When changing from the state where the PLL Output clock was stabilized, it can change to the conduct PLL state by execution of only 5 and 6.

(2) fc setup (PLL operation → PLL stop)
As an fc setup, the example of switching procedure from the PLL operation state to a PLL stop state is as follows.

<<State before switching>>	
[CGPLL0SEL]<PLL0ON> = 1	Set the PLL oscillation for fsys.
[CGPLL0SEL]<PLL0SEL> = 1	Select the PLL for fsys to "PLL is used (f_{PLL})".
[CGPLL0SEL]<PLL0ST> = 1	Indicate the status of the PLL for fsys to "PLL is used (f_{PLL})".

<<Example of switching procedure>>		
1	***[CGPLL0SEL]***<PLL0SEL> = 0	Select the PLL for fsys to "PLL is unused (fosc)".
2	***[CGPLL0SEL]***<PLL0ST> , it read.	Wait until the status of the PLL for fsys becomes "PLL is unused (fosc) (= 0)".
3	***[CGPLL0SEL]***<PLL0ON> = 0	Set the PLL operation for fsys to stop.

1.2.6. System Clock

An internal high-speed oscillation clock or external high-speed oscillation clock (connected oscillator or clock input) can be used as a source of system clock.

Dividing is possible for a system clock at ***[CGSYSCR]***<GEAR[2:0]> (clock gear). Although a setup can be changed during operation, after register writing before a clock actually changes, a maximum of 16-clock time is required of fc. Check completion of a clock change by ***[CGSYSCR]***<GEARST[2:0]>.

Note: Do not change a clock gear during operation of peripheral functions, such as a timer counter.

Table 1.4 shows the example of operation frequency by the clock gear ratio (1/1 to 1/16) to the frequency fc set up with oscillation frequency, a PLL multiplication value, etc.

Table 1.4 Example of Operation Frequency

External oscillation (MHz)	External clock input (MHz)	Internal oscillation IHOSC1 (MHz)	PLL multiplication value (after dividing)	Maximum frequency (fc) (MHz)	Operating frequency (MHz) by clock gear ratio when PLL = ON					Operating frequency (MHz) by clock gear ratio Clock gear when PLL = OFF				
					1/1	1/2	1/4	1/8	1/16	1/1	1/2	1/4	1/8	1/16
6	6	-	20	120	120	60	30	15	7.5	6	3	1.5	-	-
8	8	-	15	120	120	60	30	15	7.5	8	4	2	1	-
10	10	10	12	120	120	60	30	15	7.5	10	5	2.5	1.25	-
12	12	-	10	120	120	60	30	15	7.5	12	6	3	1.5	-
6	6	-	13.329	79.97	79.97	39.99	20	10	5	6	3	1.5	-	-
8	8	-	10	80	80	40	20	10	5	8	4	2	1	-
10	10	10	8	80	80	40	20	10	5	10	5	2.5	1.25	-
12	12	-	6.657	79.88	79.88	39.95	19.98	9.99	4.99	12	6	3	1.5	-
6	6	-	6.625	39.75	39.75	19.9	9.94	4.97	2.48	6	3	1.5	-	-
8	8	-	5	40	40	20	10	5	2.5	8	4	2	1	-
10	10	10	4	40	40	20	10	5	2.5	10	5	2.5	1.25	-
12	12	-	3.3125	39.75	39.75	19.9	9.94	4.97	2.48	12	6	3	1.5	-

1.2.6.1. Setting Method of System Clock

(1) fosc setup (internal oscillation → external oscillation)
As a fosc setup, the example of switching procedure to the external oscillation (EHOSC) from an internal oscillation (IHOSC1) is shown below.

<<State before switching>>	
[CGOSCCR]<IHOSC1EN> = 1	An internal high-speed oscillator 1 oscillates.
[CGOSCCR]<OSCSEL> = 0	The high-speed oscillation selection for fosc is an inside (IHOSC1).
[CGOSCCR]<OSCF> = 0	The high-speed oscillation selection status for fosc is an inside (IHOSC1).
An oscillator is connected to X1 and X2 pins. (Note)	-

Note: Do not connect except a resonator.

<<Example of switching procedure>>		
1	***[PHPDN]***<bit[1:0]> = 00 ***[PHIE]***<bit[1:0]> = 00	Disable the pull-down of X1/X2 pin. Disable input control of X1/X2 pin.
2	***[CGOSCCR]***<EOSCEN[1:0]> = 01	It is an external oscillation (EHOSC) about selection of an external oscillation of operation.
3	***[CGWUPHCR]***<WUCLK> = 1 ***[CGWUPHCR]***<WUPT[18:4]> = "arbitrary value"	It is the external (EHOSC) about high-speed oscillation warming-up clock selection. Oscillator stable time is set to a warming-up timer setting value.
4	***[CGWUPHCR]***<WUON> = 1	High speed oscillation warming-up is started.
5	***[CGWUPHCR]***<WUEF> is read.	It waits until it becomes the termination of high-speed oscillation warming up (= 0).
6	***[CGOSCCR]***<OSCSEL> = 1	It is high-speed oscillation selection for fosc to the exterior (EHOSC).
7	***[CGOSCCR]***<OSCF> is read.	It waits until the high-speed oscillation selection status for fosc becomes outside (= 1).
8	***[CGOSCCR]***<IHOSC1EN> = 0	An internal high-speed oscillator 1 is suspended.

(2) fosc setup (internal oscillation → external clock input)
As a fosc setup, the example of switching procedure to the external clock input (EHCLKIN) from an internal oscillation 1 (IHOSC1) is shown below.

<<State before switching>>	
[CGOSCCR]<IHOSC1EN> = 1	An internal high-speed oscillator 1 oscillates.
[CGOSCCR]<OSCSEL> = 0	The high-speed oscillation selection for fosc is an inside (IHOSC1).
[CGOSCCR]<OSCF> = 0	The high-speed oscillation selection status for fosc is an inside (IHOSC1).
Clock input to EHCLKIN	Input in the proper voltage range.

<<Example of switching procedure>>		
1	***[PHPDN]***<bit[0]> = 0 ***[PHIE]***<bit[0]> = 0	Disable the pull-down of X1/EHCLKIN pin. Disable the input control of an X1/EHCLKIN pin.
2	***[CGOSCCR]***<EOSCEN[1:0]> = 10	Selection of an external oscillation of operation is carried out to an external clock input (EHCLKIN).
3	***[CGOSCCR]***<OSCSEL> = 1	It is high-speed oscillation selection for fosc to an external clock.
4	***[CGOSCCR]***<OSCF> is read.	It waits until the high-speed oscillation selection status for fosc becomes outside (= 1).
5	***[CGOSCCR]***<IHOSC1EN> = 0	An internal high-speed oscillator 1 is suspended.

(3) fosc setup (an external oscillation/external clock input → an internal oscillation)
As a fosc setup, the example of switching procedure to the internal oscillation (IHOSC1) from an external oscillation (EHOSC) or an external clock input (EHCLKIN) is shown below.

<< State before switching >>	
[CGOSCCR]<EOSCEN[1:0]> = 01 or 10	Selection of an external oscillator of operation is an external oscillator (EHOSC) or external clock input.
[CGOSCCR]<OSCSEL> = 1	The high-speed oscillation selection for fosc is the exterior (EHOSC).
[CGOSCCR]<OSCF> = 1	The high-speed oscillation selection status for fosc is the exterior (EHOSC).

<< Example of switching procedure >>		
1	***[CGWUPHCR]***<WUCLK> = 0	Set the warming-up clock selection to internal high-speed oscillator 1 (IHOSC1).
2	***[CGWUPHCR]***<WUPT[15:4]> = 0x03C	Set the high-speed oscillation warming-up timer setting value of 163.4μs (= 0x3C) or more.
3	***[CGOSCCR]***<IHOSC1EN> = 1	An internal high-speed oscillator 1 oscillates.
4	***[CGWUPHCR]***<WUON> = 1	Start the high-speed oscillation warming-up timer
5	***[CGWUPHCR]***<WUEF> is read.	Wait until a warming-up timer status flag becomes ends (= 0).
6	***[CGOSCCR]***<OSCSEL> = 0	Set the high-speed oscillation selection for fosc to internal high-speed oscillator1 (IHOSC1).
7	***[CGOSCCR]***<OSCF> is read.	It waits until the high-speed oscillation selection status for fosc becomes an inside (= 0).
8	***[CGOSCCR]***<EOSCEN[1:0]> = 00	Set the selection of an external oscillator operation to unused.

1.2.7. Clock Supply Setting Function

This MCU has the clock on/off function for the peripheral circuits. To reduce the power consumption, this CPU can stop supplying the clock to the peripheral functions that are not used.

Except some peripheral functions, clocks are not supplied after reset.

In order to supply the clock of the function to be used, set the bit of relevance of ***[CGFSYSENA]***, ***[CGFSYSENB]***, ***[CGFSYSMENB]*** and ***[CGSPCLKEN]*** to "1".

For details, refer to "1.5. Explanation of Register".

1.2.8. Clock Output Function to Pin

This MCU has the clock output function to the pin. A low-speed clock "fs", high-speed oscillation clock "fosc", high-speed clock "fc", system clock "fsys" can be output from the SCOUT pin.

For details, refer to "1.4.2.5. *[CGSCOCR]* (SCOUT Output Control Register)".

The below table shows the use propriety state of SCOUT pin in each operation mode.

Table 1.5 List of Using SCOUT Pin in Each Operation Mode

Signal selection from SCOUT	Operation mode		
	NORMAL/IDLE	STOP1	STOP2
fosc	Yes	N/A	N/A
fc	Yes	N/A	N/A
fs	Yes	Yes	N/A
fsys	Yes	N/A	N/A

Yes: Signal can be output., N/A: Signal cannot be output.

1.2.9. Prescaler Clock

Each peripheral function has a Prescaler circuit to divide the ΦT0 clock. The ΦT0 clock inputted into the prescaler circuit can be divided by the ***[CGSYSCR]***<PRCK[3:0]>. As for ΦT0 clock after reset, fc is selected.

After register writing before a clock actually changes, a time up to 512-clock of fc is required. To confirm the completion of the clock changed, check the status of ***[CGSYSCR]***<PRCKST[3:0]>.

Note: Do not change a prescaler clock during operation of peripheral functions, such as a timer counter.

1.3. Operation Mode

There are NORMAL mode and a low-power consumption mode (IDLE, STOP1, STOP2) in TMPM3H Group(2) as an operation mode, and it can reduce power consumption by performing mode changes according to directions for use.

1.3.1. Details of Operation Mode

1.3.1.1. Feature in Each Mode

The feature in NORMAL, low-power consumption mode are follows.

- NORMAL mode
  It is a mode to operate a CPU core and peripheral circuits by a high-speed oscillation clock. After the reset release, operation mode is NORMAL mode.

- Low-power consumption mode
  Low-power consumption mode is as following.

  - IDLE mode
    It is the mode which CPU stops.
    The peripheral function should perform operation/stop by the register of each peripheral function, a clock supply setting function, etc.

Note: CPU cannot clear the watchdog timer in IDLE mode.

  - STOP1 mode
    It is the mode which all the internal circuits also including an internal oscillator stop.
    However, when an external low-speed oscillator is oscillated and it shifts to the STOP1 mode, the RTC operates.
    If the STOP1 mode is released, an internal high-speed oscillator1 (IHOSC1) will start, and operation mode will return to NORMAL mode.
    Please disable interrupt which is not used for STOP1 release before shifting to the STOP1 mode.

  - STOP2 mode
    It is the mode which holds a part of the function and cut off an internal electrical power source. STOP1 Consumption of electric power larger than the STOP2 mode can be held down. If the STOP2 mode is released, the power supply will be switched on to the Main power domain, a reset sequence will be performed, and it will return to NORMAL mode.
    As for the Main power domain, it is a function which does not supply a power supply in STOP2 mode.

Before shifting to the STOP2 mode, disable an interrupt which is not made into a release STOP2, please be sure to set up ***[RLMSHTDNOP]***<PTKEEP> = 1 and to hold the state of each port.

An Output/Pull up holds, and input permission holds a state when it sets as a port keeping function. In addition, external interrupt continues an input.

The product will be cut off the power except for the following circuit in STOP2 mode.

- External low-speed oscillator (ELOSC)
- RTC
- Backup RAM
- Port pin status
- LVD
- RLM
- IA
- I2CS
- DLCD

Regarding a power supply cutoff in the Low power Consumption mode, for details, refer to "1.3.1.4. Peripheral Function State in Low-power Consumption Mode".

1.3.1.2. Pow-power Consumption Mode

In order to shift to each low-power consumption mode, the IDLE/STOP1/STOP2 mode is chosen by standby control register ***[CGSTBYCR]***<STBY[1:0] >, and a WFI command is executed. When it shifts to a low-power consumption mode by WFI command, the restart operation from a low-power consumption mode is performed by reset or interrupt generating. To return by an interrupt, it is necessary to set up. Please refer to "Interrupt" chapter of the reference manual "Exception" for details.

Note1: TMPM3H Group(2) does not support a return by events; therefore, do not make a transition to low-power consumption mode triggered by WFE (Wait For Event).

Note2: TMPM3H Group(2) does not support low-power consumption mode by SLEEPDEEP of the Arm® Cortex®-M3 core. Do not use the <SLEEPDEEP> bit of the system control register.

1.3.1.3. Selection of Low-power Consumption Mode

low-power consumption mode selection is chosen by the setup of ***[CGSTBYCR]***<STBY [1:0]>.

Following table shows the mode chosen from a setup of <STBY [1:0]>.

Table 1.6 Low-power Consumption Mode Selection

Mode	[CGSTBYCR]<STBY[1:0]>
IDLE	00
STOP1	01
STOP2	10

Note: Do not use the settings other than the above.

1.3.1.4. Peripheral Function State in Low-power Consumption Mode

The following Table 1.7 shows the operation state of the peripheral function (block) in each low-power consumption mode.

In addition, after reset release it will be in the state where a clock is not supplied except for a part of blocks.

If needed, set up ***[CGFSYSENA]***, ***[CGFSYSENB]***, ***[CGFSYSMENB]***, ***[CGFCEN]*** and ***[CGSPCLKEN]*** and enable clock supply.

Table 1.7 Block Operation Status in Each Low-power Consumption Mode

Block		NORMAL	IDLE	STOP1		STOP2 (Note1)	
				ELOSC On	ELOSC Off	ELOSC On	ELOSC Off
Processor core (Debug included)		✓	-	-	-	×	×
DMAC		✓	✓	-	-	×	×
I/O port	Pin state	✓	✓	✓	✓	✓ (Note4)	✓ (Note4)
	Register	✓	✓	-	-	×	×
ADC		✓	✓	-	-	×	×
DAC		✓	✓	-	-	×	×
COMP		✓	✓	-	-	×	×
UART		✓	✓	-	-	×	×
I2C		✓	✓	- (Note3)	- (Note3)	× (Note3)	× (Note3)
EI2C		✓	✓	- (Note3)	- (Note3)	× (Note3)	× (Note3)
TSPI		✓	✓	-	-	×	×
A-PMD		✓	✓	-	-	×	×
A-ENC32		✓	✓	-	-	×	×
T32A		✓	✓	-	-	×	×
DLCD		✓	✓	✓	-	✓	-
TRGSEL		✓	✓	-	-	×	×
CRC		✓	✓	-	-	×	×
RTC		✓	✓	✓	-	✓	-
RMC		✓	✓	✓	-	×	×
SIWDT		✓	✓ (Note 2)	-	-	×	×
LVD		✓	✓	✓	✓	✓	✓
OFD		✓	✓	-	-	×	×
TRM		✓	N/A	-	-	×	×
CG		✓	✓	✓	✓	×	×
PLL		✓	✓	-	-	×	×
RAMP (RAM parity)		✓	✓	-	-	×	×
External high-speed oscillator (EHOSC)		✓	✓	-	-	×	×
Built-in high-speed oscillator 1 (IHOSC1)		✓	✓	-	-	×	×
Built-in high-speed oscillator 2 (IHOSC2)		✓	✓	-	-	×	×
External low-speed oscillator (ELOSC)		✓	✓	✓	-	✓	-
RLM		✓	✓	✓	✓	✓	✓
Code flash		Access possible	Access possible (Note5)	Data hold	Data hold	Data hold	Data hold
Data flash							
RAM						×	×
Backup RAM						Data hold	Data hold

✓: Operation is possible.

-: If it shifts to the object mode, the clock to a peripheral circuit stops automatically.

×: If it shifts to the object mode, the electric supply source to a module intercept automatically. When returning, initialized by the reset.

Note1: Check that the peripheral function is not running and change to STOP 2 mode.

Note2: Stop SIWDT before shifting to the IDLE mode except protection A mode.

Note3: The address match wake up function can only be used.

Note4: A port state when the ***[RLMSHTDNOP]*** <PTKEEP> is set to "1" is held.

Note5: It becomes a data hold when peripheral functions (DMA etc.) which carry out data access (R/W), except CPU, are not connected on the bus matrix.

1.3.2. Mode State Transition

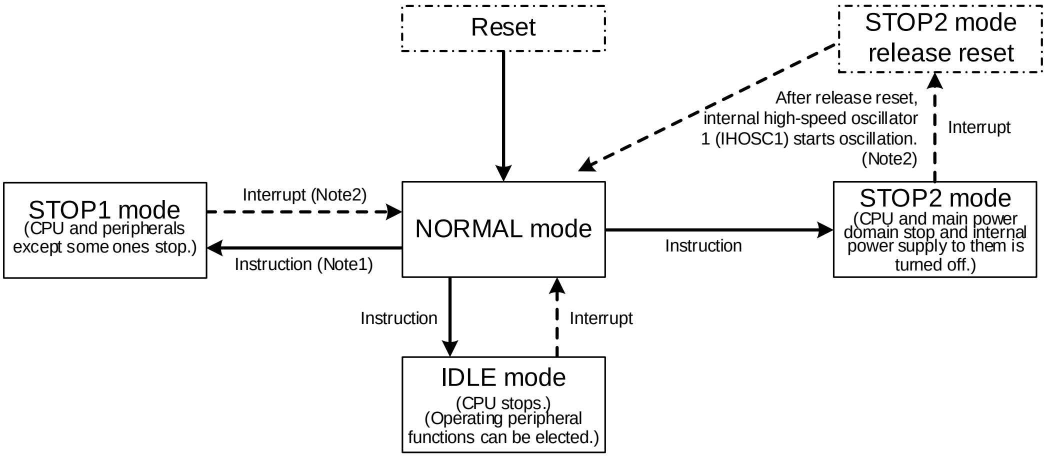

Figure 1.2 Mode State Transition

Note1: Warm up is required at returning. A warm up time must be set in the previous mode (NORMAL mode) before entering to STOP1 mode.

Note2: When the CPU returns from STOP2 mode, the CPU branches to the interrupt service routine triggered by reset. When the CPU returns from STOP1 mode, the CPU branches to the interrupt service routine triggered by interrupt events.

1.3.2.1. IDLE Mode Transition Flow

Set up the following procedure at transition to IDLE mode.

Because IDLE mode is released by an interrupt, set the interrupt before transition to IDLE mode. For the interrupts that can be used to release the IDLE mode, refer to "1.3.3.1. Release Source of Low-power Consumption Mode". Disables unused interrupts and unavailable interrupts for release IDLE mode.

Transition procedure (from NORMAL mode)		
1	***[SIWDxEN]***<WDTE> = 0	Disable SIWDT
2	***[SIWDxCR]***<WDCR[7:0]>= 0xB1	Disable SIWDT.
3	***[FCSR0]***<RDYBSY> is read	It waits until Flash will be in a Ready state (= 1).
4	***[CGSTBYCR]***<STBY[1:0]> = 00	low-power consumption mode selection is set to IDLE.
5	***[CGSTBYCR]***<STBY[1:0]> is read	Confirm "00" to written to the register at the step 4.
6	WFI command execution	Transit to IDLE.

Note: When using the protection A mode of SIWDT, step 1 and 2 are not required.

1.3.2.2. STOP1 Mode Transition Flow

Set up the following procedure at transition to STOP1.

Because STOP1 mode is released by an interrupt, set the interrupt before transition to STOP1 mode. For the interrupts that can be used to release the STOP1 mode, refer to "1.3.3.1. Release Source of Low-power Consumption Mode". Disables unused interrupts and unavailable interrupts for release STOP1.

Transition procedure (from NORMAL mode)		
1	***[SIWDxEN]***<WDTE> = 0	Disable SIWDT.
2	***[SIWDxCR]***<WDCR[7:0]> = 0xB1	Disable SIWDT.
3	***[FCSR0]***<RDYBSY> is read	Wait until Flash becomes the Ready state (= 1).
4	***[CGWUPHCR]***<WUEF> is read	Wait until the high-speed oscillation warming-up ends (= 0).
5	***[CGWUPHCR]***<WUCLK> = 0	Set the warming-up clock selection to internal high-speed oscillator 1 (IHOSC1).
	[CGWUPHCR]<WUPT[15:4]> = 0x3C	Set the high-speed oscillation warming-up timer setting value of 163.4 μs (= 0x3C) or more.
6	***[CGSTBYCR]***<STBY[1:0]> = 01	low-power consumption mode selection is set to STOP1.
7	***[CGPLL0SEL]***<PLL0SEL> = 0	Select the PLL for fsys to "PLL is unused (fosc)".
8	***[CGPLL0SEL]***<PLL0ST> is read	Wait until the status of the PLL for fsys becomes "PLL is unused (fosc) (= 0)".
9	***[CGPLL0SEL]***<PLL0ON> = 0	Stop PLL for fsys
10	***[CGOSCCR]***<IHOSC1EN> = 1	Enable the internal high-speed oscillator.
11	[CGWUPHCR]<WUON> = 1	Start the high-speed oscillation warming-up timer
12	***[CGWUPHCR]***<WUEF> is read.	Wait until a warming-up timer status flag becomes ends (= 0).
13	***[CGOSCCR]***<OSCSEL> = 0	Set the high-speed oscillation selection for fosc to internal high-speed oscillator1 (IHOSC1).
14	***[CGOSCCR]***<OSCF> is read.	Wait until the high-speed oscillation selection status for fosc becomes internal high-speed oscillator1 (IHOSC1). (= 0).
15	***[CGOSCCR]***<EOSCEN[1:0]> = 00	Set the selection of an external oscillator operation to unused.
16	***[CGOSCCR]***<IHOSC2EN> = 0	The internal high-speed oscillator 2 (IHOSC2) is stopped.
17	***[CGOSCCR]***<EOSCEN[1:0]> is read	The register writing of above 15th row is checked (= 00).
18	***[CGOSCCR]***<IHOSC2F> is read	Wait until the status of the internal high-speed oscillator 2 becomes off "0".
19	WFI command execution	Transit to STOP1.

1.3.2.3. STOP2 Mode Transition Flow

Set up the following procedure at transition to STOP2.

Because STOP2 mode is released by an interrupt, set the interrupt before transition STOP2 mode. For the interrupts that can be used to release the STOP2 mode, refer to "1.3.3.1. Release Source of Low-power Consumption Mode". Disables unused interrupts and unavailable interrupts for release STOP2.

Transition procedure (from NORMAL mode)		
1	***[SIWDxEN]***<WDTE> = 0	Disable SIWDT.
2	***[SIWDxCR]***<WDCR[7:0]> = 0xB1	Disable SIWDT.
3	***[FCSR0]***<RDYBSY> is read.	Wait until Flash becomes the Ready state (= 1).
4	[RLMSHTDNOP]<PTKEEP> = 1	IO control signal is made to hold.
5	***[CGSTBYCR]***<STBY[1:0]> = 10	low-power consumption mode selection is set to STOP2.
6	***[CGPLL0SEL]***<PLL0SEL> = 0	Select the PLL for fsys to "PLL is unused (fosc)".
7	***[CGPLL0SEL]***<PLL0ST> is read	Wait until the PLL selection status for fsys becomes PLL unused. (= 0).
8	***[CGPLL0SEL]***<PLL0ON> = 0	Stop PLL for fsys.
9	[CGWUPHCR]<WUCLK> = 0 ***[CGWUPHCR]***<WUPT[15:4]> = 0x03C	Set the warming-up clock selection to internal high-speed oscillator 1 (IHOSC1). Set the high-speed oscillation warming-up timer setting value of 163.4 μs (= 0x03C) or more.
10	***[CGOSCCR]***<IHOSC1EN> = 1	Enable the internal high-speed oscillator 1.
11	***[CGWUPHCR]***<WUON> = 1	Start the high-speed oscillation warming-up timer
12	***[CGWUPHCR]***<WUEF> is read.	Wait until the warming-up timer status flag becomes ends (= 0).
13	***[CGOSCCR]***<OSCSEL> = 0	Set the high-speed oscillation selection for fosc to internal high-speed oscillator1 (IHOSC1).
14	***[CGOSCCR]***<OSCF> is read	Wait until the high-speed oscillation selection status for fosc becomes internal high-speed oscillator1 (IHOSC1) (= 0).
15	***[CGOSCCR]***<EOSCEN[1:0]> = 00	Set the selection of an external oscillator operation to unused.
16	***[CGOSCCR]***<IHOSC2EN> = 0	The internal high-speed oscillator 2 is stopped.
17	***[CGOSCCR]***<EOSCEN[1:0]> is read	The register writing of step 15 is checked (= 00).
18	***[CGOSCCR]***<IHOSC2F> is read	Wait until the internal oscillation stable flag of the internal high-speed oscillator 2 becomes zero.
19	***[RLMRSTFLG0]***<STOP2RSTF> = 0 ***[RLMRSTFLG0]***< PINRSTF> = 0	A STOP2 reset flag/reset pin flag is cleared (Note).
20	WFI command execution ←	Transit to STOP2.
21	Jump instruction	Return to step 20.

Note: Refer to the reference manual "Exception" for a reset flag register ***[RLMRSTFLG0]***.

1.3.3. Return Operation from Low-power Consumption Mode

1.3.3.1. Release Source of Low-power Consumption Mode

Interrupt, Non-Maskable Interrupt, and reset can perform release from a low-power consumption mode. The standby release source which can be used is decided by a low-power consumption mode.

It shows the following table about details.

Table 1.8 Release Source List

Low-power consumption mode			IDLE	STOP1	STOP2
Release Source	Interrupt	INT00, INT01, INT02, INT13	✓	✓	✓
		INT03 to INT12、INT14 to INT33	✓	✓	-
		INTI2CWUP	✓	✓	✓
		INTRTC	✓	✓	✓
		INTLCDBUSF, INTLCDSTOP	✓	-	-
		INTEMG0, INTOVV0, INTPMD0	✓	-	-
		INTENC00, INTENC01	✓	-	-
		INTADAPDA, INTADAPDB	✓	-	-
		INTADACP0, INTADACP1, INTADATRG	✓	-	-
		INTADASGL, INTADACNT	✓	-	-
		INTTxRX, INTTxTX, INTTxERR	✓	-	-
		INTI2CxNST, INTI2CxATX, INTI2CxBRX, INTI2CxNA	✓	-	-
		INTUARTxRX, INTUARTxTX, INTUARTxERR	✓	-	-
		INTT32AxA, INTT32AxACAP0, INTT32AxACAP1 INTT32AxB, INTT32AxBCAP0, INTT32BxBCAP1 INTT32AxC, INTT32AxCCAP0, INTT32CxCCAP1	✓	-	-
		INTDMAATC, INTDMAAERR INTDMABTC, INTDMABERR	✓	-	-
		INTRMC	✓	✓	-
		INTPARI	✓	-	-
		INTFLCRDY, INTFLDRDY	✓	-	-
	SysTick Interrupt		✓	-	-
	Non-Maskable Interrupt (INTWDT)		✓	-	-
	Non-Maskable Interrupt (INTLVD)		✓	✓	✓
	Reset (SIWDT)		✓	-	-
	Reset (LVD)		✓	✓	✓
	Reset (OFD)		✓	-	-
	Reset (RESET_N pin)		✓	✓	✓

✓: It can be used for release. After release, an interrupt processing will start.

-: It cannot be used for release.

- Released by an interrupt request
  When interrupt releases a low-power consumption mode, it is necessary to prepare so that interrupt may be detected by CPU. The interrupt used for release STOP1 or STOP2 mode needs to set for detecting the interrupt by INTIF other than a setting of CPU.

- Released by Non-Maskable Interrupt (NMI)
  The factor of NMIs is SIWDT interrupt (INTWDT, protected mode A only) and LVD interrupt (INTLVD).

- Released by reset
  The reset can perform release from all the low-power consumption modes.
  When released by reset, all the registers will be initialized in NORMAL mode after release.

- Released by SysTick interrupt
  SysTick interrupt is available only in IDLE mode.

Refer to "Interrupt" chapter of the reference manual "Exception" about the details of interrupt.

1.3.3.2. Warming Up at Release of Low-power Consumption Mode

Warming-up may be required because of stability of an internal oscillator at the time of mode transition.

When shifting from STOP1 mode to a NORMAL mode, an internal oscillation is chosen automatically and the warming-up timer is started. The Output of a system clock is started after warming-up time progress.

For this reason, before executing the command which shifts to the STOP1 mode, set up warming-up time by ***[CGWUPHCR]***<WUPT[15:4]>. For the setting method, refer to "1.2.4.1. Warming-up Timer for High-speed Oscillation".

The following table shows the necessary of a warming-up setup at the time of each Operation mode transition.

Table 1.9 Warming Up

Operation mode transition	Warming-up setting
NORMAL → IDLE	Not required
NORMAL → STOP1	Not required
NORMAL → STOP2	Not required
IDLE → NORMAL	Not required
STOP1 → NORMAL	Required (Auto warming up)
STOP2 → RESET → NORMAL	Not required

1.3.3.3. Restart Operation from STOP2 Mode

The restart operation flow from STOP2 mode release factor interrupt generating is as follows.

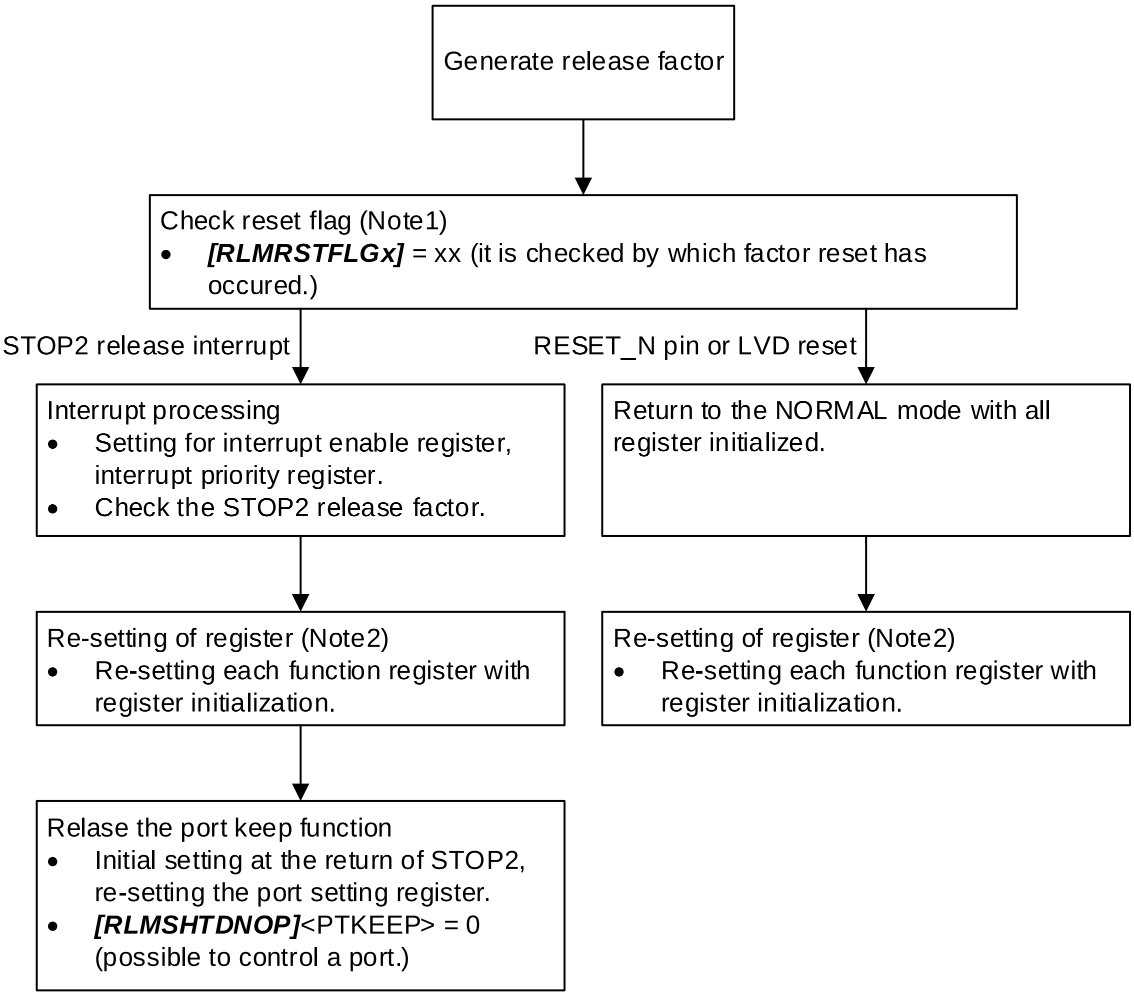

Figure 1.3 STOP2 Mode Restart Operation Flow

Note1: When STOP2 mode is released by RESET_N pin, as for a reset flag, both "STOP2 reset flag" and "reset pin flag" are materialized.

Note2: When STOP2 mode is released by LVD reset, as for a reset flag, both "STOP2 reset flag" and "reset pin flag" are materialized.

Note3: Register reset area is differ depending on the releasing STOP2 mode by an interrupt and the releasing STOP2 mode by the reset of RESET_N pin or LVD. Refer to "3.2.7.1. Reset Factor and Reset Initialized Range" for register reset area by each factor.

1.3.4. Clock Operation by Mode Transition

The clock operation at mode transition is shown below.

1.3.4.1. NORMAL → IDLE → NORMAL Operation Mode Transition

CPU stops at IDLE mode. The clock supply to a peripheral function holds a setting state. Please perform operation/ stop by the register of each peripheral function, a clock supply setting function, etc. if needed. Execution of Warming-up operation is not performed at the time of the restart operation in NORMAL mode from IDLE state.

After the command (WFI) execution which switches to IDLE mode, a program counter will show the next point and will be in a CPU idle state. With a release source, it becomes a CPU reboot and, in the case of an enable interrupt state, the shift to next point of transition command (WFI) will be done, after the interrupt processing by release source.

1.3.4.2. NORMAL → STOP1 → NORMAL Operation Mode Transition

When returning to NORMAL mode from the STOP1 mode, warming-up is started automatically.

Please set ***[CGWUPHCR]***<WUPT[15:4]> to warming-up time (163.4µs or more) before moving to the STOP1 mode.

Note: When releasing factor is RESET_N pin or LVD reset, CPU operation is started after the internal processing time for reset and the waiting time till CPU running, not the warming-up time elapse. When reset factor is not released after the internal processing time for reset elapses, starts measuring elapsed time after releasing reset factor. CPU operation is started after the waiting time till CPU running elapse.

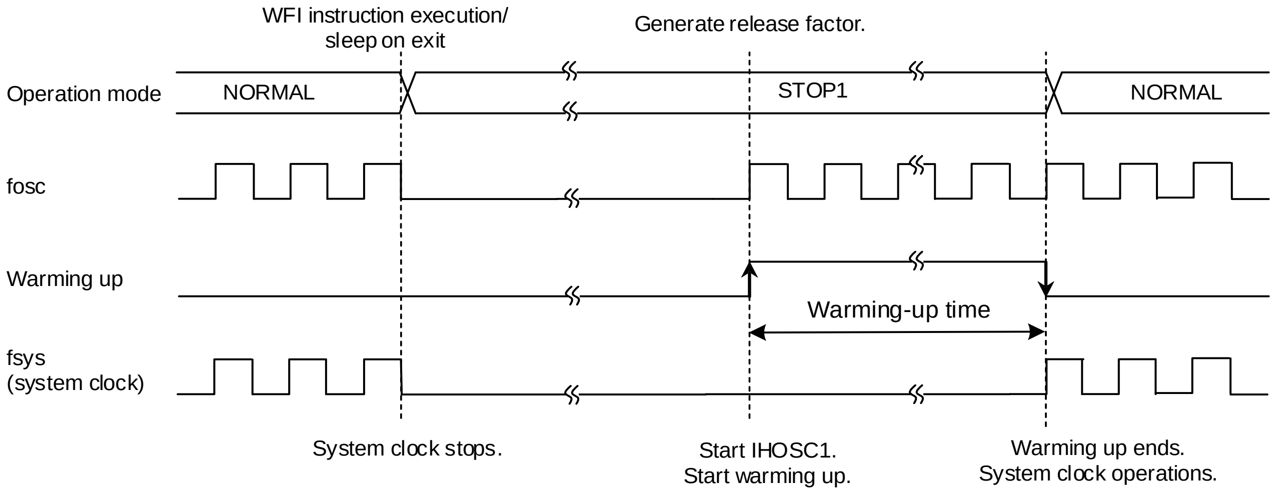

Figure 1.4 NORMAL → STOP1 → NORMAL Operation Mode Transition

1.3.4.3. NORMAL → STOP2 → RESET → NORMAL Operation Mode Transition

Warming-up is not performed when returning to NORMAL mode by reset.

Even when returning to NORMAL mode except for RESET, it branches to the interrupt routine of reset.

A reset operation is performed to an internal Main power domain after STOP2 mode released. However, reset is not performed to the backup domain which is keeping power supply.

Note: When releasing factor is RESET_N pin or LVD reset, CPU operation is started after the internal processing time for reset and the waiting time till CPU running, not the warming-up time elapse. When reset factor is not released after the internal processing time for reset elapses, starts measuring elapsed time after releasing reset factor. CPU operation is started after the waiting time till CPU running elapse.

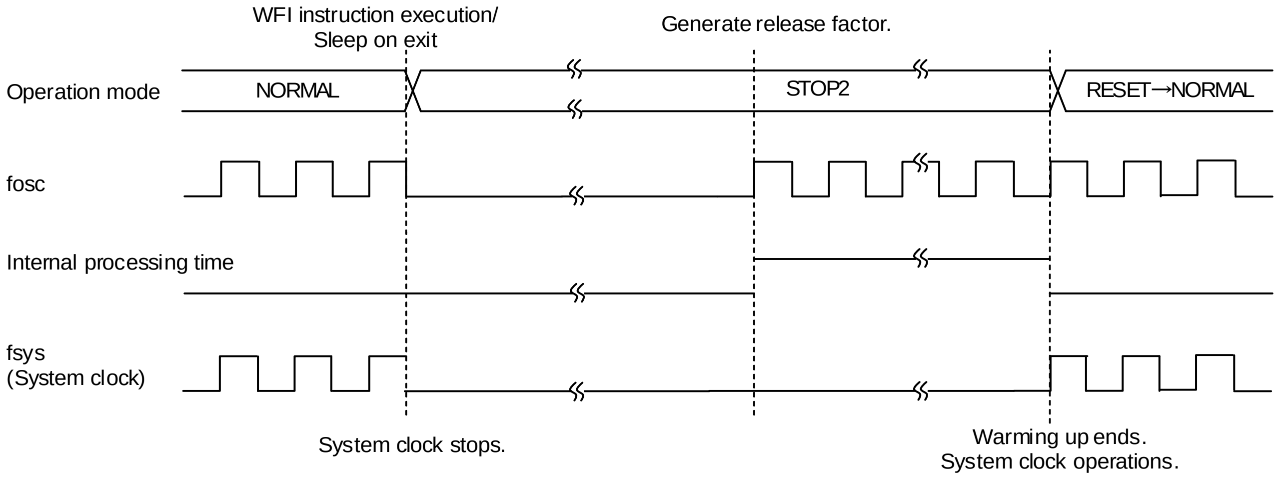

Figure 1.5 NORMAL → STOP2 → RESET → NORMAL Operation Mode Transition

1.4. Explanation of Register

1.4.1. Register List

The register related to CG and its address information is shown below.

Peripheral Function		Channel/unit	Base address
Clock Control and Operation Mode	CG	-	0x400F3000
Low-speed oscillation/power control	RLM	-	0x4003E400

1.4.1.1. Clock and Mode Control

Register name		Address (Base+)
CG Write Protection Register	***[CGPROTECT]***	0x0000
Oscillation Control Register	***[CGOSCCR]***	0x0004
System Clock Control Register	***[CGSYSCR]***	0x0008
Standby Control Register	***[CGSTBYCR]***	0x000C
SCOUT Output Control Register	***[CGSCOCR]***	0x0010
PLL Selection Register for fsys	***[CGPLL0SEL]***	0x0020
High-speed Oscillation Warming-up Register	***[CGWUPHCR]***	0x0030
Low-speed Oscillation Warming-up Register	***[CGWUPLCR]***	0x0034
Clock Supply and Stop Register B for fsysm	***[CGFSYSMENB]***	0x004C
Clock Supply and Stop Register A for fsys	***[CGFSYSENA]***	0x0050
Clock Supply and Stop Register B for fsys	***[CGFSYSENB]***	0x0054
Clock Supply and Stop Register for fc	***[CGFCEN]***	0x0058
Clock Supply and Stop Register for ADC and Debug Circuit	***[CGSPCLKEN]***	0x005C

1.4.1.2. Low-speed Oscillation/power Control (Note)

Register name		Address (Base+)
Low-speed Oscillation Control Register	***[RLMLOSCCR]***	0x0000
Power Supply Cut Off Control Register	***[RLMSHTDNOP]***	0x0001
RLM Write Protection Register	***[RLMPROTECT]***	0x000F

Note: Byte accessible registers. Bit band access cannot be performed.

1.4.2. Register Description

1.4.2.1. *[CGPROTECT]* (CG Write Protection Register)

Bit	Bit symbol	After reset	Type	Function
31:8	-	0	R	Read as "0"
7:0	PROTECT[7:0]	0xC1	R/W	Control write protection for the CG register (all registers except this register) 0xC1: CG Registers are written enabled. Other than 0xC1: Sets write protection (Protect enable)

1.4.2.2. *[CGOSCCR]* (Oscillation Control Register)

Bit	Bit symbol	After reset	Type	Function
31:20	-	0	R	Read as "0"
19	IHOSC2F	0	R	Indicates the stability flag of an internal oscillation for IHOSC2. 0: Stopping or being in warm up 1: Stable oscillation
18:17	-	0	R	Read as "0"
16	IHOSC1F	1	R	Indicates the stability flag of an internal oscillation for IHOSC1. 0: Stopping or being in warm up 1: Stable oscillation
15:10	-	0	R	Read as "0"
9	OSCF	0	R	Indicates high-speed oscillator for fosc selection status. 0: Internal high-speed oscillator 1 (IHOSC1) 1: External high-speed oscillator (EHOSC)
8	OSCSEL	0	R/W	Selects a high-speed oscillation for fosc. (Note1) 0: Internal high-speed oscillator 1 (IHOSC1) 1: External high-speed oscillator (EHOSC)
7:4	-	0	R	Read as "0"
3	IHOSC2EN	0	R/W	Enables the internal high-speed oscillator 2 (IHOSC2) (Note2) 0: Stop 1: Oscillation
2:1	EOSCEN[1:0]	0x0	R/W	Selects the operation of the external high-speed oscillator. (EHOSC) (Note3) 00: External oscillator is not used. 01: Uses the external high-speed oscillator. (EHOSC) 10: Uses the external clock. (EHCLKIN) 11: Reserved
0	IHOSC1EN	1	R/W	Internal high-speed oscillator 1. (IHOSC1) 0: Stop 1: Oscillation

Note1: When the setting is modified, confirm whether the written value has been reflected to the ***[CGOSCCR]***<OSCF> bit before executing the next operation.

Note2: Setting cannot be changed, when it is ***[SIWDxOSCCR]***<OSCPRO> = 1 (write protection of SIWDT is effective).

Note3: When using the oscillator connection, set these bits (external high-speed oscillation) to "01".

Note4: To wait stabilizing oscillation of an internal high-speed oscillator1 (IHOSC1), use a warming-up timer and confirm ***[CGWUPHCR]***<WUEF> instead of <IHOSCF1>.

1.4.2.3. *[CGSYSCR]* (System Clock Control Register)

Bit	Bit symbol	After reset	Type	Function
31:28	-	0	R	Read as "0"
27:24	PRCKST[3:0]	0x0	R	Indicates a prescaler clock (ΦT0) selection. 0000: fc 0100: fc / 16 1000: fc / 256 0001: fc / 2 0101: fc / 32 1001: fc / 512 0010: fc / 4 0110: fc / 64 0011: fc / 8 0111: fc / 128 Others: Reserved
23:19	-	0	R	Read as "0".
18:16	GEARST[2:0]	0x0	R	Indicates selection status of the gear ratio of the system clock (fsys). 000: fc 100: fc/16 001: fc / 2 010: fc / 4 011: fc / 8 Others: Reserved
15:12	-	0	R	Read as "0"
11:8	PRCK[3:0]	0x0	R/W	Selects a prescaler clock (ΦT0). 0000: fc 0100: fc / 16 1000: fc / 256 0001: fc / 2 0101: fc / 32 1001: fc / 512 0010: fc / 4 0110: fc / 64 0011: fc / 8 0111: fc / 128 Others: Reserved Selects a prescaler clock for the peripheral functions.
7:3	-	0	R	Read as "0"
2:0	GEAR[2:0]	0x0	R/W	Selects a gear ratio of the system clock (fsys). 000: fc 100: fc / 16 001: fc / 2 010: fc / 4 011: fc / 8 Others: Reserved

1.4.2.4. *[CGSTBYCR]* (Standby control register)

Bit	Bit symbol	After reset	Type	Function
31:2	-	0	R	Read as "0"
1:0	STBY[1:0]	0x0	R/W	Selects a low-power consumption mode. 00: IDLE 01: STOP1 10: STOP2 11: Reserved

1.4.2.5. *[CGSCOCR]* (SCOUT Output Control Register)

Bit	Bit symbol	After reset	Type	Function
31:7	-	0	R	Read as "0"
6:4	SCODIV[2:0]	0x0	R/W	Selects a SCOUT division ratio. (Note1) (Note2) 000: No dividing 001: Divide-by-2 010: Divide-by-4 011: Divide-by-8 100: Divide-by-16 Others: Reserved
3:1	SCOSEL[2:0]	0x0	R/W	SCOUT base clock selection (Note1) 000: fosc 001: fc 010: fs 011: fsys Others: Reserved
0	SCOEN	0	R/W	Enable SCOUT output. 0: Disable 1: Enable

Note1: When the "011: fsys" is selected by <SCOSEL[2:0]>, selection of the "000: No dividing" by <SCODIV[2:0]> is inhibited.

Note2: When the "010: fs" is selected by <SCOSEL[2:0]>, it forces selection that is without clock dividing.

1.4.2.6. *[CGPLL0SEL]* (PLL Selection Register for fsys)

Bit	Bit symbol	After reset	Type	Function
31:8	PLL0SET[23:0]	0x000000	R/W	PLL multiplication setup About a multiplication setup, refer to "1.2.5.2. Formula and Example of Setting of PLL Multiplication Value".
7:3	-	0	R	Read as "0"
2	PLL0ST	0	R	Indicate PLL for fsys selection status. 0: fosc 1: f_{PLL}
1	PLL0SEL	0	R/W	Select Clock selection for fsys 0: fosc 1: f_{PLL}
0	PLL0ON	0	R/W	Select PLL operation for fsys 0: Stop 1: Oscillation

1.4.2.7. *[CGWUPHCR]* (High-speed Oscillation Warming-up Register)

Bit	Bit symbol	After reset	Type	Function
31:20	WUPT[15:4]	0x800	R/W	Sets the upper 12 bits of the 16 bits of calculation values of the warming-up timer. About a setup of a warming-up timer, refer to "1.2.4.1. Warming-up Timer for High-speed Oscillation".
19:16	WUPT[3:0]	0x0	R	Sets the lower 4 bits of the 16 bits of calculation values of the warming-up timer. It is fixed by 0x0.
15:9	-	0	R	Read as "0"
8	WUCLK	0	R/W	Warming-up clock selection (Note1) 0: Internal high-speed oscillator (IHOSC1) 1: External high-speed oscillator (EHOSC)
7:2	-	0	R	Read as "0"
1	WUEF	0	R	Indicates status of the Warming-up timer. (Note2) 0: The end of Warming-up 1: In warming-up operation
0	WUON	0	W	Control the Warming-up timer. 0: don't care 1: Warming-up operation start.

Note1: Use the internal oscillator for warm up when the CPU returns from STOP1 mode. Do not use an external oscillator when the CPU returns from STOP1 mode.

Note2: Do not modify the registers during the warm up (<WUEF> = 1). Set the registers when <WUEF> = 0.

1.4.2.8. *[CGWUPLCR]* (Low-speed Oscillation Warming-up Register)

Bit	Bit symbol	After reset	Type	Function
31:27	-	0	R	Read as "0"
26:12	WUPTL[18:4]	0x4000	R/W	Sets the upper 15 bits of 19 bits of calculation values of the warming-up timer. About a setup of a warming-up timer, refer to "1.2.4.2. Warming-up Timer for Low-speed Oscillation".
11:8	WUPTL[3:0]	0x0	R	Sets the lower 4 bits of the 19 bits of calculation values of the warming-up timer. It is fixed by "0x0".
7:2	-	0	R	Read as "0"
1	WULEF	0	R	Indicates a status of the warming-up timer (Note) 0: The end of Warming-up 1: In warming-up operation
0	WULON	0	W	Control the warming-up timer control 0: don't care. 1: Warming-up operation start.

Note: Do not modify the registers during the warm up (<WULEF> = 1). Set the registers when <WULEF> = 0.

1.4.2.9. *[CGFSYSMENB]* (Clock Supply and Stop Register B for fsysm)

Bit	Bit symbol	After reset	Type	Function
31	IPMENB31	0	R	Read as "0".
30	IPMENB30	0	R	Read as "0".
29	IPMENB29	0	R	Read as "0".
28	IPMENB28	0	R	Read as "0".
27	IPMENB27	0	R	Read as "0".
26	IPMENB26	0	R	Read as "0".
25	IPMENB25	0	R	Read as "0".
24	IPMENB24	0	R	Read as "0".
23	IPMENB23	0	R	Read as "0".
22	IPMENB22	0	R	Read as "0".
21	IPMENB21	0	R	Read as "0".
20	IPMENB20	0	R	Read as "0".
19	IPMENB19	0	R	Read as "0".
18	IPMENB18	0	R	Read as "0".
17	IPMENB17	0	R	Read as "0".
16	IPMENB16	0	R	Read as "0".
15	IPMENB15	0	R	Read as "0".
14	IPMENB14	0	R/W	Enable the clock of EI2C ch3 0: Clock stop 1: Clock supply
13	IPMENB13	0	R/W	Enable the clock of EI2C ch2 0: Clock stop 1: Clock supply
12	IPMENB12	0	R/W	Enable the clock of EI2C ch1 0: Clock stop 1: Clock supply
11	IPMENB11	0	R/W	Enable the clock of EI2C ch0 0: Clock stop 1: Clock supply
10	IPMENB10	0	R	Read as "0".
9	IPMENB09	0	R	Read as "0".
8	IPMENB08	0	R	Read as "0".
7	IPMENB07	0	R	Read as "0".
6	IPMENB06	0	R	Read as "0".
5	IPMENB05	0	R	Read as "0".
4	IPMENB04	0	R	Read as "0".
3	IPMENB03	0	R	Read as "0".
2	IPMENB02	0	R	Read as "0".
1	IPMENB01	0	R	Read as "0".
0	IPMENB00	0	R	Read as "0".

Note1: Even if the initial value of a register is set to stop of the clock, the clock is supplied to the register during the reset.

Note2: Please write "0" into the unavailable register bits in the TMPM3HP, TMPM3HM, TMPM3HN, and TMPM3HL. For detail, refer to "1.5. Information for Each Product".

1.4.2.10. *[CGFSYSENA]* (Clock Supply and Stop Register A for fsys)

Bit	Bit symbol	After reset	Type	Function
31	IPENA31	0	R/W	Enable the Clock of T32A ch7 0: Clock stop 1: Clock supply
30	IPENA30	0	R/W	Enable the Clock of T32A ch6 0: Clock stop 1: Clock supply
29	IPENA29	0	R/W	Enable the Clock of T32A ch5 0: Clock stop 1: Clock supply
28	IPENA28	0	R/W	Enable the Clock of T32A ch4 0: Clock stop 1: Clock supply
27	IPENA27	0	R/W	Enable the Clock of T32A ch3 0: Clock stop 1: Clock supply
26	IPENA26	0	R/W	Enable the Clock of T32A ch2 0: Clock stop 1: Clock supply
25	IPENA25	0	R/W	Enable the Clock of T32A ch1 0: Clock stop 1: Clock supply
24	IPENA24	0	R/W	Enable the Clock of T32A ch0 0: Clock stop 1: Clock supply
23	IPENA23	0	R/W	Enable the Clock of RTC 0: Clock stop 1: Clock supply
22	IPENA22	0	R/W	Enable the Clock of RMC ch0 0: Clock stop 1: Clock supply
21	IPENA21	0	R/W	Enable the Clock of A-ENC32 ch0 0: Clock stop 1: Clock supply
20	IPENA20	0	R/W	Enable the Clock of A-PMD ch0 0: Clock stop 1: Clock supply
19	IPENA19	0	R/W	Enable the Clock of DMAC unit B 0: Clock stop 1: Clock supply
18	IPENA18	0	R/W	Enable the Clock of DMAC unit A 0: Clock stop 1: Clock supply
17	IPENA17	0	R/W	Enable the Clock of PORT V 0: Clock stop 1: Clock supply
16	IPENA16	0	R/W	Enable the Clock of PORT U 0: Clock stop 1: Clock supply
15	IPENA15	0	R/W	Enable the Clock of PORT T 0: Clock stop 1: Clock supply
14	IPENA14	0	R/W	Enable the Clock of PORT R 0: Clock stop 1: Clock supply
13	IPENA13	0	R/W	Enable the Clock of PORT P 0: Clock stop 1: Clock supply
12	IPENA12	0	R/W	Enable the Clock of PORT N 0: Clock stop 1: Clock supply

Bit	Bit symbol	After reset	Type	Function
11	IPENA11	0	R/W	Enable the Clock of PORT M 0: Clock stop 1: Clock supply
10	IPENA10	0	R/W	Enable the Clock of PORT L 0: Clock stop 1: Clock supply
9	IPENA09	0	R/W	Enable the Clock of PORT K 0: Clock stop 1: Clock supply
8	IPENA08	0	R/W	Enable the Clock of PORT J 0: Clock stop 1: Clock supply
7	IPENA07	0	R/W	Enable the Clock of PORT H 0: Clock stop 1: Clock supply
6	IPENA06	0	R/W	Enable the Clock of PORT G 0: Clock stop 1: Clock supply
5	IPENA05	0	R/W	Enable the Clock of PORT F 0: Clock stop 1: Clock supply
4	IPENA04	0	R/W	Enable the Clock of PORT E 0: Clock stop 1: Clock supply
3	IPENA03	0	R/W	Enable the Clock of PORT D 0: Clock stop 1: Clock supply
2	IPENA02	0	R/W	Enable the Clock of PORT C 0: Clock stop 1: Clock supply
1	IPENA01	0	R/W	Enable the Clock of PORT B 0: Clock stop 1: Clock supply
0	IPENA00	0	R/W	Enable the Clock of PORT A 0: Clock stop 1: Clock supply

Note1: Even if the initial value of a register is set to stop of the clock, the clock is supplied to the register during the reset.

Note2: Please write "0" into the unavailable register bits in the TMPM3HP, TMPM3HM, TMPM3HN, and TMPM3HL. For detail, refer to "1.5. Information for Each Product".

1.4.2.11. *[CGFSYSENB]* (Clock Supply and Stop Register B for fsys)

Bit	Bit symbol	After reset	Type	Function
31	IPENB31	1	R/W	Clock enabling of SIWDT 0: Clock stop 1: Clock supply
30	IPENB30	1	R/W	Write as "1"
29	IPENB29	1	R/W	Write as "1"
28	IPENB28	1	R/W	Write as "1"
27	IPENB27	0	R/W	Write as "0"
26	IPENB26	0	R	Read as "0".
25	IPENB25	0	R/W	Enable the Clock of UART ch7 0: Clock stop 1: Clock supply
24	IPENB24	0	R/W	Enable the Clock of UART ch6 0: Clock stop 1: Clock supply
23	IPENB23	0	R/W	Enable the Clock of TRGSEL ch0 and 1 0: Clock stop 1: Clock supply
22	IPENB22	0	R/W	Enable the Clock of TRM 0: Clock stop 1: Clock supply
21	IPENB21	0	R/W	Enable the Clock of OFD 0: Clock stop 1: Clock supply
20	IPENB20	0	R/W	Enable the Clock of CRC 0: Clock stop 1: Clock supply
19	IPENB19	0	R/W	Enable the Clock of RAMP 0: Clock stop 1: Clock supply
18	IPENB18	0	R/W	Enable the Clock of DAC ch1 0: Clock stop 1: Clock supply
17	IPENB17	0	R/W	Enable the Clock of DAC ch0 0: Clock stop 1: Clock supply
16	IPENB16	0	R/W	Enable the Clock of COMP ch0 0: Clock stop 1: Clock supply
15	IPENB15	0	R/W	Enable the Clock of ADC unit A 0: Clock stop 1: Clock supply
14	IPENB14	0	R/W	Enable the Clock of I2C ch3 0: Clock stop 1: Clock supply
13	IPENB13	0	R/W	Enable the Clock of I2C ch2 0: Clock stop 1: Clock supply
12	IPENB12	0	R/W	Enable the Clock of I2C ch1 0: Clock stop 1: Clock supply
11	IPENB11	0	R/W	Enable the Clock of I2C ch0 0: Clock stop 1: Clock supply
10	IPENB10	0	R/W	Enable the Clock of UART ch5 0: Clock stop 1: Clock supply
9	IPENB09	0	R/W	Enable the Clock of UART ch4 0: Clock stop 1: Clock supply

Bit	Bit symbol	After reset	Type	Function
8	IPENB08	0	R/W	Enable the Clock of UART ch3 0: Clock stop 1: Clock supply
7	IPENB07	0	R/W	Enable the Clock of UART ch2 0: Clock stop 1: Clock supply
6	IPENB06	0	R/W	Enable the Clock of UART ch1 0: Clock stop 1: Clock supply
5	IPENB05	0	R/W	Enable the Clock of UART ch0 0: Clock stop 1: Clock supply
4	IPENB04	0	R/W	Enable the Clock of TSPI ch4 0: Clock stop 1: Clock supply
3	IPENB03	0	R/W	Enable the Clock of TSPI ch3 0: Clock stop 1: Clock supply
2	IPENB02	0	R/W	Enable the Clock of TSPI ch2 0: Clock stop 1: Clock supply
1	IPENB01	0	R/W	Enable the Clock of TSPI ch1 0: Clock stop 1: Clock supply
0	IPENB00	0	R/W	Enable the Clock of TSPI ch0 0: Clock stop 1: Clock supply

Note1: Even if the initial value of a register is set to stop of the clock, the clock is supplied to the register during the reset.

Note2: Please write "0" into the unavailable register bits in the TMPM3HP, TMPM3HM, TMPM3HN, and TMPM3HL. For detail, refer to "1.5. Information for Each Product".

1.4.2.12. *[CGFCEN]* (Clock Supply and Stop Register for fc)

Bit	Bit symbol	After reset	Type	Function
31:8	-	0	R	Read as "0"
7	FCIPEN07	0	R/W	Enable the clock for DNF unit A, unit B and unit C. 0: Clock stop 1: Clock supply
6:0	-	0	R	Read as "0"

1.4.2.13. *[CGSPCLKEN]* (Clock Supply and Stop Register for ADC and Debug Circuit)

Bit	Bit symbol	After reset	Type	Function
31:17	-	0	R	Read as "0"
16	ADCKEN	0	R/W	Enable the clock for ADC. 0: Clock stop 1: Clock supply
15:1	-	0	R	Read as "0"
0	TRCKEN	0	R/W	Enable the clock for debug circuit (Trace/SWV). 0: Clock stop 1: Clock supply

1.4.2.14. *[RLMLOSCCR]* (Low-speed Oscillation Control Register)

Bit	Bit symbol	After reset	Type	Function
7:2	-	0	R	Read as "0"
1	-	0	R/W	Write as "0"
0	XTEN	0	R/W	Selection of an external low-speed oscillator of operation 0: Stop 1: Oscillation

Note1: It is initialized only by a power-on reset.

Note2: It is a register accessed per byte. Bit band access is not allowed.

1.4.2.15. *[RLMSHTDNOP]* (Power Supply Cut Off Control Register)

Bit	Bit symbol	After reset	Type	Function
7	RTLDOLVL	0	R/W	Write as "0"
6:1	-	0	R	Read as "0".
0	PTKEEP	0	R/W	The I/O control signal in the STOP2 mode is held. 0: Control by port 1: Hold the state when it changes into "1" from "0". It is necessary to set this bit prior to the transition to STOP2 mode.

Note: Register access is only the byte unit. Bit band access is not allowed.

1.4.2.16. *[RLMPROTECT]* (RLM Write Protection Register)

Bit	Bit symbol	After reset	Type	Function
7:0	PROTECT	0xC1	R/W	RLM register write protection control 0xC1: RLM registers can be written. (protection disabled) Other than 0xC1: RLM registers cannot be written. (protection enabled) If the write protection is enabled, ***[RLMLOSCCR]*** and ***[RLMSHTDNOP]*** registers cannot be written.

Note: Register access is only the byte unit. Bit band access is not allowed.

1.5. Information for Each Product

The information about ***[CGFSYSMENB]***, ***[CGFSYSENA]*** and ***[CGFSYSENB]*** which are different according to each product is shown below.

1.5.1. *[CGFSYSMENB]*

Table 1.10 Allocation of *[CGFSYSMENB]* by Each Product

Bit	Bit symbol	Destination	Channel number/ unit name/port name	M3HQ	M3HP	M3HN	M3HM	M3HL
31	IPMENB31	-	-	×	×	×	×	×
30	IPMENB30	-	-	×	×	×	×	×
29	IPMENB29	-	-	×	×	×	×	×
28	IPMENB28	-	-	×	×	×	×	×
27	IPMENB27	-	-	×	×	×	×	×
26	IPMENB26	-	-	×	×	×	×	×
25	IPMENB25	-	-	×	×	×	×	×
24	IPMENB24	-	-	×	×	×	×	×
23	IPMENB23	-	-	×	×	×	×	×
22	IPMENB22	-	-	×	×	×	×	×
21	IPMENB21	-	-	×	×	×	×	×
20	IPMENB20	-	-	×	×	×	×	×
19	IPMENB19	-	-	×	×	×	×	×
18	IPMENB18	-	-	×	×	×	×	×
17	IPMENB17	-	-	×	×	×	×	×
16	IPMENB16	-	-	×	×	×	×	×
15	IPMENB15	-	-	×	×	×	×	×
14	IPMENB14	EI2C	3	✓	✓	×	×	×
13	IPMENB13	EI2C	2	✓	✓	✓	✓	✓
12	IPMENB12	EI2C	1	✓	✓	✓	✓	×
11	IPMENB11	EI2C	0	✓	✓	✓	✓	✓
10	IPMENB10	-	-	×	×	×	×	×
9	IPMENB09	-	-	×	×	×	×	×
8	IPMENB08	-	-	×	×	×	×	×
7	IPMENB07	-	-	×	×	×	×	×
6	IPMENB06	-	-	×	×	×	×	×
5	IPMENB05	-	-	×	×	×	×	×
4	IPMENB04	-	-	×	×	×	×	×
3	IPMENB03	-	-	×	×	×	×	×
2	IPMENB02	-	-	×	×	×	×	×
1	IPMENB01	-	-	×	×	×	×	×
0	IPMENB00	-	-	×	×	×	×	×

✓: Available, ×: N/A

1.5.2. *[CGFSYSENA]*

Table 1.11 Allocation of *[CGFSYSENA]* by Each Product

Bit	Bit symbol	Destination	Channel number/ unit name/port name	M3HQ	M3HP	M3HN	M3HM	M3HL
31	IPENA31	T32A	7	✓	✓	✓	✓	✓
30	IPENA30	T32A	6	✓	✓	✓	✓	✓
29	IPENA29	T32A	5	✓	✓	✓	✓	✓
28	IPENA28	T32A	4	✓	✓	✓	✓	✓
27	IPENA27	T32A	3	✓	✓	✓	✓	✓
26	IPENA26	T32A	2	✓	✓	✓	✓	✓
25	IPENA25	T32A	1	✓	✓	✓	✓	✓
24	IPENA24	T32A	0	✓	✓	✓	✓	✓
23	IPENA23	RTC	-	✓	✓	✓	✓	✓
22	IPENA22	RMC	0	✓	✓	✓	✓	✓
21	IPENA21	A-ENC32	0	✓	✓	✓	✓	✓
20	IPENA20	A-PMD	0	✓	✓	✓	✓	✓
19	IPENA19	DMAC	B	✓	✓	✓	✓	✓
18	IPENA18	DMAC	A	✓	✓	✓	✓	✓
17	IPENA17	Port	V	✓	✓	×	×	×
16	IPENA16	Port	U	✓	×	×	×	×
15	IPENA15	Port	T	✓	✓	×	×	×
14	IPENA14	Port	R	✓	✓	✓	×	×
13	IPENA13	Port	P	✓	✓	✓	✓	✓
12	IPENA12	Port	N	✓	✓	✓	✓	✓
11	IPENA11	Port	M	✓	✓	✓	✓	✓
10	IPENA10	Port	L	✓	✓	✓	✓	✓
9	IPENA09	Port	K	✓	✓	✓	✓	✓
8	IPENA08	Port	J	✓	✓	✓	✓	✓
7	IPENA07	Port	H	✓	✓	✓	✓	✓
6	IPENA06	Port	G	✓	✓	✓	✓	✓
5	IPENA05	Port	F	✓	✓	✓	✓	✓
4	IPENA04	Port	E	✓	✓	✓	✓	✓
3	IPENA03	Port	D	✓	✓	✓	✓	✓
2	IPENA02	Port	C	✓	✓	✓	✓	✓
1	IPENA01	Port	B	✓	✓	✓	✓	✓
0	IPENA00	Port	A	✓	✓	✓	✓	✓

✓: Available, ×: N/A

1.5.3. *[CGFSYSENB]*

Table 1.12 Allocation of *[CGFSYSENB]* by Each Product

Bit	Bit symbol	Destination	Channel number/ unit name/port name	M3HQ	M3HP	M3HN	M3HM	M3HL
31	IPENB31	SIWDT	0	✓	✓	✓	✓	✓
30	IPENB30	-	-	×	×	×	×	×
29	IPENB29	-	-	×	×	×	×	×
28	IPENB28	-	-	×	×	×	×	×
27	IPENB27	-	-	×	×	×	×	×
26	IPENB26	-	-	×	×	×	×	×
25	IPENB25	UART	7	✓	✓	✓	×	×
24	IPENB24	UART	6	✓	✓	✓	✓	✓
23	IPENB23	TRGSEL	0, 1	✓	✓	✓	✓	✓
22	IPENB22	TRM	-	✓	✓	✓	✓	✓
21	IPENB21	OFD	-	✓	✓	✓	✓	✓
20	IPENB20	CRC	-	✓	✓	✓	✓	✓
19	IPENB19	RAMP	-	✓	✓	✓	✓	✓
18	IPENB18	DAC	1	✓	✓	✓	✓	✓
17	IPENB17	DAC	0	✓	✓	✓	✓	✓
16	IPENB16	COMP	0	✓	✓	✓	✓	✓
15	IPENB15	ADC	A	✓	✓	✓	✓	✓
14	IPENB14	I2C	3	✓	✓	×	×	×
13	IPENB13	I2C	2	✓	✓	✓	✓	✓
12	IPENB12	I2C	1	✓	✓	✓	✓	×
11	IPENB11	I2C	0	✓	✓	✓	✓	✓
10	IPENB10	UART	5	✓	✓	✓	✓	✓
9	IPENB09	UART	4	✓	✓	✓	✓	✓
8	IPENB08	UART	3	✓	✓	✓	✓	✓
7	IPENB07	UART	2	✓	✓	✓	✓	✓
6	IPENB06	UART	1	✓	✓	✓	✓	✓
5	IPENB05	UART	0	✓	✓	✓	✓	✓
4	IPENB04	TSPI	4	✓	✓	×	×	×
3	IPENB03	TSPI	3	✓	✓	✓	✓	×
2	IPENB02	TSPI	2	✓	✓	✓	✓	×
1	IPENB01	TSPI	1	✓	✓	✓	✓	×
0	IPENB00	TSPI	0	✓	✓	✓	✓	✓

✓: Available, ×: N/A

2. Memory Map

2.1. Overview

The memory maps for TMPM3H Group(2) are based on the Arm Cortex-M3 processor core memory map.

The internal ROM, internal RAM, and special function registers (SFR) of TMPM3H Group(2) are mapped to the Code, SRAM and peripheral regions of the Cortex-M3 respectively. The special function register (SFR) means the control registers of all input/output ports and peripheral functions.

The CPU register area is the processor core's internal register region.

For more information on each region, see the "Arm Cortex-M3 Processor Technical Reference Manual".

Note that access to regions indicated as "Fault" causes a bus fault if bus faults are enabled, or causes a hard fault if bus faults are disabled. Also, do not access the vendor-specific region.

2.1.1. TMPM3HxF10B

- Code Flash: 1MB
- RAM: 128KB
- Data Flash: 32KB
- Target products: TMPM3HQF10BFG, TMPM3HPF10BFG, TMPM3HPF10BDFG, TMPM3HNF10BFG, TMPM3HNF10BDFG, TMPM3HMF10BFG, TMPM3HLF10BUG

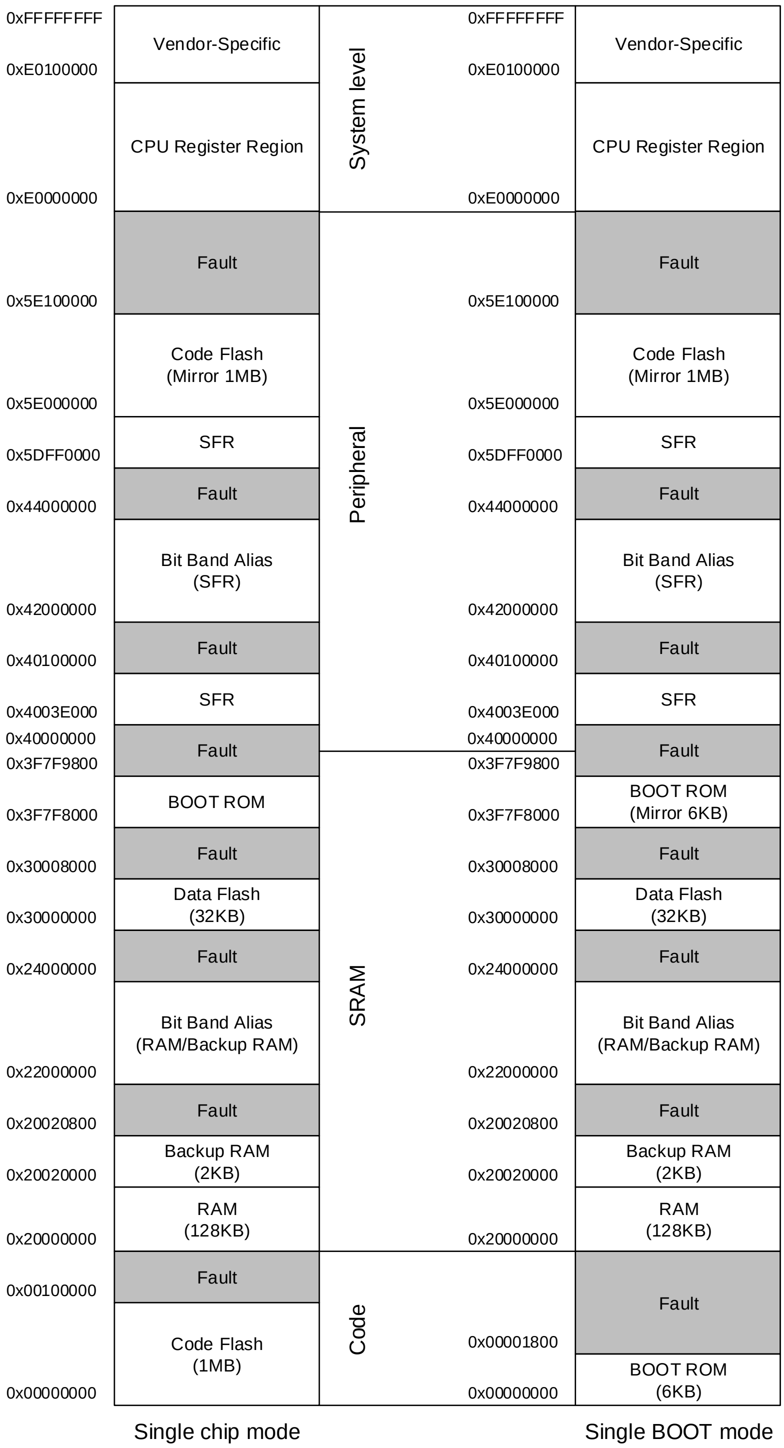

Figure 2.1 TMPM3HxF10

2.1.2. TMPM3HxFDB

- Code Flash: 512KB
- RAM: 128KB
- Data Flash: 32KB
- Target products: TMPM3HNFDBFG

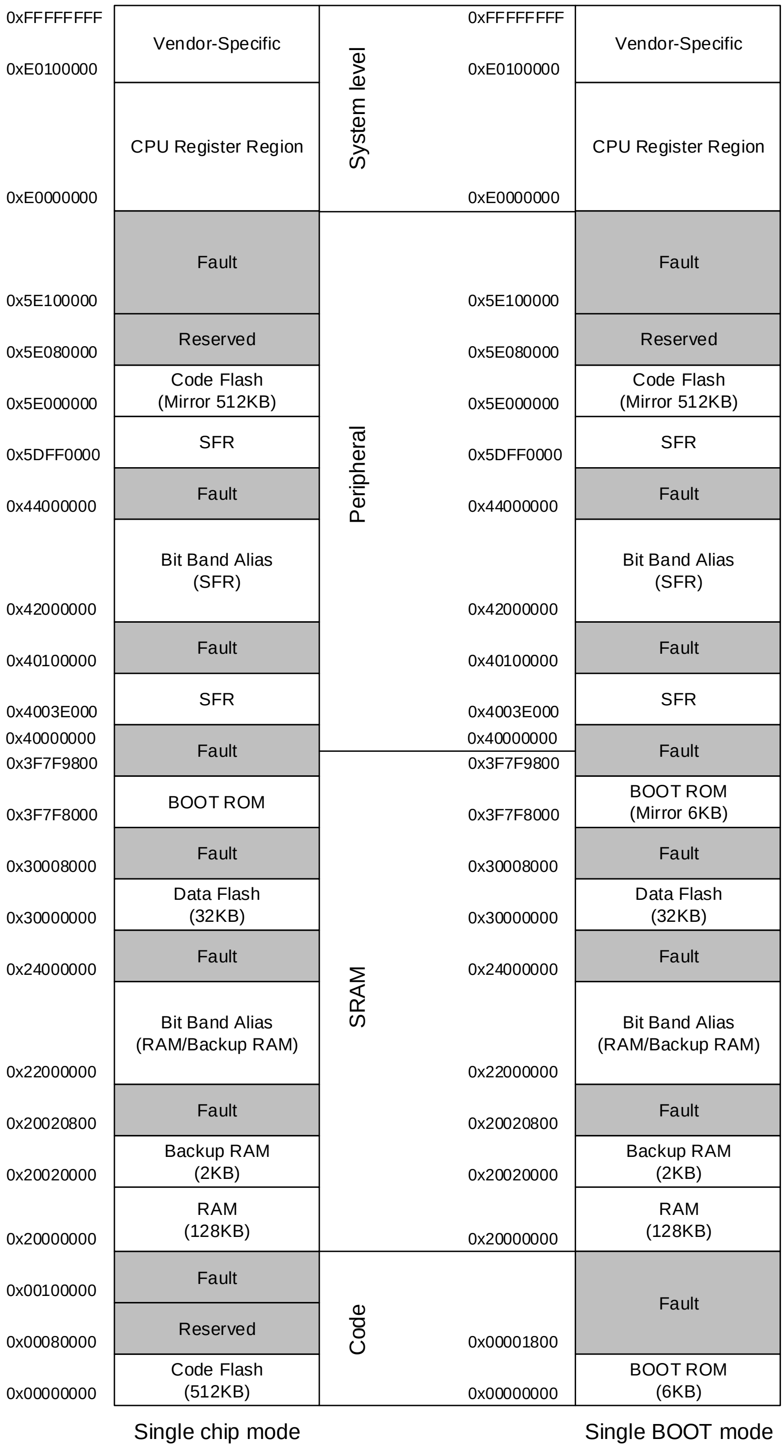

Figure 2.2 TMPM3HxFD

2.2. Bus Matrix

TMPM3H Group(2) contains two bus masters such as a CPU core and DMA controllers.

Bus masters connect to slave ports (S0 to S4) of Bus Matrix. In the bus matrix, master ports (M0 to M14) connect to peripheral functions via connections described as (o) or (●) in the following figure. (●) shows a connection to a mirror area.

While multiple slaves are connected on the same bus master line in the Bus Matrix, if multiple slave accesses are generated at the same time, a priority is given to access from a master with the smallest slave number.

2.2.1. Structure

2.2.1.1. Single Chip Mode

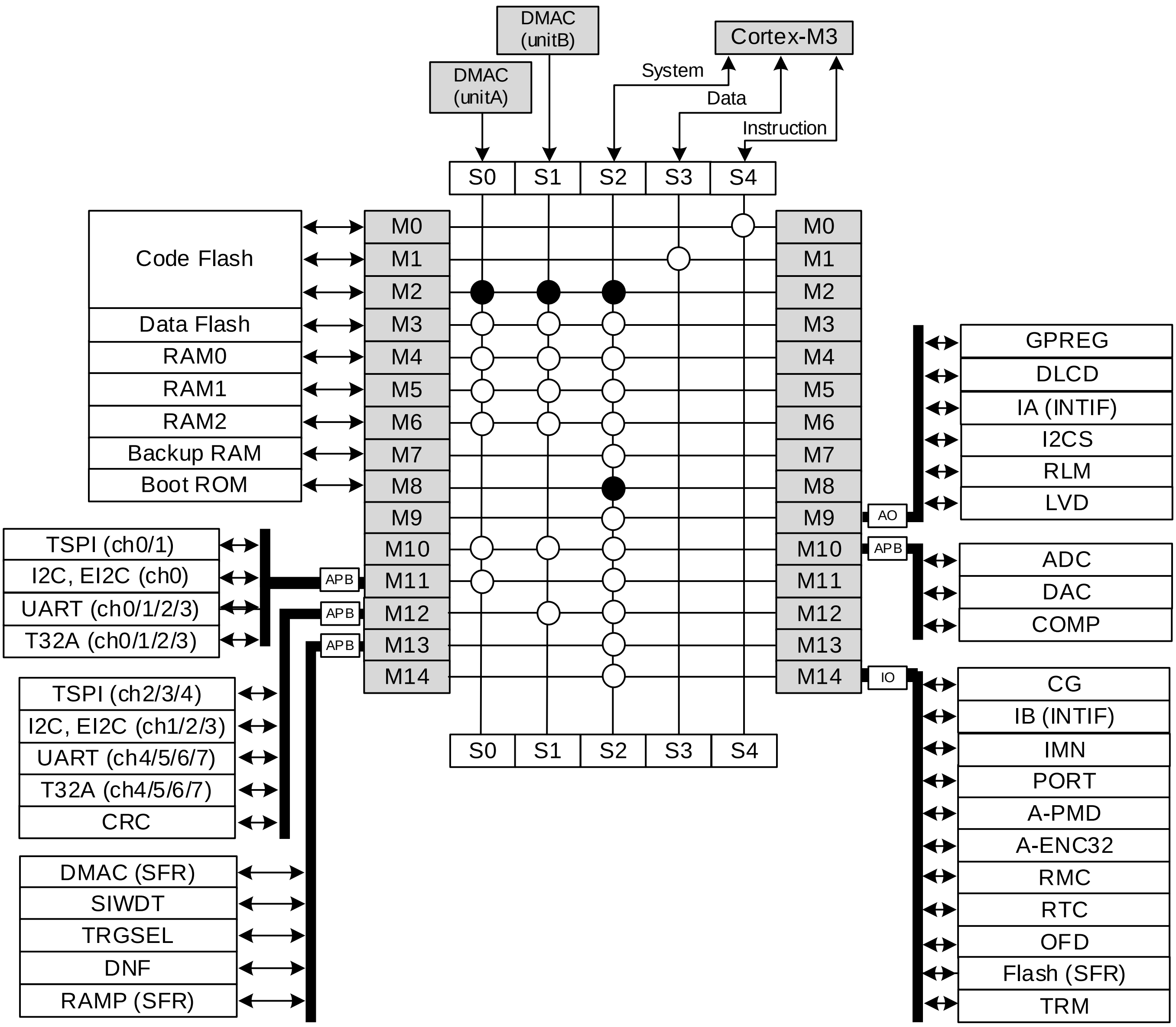

Figure 2.3 Single Chip Mode

2.2.1.2. Single Boot Mode

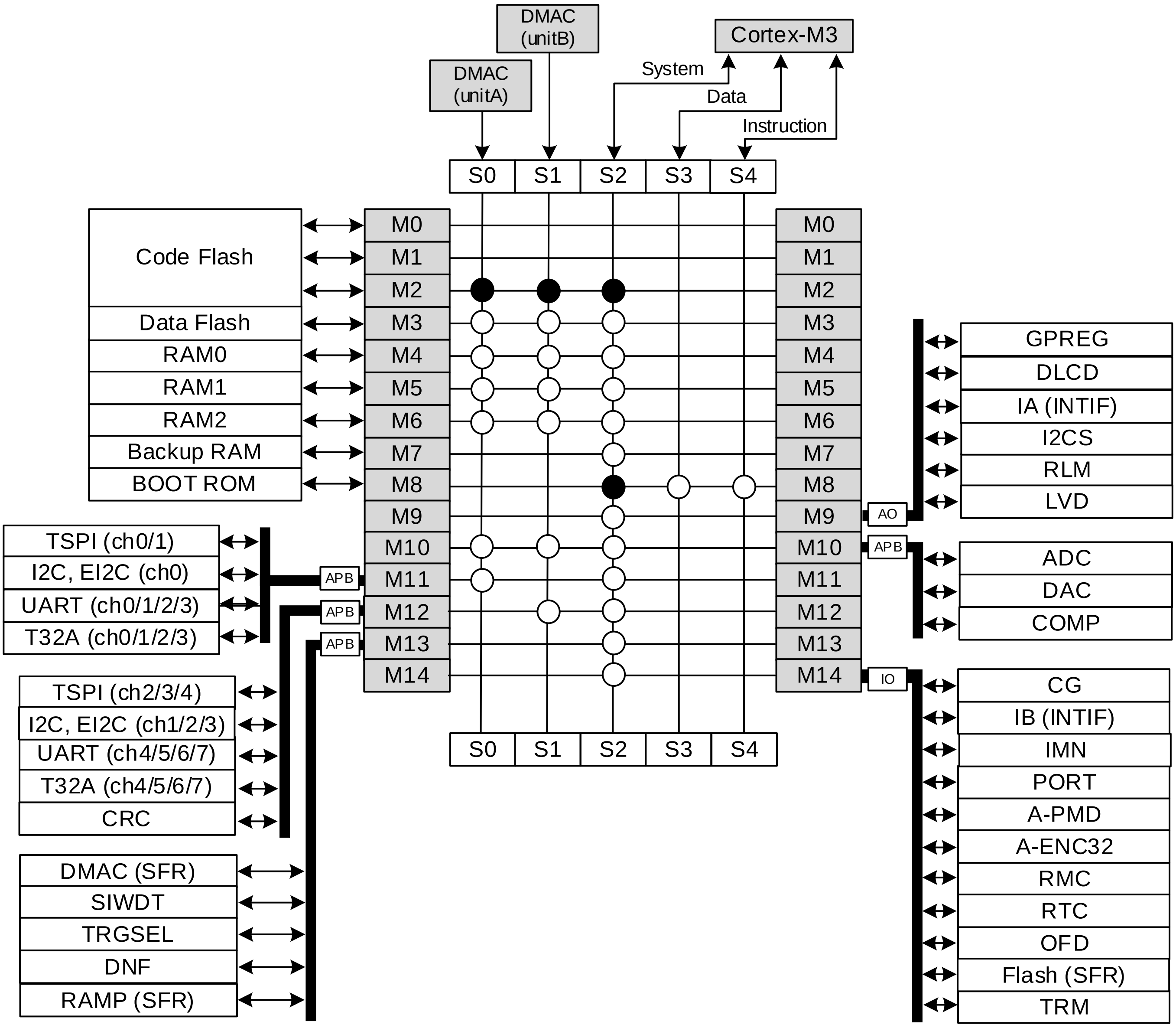

Figure 2.4 Single Boot Mode

2.2.2. Connection Table

2.2.2.1. Code area/ SRAM area

(1) Single chip mode

Table 2.1 Single Chip Mode

Start Address	Slave		Master DMAC (unit A) S0	Master DMAC (unit B) S1	Master Core S-Bus S2	Master Core D-Bus S3	Master Core I-Bus S4
0x00000000	Code Flash	M0	Fault	Fault	-	Fault	✓
		M1	Fault	Fault	-	✓	Fault
0x00100000	Fault	-	Fault	Fault	-	Fault	Fault
0x20000000	RAM0	M4	✓	✓	✓	-	-
0x20008000	RAM1	M5	✓	✓	✓	-	-
0x20010000	RAM2	M6	✓	✓	✓	-	-
0x20020000	Backup RAM	M7	Fault	Fault	✓	-	-
0x20020800	Fault	-	Fault	Fault	Fault	-	-
0x22000000	Bit band alias	-	Fault	Fault	✓	-	-
0x24000000	Fault	-	Fault	Fault	Fault	-	-
0x30000000	Data Flash	M3	✓	✓	✓	-	-
0x30008000	Fault	-	Fault	Fault	Fault	-	-
0x3F7F8000	Boot ROM	M8	Fault	Fault	✓	-	-
0x3F7F9800	Fault	-	Fault	Fault	Fault	-	-
For the address of this area, refer to the "Table 2.3 Peripheral Area".							
0x5E000000	Code Flash (Mirror)	M2	✓	✓	✓	-	-

✓: Accessible, -: No access, Fault: Fault occurred

(2) Single boot mode

Table 2.2 Single Boot Mode

Start Address	Slave		Master DMAC (unit A) S0	Master DMAC (unit B) S1	Master Core S-Bus S2	Master Core D-Bus S3	Master Core I-Bus S4
0x00000000	Boot ROM	M8	Fault	Fault	-	✓	✓
0x00001800	Fault	-	Fault	Fault	-	Fault	Fault
0x20000000	RAM0	M4	✓	✓	✓	-	-
0x20008000	RAM1	M5	✓	✓	✓	-	-
0x20010000	RAM2	M6	✓	✓	✓	-	-
0x20020000	Backup RAM	M7	Fault	Fault	✓	-	-
0x20020800	Fault	-	Fault	Fault	Fault	-	-
0x22000000	Bit band alias	-	Fault	Fault	✓	-	-
0x24000000	Fault	-	Fault	Fault	Fault	-	-
0x30000000	Data Flash	M3	✓	✓	✓	-	-
0x30008000	Fault	-	Fault	Fault	Fault	-	-
0x3F7F8000	Boot ROM (Mirror)	M8	Fault	Fault	✓	-	-
0x3F7F9800	Fault	-	Fault	Fault	Fault	-	-
For the address of this area, refer to the "Table 2.3 Peripheral Area"							
0x5E000000	Code Flash (Mirror)	M2	✓	✓	✓	-	-

✓: Accessible, -: No access, Fault: Fault occurred

2.2.2.2. Peripheral Areas

Table 2.3 Peripheral Areas

Start Address	Slave		Master				
			DMAC (unit A)	DMAC (unit B)	Core S-Bus	Core D-Bus	Core I-Bus
			S0	S1	S2	S3	S4
0x40000000	Fault	-	Fault	Fault	Fault	-	-
0x4003E000	IA (INTIF)	M9	Fault	Fault	✓	-	-
0x4003E400	RLM		Fault	Fault	✓	-	-
0x4003E800	I2CS		Fault	Fault	✓	-	-
0x4003EC00	LVD		Fault	Fault	✓	-	-
0x4003F200	DLCD		Fault	Fault	✓	-	-
0x4004C000	DMAC (SFR)	M13	Fault	Fault	✓	-	-
0x40054000	DAC (ch0/1)	M10	✓	✓	✓	-	-
0x40098000	TSPI (ch0/1)	M11	✓	Fault	✓	-	-
0x4009A000	TSPI (ch2/3/4)	M12	Fault	✓	✓	-	-
0x400A0000	I2C (ch0)	M11	✓	Fault	✓	-	-
0x400A1000	I2C (ch1/2/3)	M12	Fault	✓	✓	-	-
0x400A5000	EI2C (ch0)	M11	✓	Fault	✓	-	-
0x400A6000	EI2C (ch1/2/3)	M12	Fault	✓	✓	-	-
0x400B8800	ADC	M10	✓	✓	✓	-	-
0x400BA000	T32A (ch0/1/2/3)	M11	✓	Fault	✓	-	-
0x400BA400	T32A (ch4/5/6/7)	M12	Fault	✓	✓	-	-
0x400BB000	UART (ch0/1/2/3)	M11	✓	Fault	✓	-	-
0x400BB400	SIWDT	M13	Fault	Fault	✓	-	-
0x400BB600	DNF (A/B)		Fault	Fault	✓	-	-
0x400BB800	TRGSEL		Fault	Fault	✓	-	-
0x400BBB00	RAMP (Parity)		Fault	Fault	✓	-	-
0x400BBC00	CRC	M12	Fault	✓	✓	-	-
0x400BBD00	UART (ch4/5)		Fault	✓	✓	-	-
0x400BC000	COMP	M10	✓	✓	✓	-	-
0x400BC400	UART (ch6/7)	M12	Fault	✓	✓	-	-
0x400BE000	DNF (C)	M13	Fault	Fault	✓	-	-
0x400C0000	PORT	M14	Fault	Fault	✓	-	-
0x400CC000	RTC		Fault	Fault	✓	-	-
0x400E7000	RMC		Fault	Fault	✓	-	-
0x400F1000	OFD		Fault	Fault	✓	-	-
0x400F3000	CG		Fault	Fault	✓	-	-
0x400F3200	TRM		Fault	Fault	✓	-	-
0x400F4E00	IB (INTIF)		Fault	Fault	✓	-	-
0x400F4F00	IMN		Fault	Fault	✓	-	-
0x400F6000	A-PMD		Fault	Fault	✓	-	-
0x400F7000	A-ENC32		Fault	Fault	✓	-	-
0x40100000	Fault	-	Fault	Fault	Fault	-	-
0x42000000	Bit Band Alias	-	Fault	Fault	✓	-	-
0x44000000	Fault	-	Fault	Fault	Fault	-	-
0x5DFF0000	Flash (SFR)	M14	Fault	Fault	✓	-	-

✓: Accessible, -: No access, Fault: Fault occurred

3. Power Supply and Reset Operation

3.1. Outline

This section describes how to turn on a power supply, and how to assert and deassert a power-on reset and reset.

Function classification	Factor	Functional description
Cold reset (Reset by turning on a power supply)	Power-on Reset	Reset which occurs at the time of turning on or off a power supply.
	LVD reset	Reset which occurs when a power supply voltage is the set-up voltage or below.
	Reset pin	Reset by a RESET_N pin
	PORF reset	Reset which occurs at the time of a power supply turning on or turning off. It is for Flash memory and debug circuit with priority.
Warm reset (Reset without turning on a power supply)	Internal reset	Reset by SIWDT, OFD, LVD, LOCKUP, and <SYSRESETREQ>
	Reset pin	Reset by a RESET_N pin
Reset by STOP2 mode release	Interrupt	Reset which is performed to main power domain during return operation from the STOP2 mode. (STOP2REQ)
	LVD reset	Reset when DVDD5 is equal to or less than the voltage which is set on LVD circuit.
	Reset pin	Reset by a RESET_N pin

3.2. Function and Operation

This chapter explains about power on, power off, and reset.

Note: Refer to the datasheet "Electrical Characteristics" chapter for the time and voltage of description of the symbol in a figure.

3.2.1. Cold Reset

When turn on a power supply, the stabilization times for the built-in regulator, the built-in Flash memory, and the built-in high-speed oscillator are necessary. The TXZ + family automatically inserts a wait time for the stabilization of these circuits.

When turning on the power, please make sure that the slope of the power supply voltage rises to the right.

When the power supply voltage drops and rises near POR and PORF detection, it may not operate normally even if the power supply voltage rises to the guaranteed operating range.

3.2.1.1. Reset by Power-on Reset Circuit (without Using RESET_N Pin)

After a supply voltage exceeds the release voltage of a power-on reset (POR), internal reset is deasserted after "Internal initialization time" is elapsed. Please increase a supply voltage goes up into an operating voltage range before "Internal initialization time" is elapsed. The CPU operates after internal reset is released.

After a supply voltage exceeds the release voltage of a power-on reset (POR), LVD continues to output reset signal until supply voltage exceeds the LVD release voltage. And internal reset has priority during the time of "Internal initialization time". When rising time of a supply voltage beyond "Internal initialization time", please refer to "3.2.1.3. Continuation of Reset by LVD".

For example, if the operating voltage of a circuit board is more than 2.7V, after power-on reset released increase a supply voltage to 2.7V before "Internal initialization time" is elapsed. And if the operating voltage of a circuit board is more than 4.5V, after power-on reset released increase a supply voltage to 4.5V before "Internal initialization time" is elapsed.

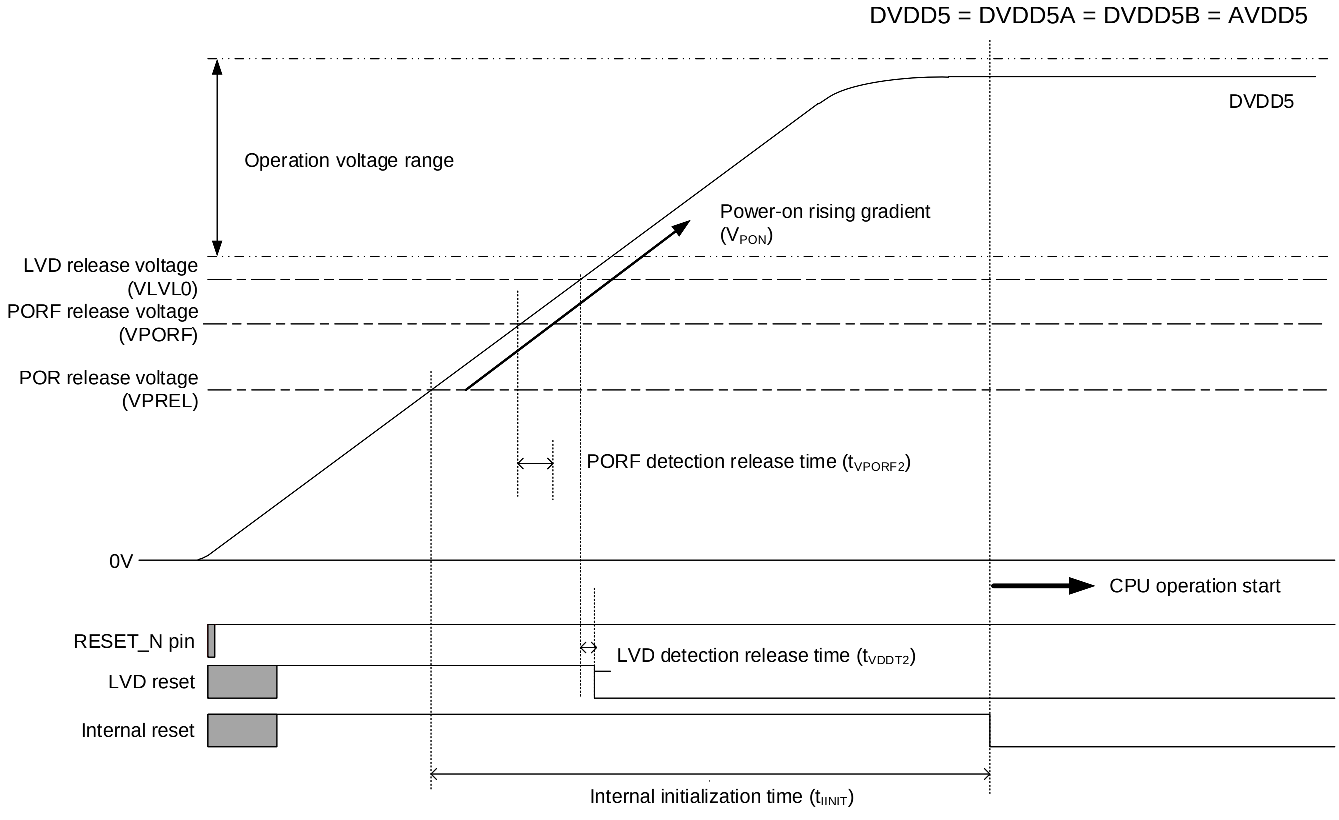

Figure 3.1 Reset Operation by Power-on Reset Circuit

Note: When you use only a power-on reset Circuit without RESET_N pin, the RESET_N pin should input "High" level or opened.

3.2.1.2. Reset by RESET_N Pin

When turn on a power supply, it can control the timing of reset release by using RESET_N pin.

After a supply voltage exceeds the release voltage of a power-on reset and even after "Internal initialization time" elapsed and RESET_N pin is still "Low", internal reset is extended.

After a supply voltage goes up into an operating voltage range and a RESET_N pin becomes "High", Internal reset is deasserted after "CPU operation latency time" elapses.

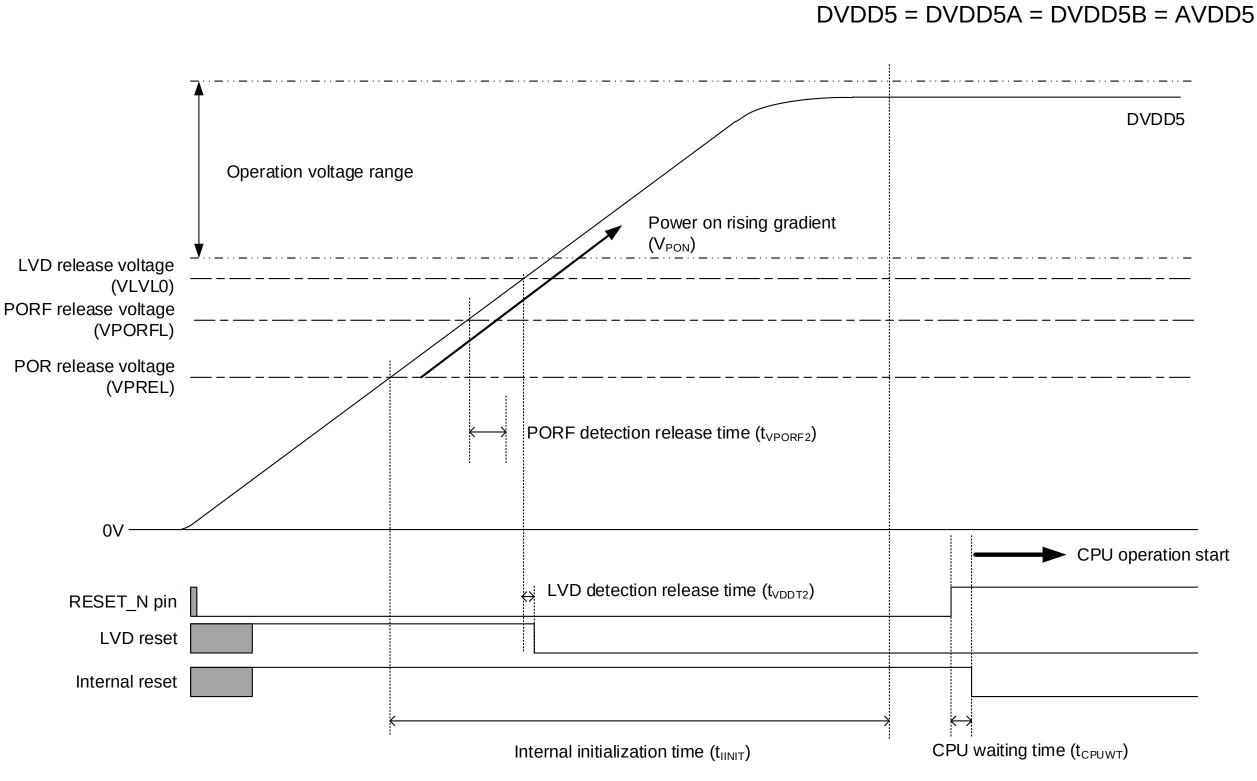

Figure 3.2 Reset Operation by RESET_N pin (1)

In case of RESET_N pin input change from "Low" to "High" before "Internal initialization time" elapses, internal reset signal is released after "Internal initialization time" elapses.

Please goes up a supply voltage into an operating voltage range before "Internal initialization time" elapses. The CPU operates after internal reset release.

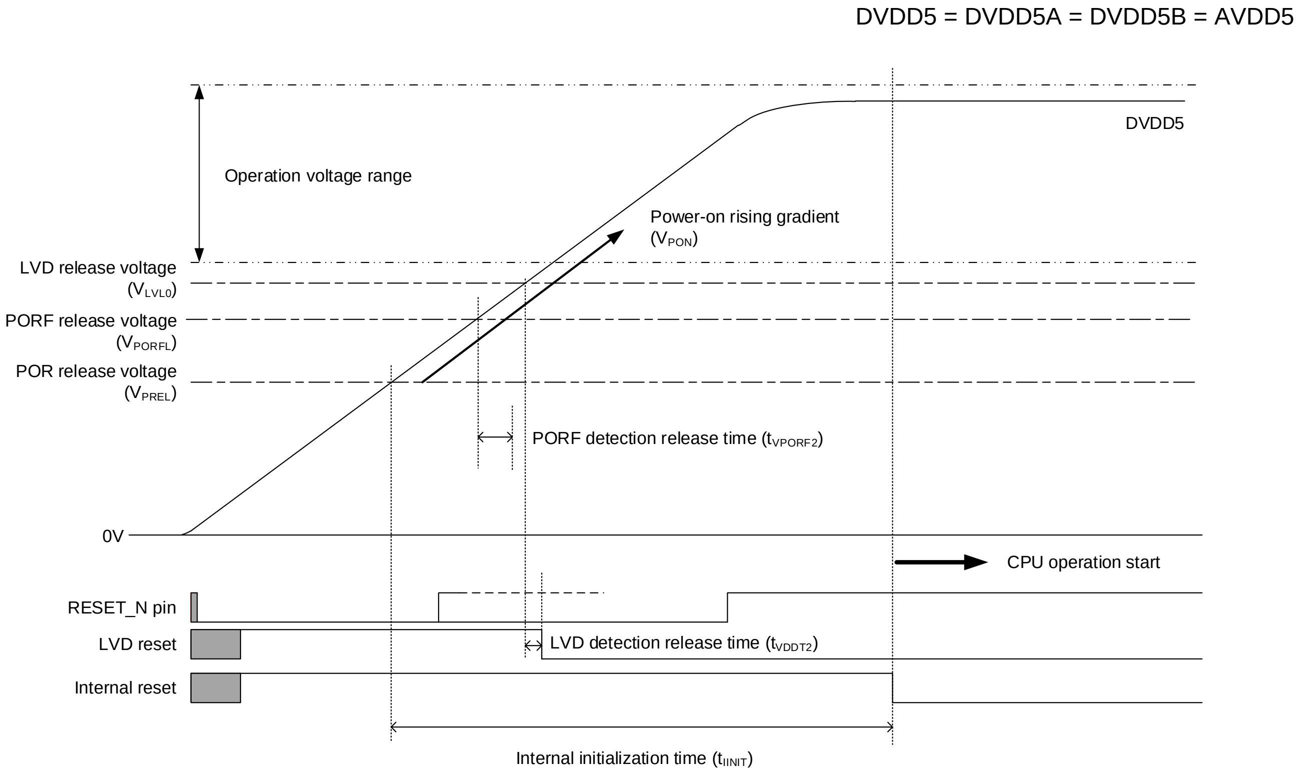

Figure 3.3 Reset Operation by RESET_N Pin (2)

3.2.1.3. Continuation of Reset by LVD

When the power supply voltage has not exceeded the LVD release voltage even after "Internal initialization time" elapses, LVD generates the reset signal and the reset state continues. After the power supply voltage exceeds the LVD release voltage and "LVD detection release time" + "CPU operation wait time" elapses, the internal reset is deasserted. And CPU starts operating. Refer to reference manual "Voltage detection circuit" for detail of LVD.

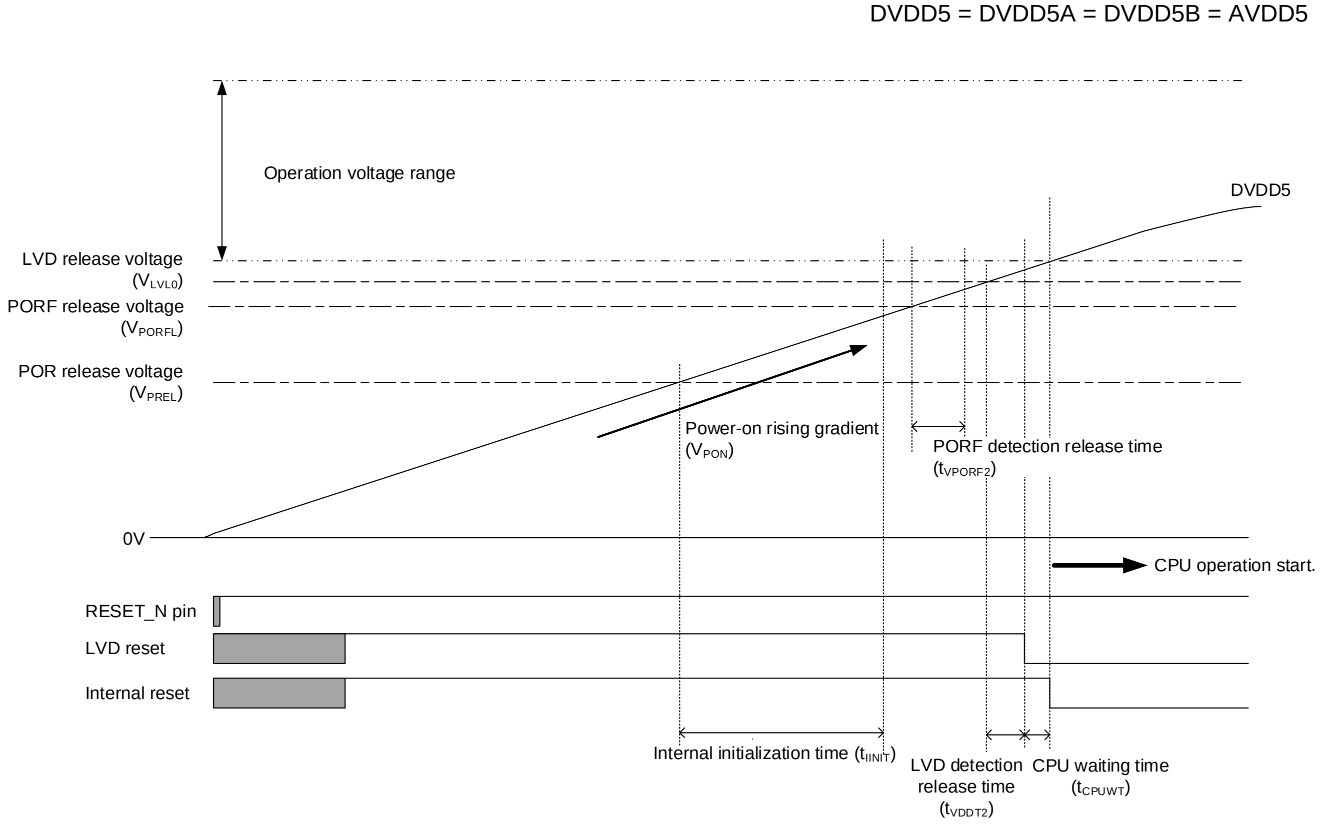

Figure 3.4 Reset Operation by LVD Reset

3.2.2. Warm Reset

3.2.2.1. Warm Reset by RESET_N Pin

When resetting with the RESET_N pin, set the RESET_N pin to "Low" for at least 17.2 μs or more while the power supply voltage is within the operating range.

When the "Low" period of a RESET_N pin is longer than "Internal processing time", after a RESET_N pin changes to "High", Internal reset is released after "CPU waiting time" elapsed.

When the "Low" period of a RESET_N pin is shorter than "Internal processing time", after internal reset is extended and from a RESET_N pin changes "Low", Internal reset is release after "Internal processing time" + "CPU waiting time" has elapsed, internal reset will be released.

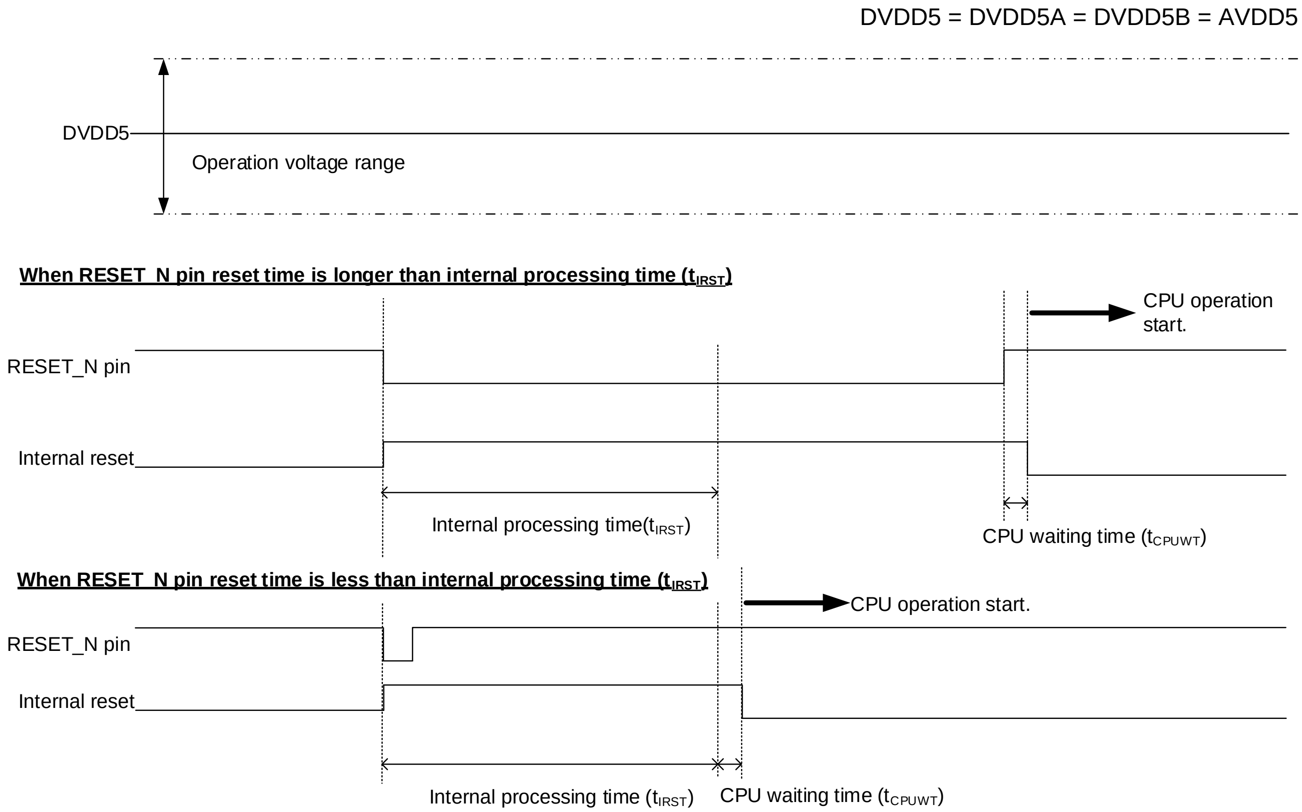

Figure 3.5 Warm Reset Operation

3.2.2.2. Warm Reset by Internal Reset

In case of reset asserted by internal factors, such as SIWDT, OFD, LVD, LOCKUP, and <SYSRESETREQ>, Internal reset is released after "Internal processing time" + "CPU waiting time" elapsed.

3.2.3. Reset by STOP2 Mode Release

When RESET_N pin is changed to "Low" or LVD reset occurred during STOP2 mode, STOP2 released. The power supply is turned on and assert reset to Main Power Domain. After RESET_N pin is changed to "High" or LVD reset is released, start operation in NORMAL mode. At that time, condition of CPU is as same as cold reset except ***[RLMLOSCCR]***, ***[RLMRSTFLG0]***, ***[RLMRSTFLG1]***.

When asserted interrupt request during STOP2 mode, also STOP2 released. The power supply is turned on and assert reset to Main Power Domain in the sequence of releasing STOP2 mode. Refer to the reference manual "Clock Control and Operation Mode" for the operation at STOP2 releasing.

3.2.4. Starting Single Boot Mode by Reset

When "Low" is input to a BOOT_N pin, and then reset release, "single boot mode" will be started.

When turn on power supply, the time of input "Low" to the RESET_N pin is equal to or longer than "Internal initialization time" to reset. And deassert RESET_N pin to "High", after a supply voltage goes up into an operating voltage range.

Refer to the reference manual "Flash Memory" for the details of "Single Boot Mode".

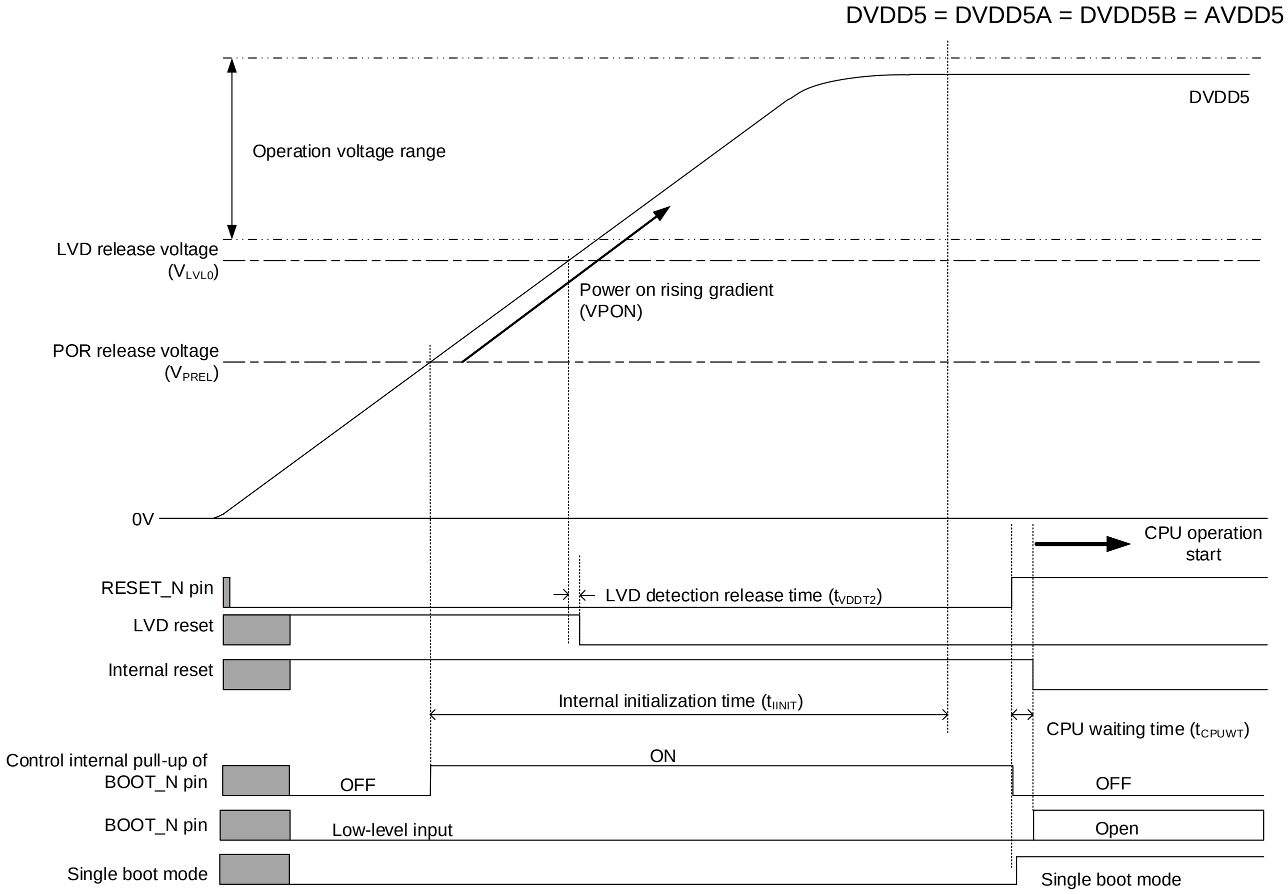

Figure 3.6 Power Supply is Turned On and Starting Single Boot Mode

When the supply voltage is stable within an operating voltage range, input "Low" to RESET_N pin for reset equal to or longer than "Internal processing time", while "Low" is input to the BOOT_N pin.

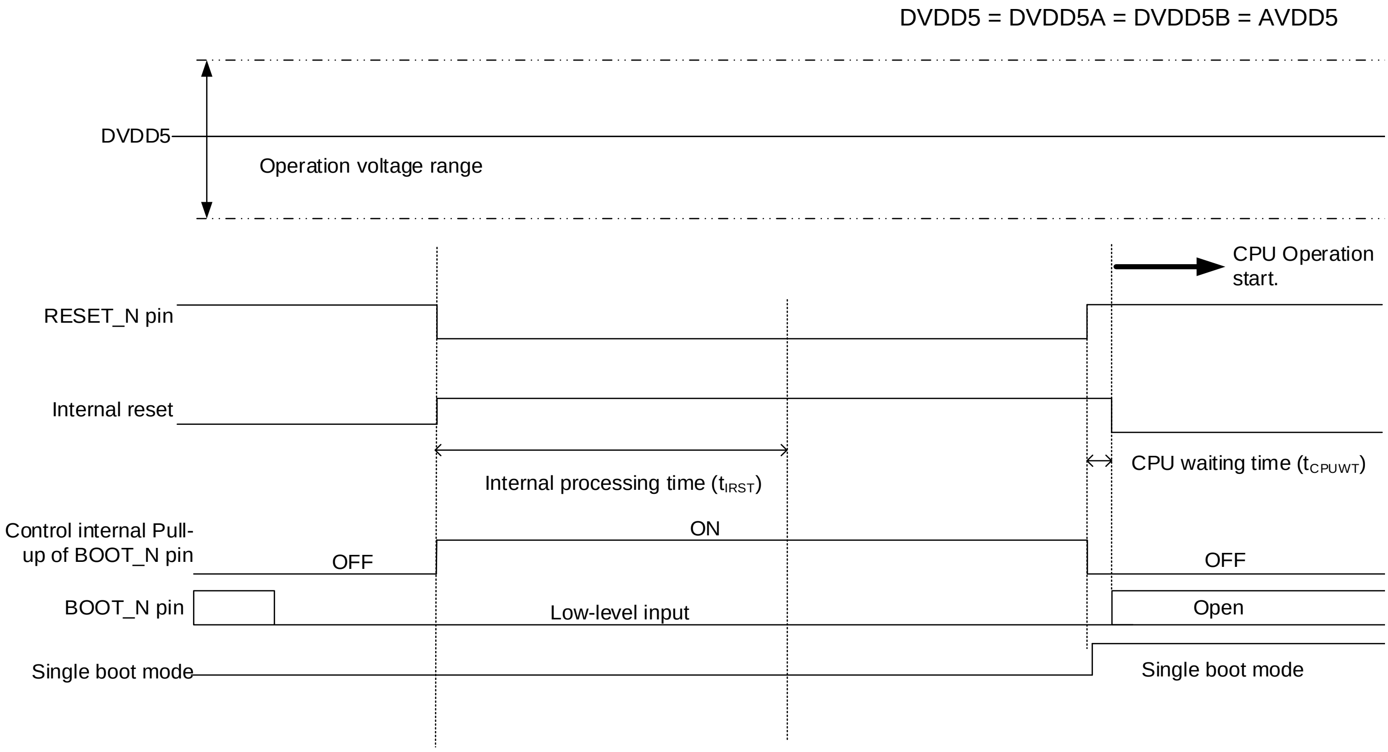

Figure 3.7　Starting Single Boot Mode when Power Supply is Stable

3.2.5. Power-on Reset Circuit

The power-on reset circuit (POR) generates a reset signal when the power is turned on or turned off.

Note: The power-on reset Circuit may not operate correctly due to the fluctuation of the power supply. Equipment should be designed with full consideration of the electrical characteristics.

The power-on reset Circuit consists of a Detection voltage generation circuit, a Reference voltage generation circuit, and a Comparator.

The supply voltage has referred to DVDD5 (= DVDD5A = DVDD5B).

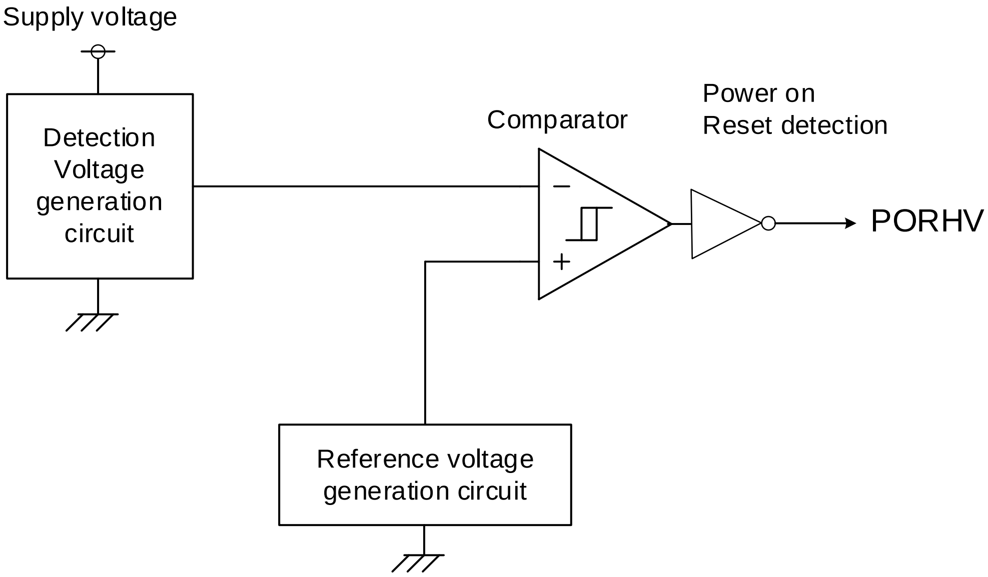

Figure 3.8 Power-on Reset Circuit

3.2.5.1. Operation at Time of Turn On

When turn on power supply, while the power supply voltage is equal to or lower than power-on reset release voltage (V_{PREL}), the power-on reset detection signal is generated. Refer to "Figure 3.1 Reset Operation by Power-on Reset Circuit" for detail.

While the power-on reset signal is generated, the reset is asserted to the CPU and the peripherals.

3.2.5.2. Operation at Time of Turn Off

When turn off power supply, after the power supply voltage is equal to or lower than power-on reset detection voltage (V_{PDET}), the power-on reset detection signal is generated.

While the power-on reset signal is generated, the reset is asserted to the CPU and the peripherals.

3.2.6. About Turn On Power Supply after Turn Off

When the power supply is turned off, a power supply voltage must be down gentler gradient than Max value of "Power gradient (V_{POFF})" specified in "Electrical Characteristics".

3.2.6.1. When Using External Reset Circuit or Internal LVD Reset Output

When the power supply is turned off and the power supply voltage drops below the operation guaranteed voltage, reset is performed with an external reset circuit or built-in LVD (when the voltage is less than the set voltage). After that, from the state where the reset is applied, please follow the same constraints as when turning on the power and turned on the power supply voltage.

3.2.6.2. When not Using External Reset Circuit and Internal LVD Reset Output

When the power supply is turned off and the power supply voltage drops below the operation guaranteed voltage, be sure to lower the power supply voltage below the power-on reset detection voltage (V_{PDET}) and hold it for 200μs or more. After that, please follow the same constraints as when turning on the power and turned on the power supply voltage.

When the power supply voltage drops below the power-on reset detection voltage (V_{PDET}) and cannot be held for 200μs or more, or when the same constraints as at power on cannot keep, the CPU may not operate properly.

3.2.7. After Reset Release

All of the control registers of the Cortex-M3 core and the peripheral function control register (SFR) are initialized by reset. But depend on the reset factor, initialized range is different.

Please refer to "Table 3.1 Reset Factor and Initialized Range" for the initialized range by each reset factor.

The reset factor when reset occurs can be checked by a reset flag register which are ***[RLMRSTFLG0]*** and ***[RLMRSTFLG1]***. For detail of ***[RLMRSTFLG0]*** and ***[RLMRSTFLG1]***, please refer to the reference manual "Exception".

After the reset is released, CPU starts operation by a clock of internal high-speed oscillator1 (IHOSC1). The external clock and PLL multiple circuit should be set if necessary.

3.2.7.1. Reset Factor and Reset Initialized Range

A reset factor and the range initialized are shown in Table 3.1.

Table 3.1 Reset Factor and Initialized Range

Registers and peripheral function		Reset factors									
		STOP2 mode release		Cold reset	Warm reset (Note1)						
		Interrupt factor	Reset pin (Note1) (Note4)	POR (Note1)	RESET_N pin	OFD reset	WDT reset	LVD reset	PORF reset	CPU <SYSRESETREQ> reset	CPU LOCKUP reset
	Reset signal name	STOP2 REQ	RESET_N	PORHV	RESET_N	OFD RSTOUT	WDT RSTOUT	LVD RSTOUT	PORF RESET	SYS RESET REQ	LOCKUP RESET REQ
RTC	***[RTCSECR]*** ***[RTCMINR]*** ***[RTCHOURR]*** ***[RTCDAYR]*** ***[RTCDATER]*** ***[RTCMONTHR]*** ***[RTCYEARR]*** ***[RTCADJCTL]*** ***[RTCADJDAT]*** ***[RTCADJSIGN]*** ***[RTCPAGER]*** (Note2)	×	×	×	×	×	×	×	×	×	×
	Others	×	✓	✓	✓	✓	✓	✓	✓	✓	✓
Low-speed oscillation Power control reset flag	***[RLMSHTDNOP]*** ***[RLMPROTECT]***	×	✓	✓	✓	✓	✓	✓	✓	✓	✓
	[RLMLOSCCR] ***[RLMRSTFLG0]*** ***[RLMRSTFLG1]***	×	×	✓	×	×	×	×	×	×	×
Interrupt control	***[IAIMCxx]*** ***[IANIC00]***	×	✓	✓	✓	✓	✓	✓	✓	✓	✓
	[IBIMCxxx] ***[IBNIC00]***	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Flash	***[FCSBMR]***	✓	✓	✓	×	×	×	×	✓	×	×
Port	All registers	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
DLCD (Note3)		×	✓	✓	✓	✓	✓	✓	✓	✓	✓
OFD		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
LVD		×	✓	✓	✓	×	×	×	×	×	×
Debugging interface		✓	✓	✓	×	×	×	×	✓	×	×
Others		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

✓: It is initialized.

×: It is not initialized.

Note1: When reset is performed, the data of on-chip RAM will not be guaranteed.
Note2: ***[RTCPAGER]***<ENATMR><ENAALM> are not initialized. Other symbols are initialized.
Note3: ***[DLCDBUFn]*** display buffers are not initialized.
Note4: Reset area when releasing STOP2 mode by LVD reset is as same as reset area released by the warm reset.

4. Revision History

Table 4.1 Revision History

Revision	Date	Description
1.0	2023-04-28	- First release
1.1	2024-04-22	- 1.2.6.1. The setting method of a system clock Step 1 is changed in (2) fosc setup (internal oscillation → external clock input) Step 5 is changed in (3) fosc setup (an external oscillation/external clock input → an internal oscillation) - 1.3.2. Mode State Transition Figure 1.2 is changed. - 1.3.2.1. IDLE mode transition flow Note is added. - 1.3.2.2. STOP1 Mode Transition Flow Step 12 is changed in a table. Note is deleted. - 1.3.2.3. STOP2 Mode Transition Flow Note2 is deleted.

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