3-Phase Multi-Level Inverter using MOSFET

Reference Guide

RD208-RGUIDE-01

TOSHIBA ELECTRONIC DEVICES & STORAGE CORPORATION

Table of Contents

1. Introduction

This Reference Guide (hereafter referred to as this guide) describes the specifications and operation procedure of 3-Phase Multi-Level Inverter using MOSFET (hereafter referred to as this inverter).

3-phase inverters are used to drive induction motors and synchronous motors used in industrial robots, etc. When output is AC 200 V, and a common 2-level inverter configuration is used, then one 600 V MOSFET is used on each of the upper and lower arms. By using a multi-stack MOSFET configuration per arm, the resolution of the voltage output is increased, and precise voltage output control is achieved, thus realizing a highly efficient inverter. This inverter uses four MOSFETs in each of the upper and lower arms, enabling up to 5-level PWM voltage output.

150 V power MOSFET TPH9R00CQ5 is used as a switching device. TPH9R00CQ5 features a high-speed built-in diode. It can reduce switching-loss in the inverter operation with inductive loads such as motors. Since four TPH9R00CQ5 are used for each arm, the configuration apparently operates as a MOSFET with a withstanding voltage of 600 V.

A small, high-speed switching driver coupler TLP152 is used for driving MOSFETs.

2. Specifications

Table 2.1 lists the main specifications of this inverter.

Table 2.1 Specifications of 3-Phase Multi-Level Inverter using MOSFET

Item	Specifications
Inverter Power Supply Input	DC 400 V (Max.)
Control Power Supply Input	DC 5 V, 100 mA (Max.)
Rated Output	AC 200 to 240 V, 10 A
Inverter Drive System	5-level (Max.) NPC method
Switching Frequency	100 kHz (Typ.) (Set by software)
Sensor Output	Bus voltage Low-side arm current (U/V/W phase)
Error Detection Output	Overcurrent (U/V/W phase)
Cooling System	Convection cooling
Board Size	240 x 150 mm
Board Layer Configuration	6-layer through-hole (outer layer 35 µm, inner layer 70 µm)

2.1. Circuit Block Diagram

Fig. 2.1 shows the block diagram of this inverter.

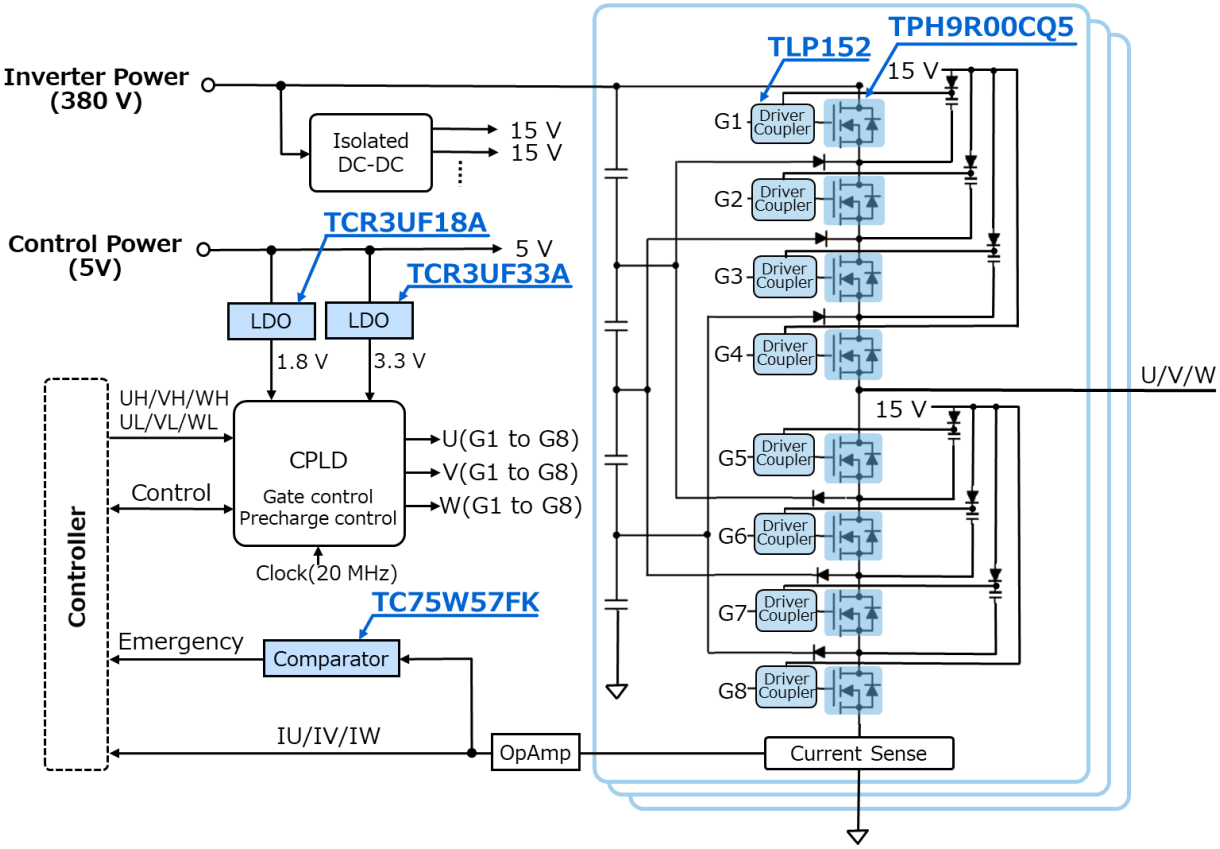


Fig. 2.1 Block Diagram of 3-Phase Multi-Level Inverter using MOSFET

2.2. Appearance and Component Layout

Fig. 2.2, 2.3 and 2.4 show the appearance of this inverter, and Fig. 2.5 and 2.6 show the layout of main components.

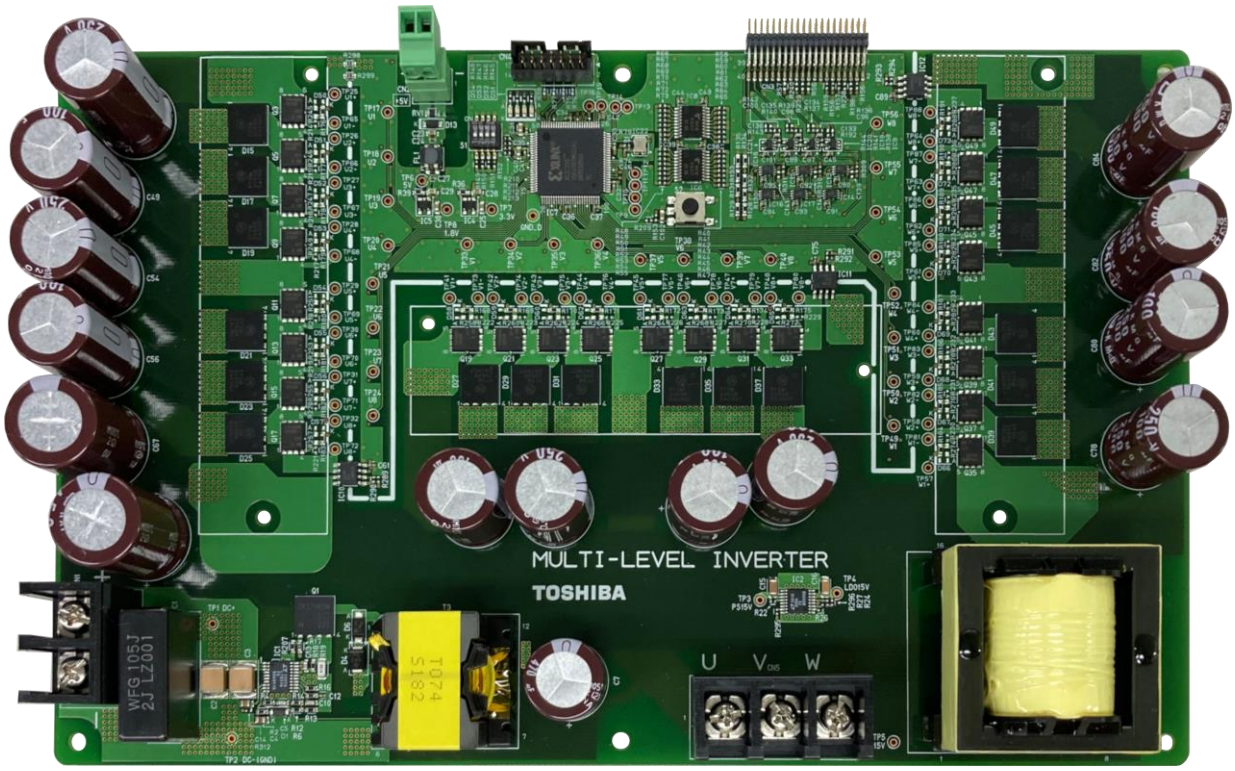


Fig. 2.2 3-Phase Multi-Level Inverter using MOSFET
Front Side View of PCB

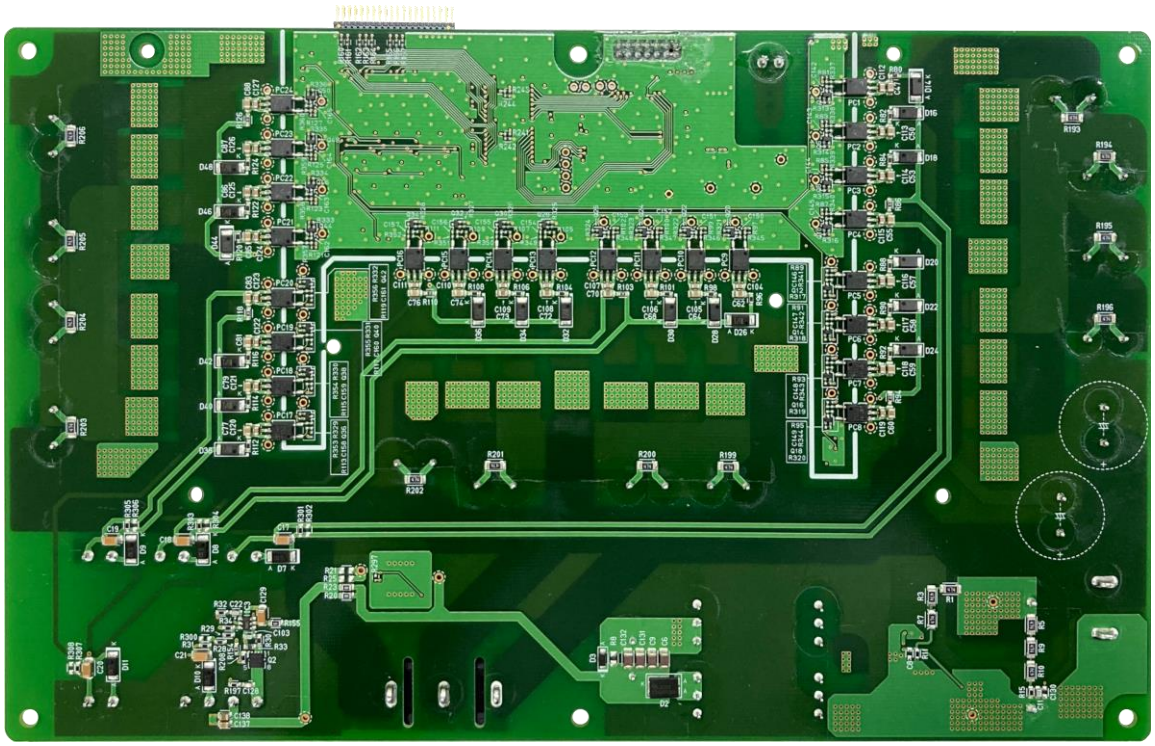


Fig. 2.3 3-Phase Multi-Level Inverter using MOSFET
Back Side View of PCB

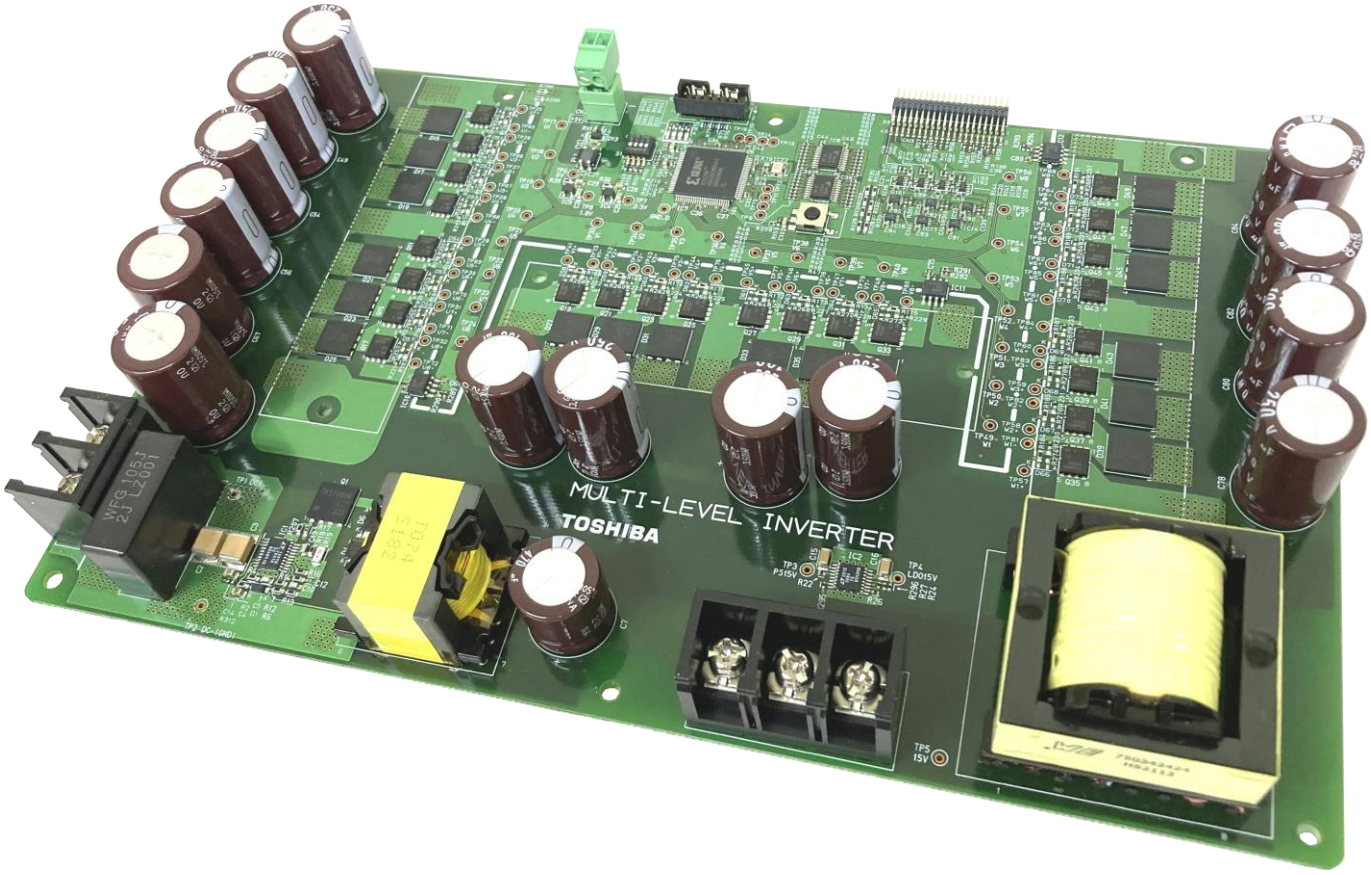


Fig. 2.4 3-Phase Multi-Level Inverter using MOSFET
Side View of PCB

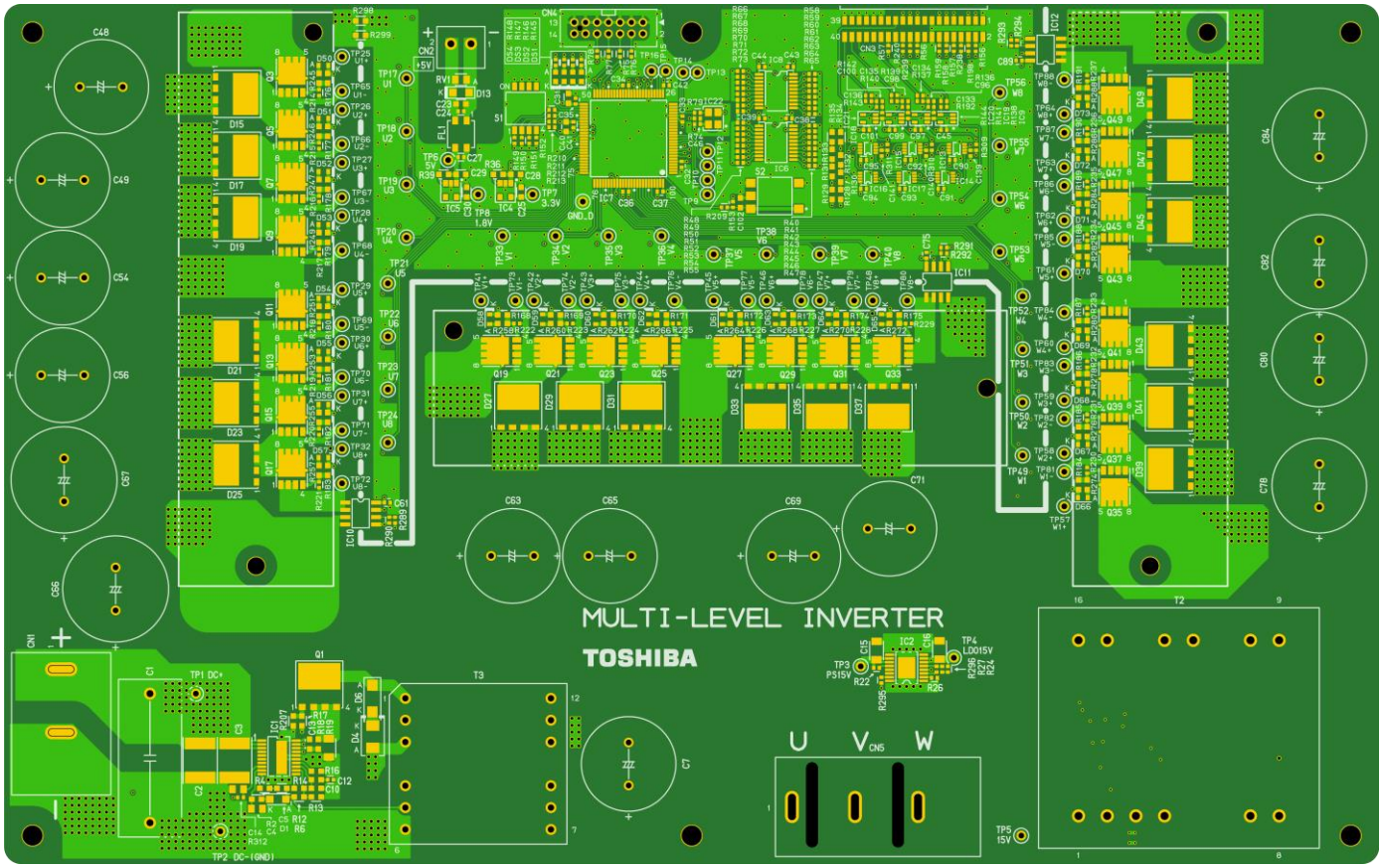


Fig. 2.5 Main Component Layout (Front)

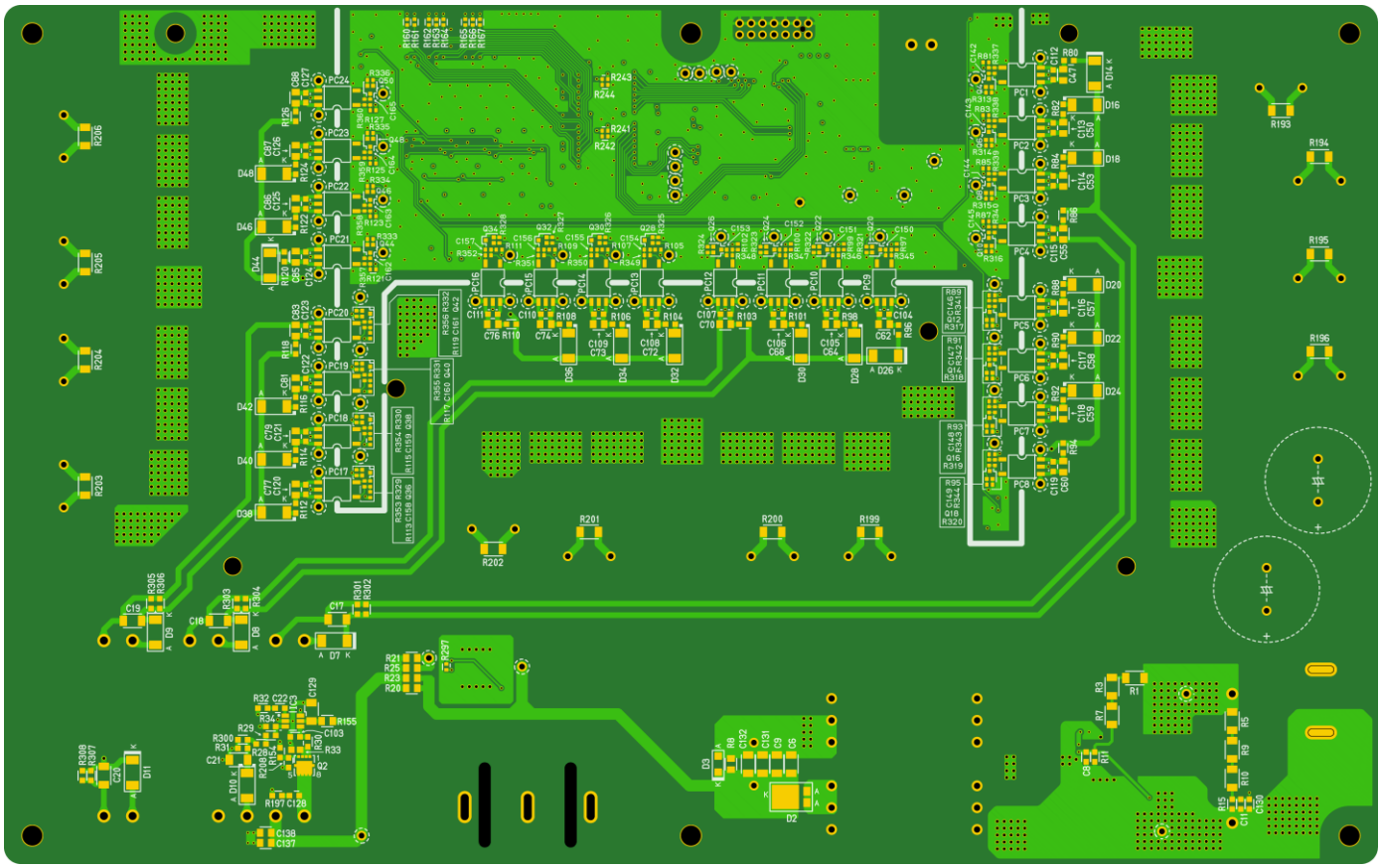


Fig. 2.6 Main Component Layout (Back)

3. Schematic, Bill of Material, and PCB Pattern

3.1. Schematic

Refer to the following file:

RD208-SCHEMATIC-xx.pdf

(xx is the revision number.)

3.2. Bill of Material

Refer to the following file:

RD208-BOM-xx.pdf

(xx is the revision number.)

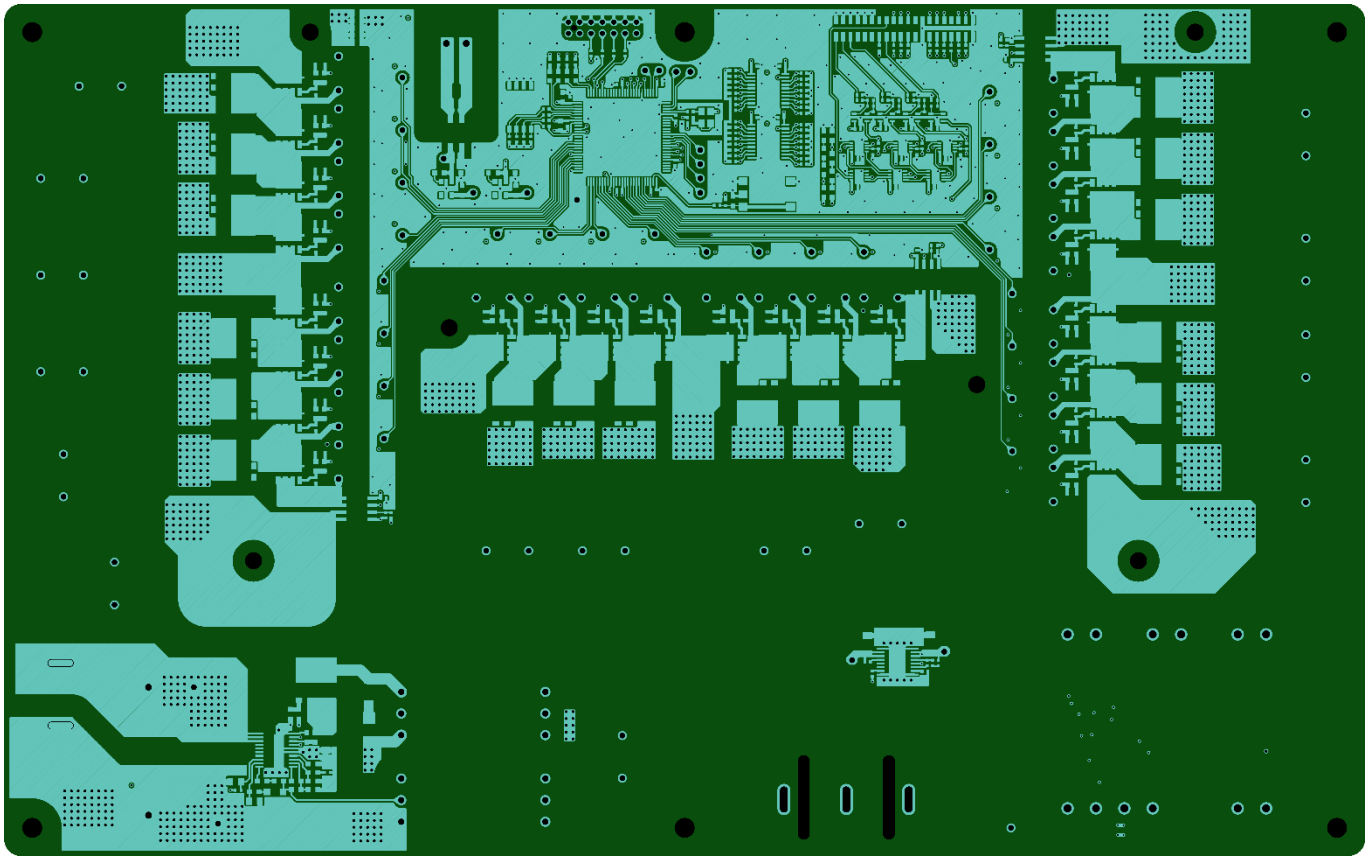
3.3. PCB Pattern

Fig. 3.1 shows the PCB pattern of this inverter.

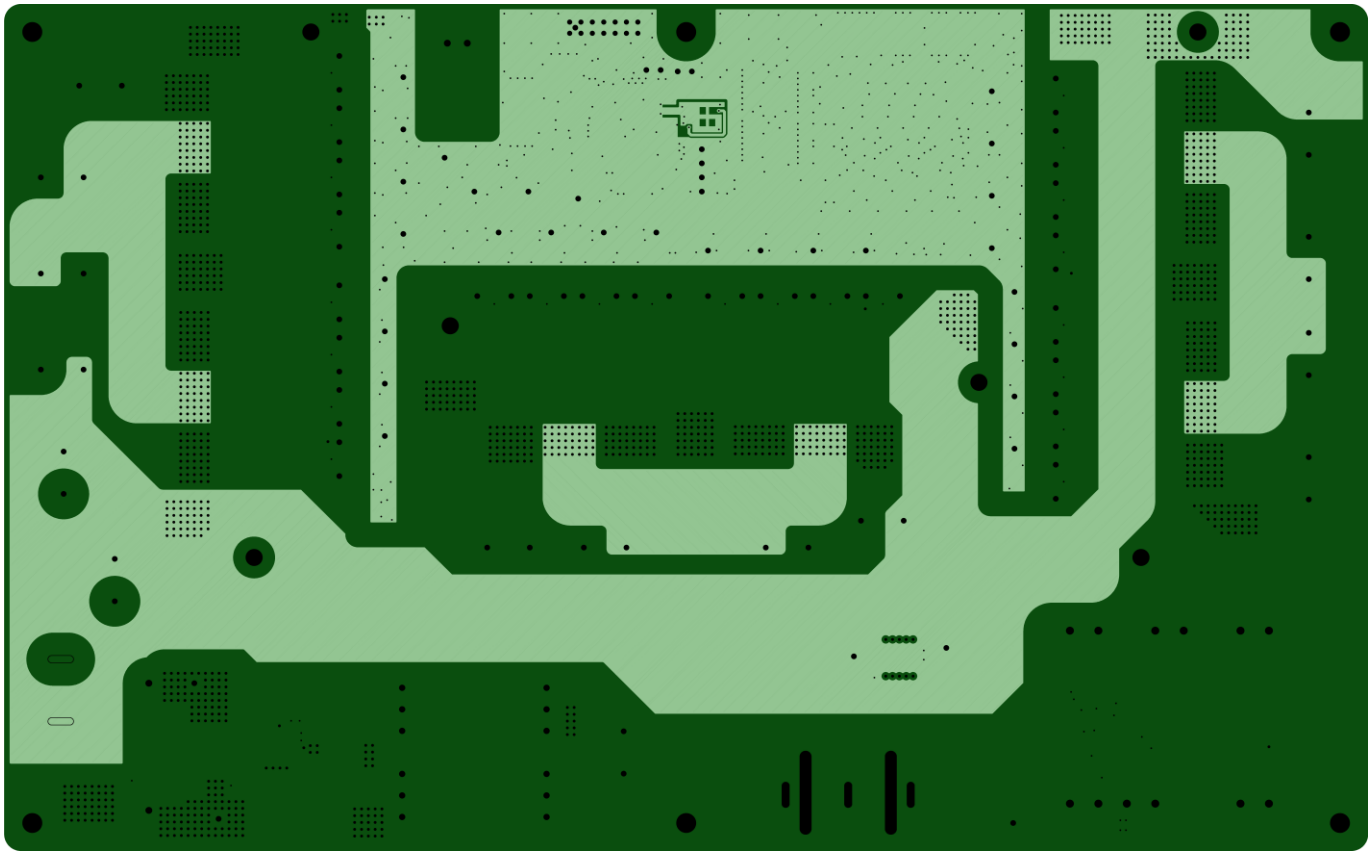
Also refer to the following file:

RD208-LAYER-xx.pdf

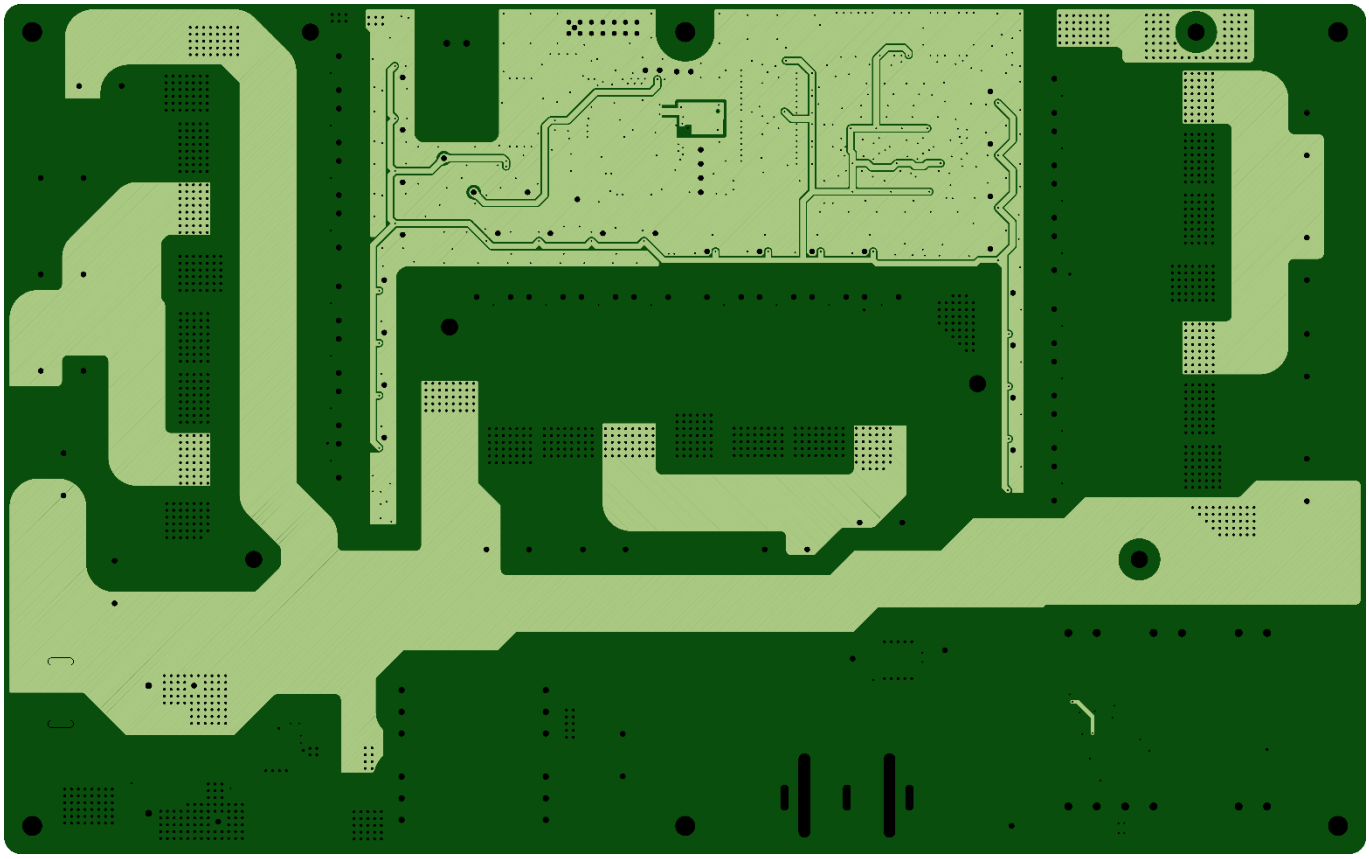
(xx is the revision number.)



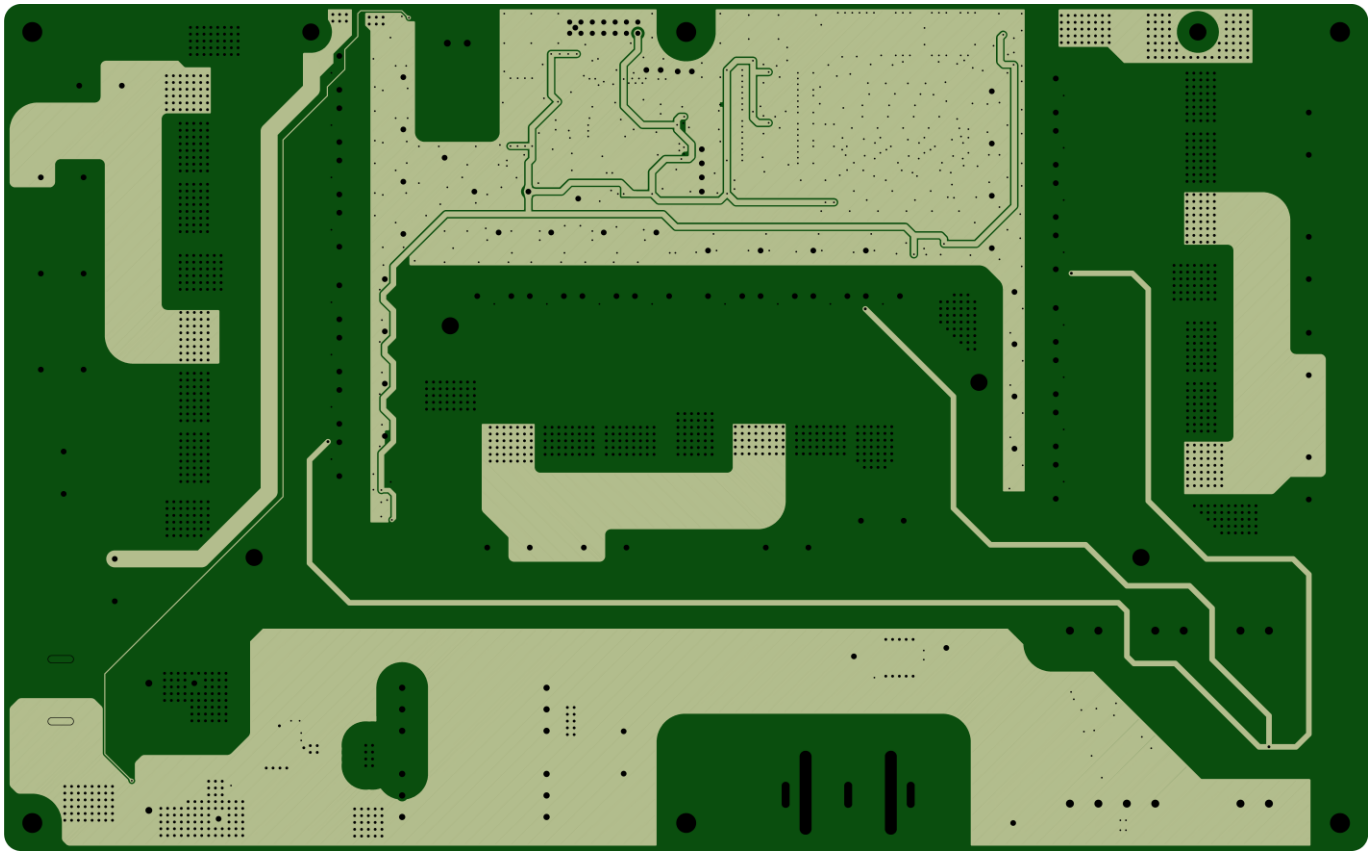
<Layer 1 Front Side>



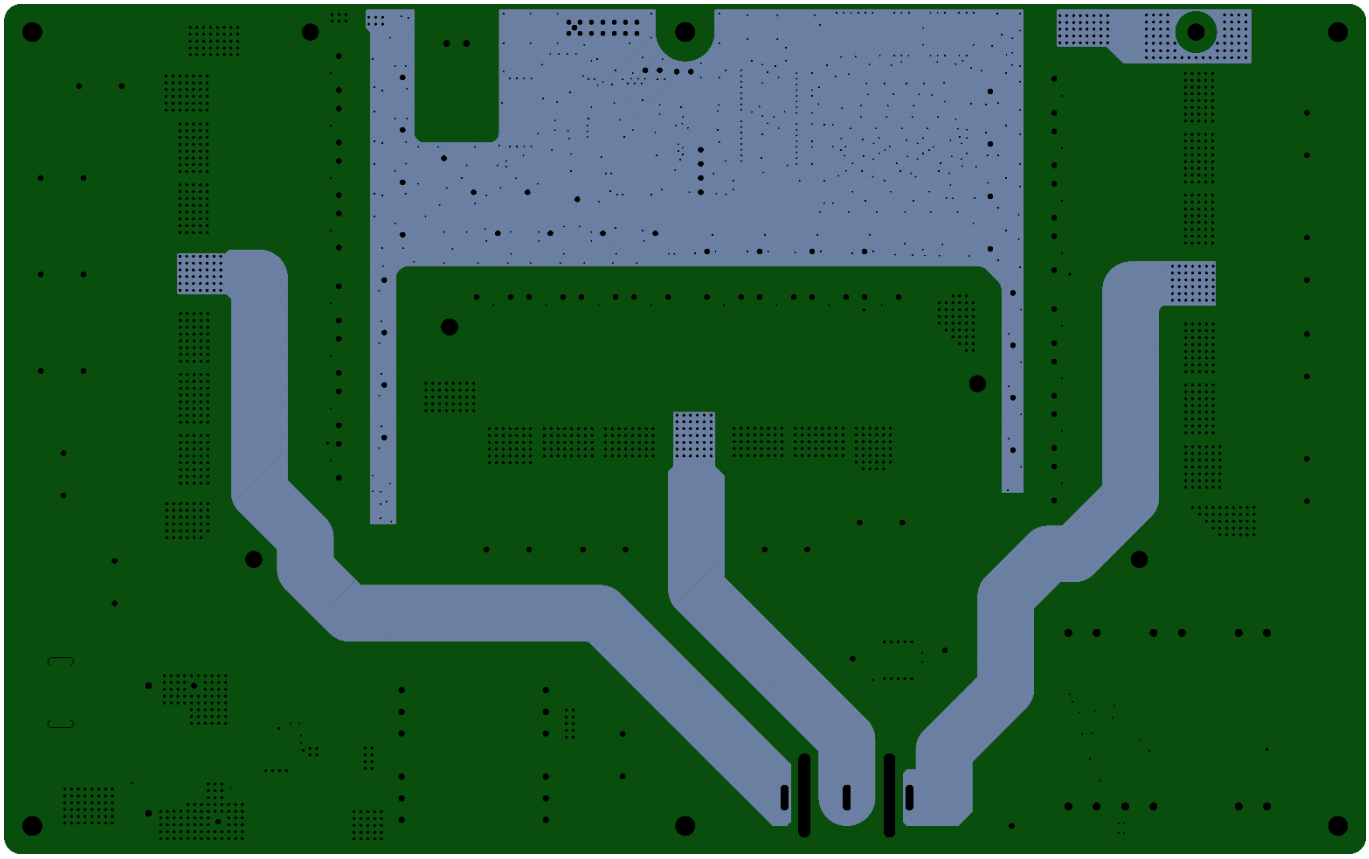
<Layer 2>



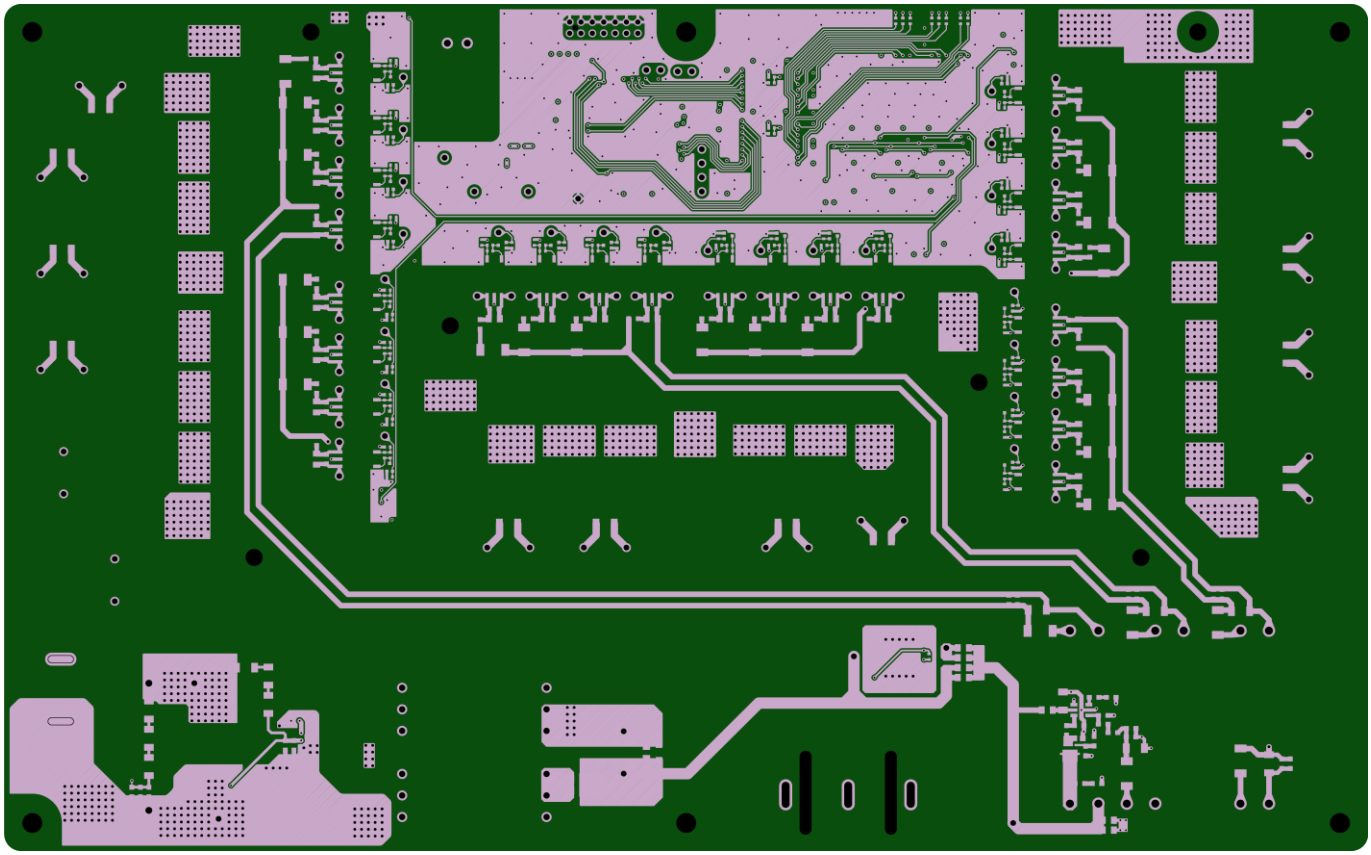
<Layer 3>



<Layer 4>



<Layer 5>



<Layer 6 Back Side>

Fig. 3.1 PCB Pattern (Front View)

4. Operation

4.1. Name and Function of Components

4.1.1. Inverter Input Power Supply Connector (CN1)

This connector is used to input DC power as the inverter power supply. Max. DC 400 V can be input. OTB-640NS-B-2P-C (Osada) connector is used.

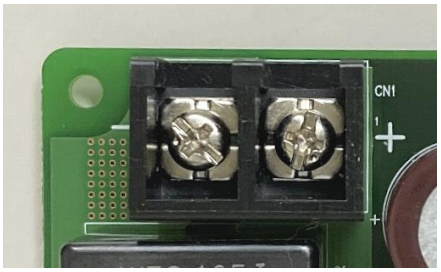


Fig. 4.1 Inverter Input Power Supply Connector (CN1)

Table 4.1 Inverter Input Power Supply Connector Specifications

Pin	Net Name	
1	VP_380R0_INV	DC bus-voltage (+) max. 400 V
2	GND	DC bus-voltage (-)

4.1.2. Control Power Supply Connector (CN2)

This connector is used to input 5 V (max. 100 mA) as the control power supply. MCV1,5/2-G-3.5 (Phoenix Contact) connector is used.

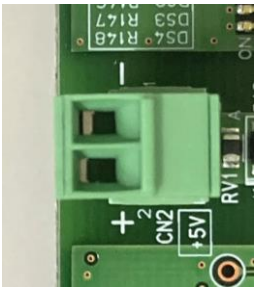


Fig. 4.2 Control Power Supply Connector (CN2)

Table 4.2 Control Power Supply Connector Specifications

Pin	Net Name	
1	5V_RTN	Control power supply (GND)
2	5V_IN	Control power supply (5 V)

4.1.3. Controller Connector (CN3)

This connector is used to connect a controller, such as an external MCU. FTSH-120-04-F-DH-A (Samtec) connector is used. Many of the control signals are connected to CPLD (IC7), and the application can be changed by programming CPLD. Digital input/output signals are connected to CPLD using a bi-directional bus transceiver, enabling 5 V input/output.

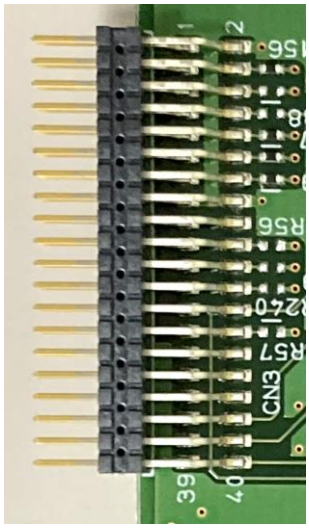


Fig. 4.3 Controller Connector (CN3)

Table 4.3 Controller Connector Specifications

Pin	Net Name	I/O	Application Example	Pin	Net Name	I/O	Application Example
1	GND	-		2	GND	-	
3	MCU_TCK	I	CPLD-JTAG signal (TCK)	4	MCU_TDO	O	CPLD-JTAG signal (TDO)
5	MCU_TDI	I	CPLD-JTAG signal (TDI)	6	MCU_RSV1	-	CPLD control signal (Reserved 1)
7	(n.c.)			8	MCU_RSV2	-	CPLD control signal (Reserved 2)
9	MCU_UH	I	U-phase high-side gate signal	10	MCU_UL	I	U-phase low-side gate signal
11	MCU_VH	I	V-phase high-side gate signal	12	MCU_VL	I	V-phase low-side gate signal
13	MCU_WH	I	W-phase high-side gate signal	14	MCU_WL	I	W-phase low-side gate signal
15	GND	-		16	GND	-	
17	(n.c.)			18	(n.c.)		
19	MCU_TMS	I	CPLD-JTAG signal (TMS)	20	VP_5R0_PRH_D	-	Internal 5 V power supply
21	MCU_MODE	O	CPLD operation mode signal	22	MCU_RSV3	-	CPLD control signal (Reserved 3)
23	MCU_RESET	O	CPLD reset signal	24	MCU_RSV4	-	CPLD control signal (Reserved 4)
25	MCU_EMG	O	Output during error	26	MCU_VDC	O	Bus voltage output
27	(n.c.)			28	VP_5R0_PRH_D	-	Internal 5 V power supply
29	GND	-		30	(n.c.)		
31	GND	-		32	(n.c.)		
33	GND	-		34	(n.c.)		
35	GND	-		36	MCU_IU	O	U-phase current output
37	GND	-		38	MCU_IV	O	V-phase current output
39	GND	-		40	MCU_IW	O	W-phase current output

4.1.4. CPLD Programming Connector (CN4)

This connector is used to program CPLD. 0878311420 (Molex) connector is used.

Fig. 4.4 CPLD Programming Connector (CN4)

4.4 CPLD Programming Connector Specifications

Pin	Net Name	Pin	Net Name	I/O	Use
1	GND	2	VP_3R3_PRH_D	-	Internal 3.3 V power supply
3		4	CN_TMS	I	CPLD-JTAG signal (TMS)
5		6	CN_TCK	I	CPLD-JTAG signal (TCK)
7		8	CN_TDO	O	CPLD-JTAG signal (TDO)
9		10	CN_TDI	I	CPLD-JTAG signal (TDI)
11		12	(n.c.)		
13		14	(n.c.)		

4.1.5. Inverter Output Connector (CN5)

This connector is used as 3-phase AC output of the inverter. Connect to load such as a motor. OTB-640NS-B-3P-C (Osada) connector is used.

Fig. 4.5 Inverter Output Connector (CN5)

Table 4.5 Inverter Output Connector Specifications

Pin	Net Name	
1	OUT_U	U-phase inverter output
2	OUT_V	V-phase inverter output
3	OUT_W	W-phase inverter output

4.2. Checking Operation

4.2.1. Preparation

Connect the controller, such as a MCU board, to the controller connector (CN3). Connect a load such as a 3-phase motor to the inverter output connector (CN5). Connect the control power supply (5 V) to the control power supply connector (CN2). Connect the inverter input power supply to the inverter input power supply connector (CN1). Turn on the control power supply (5 V) (connected to CN2) and then turn on the inverter input power supply (connected to CN1).

4.2.2. Operation Procedure

Based on the gate control signals (MCU_UH, MCU_UL, MCU_VH, MCU_VL, MCU_WH, MCU_WL) from the controller connected to the controller connector (CN3) and CPLD control signals (MCU_RESET, MCU_MODE, MCU_RSV1, MCU_RSV2, MCU_RSV3, MCU_RSV4), the logic programmed in CPLD generates the gate signals. When operating the inverter, the bootstrap capacitor used as the gate driver power supply for each MOSFET in the MOSFET stack arm needs to be charged, and the charge sequencing needs to be implemented in the logical circuit inside CPLD, etc. Refer to the design guide for more details.

4.2.3. Operation when Overcurrent Error is Detected

The MCU_EMG (Emergency) signal at pin 25 of the controller connector (CN3) becomes L-level when following overcurrent error is detected. And when the current returns to normal range, the MCU_EMG signal returns to the H level.

(1) U-phase overcurrent detection:When U-phase leg current exceeds +20 A or falls below -20 A
(2) V-phase overcurrent detection: When V-phase leg current exceeds +20 A or falls below -20 A
(3) W-phase overcurrent detection: When W-phase leg current exceeds +20 A or falls below -20 A

4.3. Precautions for Evaluation (To Prevent Electric Shock, Burn Injury, etc.)

Pay special attention to the following when operating this inverter.

- Make sure that the polarities of all connections are correct before supplying electricity.
- Make sure that the capacitor is sufficiently discharged before touching the BOARD. Since high voltage is applied to the smoothing capacitor, it takes time to fully discharge the capacitor even after the power supply is turned off.
- When checking the operation, cover the BOARD with an acrylic case for safety.
- MOSFET and other conponents generate heat during operation. Be careful not to get burned when handling them.

Terms of Use

This terms of use is made between Toshiba Electronic Devices and Storage Corporation (“We”) and customers who use documents and data that are consulted to design electronics applications on which our semiconductor devices are mounted (“this Reference Design”). Customers shall comply with this terms of use. Please note that it is assumed that customers agree to any and all this terms of use if customers download this Reference Design. We may, at its sole and exclusive discretion, change, alter, modify, add, and/or remove any part of this terms of use at any time without any prior notice. We may terminate this terms of use at any time and for any reason. Upon termination of this terms of use, customers shall destroy this Reference Design. In the event of any breach thereof by customers, customers shall destroy this Reference Design, and furnish us a written confirmation to prove such destruction.

1. Restrictions on usage

1. This Reference Design is provided solely as reference data for designing electronics applications. Customers shall not use this Reference Design for any other purpose, including without limitation, verification of reliability.
2. This Reference Design is for customer's own use and not for sale, lease or other transfer.
3. Customers shall not use this Reference Design for evaluation in high or low temperature, high humidity, or high electromagnetic environments.
4. This Reference Design shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable laws or regulations.

2. Limitations

1. We reserve the right to make changes to this Reference Design without notice.
2. This Reference Design should be treated as a reference only. We are not responsible for any incorrect or incomplete data and information.
3. Semiconductor devices can malfunction or fail. When designing electronics applications by referring to this Reference Design, customers are responsible for complying with safety standards and for providing adequate designs and safeguards for their hardware, software and systems which minimize risk and avoid situations in which a malfunction or failure of semiconductor devices could cause loss of human life, bodily injury or damage to property, including data loss or corruption. Customers must also refer to and comply with the latest versions of all relevant our information, including without limitation, specifications, data sheets and application notes for semiconductor devices, as well as the precautions and conditions set forth in the "Semiconductor Reliability Handbook".
4. When designing electronics applications by referring to this Reference Design, customers must evaluate the whole system adequately. Customers are solely responsible for all aspects of their own product design or applications. WE ASSUME NO LIABILITY FOR CUSTOMERS' PRODUCT DESIGN OR APPLICATIONS.
5. No responsibility is assumed by us for any infringement of patents or any other intellectual property rights of third parties that may result from the use of this Reference Design. No license to any intellectual property right is granted by this terms of use, whether express or implied, by estoppel or otherwise.
6. THIS REFERENCE DESIGN IS PROVIDED "AS IS". WE (a) ASSUME NO LIABILITY WHATSOEVER, INCLUDING WITHOUT LIMITATION, INDIRECT, CONSEQUENTIAL, SPECIAL, OR INCIDENTAL DAMAGES OR LOSS, INCLUDING WITHOUT LIMITATION, LOSS OF PROFITS, LOSS OF OPPORTUNITIES, BUSINESS INTERRUPTION AND LOSS OF DATA, AND (b) DISCLAIM ANY AND ALL EXPRESS OR IMPLIED WARRANTIES AND CONDITIONS RELATED TO THIS REFERENCE DESIGN, INCLUDING WARRANTIES OR CONDITIONS OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, ACCURACY OF INFORMATION, OR NONINFRINGEMENT.

3. Export Control

Customers shall not use or otherwise make available this Reference Design for any military purposes, including without limitation, for the design, development, use, stockpiling or manufacturing of nuclear, chemical, or biological weapons or missile technology products (mass destruction weapons). This Reference Design may be controlled under the applicable export laws and regulations including, without limitation, the Japanese Foreign Exchange and Foreign Trade Law and the U.S. Export Administration Regulations. Export and re-export of this Reference Design are strictly prohibited except in compliance with all applicable export laws and regulations.

4. Governing Laws

This terms of use shall be governed and construed by laws of Japan.