3-Phase Multi-Level Inverter using MOSFET

Design guide

RD208-DGUIDE-01

TOSHIBA ELECTRONIC DEVICES & STORAGE CORPORATION

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1. Introduction

This Design Guide (hereafter referred to as this guide) describes the design of 3-Phase Multi-Level Inverter (hereafter referred to as this inverter) using MOSFET.

3-phase inverters are used to drive induction motors and synchronous motors used in industrial robots, etc. When output is AC 200 V, and a common 2-level inverter configuration is used, then one 600 V MOSFET is used on each of the upper and lower arms. By using a multi-stack MOSFET configuration per arm, the resolution of the voltage output is increased, and precise voltage output control is achieved, thus realizing a highly efficient inverter. This inverter uses four MOSFETs in each of the upper and lower arms, enabling up to five-level PWM voltage output.

150 V power MOSFET TPH9R00CQ5 is used as a switching device. TPH9R00CQ5 features a high-speed built-in diode. It can reduce switching-loss in the inverter operation with inductive loads such as motors. Since four TPH9R00CQ5 are used for each arm, the configuration apparently operates as a MOSFET for withstanding voltage 600 V.

A small, high-speed switching driver coupler TLP152 is used for driving MOSFETs.

2. Components Used

This section introduces the components that are used in this inverter. Toshiba has an extensive lineup of power semiconductors, driver couplers, and LDOs, including those used this time.

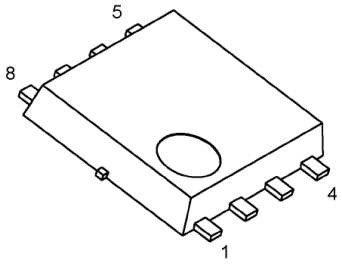
2.1. Power MOSFET TPH9R00CQ5

This inverter uses TPH9R00CQ5 for inverter switching.

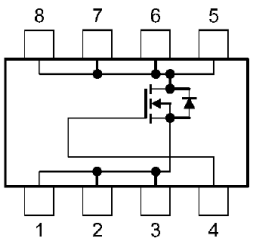
Features

- Fast reverse recovery time: t_{rr} = 40 ns (Typ.)
- Small reverse recovery charge: Q_{rr} = 34 nC (Typ.)
- Small gate charge: Q_{SW} = 11.7 nC (Typ.)
- Low on-resistance: $R_{DS(ON)}$ = 7.3 mΩ (Typ.) (V_{GS} = 10 V)
- Low leakage current: I_{DSS} = 10 μA (Max.) (V_{DS} = 150 V)
- Easy-to-use enhancement type: V_{th} = 3.1 to 4.5 V (V_{DS} = 10 V, I_D = 1.0 mA)

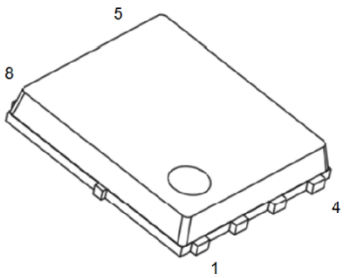
Appearance and Pin Layout



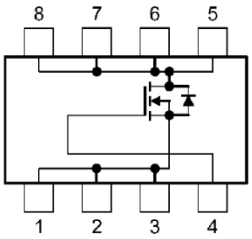
SOP Advance



1, 2, 3: Source
4: Gate
5, 6, 7, 8: Drain



SOP Advance(N)



1, 2, 3: Source
4: Gate
5, 6, 7, 8: Drain

The package can be selected according to your preference.

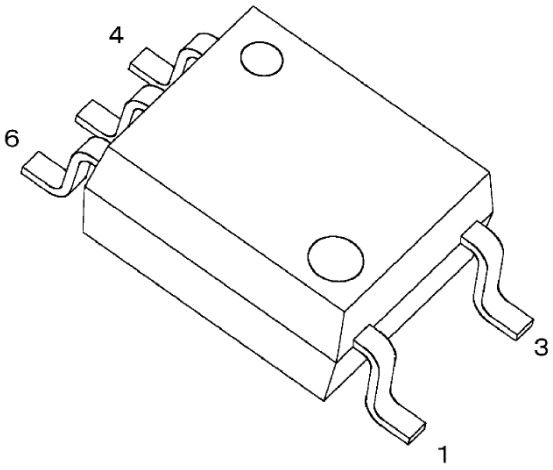
2.2. Gate Driver Coupler TLP152

This inverter uses TLP152 as the gate driver for MOSFET used in the inverter circuit.

Features

- Buffer logic output type (totem pole output)
- Output peak current: ± 2.5 A (Max.)
- Operating temperature range: -40 to 100 ℃
- Supply current: 3.0 mA (Max.)
- Supply voltage: 10 to 30 V
- Threshold input current: 7.5 mA (Max.)
- Propagation delay time: tpHL = 190 ns (Max.), tpLH = 170 ns (Max.)
- Common-mode transient immunity: ± 20 kV/μs (Min.)
- Isolation voltage: 3750 Vrms (Min.)
- Safety standard compliance

Appearance and Pin Layout



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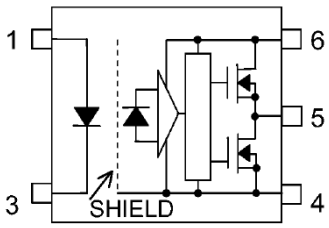


1: Anode
3: Cathode
4: GND
5: V_O
6: V_{CC}

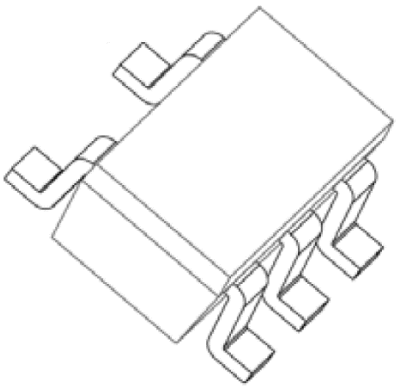
2.3. LDO Power Regulator TCR3UF Series

This inverter uses TCR3UF33A and TCR3UF18A as a stabilized power source for CPLD, etc.

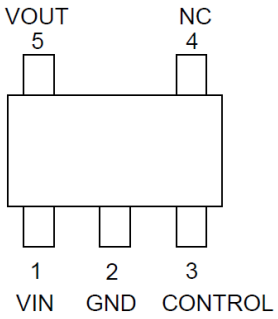
Features

- Low bias current I_B = 0.34 μA (Typ.) @ I_{OUT} = up to 0 mA, power 1.5 V
- High ripple rejection ratio = 70 dB (Typ.) @ 0.8 V output
- Fast load transient response -51/+36 mV @ 0.8 V output, I_{OUT} = 1 mA ⇔ 50 mA
- Low dropout voltage V_{DO} = 206 mV (Typ.) @ 3.3 V out, I_{OUT} = 300 mA
- Wide output voltage lineup (V_{OUT} = 0.8 to 5.0 V)
- High output voltage accuracy ± 1.0 % (1.8 V ≦ V_{OUT})
- Auto-discharge (TCR3UFxxA series) / Non-discharge (TCR3UFxxB series)
- Overcurrent protection
- Thermal shutdown
- Inrush current reduction
- Control pin has pull-down connection
- Ceramic capacitors can be used (C_{IN} = 1 μF, C_{OUT} = 1 μF).
- General purpose package SMV(SOT-25)(SC-74A)

Appearance and Pin Layout



SMV(SOT-25)(SC-74A)



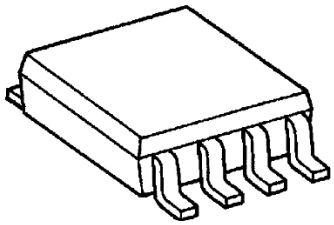
2.4. Comparator TC75W57FK

This inverter uses TC75W57FK as a comparator for overcurrent detection.

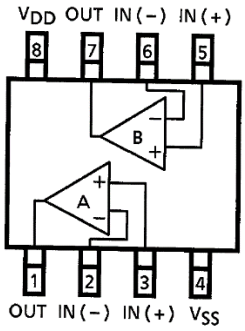
Features

- Low current consumption: I_{DD} = 200 μA (Typ.)
- Single power supply operation
- Wide common mode input voltage range: V_{SS} to V_{DD}-0.9 V
- Push-pull output circuit
- Low input bias current
- Small package

Appearance and Pin Layout



SSOP8-P-0.50A



3. Multi-Level Inverter

3.1. Operation of 2-Level Inverter

An example of a half-bridge circuit that is a component of a typical 2-level inverter is shown in Fig. 3.1. As shown in the diagram, a MOSFET (Q1) is used for the upper arm and a MOSFET (Q2) is used for the lower arm as a switching element. Bus-voltage E is supplied. As shown in Fig. 3.2, two levels of voltage, E (bus voltage) or 0 (GND voltage), are output from the inverter output Vout by turning Q1, Q2 on/off.

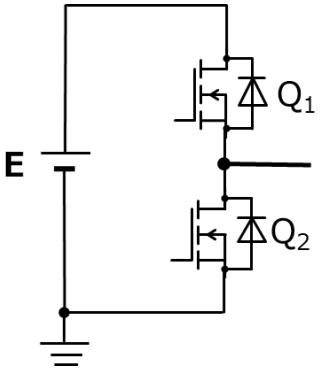


Fig. 3.1 Example of Half-Bridge Circuit

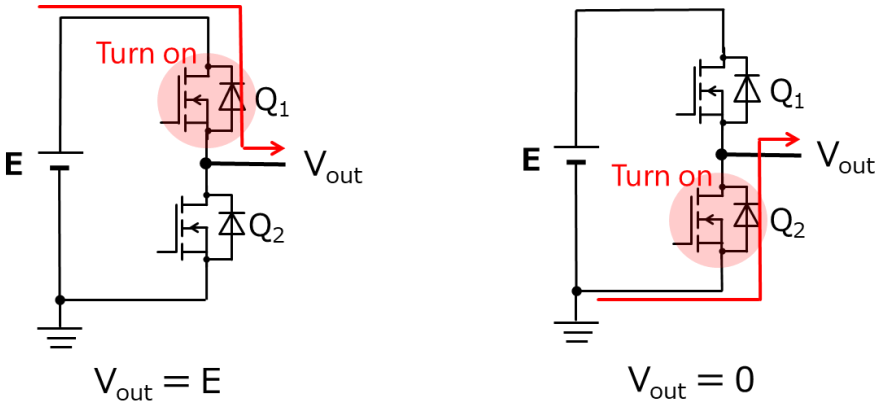


Fig. 3.2 Switching Operation of 2-Level Inverter

Output voltage is controlled by PWM control of these switching devices. Fig. 3.3 shows an example of voltage output as a sine wave.

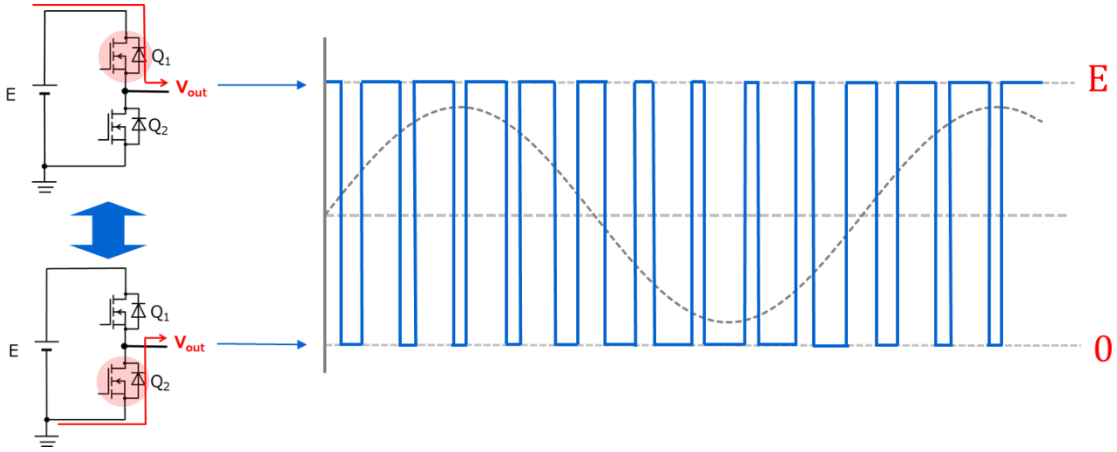


Fig. 3.3 Example of Voltage Output (Sine Wave) using a 2-Level Inverter

Fig. 3.4 shows the configuration of a 3-phase 2-level inverter. A 3-phase 2-level inverter has a 3-phase full-bridge configuration consisting of three half-bridge circuits. By PWM controlled switching of each phase, 3-phase alternating current with a 120° phase difference between each phase is output. Fig. 3.5 shows an example of sine wave phase voltage output of 3-phase 2-level inverter.

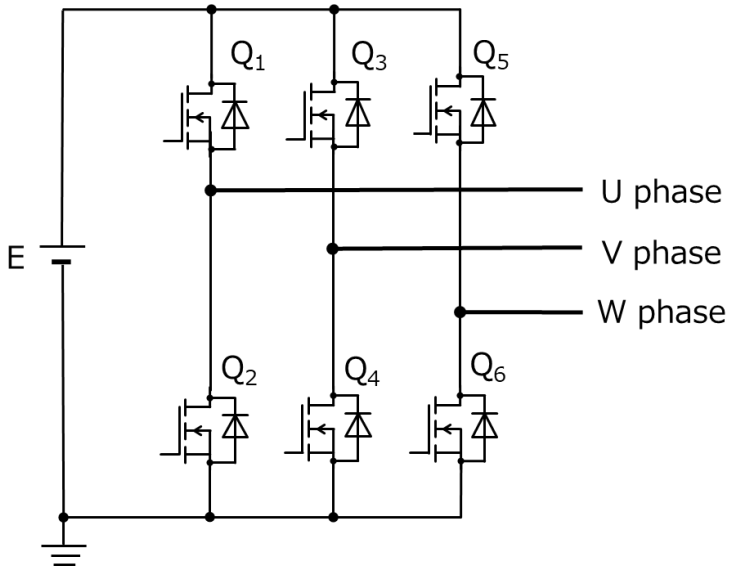


Fig. 3.4 Configuration Example of 3-Phase 2-Level Inverter

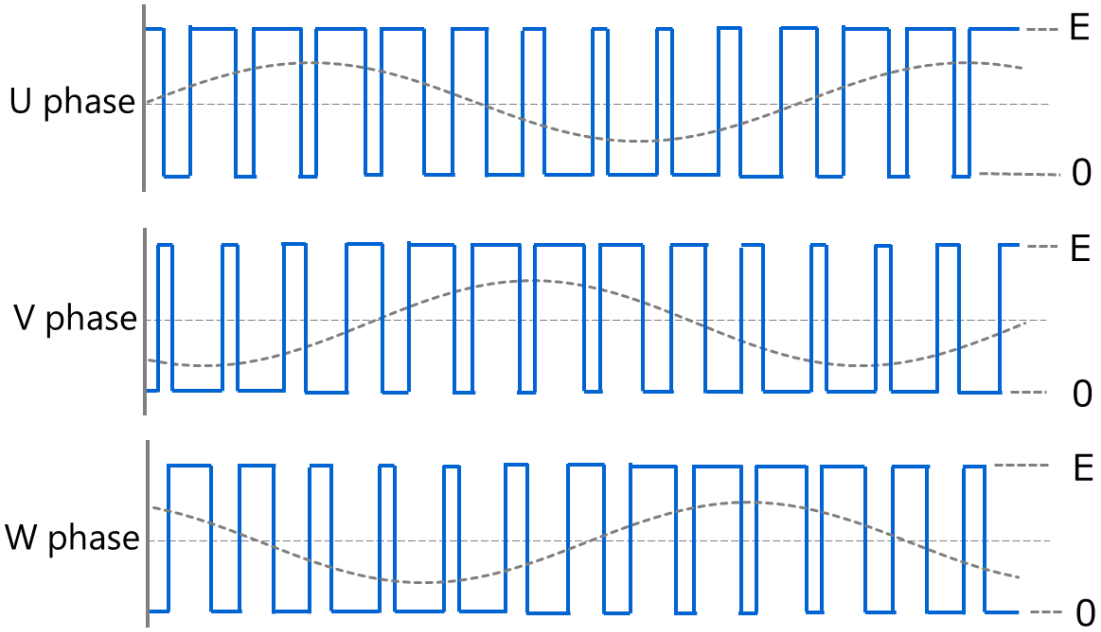


Fig. 3.5 Example of Phase Voltage (Sine Wave) Output of 3-Phase 2-Level Inverter

3.2. Overview of Multi-Level Inverter

In the above mentioned 2-level inverter, one switching element such as a MOSFET is used for each arm, but in the multi-level inverter a configuration with a stack of multiple switching elements is used for each arm. Since the multi-level inverter can increase the resolution of the output voltage by dividing the input voltage, a waveform similar to a sine wave can be output and the efficiency is expected to be better compared to the 2-level inverter. In addition, the output ripple current and harmonics can be reduced without increasing the switching frequency. Furthermore, the appropriate gate control circuit enables the use of low voltage switching elements compared to the 2-level inverter.

Multi-level inverters can be built using various circuit design methods, including NPC (Neutral Point Clamped) method, a T-NPC method, and a flying capacitor method, however this inverter uses NPC method.

3.3. Operation of Multi-Level Inverter

Fig. 3.6 shows the switching operation of the 3-level inverter using two MOSFET for each of the upper and lower arms. The inverter output voltage Vout provides three levels of output: bus voltage E when Q_1 and Q_2 are on, $\frac{1}{2}$E when Q_2 and Q_3 are on, and 0 when Q_3 and Q_4 are on. Q_1 and Q_3, and Q_2 and Q_4 performs complementary operation and therefore are not turned on at the same time. In addition to supplying current to the load from the power supply side during inverter operation, there is a period in which the current returns from the inductive load to the power supply side, therefore, the direction of the current is shown in both directions in Fig. 3.6.

In this way, a 3-level inverter doubles the number of switching elements compared to a 2-level inverter, but the resolution of the output voltage is 1.5 times that of the 2-level inverter, so there is an advantage that the output voltage can be finely controlled. An example of phase voltage output for a 3-level inverter is shown in Fig. 3.7.

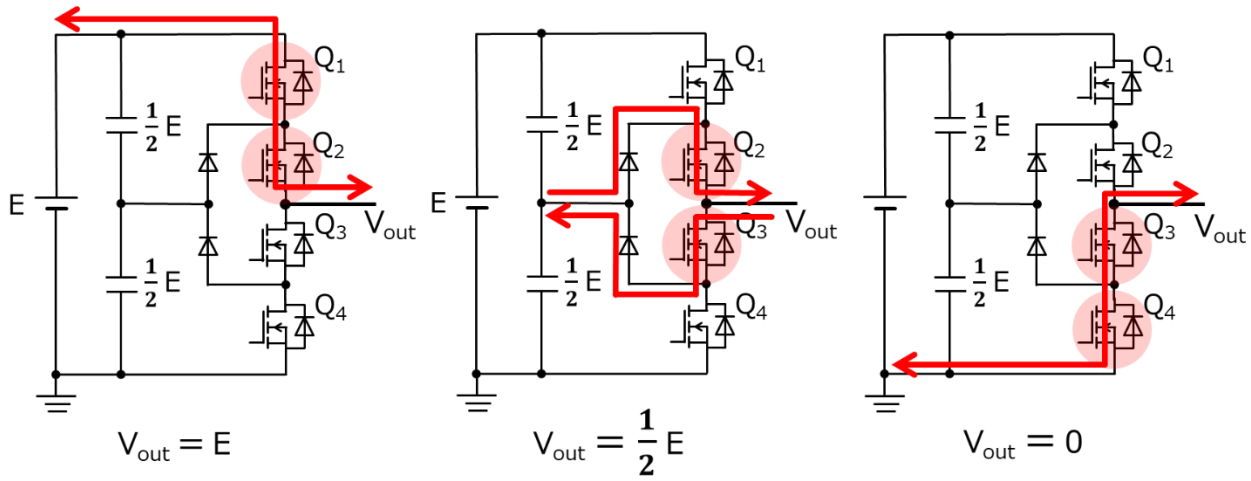


Fig. 3.6 3-Level Inverter Switching Operation

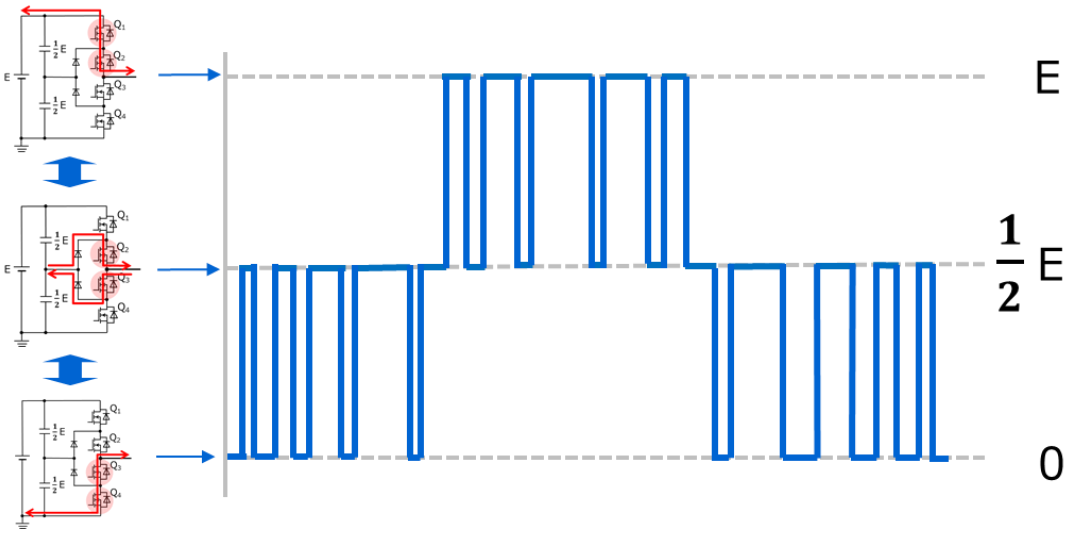


Fig. 3.7 Example of Phase Voltage Output of 3-Level Inverter

Here, the amplitude of the output voltage and the voltage applied to each switching element in both 2-level inverter and the 3-level inverter is considered. If both bus voltages are the same E, the output of the 2-level inverter is E and 0, so the amplitude of the output voltage is E, and the voltage applied to each switching element is E. On the other hand, since the output of the 3-level inverter is E, $\frac{1}{2}$E, and 0, the amplitude of the output voltage in each switching section is $\frac{1}{2}$E, and the voltage applied to each switching element is also $\frac{1}{2}$E. Since the voltage applied to each switching element of 3-level inverter is $\frac{1}{2}$ compared to a 2-level inverter, therefore, a switching element with half withstand voltage can be used. Generally, when the withstand voltage of a switching element such as a MOSFET is high, the loss in the switching application tends to deteriorate due to an increase in the on-resistance per unit area, etc., but with a multi-level inverter, a device with low withstand voltage can be used, thereby reducing the loss in the inverter.

Likewise, Fig. 3.8 shows the switching operation of a 5-level inverter using four MOSFET stack for each of the upper and lower arms. The inverter output voltage Vout has five levels of output: E, $\frac{3}{4}$E, $\frac{1}{2}$E, $\frac{1}{4}$E, and 0 which are produced by switching the MOSFETs. An example of phase voltage output for a 5-level inverter is shown in Fig. 3.9. The 5-level inverter can control the output voltage more precisely than the 3-level inverter. Compared to a 2-level inverter, a 5-level inverter applies $\frac{1}{4}$voltage to each switching element. Therefore, a switching element with $\frac{1}{4}$withstand voltage to the bus voltage can be used.

As shown in Fig. 3.10, this inverter uses a 5-level inverter to realize a 3-phase inverter.

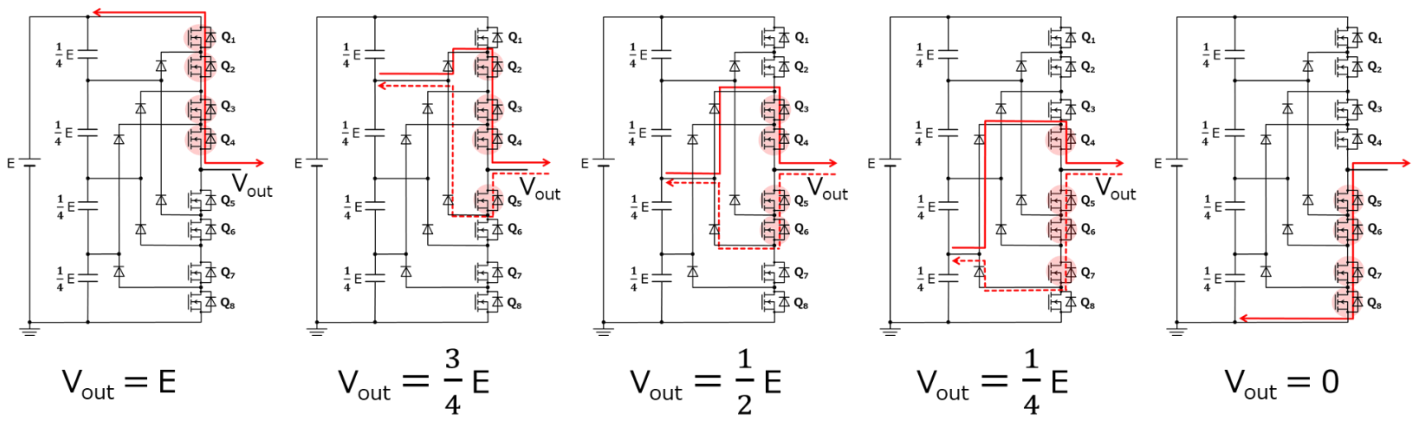


Fig. 3.8 Switching Operation of 5-Level Inverter

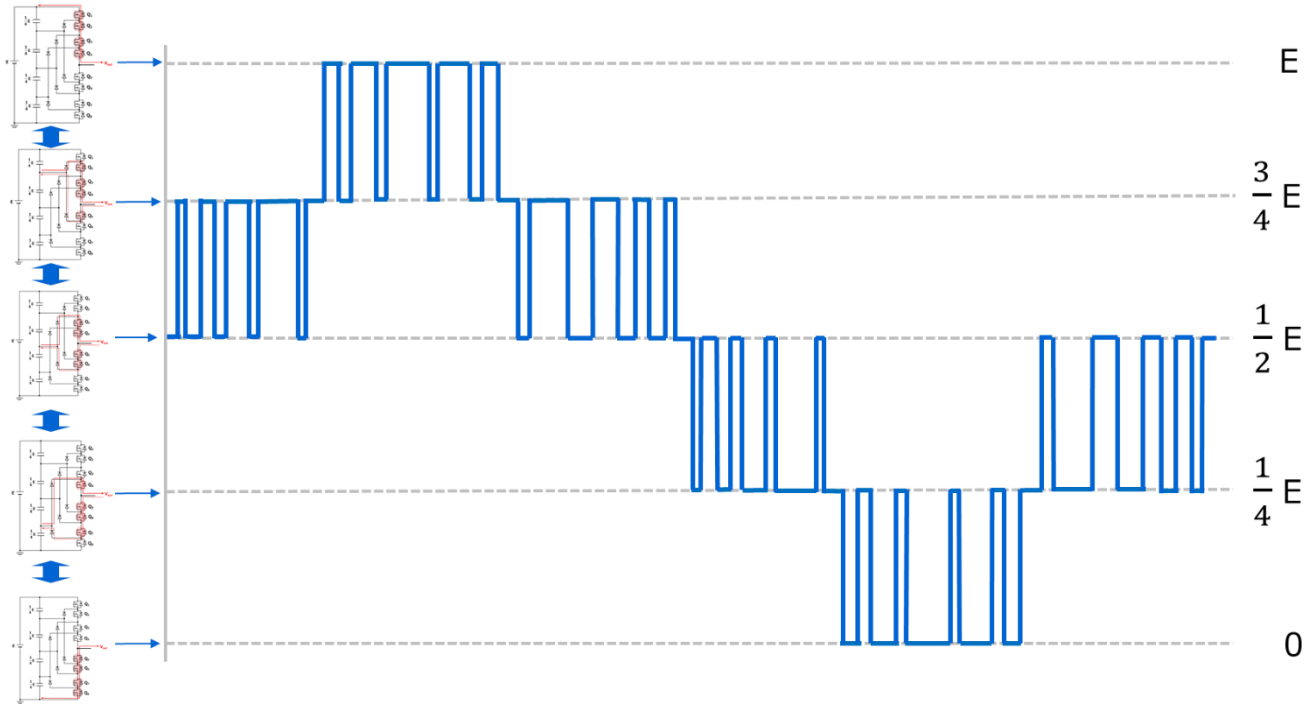


Fig. 3.9 Example of Phase Voltage Output of 5-Level Inverter

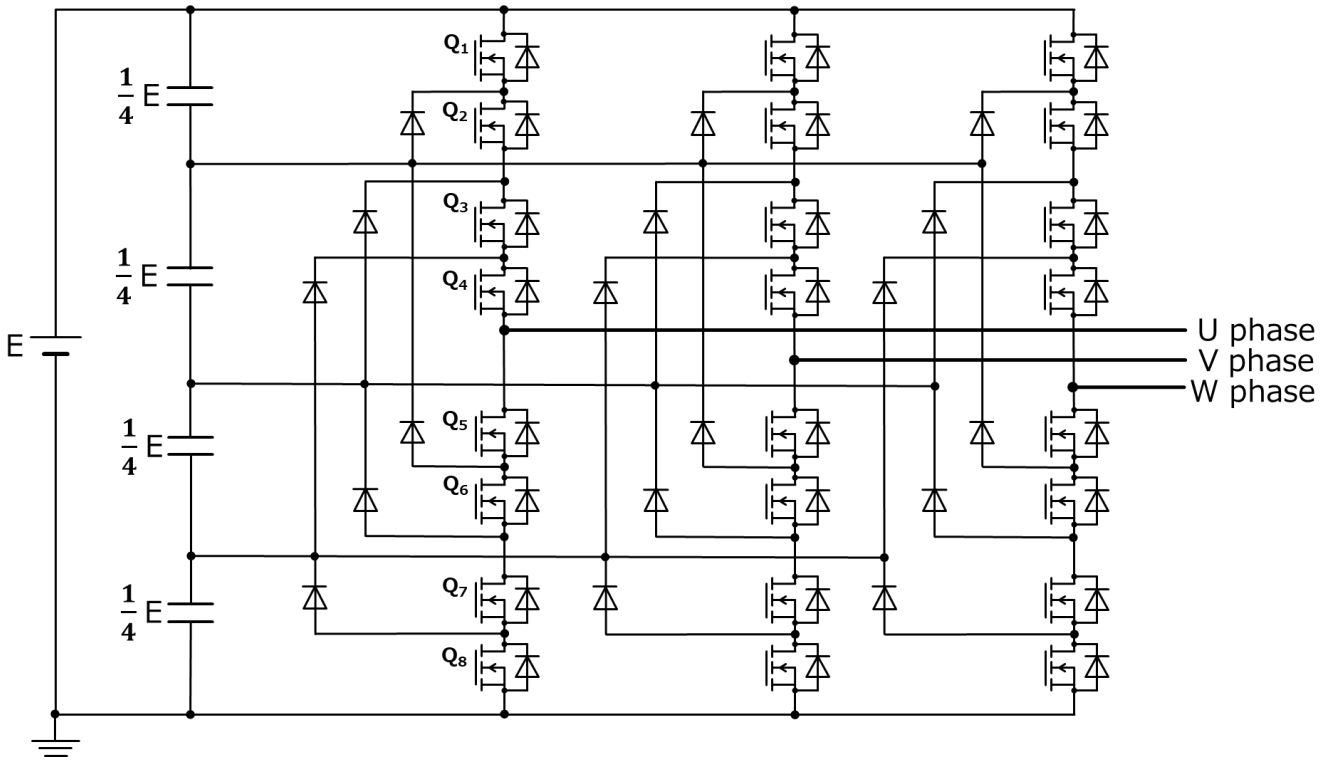


Fig. 3.10 Example of 3-Phase, 5-Level Inverter Configuration

4. Circuit Design

This section describes the gist of the circuit design. Refer to RD208-SCHEMATIC for the schematic and to RD208-BOM for the bill of material. Fig. 4.1 shows the block diagram of this inverter.

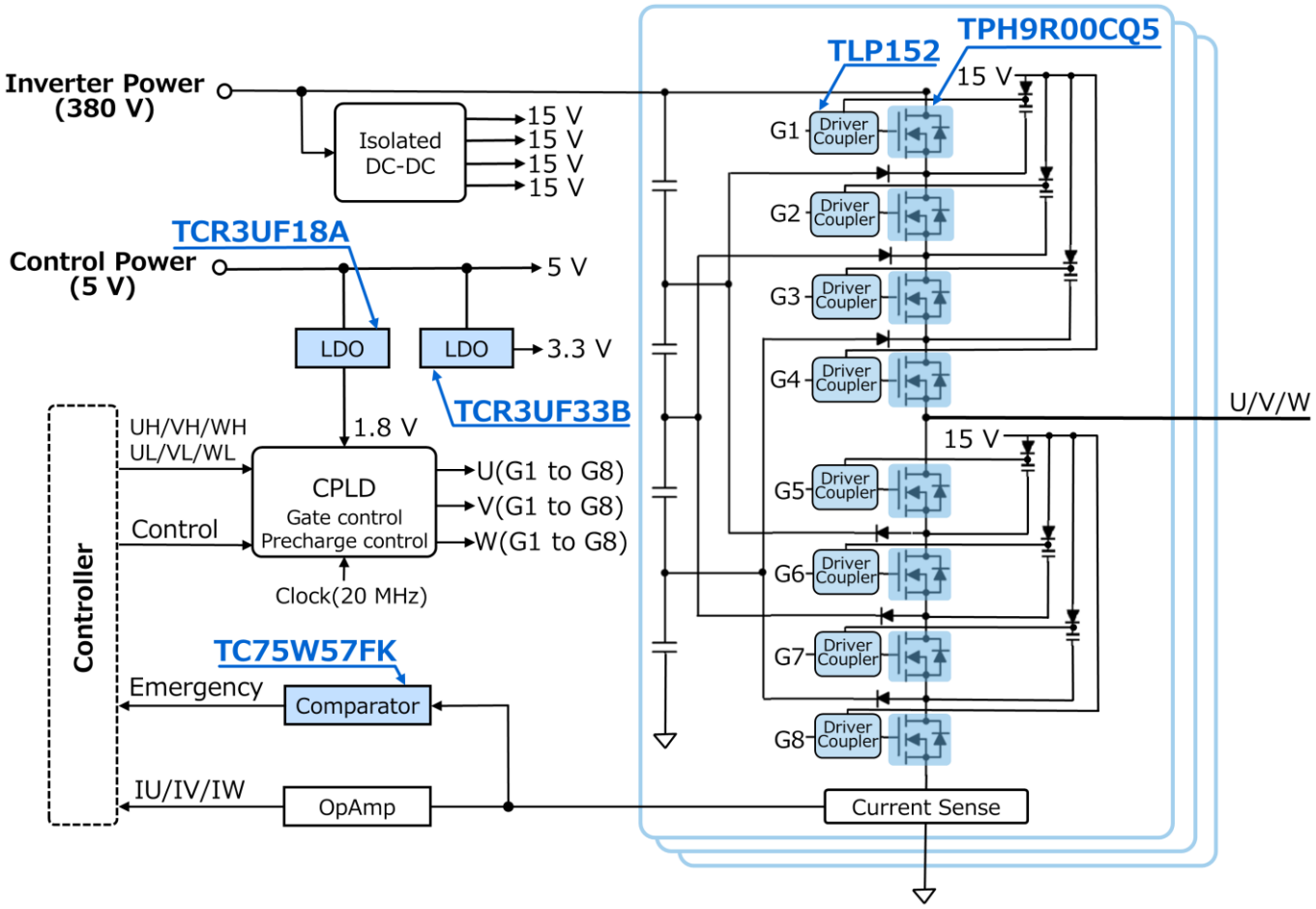


Fig. 4.1 Block Diagram of 3-Phase Multi-Level Inverter using MOSFET

4.1. Isolated Power Supply Circuit

This inverter operates using DC 400 V (Max.) supplied from the inverter power supply connector (CN1) and DC 5 V supplied from the control power supply connector (CN2). The isolated power supply circuit takes DC 400 V input and generates power for the gate-drive circuit. Fig. 4.2 shows the configuration of the isolated power supply circuit.

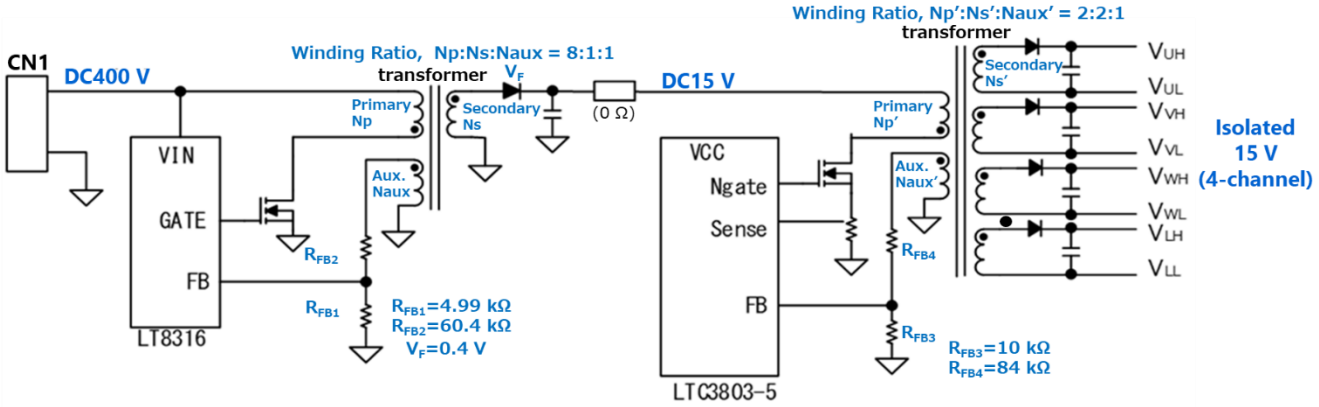


Fig. 4.2 Isolated Power Supply Circuit

4.1.1. DC 400 V In /DC 15 V Out Isolated DC-DC Converter

In Fig. 4.2, the voltage output V_{out1} of the first stage of the isolated power supply (DC 400 V input/DC 15 V output) is determined by the voltage dividing resistors (R_{FB1}, R_{FB2}) connected to the FB pin of the power supply controller IC (LT8316), the winding ratio N_{TS} of the Aux. and Secondary windings of the transformer (N_{TS} = 1 for this circuit because the winding ratio is 1:1), and the voltage drop V_F of the output diode (V_F = 0.4 V for this circuit).

$$V_{out1} = \left(1 + \frac{R_{FB2}}{R_{FB1}}\right) \times \frac{Internal\ \ reference\ \ voltage\ \ 1.22\ \ (V)}{N_{TS}} - V_F$$

And

$$R_{FB1} = 4.99\ \ k\Omega, \quad R_{FB2} = 60.4\ \ k\Omega,$$

Therefore

$$V_{out1} = \left(1 + \frac{60.4 \times 10^3}{4.99 \times 10^3}\right) \times \frac{1.22}{1} - 0.4$$
$$\cong 15.6\ \ (V)$$

4.1.2. DC 15 V In /DC 15 V-4channel Out Isolated DC-DC Converter

In Fig. 4.2, the output voltage V_{out2} of the subsequent stage (DC 15 V input /DC 15 V-4channel output) is determined by the voltage dividing resistors (R_{FB3}, R_{FB4}) connected to FB pin of the power supply controller IC (LTC3803-5) and the winding ratio $N_{TS'}$ of the Aux. and Secondary windings of the transformer ($N_{TS'}$ = 0.5 for this circuit because the winding ratio is 1:2).

$$V_{out2} = \left(1 + \frac{R_{FB4}}{R_{FB3}}\right) \times \frac{Internal\ \ reference\ \ voltage\ \ 0.8\ \ (V)}{N_{TS}}$$

And

$$R_{FB3} = 10\ \ k\Omega, \quad R_{FB2} = 84\ \ k\Omega,$$

Therefore

$$V_{out2} = \left(1 + \frac{84 \times 10^3}{10 \times 10^3}\right) \times \frac{0.8}{0.5} \cong 15.0\ \ (V)$$

4.2. CPLD Power Supply Circuit (3.3 V, 1.8 V)

It generates the power supply for CPLD that performs gate-control by using DC 5 V supplied from the control power supply connector. CPLD used in this inverter has a I/O voltage of 3.3 V and core voltage of 1.8 V. LDO TCR3UF33A (IC4) is used to generate 3.3 V and LDO TCR3UF18A (IC5) is used to generate 1.8 V. Fig. 4.3 shows the power supply for CPLD.

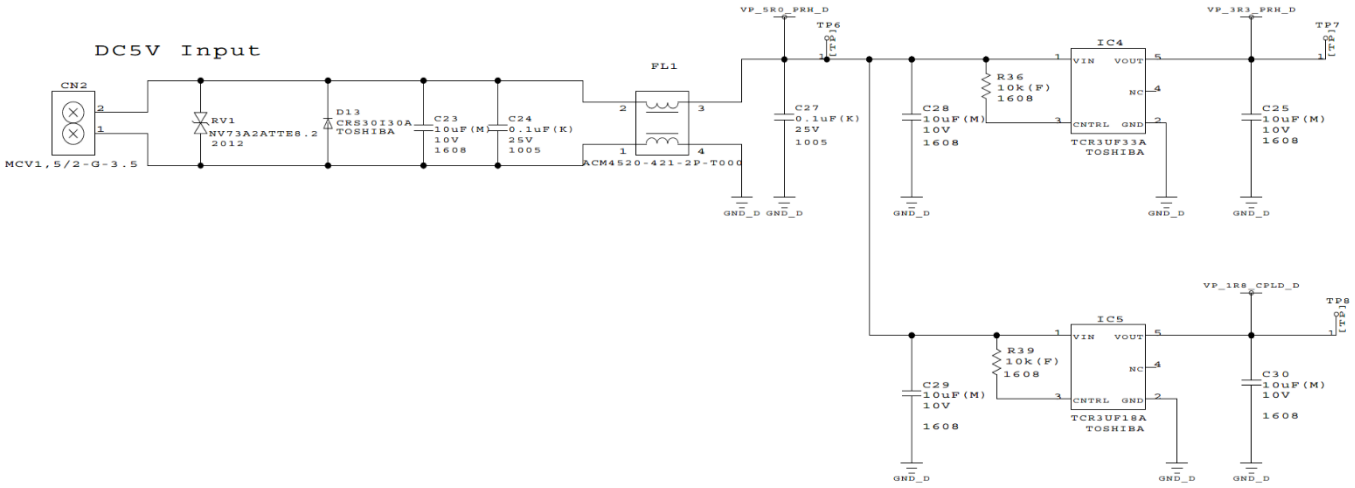


Fig. 4.3 Power supply for CPLD

4.3. Gate Driver Power Supply Circuit

Since the source voltage level of each MOSFET of the inverter arm changes during switching operation, a gate driver power supply is required for each MOSFET in the stack. And, since the base voltage level of upper arms of each phase and all lower arms (same voltage for all phases) is different, thus four separate isolated power supplies are required. Thus, four different channels of 15 V isolated power supply are used for U-phase upper arm, the V-phase upper arm, the W-phase upper arm, and the lower arms of all phases (common for the U/V/W phase). Furthermore, the power supplies of gate drivers for MOSFETs other than the lowest MOSFET in the arm are implemented by a bootstrap circuit consisting of a diode and a capacitor.

To charge (pre-charge) the capacitors for gate driver of each MOSFET in the stack, an external controller or a CPLD installed in the inverter must be used to control the gate signal. This is necessary before starting the inverter operation. Fig. 4.4 shows the charging sequence of the power supply capacitors of the gate drivers using the upper arm as an example. The gate driver of Q_4 can always work since 15 V isolated power supply is always supplied. As shown in Fig. 4.4 (a), Q_3 gate driver power supply capacitor is charged by turning on Q_4 for a period of time to enable Q_3 gate driver. Then, as shown in (b), Q_2 gate driver power supply capacitor is charged by turning on Q_4 and Q_3 for a period of time to enable Q_2 gate driver. Finally, as shown in (c), Q_1 gate driver power supply capacitor is charged by turning on Q_4, Q_3 and Q_2 for a period of time to enable Q_1 gate driver. Other arms also require a similar charging sequence before starting the inverter operation.

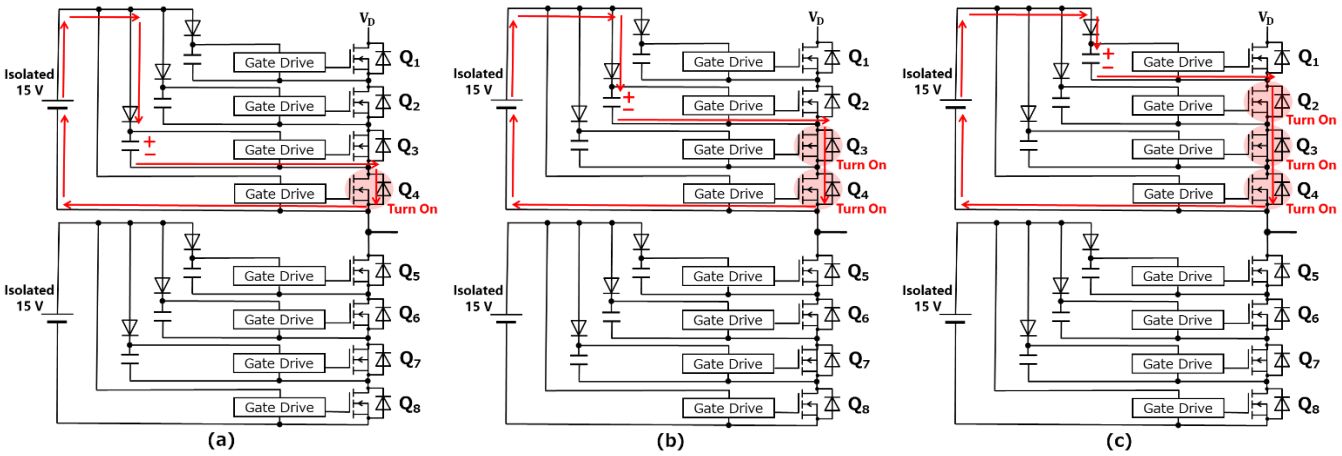


Fig. 4.4 Charging Sequence of Gate Driver Power Supply Capacitors

4.4. Gate Drive Circuit

The driver coupler TLP152 is used as a gate driver of MOSFET. When the gate control signal from CPLD goes to H level, MOSFET (SSM3K15AFU) is turned on and the current flows through the primary-side diode of TLP152. This turns on the high-side circuit of the secondary side of TLP152, which turns on MOSFET (TPH9R00CQ5). On the other hand, when the gate-control signal from CPLD is turned off, the diode on the primary side of TLP152 is turned off. Therefore, MOSFET (TPH9R00CQ5) connected to the secondary side is also turned off. Fig. 4.5 shows the gate-drive operation of MOSFET (TPH9R00CQ5) for inverter switching in this case. By default, the external gate resistance when turning on is 22 Ω and the external gate resistance when turning off is 22 Ω. However, since the optimum value differs depending on the switching frequency, bus voltage, etc., therefore the value of gate resistance must be optimized according to the actual design specifications.

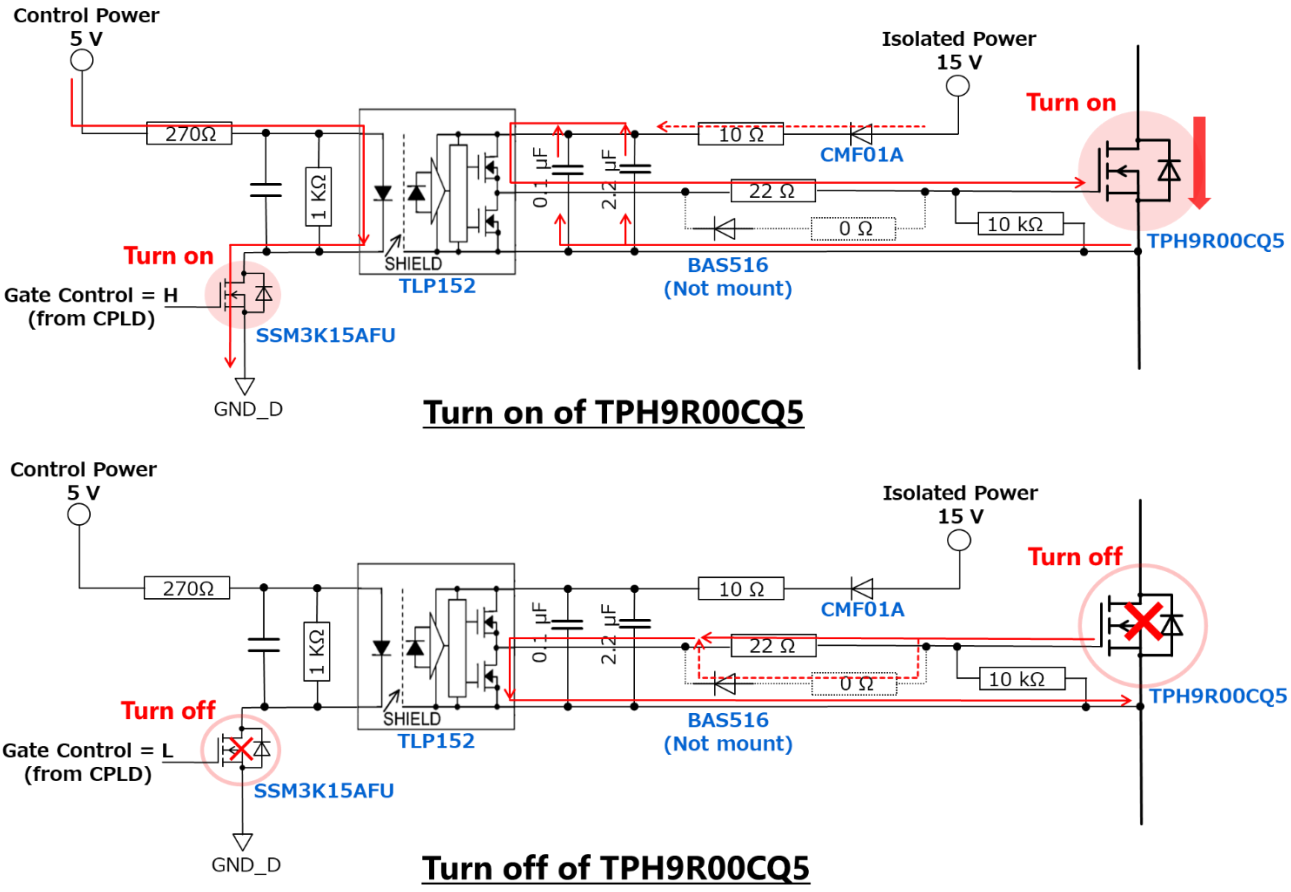


Fig. 4.5 Gate Drive Operation of MOSFET for Inverter Switching

4.5. Current Detector

4.5.1. Current Sensor

Fig. 4.6 shows the configuration of the current sensors. A current sensor is connected to each phase of the inverter circuit, and the current of each phase is converted to voltage output and then is input to the current measurement output circuit and overcurrent detection circuit. The relationship between the input current and the output voltage of current sensor is as follows.

$$V_{ISEN\_OUT} = S \times I_{phase} + V_{REF} \quad \cdots\cdots(1)$$

Here

V_{ISEN_OUT} : Current sensor output voltage [V]

S : Sensitivity = 0.05 [V/A]

I_{phase} : Input current of each phase [A]

V_{REF} : Reference voltage = 1.65 [V]

From the above, output voltage V_{ISEN_OUT} of current sensor, when the current is flowing towards ground the output voltage is more than the reference voltage of 1.65 V, and when the current is coming from the ground then the output voltage is less than the reference voltage of 1.65 V.

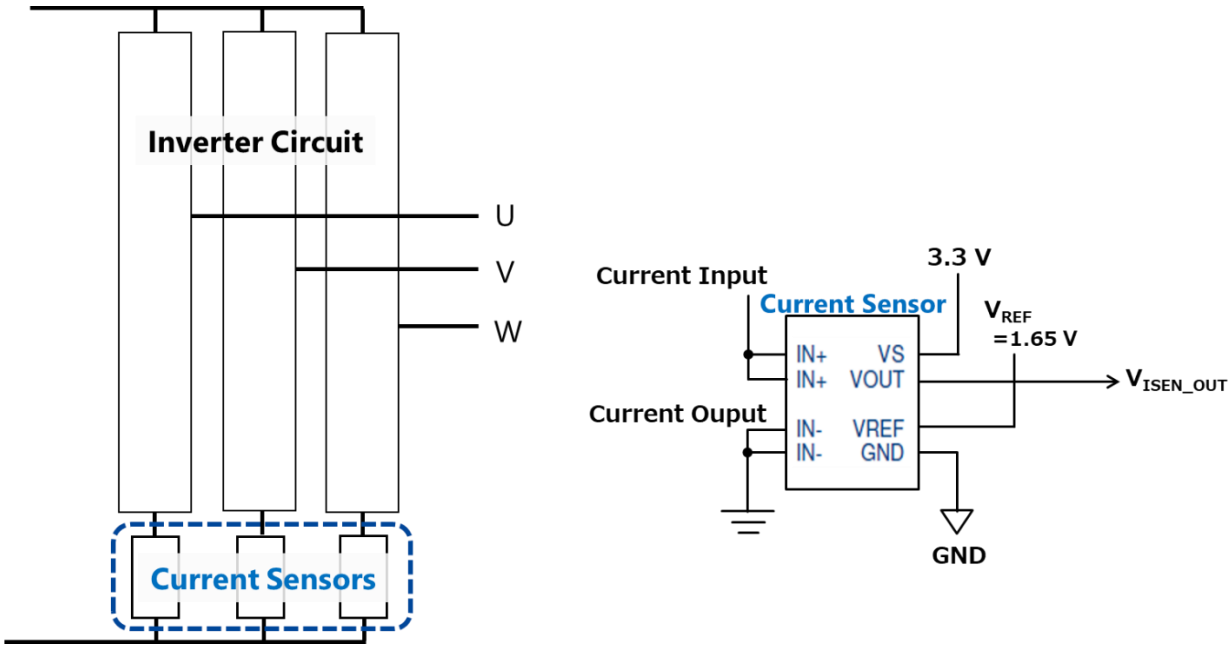


Fig. 4.6 Current Sensor

4.5.2. Current Measurement Output Circuit

Fig. 4.7 shows the current measurement output circuit.

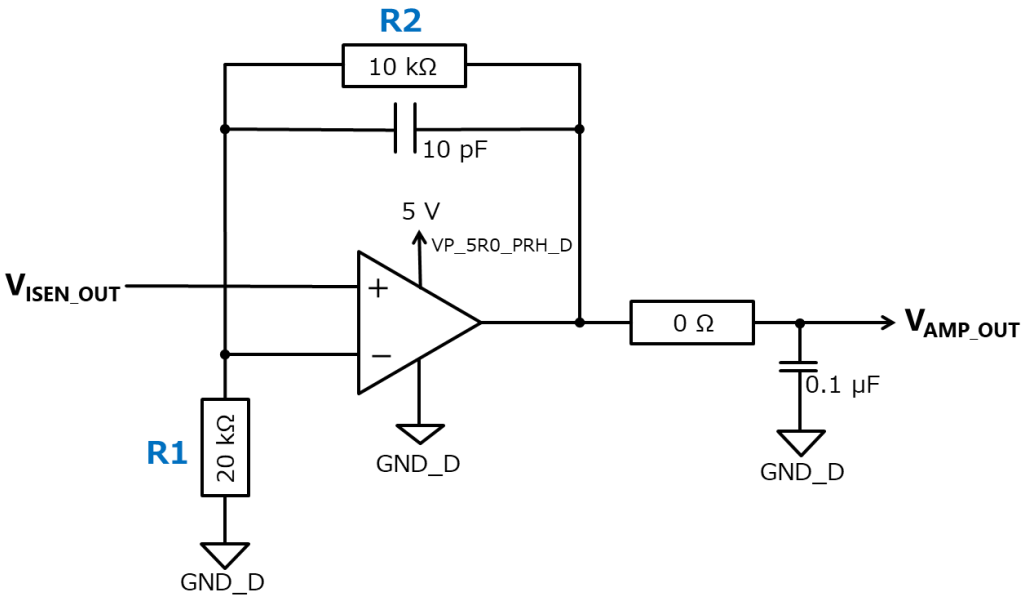


Fig. 4.7 Current Measurement Output Circuit

The output voltage V_{ISEN_OUT} of the current sensor in each phase is amplified by a non-inverting amplifier using an operational amplifier and is output to the controller connector. The output voltage V_{AMP_OUT} to the controller connector is expressed by the following equation. When the resistance R1 = 20 kΩ and R2 = 10 kΩ as shown in Fig. 4.7, output V_{AMP_OUT} is as shown below.

$$
\begin{aligned}
V_{AMP\_OUT} &= \frac{R1 + R2}{R1} \times V_{ISEN\_OUT} \\
&= \frac{20 \times 10^3 + 10 \times 10^3}{20 \times 10^3} \times V_{ISEN\_OUT} \\
&= 1.5 \times V_{ISEN\_OUT} \\
&= 0.075 \times I_{phase} + 2.475
\end{aligned}
$$

4.5.3. Overcurrent Detection Circuit

Fig. 4.8 shows the overcurrent detection circuit.

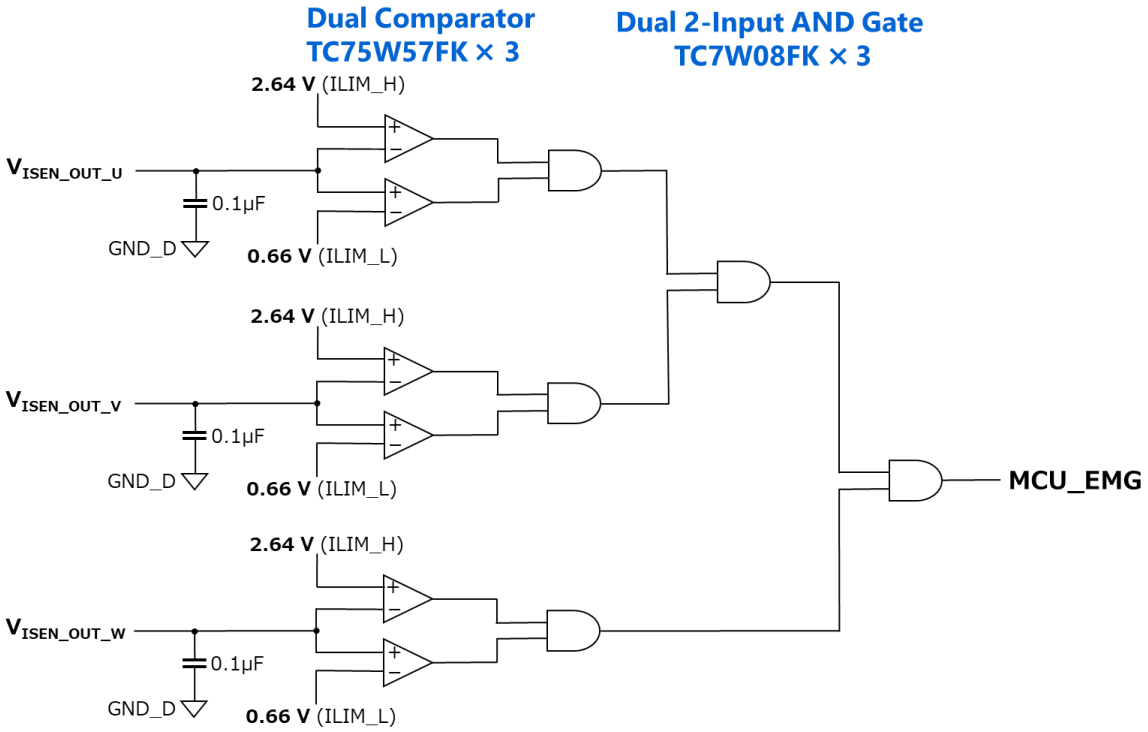


Fig. 4.8 Overcurrent Detection Circuit

V_{ISEN_OUT} input from each phase is compared by the comparator. The comparator inputs are connected with ILIM_H (2.64 V) or ILIM_L (0.66 V) as reference voltages. According to the above equation (1) these voltages are equivalent to I_{phase} = 20 A when V_{ISEN_OUT} = 2.64 V and I_{phase} = -20 A when V_{ISEN_OUT} = 0.66 V. When ILIM_H is the + input of the comparator, and V_{ISEN_OUT} is the -input of the comparator, and if V_{ISEN_OUT} > 2.64 V (that is, I_{phase} > 20 A), then the comparator output is L level. Also, if V_{ISEN_OUT} is the + input of the comparator, and ILIM_L is the -input of the comparator, and if V_{ISEN_OUT} < 0.66 V (that is, I_{phase} <-20 A), then the comparator output is L level. This comparison is done with each phase sensor output $V_{ISEN\_OUT\_U}$, $V_{ISEN\_OUT\_V}$, $V_{ISEN\_OUT\_W}$. The overcurrent detection signal MCU_EMG has a negative logic output that becomes L level output when overcurrent is detected. When any of the six comparators' outputs are L level, then the output of the final AND gate (= MCU_EMG signal) becomes L, indicating that overcurrent error has occurred.

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