32-bit RISC Microcontroller

TXZ+ Family

Reference Manual

Flash Memory

(Code Flash: 1.0MB/512KB/256KB/128KB)
(Data Flash: 32KB)

(FLASH10MUD32-A)

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TOSHIBA ELECTRONIC DEVICES & STORAGE CORPORATION

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Conventions

- Numeric formats follow the rules as shown below:
  Hexadecimal: 0xABC
  Decimal: 123 or 0d123 - Only when it needs to be explicitly shown that they are decimal numbers.
  Binary: 0b111 - It is possible to omit the "0b" when the number of bit can be distinctly understood from a sentence.
- "_N" is added to the end of signal names to indicate low active signals.
- It is called "assert" that a signal moves to its active level, "deassert" to its inactive level.
- When two or more signal names are referred, they are described like as [m: n].
  Example: S[3: 0] shows four signal names S3, S2, S1 and S0 together.
- The characters surrounded by ***[ ]*** defines the register.
  Example: ***[ABCD]***
- "n" substitutes suffix number of two or more same kind of registers, fields, and bit names.
  Example: ***[XYZ1], [XYZ2], [XYZ3] → [XYZn]***
- "x" substitutes suffix number or character of units and channels in the Register List.

  In case of unit, "x" means A, B, and C . . .
  Example: ***[ADACR0], [ADBCR0], [ADCCR0] → [ADxCR0]***
  In case of channel, "x" means 0, 1, and 2 . . .
  Example: [***T32A0RUNA], [T32A1RUNA], [T32A2RUNA] → [T32AxRUNA]***
- The bit range of a register is written like as [m: n].
  Example: Bit[3: 0] expresses the range of bit 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.
  Example: ***[ABCD]***<EFG> = 0x01 (hexadecimal), ***[XYZn]***<VW> = 1 (binary)
- Word and Byte represent the following bit length.
  Byte: 8 bits
  Half word: 16 bits
  Word: 32 bits
  Double word: 64 bits
- Properties of each bit in a register are expressed as follows:
  R: Read only
  W: Write only
  R/W: Read and Write are possible
- Unless otherwise specified, register access supports only word access.
- The register defined as reserved must not be rewritten. Moreover, do not use the read value.
- The value read from the bit having default value of "-" is unknown.
- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value, In the cases that default is "-", follow the definition of each register.
- Reserved bits of the Write-only register should be written with their default value. In the cases that default is "-", follow the definition of each register.
- Do not use read-modified-write processing to the register of a definition which is different by writing and read out.

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Terms and Abbreviation

Some of abbreviations used in this document are as follows:

ACK	Acknowledgement
Addr	Address
Adr	Address
BLK	Block
KB	Kilo Bytes
PG	Page
POR	Power On Reset
SFR	Special Function Register
UART	Universal Asynchronous Receiver Transmitter

1. Outline

The code flash which stores a program code, and the data flash which stores data are explained.
A code flash stores an instruction code, and CPU reads and executes it.

There is user information area which can be accessed in a code flash by bank change. Since user information area is not erased by a chip erasing command, for example, a unique management number etc. can be written to it

A data flash stores data, and even if power supply is intercepted, it keeps data.

Table 1.1 Functional description (code flash)

Flash memory	Function classification	Function	Functional Description	Comments
Code Flash 1.0MB 512KB 256KB 128KB	Programming and Erasing	Automatic Programming	Data programming is performed at 4 words (16 bytes).	
		Automatic chip erasing	Erasing all area of a flash memory is performed automatically. Object: Code flash Data flash	Except User information area in code flash.
		Automatic area erasing	Erasing in an area unit is performed automatically.	
		Automatic block erasing	Erasing in a block unit is performed automatically.	
		Automatic page erasing	Erasing in a page unit is performed automatically.	
	Program/erase protection	Protection	Programming and erasing can be prohibited per block.(Note)	
	Security	Security	Prohibition of read-out from the flash memory by a flash writer and of using a debugging tools.	
	Memory swap	Automatic memory swap	Swap /swap release /swap size specification of a code flash block is performed automatically.	
	Execute Instruction	Execute Instruction	Instructions can be executed.	
	Program/erase to other area	Program/erase to other area of code/data flash	Basic operation to a code/data flash can be performed.	Dual mode
	Read Control	Access time	The access time of flash memory can be changed to optimize the user conditions (system clock).	
		Read Buffer	Access on a minimum of one clock is possible.	

Note: First 32KB is protected by page unit.

Table 1.2 Functional description (user information area)

Flash memory	Function classification	Function	Functional Description	Comments
User information area (Code Flash) 4KB	Programming and Erasing	Automatic Programming	Data programming is performed at 4 words (16 bytes).	
		Automatic page erasing	Erasing all the User information area is performed automatically.	
	Security	Security	Prohibition of read-out of the flash memory by a flash writer and the usage restrictions of a debugging function can be carried out.	It is controlled by the operation on the code flash side.
	Execute Instruction	-	-	Execution of instruction cannot be performed.

Table 1.3 Functional description (data flash)

Flash memory	Function classification	Function	Functional Description	Comments
Data Flash 32KB	Programming and Erasing	Automatic Programming	Data programming is performed at 1 word (4 bytes).	
		Automatic area erasing	Erasing in an area unit is performed automatically.	
		Automatic block erasing	Erasing in a block unit is performed automatically.	
		Automatic page erasing	Erasing in a page unit is performed automatically.	
	Program/erase protection	Protection	Programming and erasing can be prohibited per block.	
	Security	Security	Prohibition of read-out of the flash memory by a flash writer and the usage restrictions of a debugging function can be carried out.	It becomes effective simultaneously by the operation on the code flash side.
	Execute Instruction	Execute Instruction	Instructions can be executed.	No read buffer
	program/erase to other Flash area	program/erase to code Flash area	Basic operation to a code flash can be performed.	Dual mode

1.1. Memory map

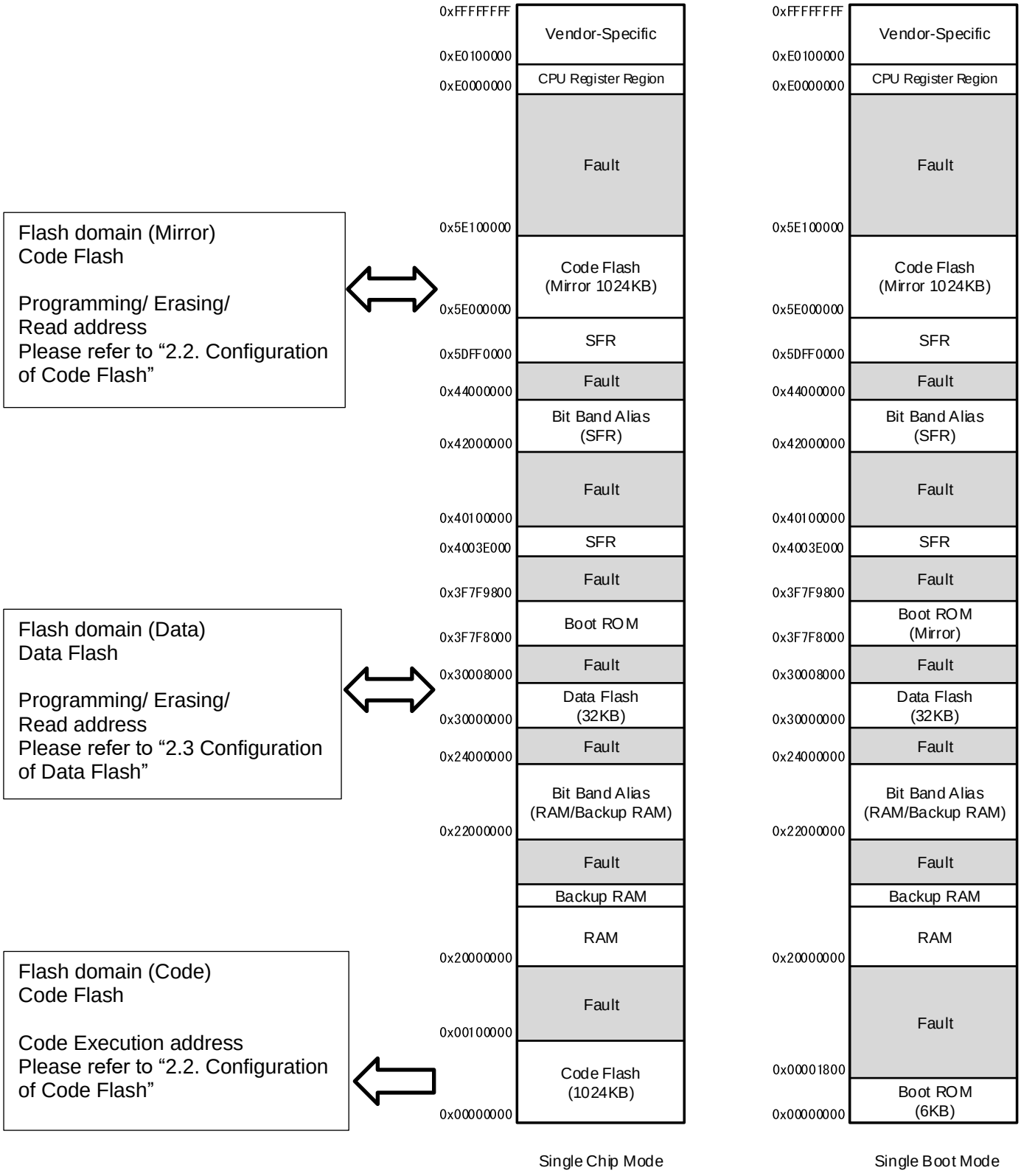

Figure 1.1 The example of a memory map (1024KB)

Note: For details on the built-in flash memory for each product, refer to the chapter “Memory Map” in the reference manual “Clock Control and Operation Modes”.

2. Configuration

2.1. Block Diagrams

The Block Diagrams of a Flash memory and a signal list are shown.

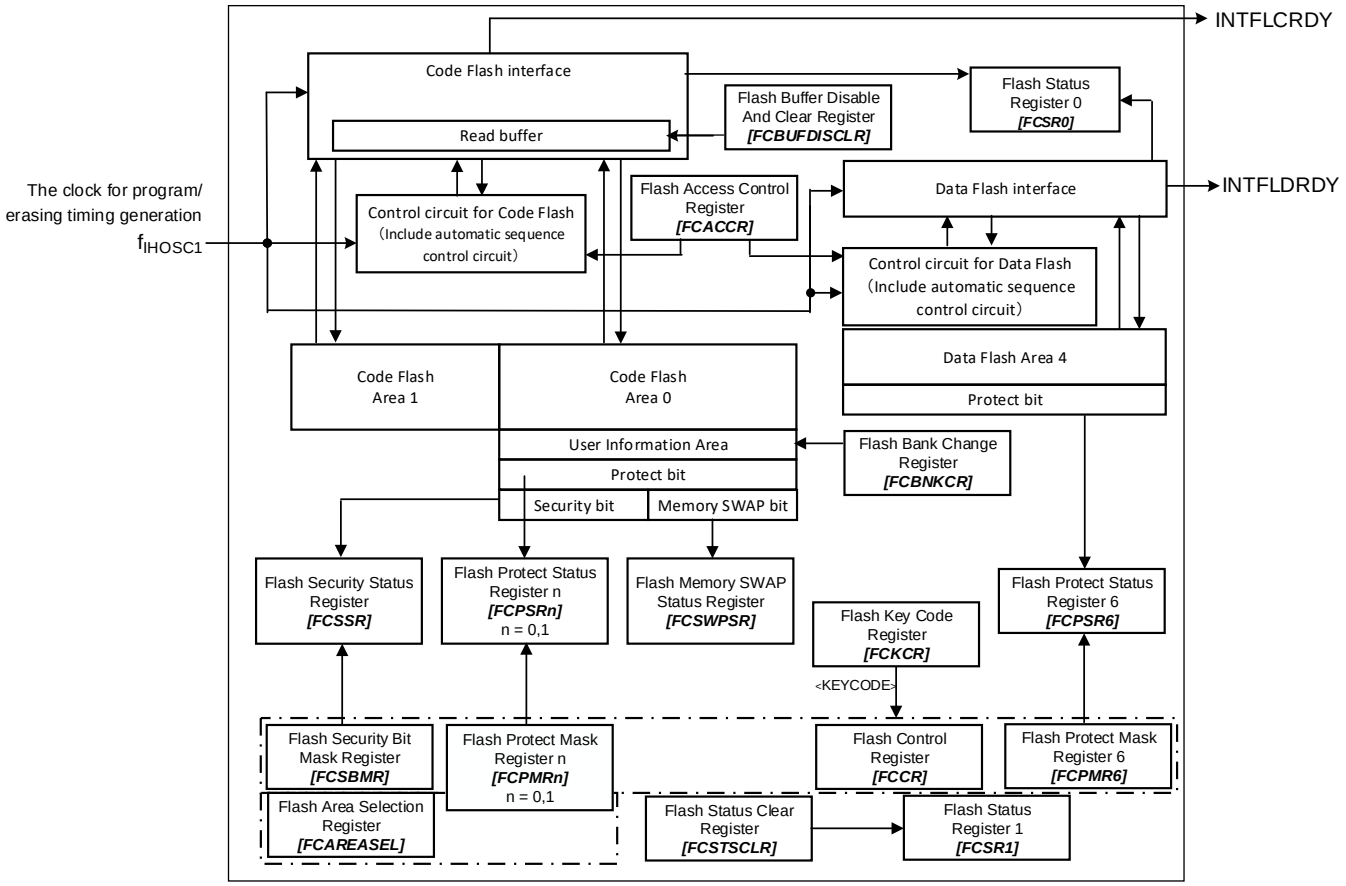

Figure 2.1 The Block Diagrams of a flash memory

Table 2.1 Signal list

No	Symbol	Signal name	I/O	Related reference manual
1	f_{IHOSC1}	The clock for programming/ erasing timing generation	Input	Clock Control and Operation Mode
2	**INTFLCRDY**	Code FLASH Ready interrupt	Output	Exception
3	**INTFLDRDY**	Data FLASH Ready interrupt	Output	Exception

2.2. Configuration of Code Flash

2.2.1. Unit of the composition

There are "Area", "Block", and "Page" as a unit of the composition of a code flash, and the respective sizes are as follows.

- Area : 512 KB
- Block : 32 KB
- Page : 4 KB

Erasing is performed in the unit of Page, Block, Area or on whole chip (Data Flash is included.).
Protection is performed in the unit of Page (only Block0) or Block (except for Block0).
Programming is performed in the unit of 16 bytes (4 bytes x 4 times).

Table 2.2 Block Configuration of 1024KB code flash

Area	Block	Page	Code execution address	Program/erase/read address
0	0	0	0x00000000 to 0x00000FFF	0x5E000000 to 0x5E000FFF
		:	:	:
		7	0x00007000 to 0x00007FFF	0x5E007000 to 0x5E007FFF
	1	8 to 15	0x00008000 to 0x0000FFFF	0x5E008000 to 0x5E00FFFF
	2	16 to 23	0x00010000 to 0x00017FFF	0x5E010000 to 0x5E017FFF
	3	24 to 31	0x00018000 to 0x0001FFFF	0x5E018000 to 0x5E01FFFF
	4	32 to 39	0x00020000 to 0x00027FFF	0x5E020000 to 0x5E027FFF
	5	40 to 47	0x00028000 to 0x0002FFFF	0x5E028000 to 0x5E02FFFF
	6	48 to 55	0x00030000 to 0x00037FFF	0x5E030000 to 0x5E037FFF
	7	56 to 63	0x00038000 to 0x0003FFFF	0x5E038000 to 0x5E03FFFF
	8	64 to 71	0x00040000 to 0x00047FFF	0x5E040000 to 0x5E047FFF
	9	72 to 79	0x00048000 to 0x0004FFFF	0x5E048000 to 0x5E04FFFF
	10	80 to 87	0x00050000 to 0x00057FFF	0x5E050000 to 0x5E057FFF
	11	88 to 95	0x00058000 to 0x0005FFFF	0x5E058000 to 0x5E05FFFF
	12	96 to 103	0x00060000 to 0x00067FFF	0x5E060000 to 0x5E067FFF
	13	103 to 111	0x00068000 to 0x0006FFFF	0x5E068000 to 0x5E06FFFF
	14	112 to 119	0x00070000 to 0x00077FFF	0x5E070000 to 0x5E077FFF
	15	120 to 127	0x00078000 to 0x0007FFFF	0x5E078000 to 0x5E07FFFF
1	16	128 to 135	0x00080000 to 0x00087FFF	0x5E080000 to 0x5E087FFF
	17	136 to 143	0x00088000 to 0x0008FFFF	0x5E088000 to 0x5E08FFFF
	18	144 to 151	0x00090000 to 0x00097FFF	0x5E090000 to 0x5E097FFF
	19	152 to 159	0x00098000 to 0x0009FFFF	0x5E098000 to 0x5E09FFFF
	20	160 to 167	0x000A0000 to 0x000A7FFF	0x5E0A0000 to 0x5E0A7FFF
	21	168 to 175	0x000A8000 to 0x000AFFFF	0x5E0A8000 to 0x5E0AFFFF
	22	176 to 183	0x000B0000 to 0x000B7FFF	0x5E0B0000 to 0x5E0B7FFF
	23	184 to 191	0x000B8000 to 0x000BFFFF	0x5E0B8000 to 0x5E0BFFFF
	24	192 to 199	0x000C0000 to 0x000C7FFF	0x5E0C0000 to 0x5E0C7FFF
	25	200 to 207	0x000C8000 to 0x000CFFFF	0x5E0C8000 to 0x5E0CFFFF
	26	208 to 215	0x000D0000 to 0x000D7FFF	0x5E0D0000 to 0x5E0D7FFF
	27	216 to 223	0x000D8000 to 0x000DFFFF	0x5E0D8000 to 0x5E0DFFFF
	28	224 to 231	0x000E0000 to 0x000E7FFF	0x5E0E0000 to 0x5E0E7FFF
	29	234 to 239	0x000E8000 to 0x000EFFFF	0x5E0E8000 to 0x5E0EFFFF

Area	Block	Page	Code execution address	Program/erase/read address
	30	240 to 247	0x000F0000 to 0x000F7FFF	0x5E0F0000 to 0x5E0F7FFF
	31	248 to 255	0x000F8000 to 0x000FFFFF	0x5E0F8000 to 0x5E0FFFFF

Table 2.3 Block Configuration of 512KB code flash

Area	Block	Page	Code execution address	Program/erase/read address
0	0	0	0x00000000 to 0x00000FFF	0x5E000000 to 0x5E000FFF
		:	:	:
		7	0x00007000 to 0x00007FFF	0x5E007000 to 0x5E007FFF
	1	8 to 15	0x00008000 to 0x0000FFFF	0x5E008000 to 0x5E00FFFF
	2	16 to 23	0x00010000 to 0x00017FFF	0x5E010000 to 0x5E017FFF
	3	24 to 31	0x00018000 to 0x0001FFFF	0x5E018000 to 0x5E01FFFF
	4	32 to 39	0x00020000 to 0x00027FFF	0x5E020000 to 0x5E027FFF
	5	40 to 47	0x00028000 to 0x0002FFFF	0x5E028000 to 0x5E02FFFF
	6	48 to 55	0x00030000 to 0x00037FFF	0x5E030000 to 0x5E037FFF
	7	56 to 63	0x00038000 to 0x0003FFFF	0x5E038000 to 0x5E03FFFF
	8	64 to 71	0x00040000 to 0x00047FFF	0x5E040000 to 0x5E047FFF
	9	72 to 79	0x00048000 to 0x0004FFFF	0x5E048000 to 0x5E04FFFF
	10	80 to 87	0x00050000 to 0x00057FFF	0x5E050000 to 0x5E057FFF
	11	88 to 95	0x00058000 to 0x0005FFFF	0x5E058000 to 0x5E05FFFF
	12	96 to 103	0x00060000 to 0x00067FFF	0x5E060000 to 0x5E067FFF
	13	103 to 111	0x00068000 to 0x0006FFFF	0x5E068000 to 0x5E06FFFF
	14	112 to 119	0x00070000 to 0x00077FFF	0x5E070000 to 0x5E077FFF
	15	120 to 127	0x00078000 to 0x0007FFFF	0x5E078000 to 0x5E07FFFF

Table 2.4 Block Configuration of 256KB code flash

Area	Block	Page	Code execution address	Program/erase/read address
0	0	0	0x00000000 to 0x00000FFF	0x5E000000 to 0x5E000FFF
		:	:	:
		7	0x00007000 to 0x00007FFF	0x5E007000 to 0x5E007FFF
	1	8 to 15	0x00008000 to 0x0000FFFF	0x5E008000 to 0x5E00FFFF
	2	16 to 23	0x00010000 to 0x00017FFF	0x5E010000 to 0x5E017FFF
	3	24 to 31	0x00018000 to 0x0001FFFF	0x5E018000 to 0x5E01FFFF
	4	32 to 39	0x00020000 to 0x00027FFF	0x5E020000 to 0x5E027FFF
	5	40 to 47	0x00028000 to 0x0002FFFF	0x5E028000 to 0x5E02FFFF
	6	48 to 55	0x00030000 to 0x00037FFF	0x5E030000 to 0x5E037FFF
	7	56 to 63	0x00038000 to 0x0003FFFF	0x5E038000 to 0x5E03FFFF

Table 2.5 Block Configuration of 128KB code flash

Area	Block	Page	Code execution address	Program/erase/read address
0	0	0	0x00000000 to 0x00000FFF	0x5E000000 to 0x5E000FFF
		:	:	:
		7	0x00007000 to 0x00007FFF	0x5E007000 to 0x5E007FFF

Area	Block	Page	Code execution address	Program/erase/read address
	1	8 to 15	0x00008000 to 0x0000FFFF	0x5E008000 to 0x5E00FFFF
	2	16 to 23	0x00010000 to 0x00017FFF	0x5E010000 to 0x5E017FFF
	3	24 to 31	0x00018000 to 0x0001FFFF	0x5E018000 to 0x5E01FFFF

2.2.2. User Information Area Configuration of Code Flash

User information area becomes accessible on bank switching.

Table 2.6 User Information Area Configuration of Code Flash

Area	User information area	Program/erase/read address	Page size (KB)
0	Page5	0x5E005000 to 0x5E005FFF	4

2.2.3. Program/Erase Time of Code Flash

Table 2.7 shows reference times of programming and erasing.

Table 2.7 Program/Erase Time of Code Flash

Capacity of Flash Memory (KB)	Programming time (Note1)		Erasing time (Note1)			
	programming unit (4-word)	Word	Page	Block	Area	Whole Chip (Note2)
1024	91µs	22.6µs	1.1ms	8.4ms	9.1ms	30.4ms
512						
256						21.3ms
128						

Note1: The times above-mentioned are for reference only which are calculated the Oscillation frequency of IHOSC1 on the standard (10MHz<Typ.>). And they indicate the case of the initial value of each register after reset. A data transfer time is excluded.

Note2: Total execution time of automatic chip erasing, automatic protect bit erasing (code and data) and automatic security bit erasing. An execution time of automatic chip erasing is when no blocks are protected.

2.3. Configuration of Data Flash

2.3.1. Unit of the composition

There are "Area", "Block", and "Page" as a unit of the composition of a data flash, and the respective sizes are as follows.

- Area : 32 KB
- Block : 4 KB
- Page : 256 byte

Erasing is performed in the unit of Page, Block, Area or on whole chip (Code Flash is included.).
Protection is performed in the unit of Block.
Programming is performed in the unit of 4 bytes (1 word).

2.3.2. Block Configuration of Data Flash

Table 2.8 Block configuration of 32 KB data flash

Area	Block	Page	Program/erase/read address
4	0	0	0x30000000 to 0x300000FF
		:	:
		15	0x30000F00 to 0x30000FFF
	1	16 to 31	0x30001000 to 0x30001FFF
	2	32 to 47	0x30002000 to 0x30002FFF
	3	48 to 63	0x30003000 to 0x30003FFF
	4	64 to 79	0x30004000 to 0x30004FFF
	5	80 to 95	0x30005000 to 0x30005FFF
	6	96 to 111	0x30006000 to 0x30006FFF
	7	112 to 127	0x30007000 to 0x30007FFF

2.3.3. Program/Erase Time of Data Flash

Table 2.9 shows reference times of programming and erasing.

Table 2.9 Program/Erase Time of Data Flash

Capacity (KB)	Programming time (Note)	Erasing time (Note)		
	Word	Page	Block	Area
32	78μs	1.1ms	16.2ms	9.1ms

Note: The time above-mentioned is for reference only which calculated the Oscillation frequency of IHOSC1 on the standard (10MHz<Typ.>). And indicate the case of the initial value of each register after reset. A data transfer time is excluded.

3. Function and Operation Explanations

Code flash and data flash are generally compliant with the JEDEC standards except for some specific functions. Therefore, if a user is currently using a Flash memory as an external memory, it is easy to implement the functions into this device. Furthermore, to provide easy program or erase operation, this flash memory contains a dedicated circuit to perform program or chip erase automatically.

Table 3.1 JEDEC compliant functions

JEDEC compliant functions	Modified, added, or deleted functions
- Automatic programming - Automatic chip erasing - Automatic block erasing	<Addition> Automatic area erasing, automatic page erasing, automatic memory swap/erasing <Modified> Program/erase protect (only protection of program is supported) <Deleted> Erase resume/suspend function

Precautions

(1) Make sure to set ***[CGOSCCR]***<IHOSC1EN>=1 to oscillate the internal high speed oscillator1 (IHOSC1) when data is programmed or erased code flash, data flash, user information area. Also oscillate the IHOSC1 before the operations related to the flash memory including protection and security operations. IHOSC1 is timing clock for programming/Erasing of flash memory.

(2) Set up with procedure of oscillation start of internal oscillator1(IHOSC1). And operate flash memory after oscillation is stabilized.

[CGWUPHCR] = 0x03C00000	Set warming up time to 163.4μs or more (Count by internal oscillation)
[CGOSCCR]<IHOSC1EN>=1	Enable internal oscillator1 to oscillate
[CGWUPHCR]<WUON>=1	Start warming up timer
Read ***[CGWUPHCR]***<WUEF>	Wait finish of warming up timer status (<WUEF>=0)

Please refer to reference manual “Clock Control and Operation Mode” about IHOSC1 and warming up.

(3) Do not power off while Flash is busy (Programming or Erasing, ***[FCSR0]***<RDYBSY>=0).

(4) Do not enter STOP1/STOP2 mode while Flash is busy (Programming or Erasing, ***[FCSR0]***<RDYBSY>=0).

(5) Make sure not to occur reset by SIWDT or LVD while Flash is busy (Programming or Erasing, ***[FCSR0]***<RDYBSY>=0).

3.1. Code Flash

3.1.1. Command Sequence

3.1.1.1. List of Command Sequence

This section shows addresses and data of the bus write cycle in each command of code flash.

Except the 5th bus cycle of ID-Read command, all cycles are “bus write cycles”. A bus write cycle is performed by a 32-bit (1 word) data transfer instruction. “Table 3.2 Command Sequence (code flash)” only shows the lower 8 bits data.

For details of addresses, refer to “Table 3.3Address bit configuration in the bus write cycle (Code flash)”. Use the values in the table below to Addr[11:4] where “Command” is inputted.

Note: Each command address is set to a flash area (mirror).

Table 3.2 Command Sequence (code flash)

Sequence / Command	1st bus cycle	2nd bus cycle	3rd bus cycle	4th bus Cycle	5th bus cycle	6th bus cycle	7th bus cycle
	Address	Address	Address	Address	Address	Address	Address
	Data	Data	Data	Data	Data	Data	Data
Read/Reset	0xYYYYXXXX	-	-	-	-	-	-
	0xF0	-	-	-	-	-	-
ID-Read	0xYYYYX55X	0xYYYYXAAX	0xYYYYX55X	IA	0xYYYYXXXX	-	-
	0xAA	0x55	0x90	0x00	ID	-	-
Automatic programming	0xYYYYX55X	0xYYYYXAAX	0xYYYYX55X	PA	PA	PA	PA
	0xAA	0x55	0xA0	PD0	PD1	PD2	PD3
Automatic page erasing	0xYYYYX55X	0xYYYYXAAX	0xYYYYX55X	0xYYYYX55X	0xYYYYXAAX	PGA	-
	0xAA	0x55	0x80	0xAA	0x55	0x40	-
Automatic block erasing	0xYYYYX55X	0xYYYYXAAX	0xYYYYX55X	0xYYYYX55X	0xYYYYXAAX	BA	-
	0xAA	0x55	0x80	0xAA	0x55	0x30	-
Automatic area erasing	0xYYYYX55X	0xYYYYXAAX	0xYYYYX55X	0xYYYYX55X	0xYYYYXAAX	AA	-
	0xAA	0x55	0x80	0xAA	0x55	0x20	-
Automatic code area erasing	0xYYYYX55X	0xYYYYXAAX	0xYYYYX55X	0xYYYYX55X	0xYYYYXAAX	0xYYYYX55X	-
	0xAA	0x55	0x80	0xAA	0x55	0x11	-
Automatic chip erasing	0xYYYYX55X	0xYYYYXAAX	0xYYYYX55X	0xYYYYX55X	0xYYYYXAAX	0xYYYYX55X	-
	0xAA	0x55	0x80	0xAA	0x55	0x10	-
Automatic protect bit programming	0xYYYYX55X	0xYYYYXAAX	0xYYYYX55X	PBA(Note)	-	-	-
	0xAA	0x55	0x9A	0x9A	-	-	-

Sequence / Command	1st bus cycle	2nd bus cycle	3rd bus cycle	4th bus Cycle	5th bus cycle	6th bus cycle	7th bus cycle
	Address	Address	Address	Address	Address	Address	Address
	Data	Data	Data	Data	Data	Data	Data
Automatic protect bit erasing	0xYYYYX55X	0xYYYYXAAX	0xYYYYX55X	0xYYYYX55X	0xYYYYXAAX	PBA(Note)	-
	0xAA	0x55	0x80	0xAA	0x55	0x60	-
Automatic memory swap programming	0xYYYYX55X	0xYYYYXAAX	0xYYYYX55X	MSA(Note)	-	-	-
	0xAA	0x55	0x9A	0x9A	-	-	-
Automatic memory swap erasing	0xYYYYX55X	0xYYYYXAAX	0xYYYYX55X	0xYYYYX55X	0xYYYYXAAX	MSA(Note)	-
	0xAA	0x55	0x80	0xAA	0x55	0x60	-
Automatic security bit programming	0xYYYYX55X	0xYYYYXAAX	0xYYYYX55X	SBA(Note)	-	-	-
	0xAA	0x55	0x9A	0x9A	-	-	-
Automatic security bit erasing	0xYYYYX55X	0xYYYYXAAX	0xYYYYX55X	0xYYYYX55X	0xYYYYXAAX	SBA(Note)	-
	0xAA	0x55	0x80	0xAA	0x55	0x60	-

Note: Please refer to “Table 3.3 Address bit configuration in the bus write cycle (Code flash)”.

Supplementary explanation
IA: ID address
ID: ID data output
PGA: Page address
BA: Block address
AA: Area address
PA: Program address (write)
PD: Program data (32-bit data)
After the 4th bus cycle, 4 word data are sequentially input in address order.
PBA: Protect bit address
MSA: Memory swap address
SBA: Security bit address

3.1.1.2. Address Bit Configuration in the Bus Write Cycle (Code Flash)

Please refer to Table 3.3 with “Table 3.2 Command Sequence (code flash)”.

Specify addresses in the first bus cycle and later cycle based on address setting of bus write cycle of normal command.

Table 3.3 Address bit configuration in the bus write cycle (Code flash)

[Normal command]

Address	Adr [31:24]	Adr [23:21]	Adr [20:19]	Adr [18:12]	Adr [11:4]	Adr [3:0]
Normal command	Address setting of bus write cycle of normal command					
	0x5E	“000” Fixed	Area 0:00 1:01	"0" Recommended	Command	"0" Recommended

[Read/reset, ID-Read]

Address	Adr [31:24]	Adr [23:21]	Adr [20:16]	Adr [15:14]	Adr [13:0]
Read/ reset	Address setting of 1st bus write cycle of Read/reset				
	0x5E	“000” Fixed	"0" Recommended		
ID-Read	IA: ID address (address setting of the 4th bus write cycle of ID-Read)				
	0x5E	“000” Fixed	"00000" fixed	ID address	"0" Recommended

[Automatic chip erasing]

Address	Adr [31:24]	Adr [23:21]	Adr [20:12]	Adr [11:4]	Adr [3:0]
Chip erasing	Address setting of 1st to 6th bus write cycle of chip erasing				
	0x5E	“000” Fixed	"0" Recommended	Command	"0" Recommended

[Automatic area erasing]

Address	Adr [31:24]	Adr [23:21]	Adr [20:19]	Adr [18:0]
Area erasing	AA: Area Address (address setting of the 6th bus write cycle of area erase command)			
	0x5E	“000” Fixed	Area 0:00 1:01	"0" Recommended

[Automatic block erasing]

Address	Adr [31:24]	Adr [23:21]	Adr [20:19]	Adr [18:15]	Adr [14:0]
Block erasing	BA: Block address (address setting of the 6th bus write cycle of block erasing command)				
	0x5E	“000” Fixed	Area 0:00 1:01	Block address	"0" Recommended

[Automatic page erasing]

Address	Adr [31:24]	Adr [23:21]	Adr [20:19]	Adr [18:12]	Adr [11:0]
Page erasing	PGA: Page Address (address setting of the 6th bus write cycle of page erasing command)				
	0x5E	“000” Fixed	Area 0:00 1:01	Page address	"0" Recommended

[Automatic programming]

Address	Adr [31:24]	Adr [23:21]	Adr [20:19]	Adr [18:4]	Adr [3:0]
Program	PA: Program address (address setting of the 4th to 7th bus write cycle of the program)				
	0x5E	“000” Fixed	Area 0:00 1:01	Program address	"0" Recommended

[Automatic protect bit programming/erasing]

Address	Adr [31:24]	Adr [23:21]	Adr [20:19]	Adr [18:12]	Adr [11:4]	Adr [3:0]
Protect bit erasing	PBA: Protect Bit Address (address setting of the 6th bus write cycle of Protect bit erasing)					
	0x5E	“000” Fixed	“00” Fixed	“0000010” Fixed	"0" Recommended	
Protect bit programming	PBA: Protect Bit Address (address setting of the 4th bus write cycle of Protect bit programming)					
	0x5E	“000” Fixed	“00” Fixed	“0000010” Fixed	Protect bit address	"0" Recommended

[Automatic memory swap erasing/programming]

Address	Adr [31:24]	Adr [23:21]	Adr [20:19]	Adr [18:12]	Adr [11:4]	Adr [3:0]
Memory swap erasing	MSA: address setting of the 6th bus write cycle of memory swap erasing					
	0x5E	“000” Fixed	“00” Fixed	“0000011” Fixed	"0" Recommended	
Memory swap programming	MSA: address setting of the 4th bus write cycle of memory swap programming					
	0x5E	“000” Fixed	“00” Fixed	“0000011” Fixed	Memory swap address	"0" Recommended

[Automatic security bit programming/erasing]

Address	Adr [31:24]	Adr [23:21]	Adr [20:19]	Adr [18:12]	Adr [11:0]
Security bit Erasing	SBA: Address of the 6th bus write cycle of security bit erasing				
	0x5E	“000” Fixed	“00” Fixed	“0000001” Fixed	"0" Recommended
Security bit programming	SBA: Address of the 4th bus write cycle of security bit programming				
	0x5E	“000” Fixed	“00” Fixed	“0000001” Fixed	"0" Recommended

3.1.1.3. Area Address (AA), Block Address (BA): Code Flash

Table 2.2 to Table 2.3 show area addresses and block addresses. An address of the area or block to be erased should be specified in the 6th bus write cycle of automatic area erasing command and automatic block erasing command. In single chip mode, an address of the mirror area should be specified.

3.1.1.4. Protect Bit Assignment (PBA): Code flash

A protect bit can be controlled in the unit of one bit.
Table 3.4 shows the protect bit selection of the automatic protect bit programming.

Table 3.4 Protect bit programming address

Area	Block	Page	Register	Protect bit	PBA[11:4]								Example of address [31:0]
					Adr [11]	Adr [10]	Adr [9]	Adr [8]	Adr [7]	Adr [6]	Adr [5]	Adr [4]	
0	0	0	*[FCPSR0]*	<PG0>	0	0	0	0	0	0	0	0	0x5E002000
		1		<PG1>	0	0	0	0	0	0	0	1	0x5E002010
		2		<PG2>	0	0	0	0	0	0	1	0	0x5E002020
		3		<PG3>	0	0	0	0	0	0	1	1	0x5E002030
		4		<PG4>	0	0	0	0	0	1	0	0	0x5E002040
		5		<PG5>	0	0	0	0	0	1	0	1	0x5E002050
		6		<PG6>	0	0	0	0	0	1	1	0	0x5E002060
		7		<PG7>	0	0	0	0	0	1	1	1	0x5E002070
	1	8 to 15	*[FCPSR1]*	<BLK1>	0	0	0	0	1	0	0	0	0x5E002080
	2	16 to 23		<BLK2>	0	0	0	0	1	0	0	1	0x5E002090
	3	24 to 31		<BLK3>	0	0	0	0	1	0	1	0	0x5E0020A0
	4	32 to 39		<BLK4>	0	0	0	0	1	0	1	1	0x5E0020B0
	5	40 to 47		<BLK5>	0	0	0	0	1	1	0	0	0x5E0020C0
	6	48 to 55		<BLK6>	0	0	0	0	1	1	0	1	0x5E0020D0
	7	56 to 63		<BLK7>	0	0	0	0	1	1	1	0	0x5E0020E0
	8	64 to 71		<BLK8>	0	0	0	0	1	1	1	1	0x5E0020F0
	9	72 to 79		<BLK9>	0	0	0	1	0	0	0	0	0x5E002100
	10	80 to 87		<BLK10>	0	0	0	1	0	0	0	1	0x5E002110
	11	88 to 95		<BLK11>	0	0	0	1	0	0	1	0	0x5E002120
	12	96 to103		<BLK12>	0	0	0	1	0	0	1	1	0x5E002130
	13	104 to 111		<BLK13>	0	0	0	1	0	1	0	0	0x5E002140
	14	112 to 119		<BLK14>	0	0	0	1	0	1	0	1	0x5E002150
	15	120 to 127		<BLK15>	0	0	0	1	0	1	1	0	0x5E002160
1	16	128 to 135		<BLK16>	0	0	0	1	0	1	1	1	0x5E002170
	17	136 to 143		<BLK17>	0	0	0	1	1	0	0	0	0x5E002180
	18	144 to 151		<BLK18>	0	0	0	1	1	0	0	1	0x5E002190

Area	Block	Page	Register	Protect bit	PBA[11:4]								Example of address [31:0]
					Adr [11]	Adr [10]	Adr [9]	Adr [8]	Adr [7]	Adr [6]	Adr [5]	Adr [4]	
	19	152 to 159		<BLK19>	0	0	0	1	1	0	1	0	0x5E0021A0
	20	160 to 167		<BLK20>	0	0	0	1	1	0	1	1	0x5E0021B0
	21	168 to 175		<BLK21>	0	0	0	1	1	1	0	0	0x5E0021C0
	22	176 to 183		<BLK22>	0	0	0	1	1	1	0	1	0x5E0021D0
	23	184 to 191		<BLK23>	0	0	0	1	1	1	1	0	0x5E0021E0
	24	192 to 199		<BLK24>	0	0	0	1	1	1	1	1	0x5E0021F0
	25	200 to 207		<BLK25>	0	0	1	0	0	0	0	0	0x5E002200
	26	208 to 215		<BLK26>	0	0	1	0	0	0	0	1	0x5E002210
	27	216 to 223		<BLK27>	0	0	1	0	0	0	1	0	0x5E002220
	28	224 to 231		<BLK28>	0	0	1	0	0	0	1	1	0x5E002230
	29	232 to 239		<BLK29>	0	0	1	0	0	1	0	0	0x5E002240
	30	240 to 247		<BLK30>	0	0	1	0	0	1	0	1	0x5E002250
	31	248 to 255		<BLK31>	0	0	1	0	0	1	1	0	0x5E002260

3.1.1.5. ID-Read Code (IA, ID): Code Flash

Table 3.5 shows the code assignment and the contents of ID-Read command.

Table 3.5 ID-Read Command code assignment and the code contents

Code	ID[15:0]	IA[15:14]	Example of address [31:0]
Manufacturer code	0x0098	00	0x5E000000
Device code	0x005A	01	0x5E004000
-	Reserved	10	N/A
Macro code	(Note)	11	0x5E00C000

Note: The ID is depend on a product and memory size. For the details, refer to reference manual "Product Information".

3.1.1.6. Memory Swap Bit Assignment (MSA)

"Table 3.6 Setting values assigned to Memory swap address using Memory Swap command, and example of address" shows the setting values of "Memory swap address" assigned in the 4th bus write cycle of the auto memory swap command.

Table 3.6 Setting values assigned to Memory swap address using Memory Swap command, and example of address

Register		MSA[11:4]						Example of address [31:0]
		Adr [11:9]	Adr [8]	Adr [7]	Adr [6]	Adr [5]	Adr [4]	
[FCSWPSR]	<SWP0>	000	0	0	0	0	0	0x5E003000
	<SWP1>	000	0	0	0	0	1	0x5E003010
	<SIZE0>	000	0	0	0	1	0	0x5E003020
	<SIZE1>	000	0	0	0	1	1	0x5E003030
	<SIZE2>	000	0	0	1	0	0	0x5E003040
	<SIZE3>	000	0	0	1	0	1	0x5E003050
	<SIZE4>	000	0	0	1	1	0	0x5E003060

3.2. Data Flash

3.2.1. Command Sequence

3.2.1.1. List of Command Sequence

This section shows addresses and data of the bus write cycle in each command of data flash.

Except the 5th bus cycle of ID-Read command, all cycles are “bus write cycles”. A bus write cycle is performed by a 32-bit (1 word) data transfer instruction. Table 3.7 only shows the lower 8 bits data.

For details of addresses, refer to “Table 3.8 Address bit configuration in the bus write cycle (data flash)”. Use the values in the table below to Addr[11:4] where “Command” is inputted.

Note: Each command address is set in a flash area (data).

Table 3.7 Command sequence (Data flash)

Sequence / Command	1st bus cycle	2nd bus cycle	3rd bus cycle	4th bus cycle	5th bus cycle	6th bus cycle	7th bus cycle
	Address	Address	Address	Address	Address	Address	Address
	Data	Data	Data	Data	Data	Data	Data
Read/reset	0xYYYYXXXX	-	-	-	-	-	-
	0xF0	-	-	-	-	-	-
ID-Read	0xYYYYX55X	0xYYYYXAAX	0xYYYYX55X	IA	0xYYYYXXXX	-	-
	0xAA	0x55	0x90	0x00	ID	-	-
Automatic programming	0xYYYYX55X	0xYYYYXAAX	0xYYYYX55X	PA	-	-	-
	0xAA	0x55	0xC0	PD0	-	-	-
Automatic page erasing	0xYYYYX55X	0xYYYYXAAX	0xYYYYX55X	0xYYYYX55X	0xYYYYXAAX	PGA	-
	0xAA	0x55	0x80	0xAA	0x55	0x40	-
Automatic block erasing	0xYYYYX55X	0xYYYYXAAX	0xYYYYX55X	0xYYYYX55X	0xYYYYXAAX	BA	-
	0xAA	0x55	0x80	0xAA	0x55	0x30	-
Automatic area erasing	0xYYYYX55X	0xYYYYXAAX	0xYYYYX55X	0xYYYYX55X	0xYYYYXAAX	AA	-
	0xAA	0x55	0x80	0xAA	0x55	0x20	-
Automatic Protect bit programming	0xYYYYX55X	0xYYYYXAAX	0xYYYYX55X	PBA(Note)	-	-	-
	0xAA	0x55	0x9A	0x9A	-	-	-
Automatic Protect bit erasing	0xYYYYX55X	0xYYYYXAAX	0xYYYYX55X	0xYYYYX55X	0xYYYYXAAX	PBA(Note)	-
	0xAA	0x55	0x80	0xAA	0x55	0x60	-

Note: Please refer to “Table 3.8 Address bit configuration in the bus write cycle (data flash)”.

Supplementary explanation
IA: ID address
ID: ID data output
PGA: Page address
BA: Block address
AA: Area address
PA: Program address (write)
PD: Program data (32-bit data)
PBA: Protect bit address

3.2.1.2. Address Configuration in the Bus Write Cycle (Data Flash)

Please refer to Table 3.8 with “Table 3.7 Command sequence (Data flash)”.

Specify addresses in the first bus cycle and later cycle, based on “address setting of bus write cycle of normal command”.

Table 3.8 Address bit configuration in the bus write cycle (data flash)

[Normal command]

Address	Adr [31:24]	Adr [23:16]	Adr [15]	Adr [14:12]	Adr [11:4]	Adr [3:0]
Normal command	Address setting of bus write cycle of normal command					
	0x30	“00000000” Fixed	Area4: 0	"0” Recommended	Command	"0” Recommended

[Read/reset, ID-Read]

Address	Adr [31:24]	Adr [23:16]	Adr [15]	Adr [14:13]	Adr [12:0]
Read /reset	Address setting of 1st bus write cycle of read/reset				
	0x30	“00000000” Fixed	"0” Recommended		
ID-Read	IA: ID Address (address setting of 4th bus write cycle of ID-Read)				
	0x30	“00000000” Fixed	"0” Fixed	ID address	"0” Recommended

[Automatic area erasing]

Address	Adr [31:24]	Adr [23:16]	Adr [15]	Adr [14:0]
Area erasing	AA: Area Address (address setting of 6th bus write cycle of area erasing command)			
	0x30	“00000000” Fixed	Area4: 0	"0” Recommended

[Automatic block erasing]

Address	Adr [31:24]	Adr [23:16]	Adr [15]	Adr [14:12]	Adr [11:0]
Block erasing	BA: Block Address (address setting of 6th bus write cycle of block erasing command)				
	0x30	“00000000” Fixed	Area4: 0	Block address	"0” Recommended

[Automatic page erasing]

Address	Adr [31:24]	Adr [23:16]	Adr [15]	Adr [14:8]	Adr [7:0]
Page erasing	PGA: Page Address (address setting of 6th bus write cycle of page erasing command)				
	0x30	“00000000” Fixed	Area4: 0	Page address	"0” Recommended

[Automatic programming]

Address	Adr [31:24]	Adr [23:16]	Adr [15]	Adr [14:2]	Adr [1:0]
Program	PA: Program Address (address setting of 4th bus write cycle of programming command)				
	0x30	“00000000” Fixed	Area4: 0	Program address	"0” Recommended

[Automatic protect bit programming/erasing]

Address	Adr [31:24]	Adr [23:16]	Adr [15]	Adr [14:8]	Adr [7:2]	Adr [1:0]
Protect bit erasing	PBA: Protect Bit Address (Address setting of 6th bus write cycle of protect bit erasing command)					
	0x30	“00000000” Fixed	“0” Fixed	“0000001” Fixed	"0” Recommended	
Protect bit programming	PBA: Protect Bit Address (address setting of 4th bus write cycle of protect bit programming command)					
	0x30	“00000000” Fixed	“0” Fixed	“0000001” Fixed	Protect bit Address	"0” Recommended

3.2.1.3. Area Address (AA), Block Address (BA)

“Table 2.8 Block configuration of 32 KB data flash” shows area addresses and block addresses. An address of the area or block to be erased should be specified in the 6th bus write cycle of automatic area erasing command and automatic block erasing command.

3.2.1.4. Protect Bit Address (PBA)

A protect bit can be controlled in the unit of one bit.

Table 3.9 shows the protect bit selection of the automatic protect bit program.

Table 3.9 Protect bit program address (Data flash)

Area	Block	Register	Protect bit	PBA[7:2]					Example of address [31:0]
				Adr [7:6]	Adr [5]	Adr [4]	Adr [3]	Adr [2]	
4	0	*[FCPSR6]*	<DBLK0>	00	0	0	0	0	0x30000100
	1		<DBLK1>	00	0	0	0	1	0x30000104
	2		<DBLK2>	00	0	0	1	0	0x30000108
	3		<DBLK3>	00	0	0	1	1	0x3000010C
	4		<DBLK4>	00	0	1	0	0	0x30000110
	5		<DBLK5>	00	0	1	0	1	0x30000114
	6		<DBLK6>	00	0	1	1	0	0x30000118
	7		<DBLK7>	00	0	1	1	1	0x3000011C

3.2.1.5. ID-Read Code (IA, ID): Data Flash

Table 3.10 shows the code assignment and the contents of ID-Read command.

Table 3.10 ID-Read command code assignment and the contents (Data flash)

Code	ID[15:0]	IA[14:13]	Example of address [31:0]
Manufacturer code	0x0098	00	0x30000000
Device code	0x005A	01	0x30002000
-	Reserved	10	N/A
Macro code	(Note)	11	0x30006000

Note: The ID is depend on a product and memory size. For the details, refer to reference manual "Product Information".

3.3. Flowchart

This section shows examples of code flash programming.

3.3.1. Automatic Programming

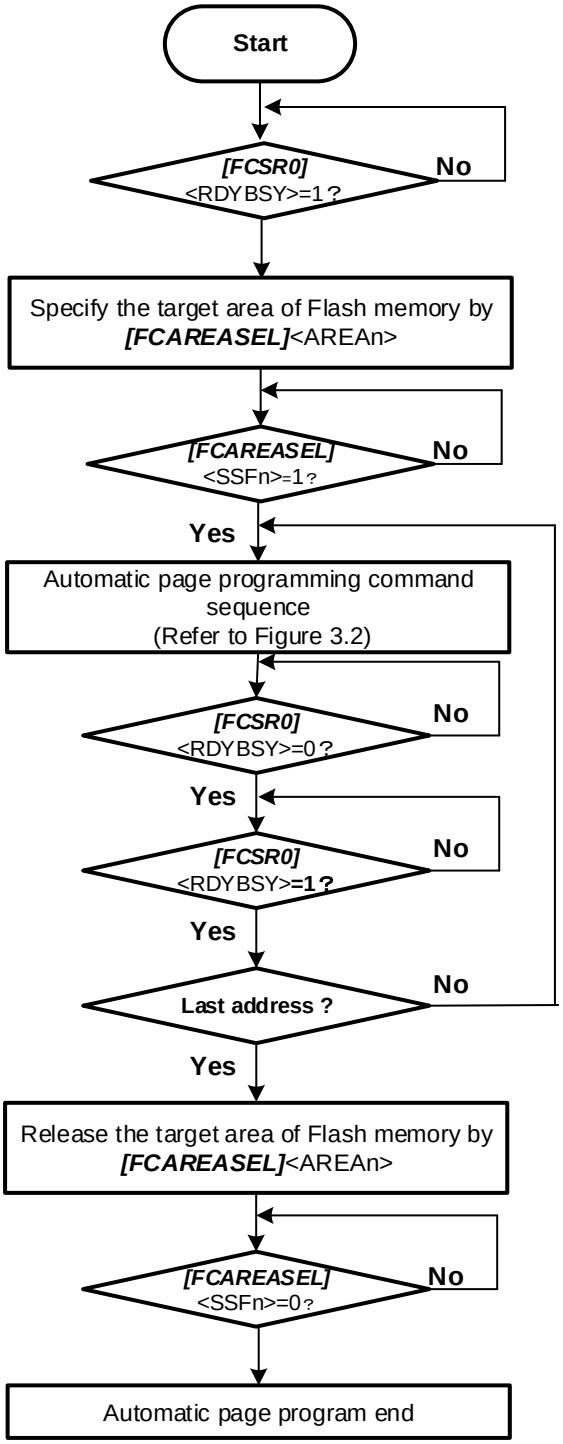

Figure 3.1 Flowchart of automatic programming (1)

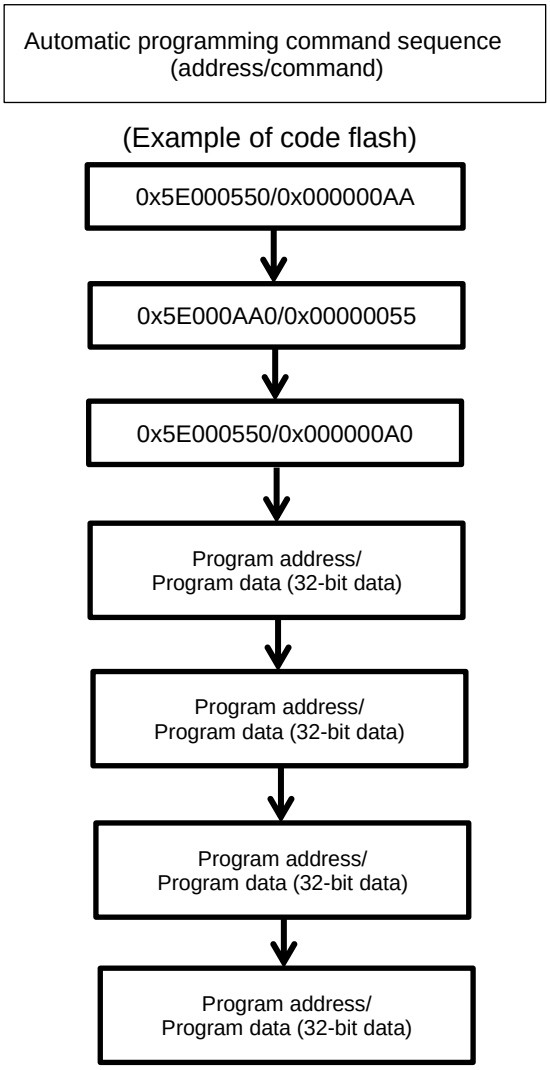

Figure 3.2 Flowchart of automatic programming (2)

3.3.2. Automatic Erasing

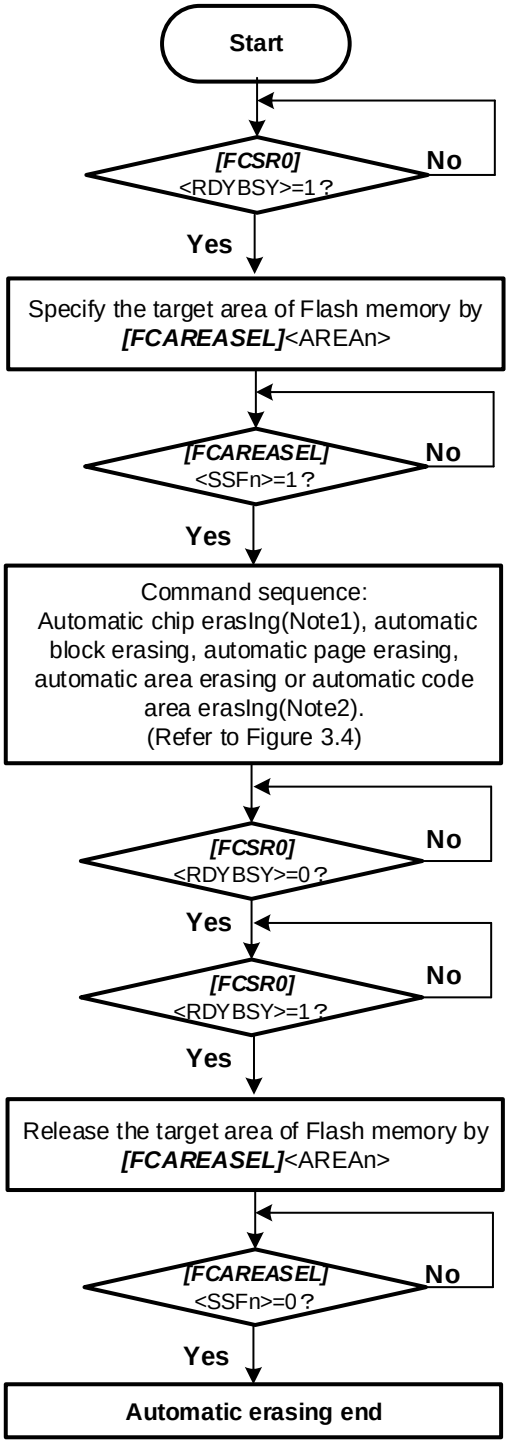

Figure 3.3 Flowchart of automatic erasing (1)

Note1: When executing automatic chip erasing command sequence, please select all the area of a code flash, and the area of a data flash.
Note2: When executing automatic code area erasing command sequence, please select all the area of a code flash.

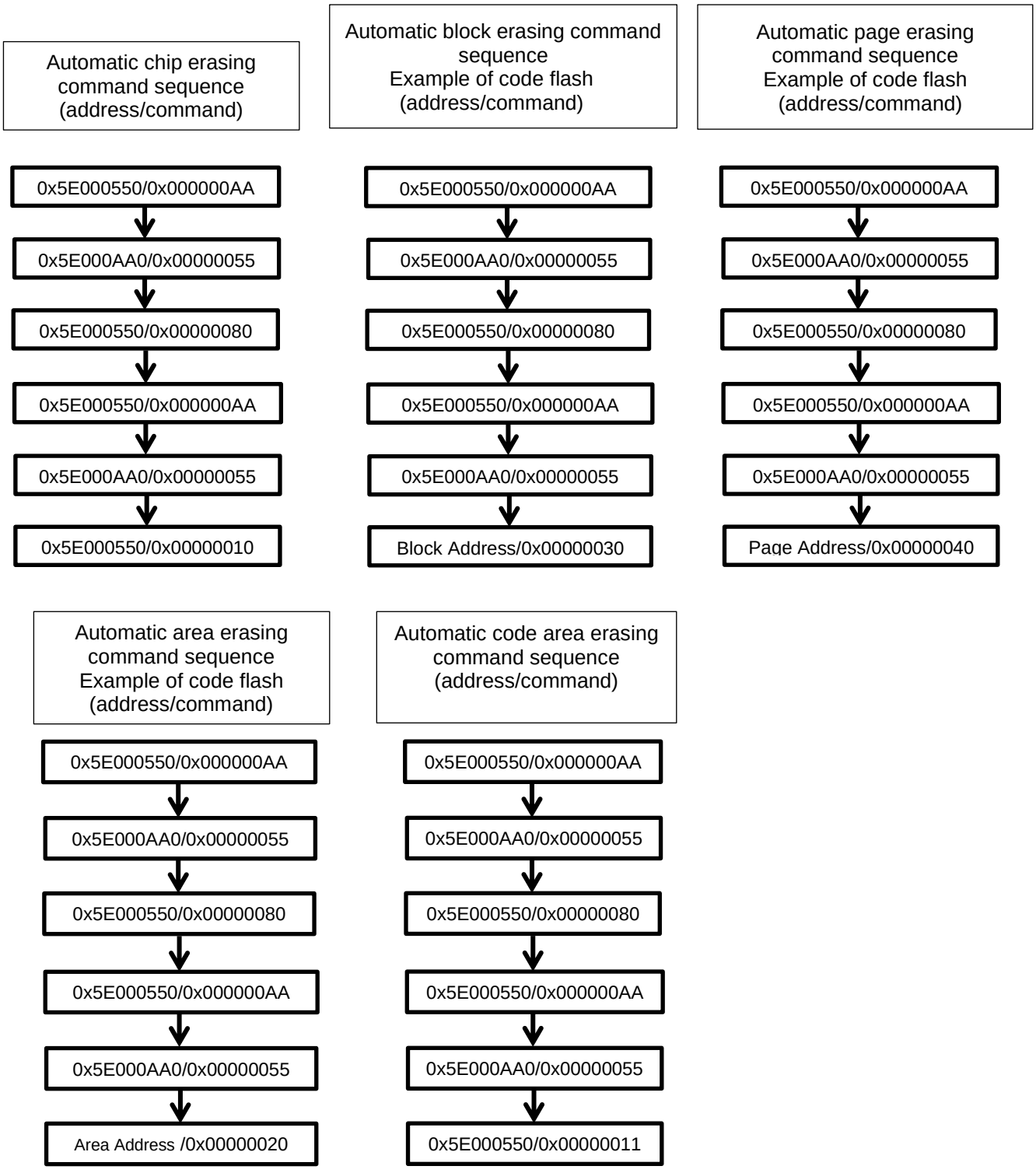

Figure 3.4 Flowchart of automatic erasing (2)

3.3.3. Protect bit

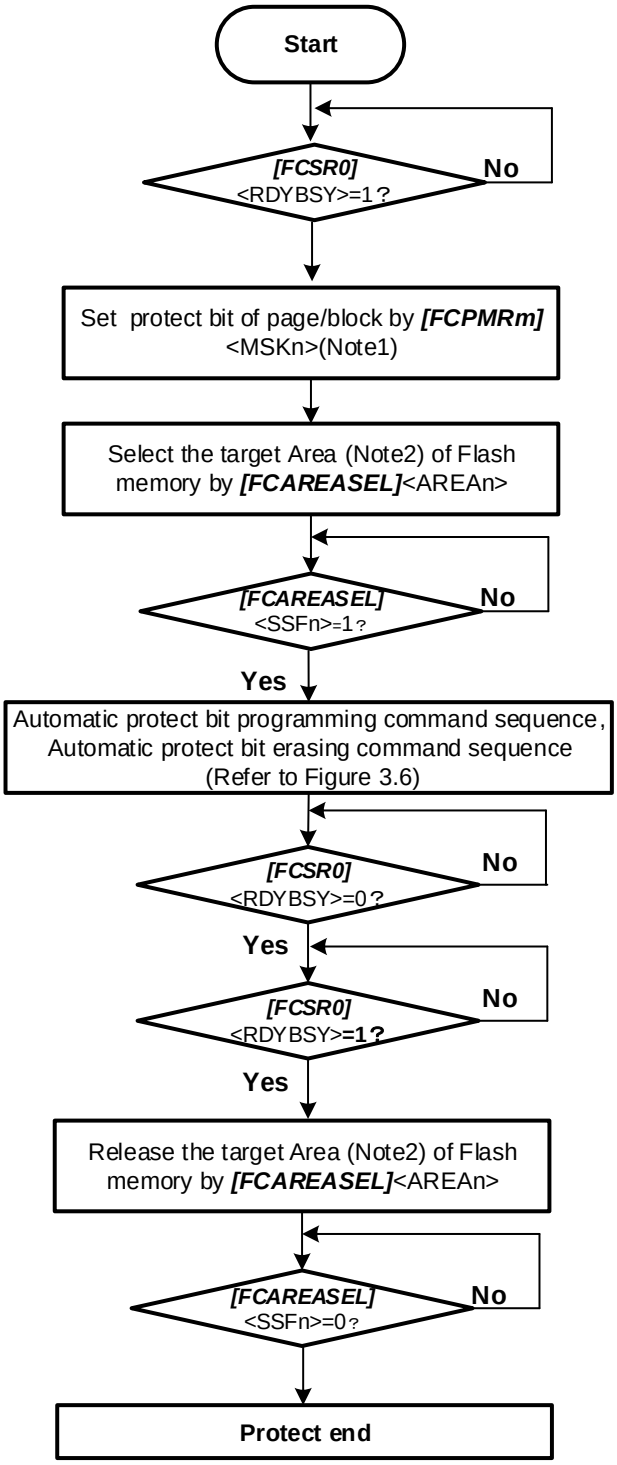

Figure 3.5 Flowchart of protect (1)

Note1: <MSKn> represents <PMn>, <MSKn>, and <DMSKn>.

Note2: Area “0” is selected for Code Flash. Area “4” is selected for Data Flash.

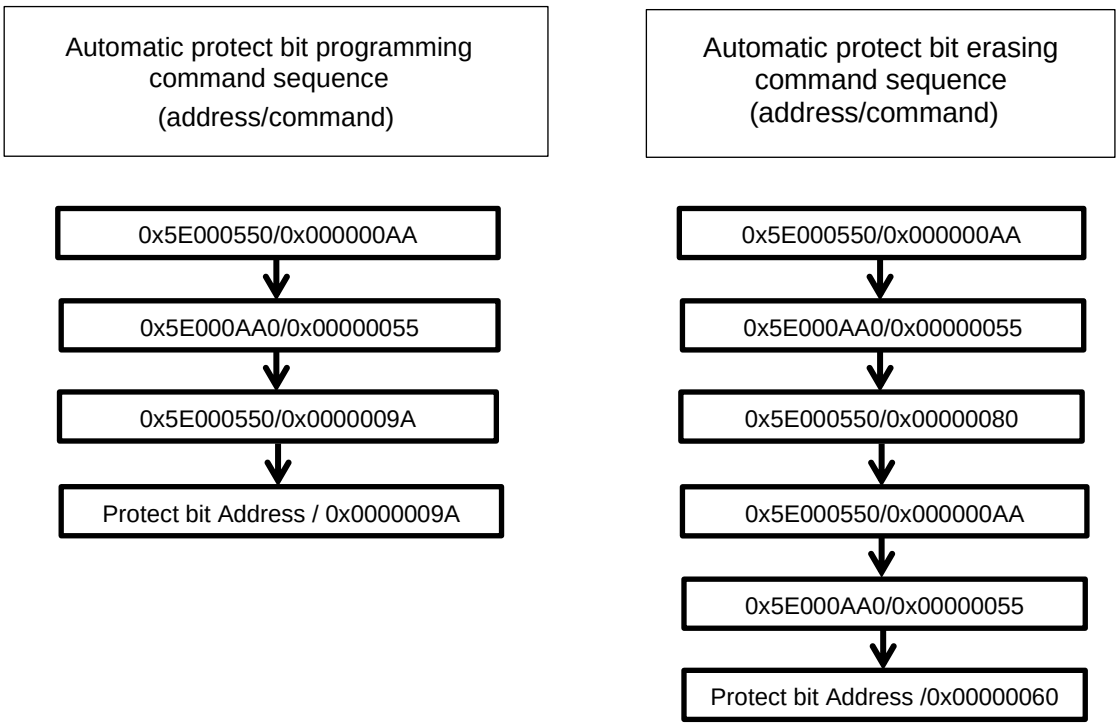

Figure 3.6 Flowchart of protect (2)

3.3.4. Security bit

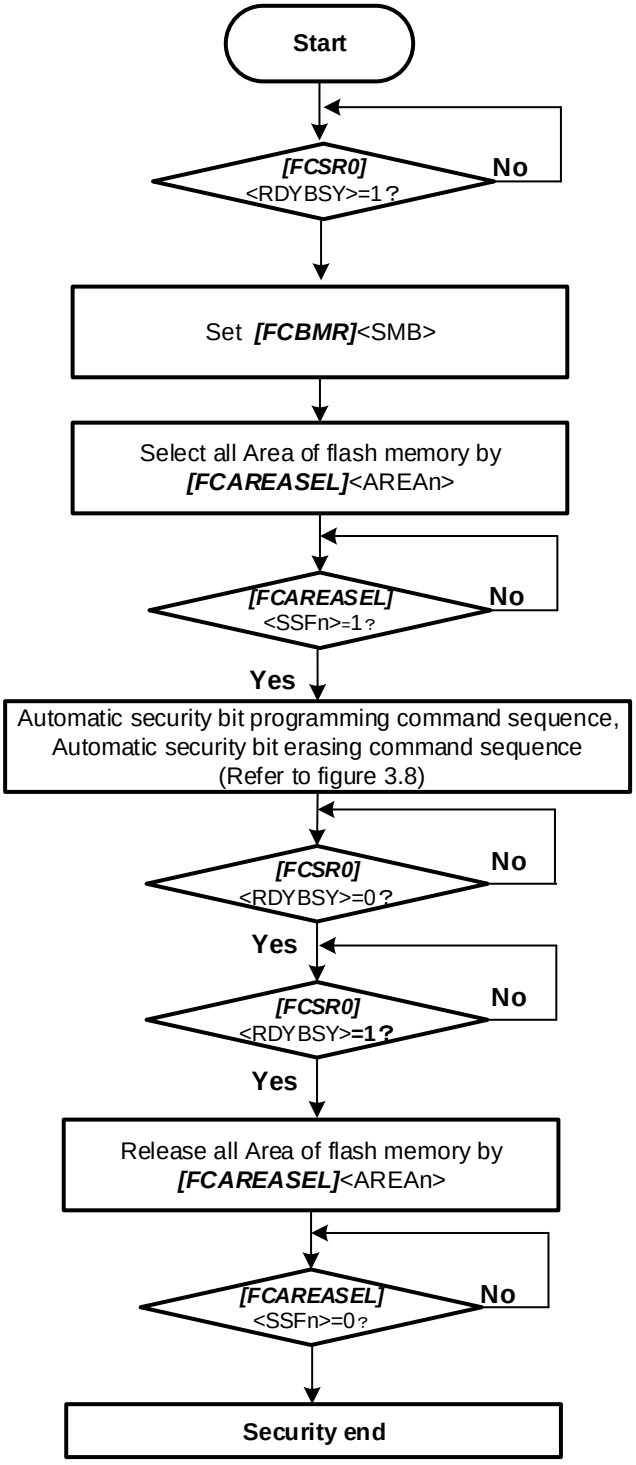

Figure 3.7 Flowchart of security (1)

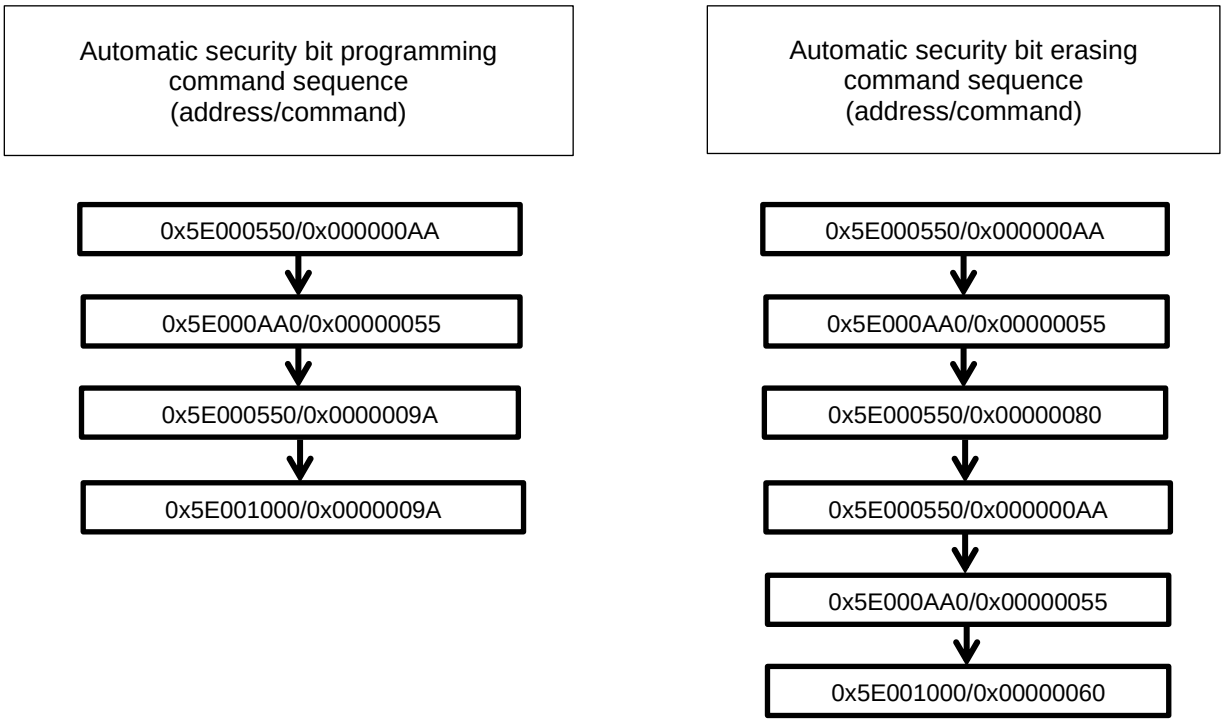

Figure 3.8 Flowchart of security (2)

3.3.5. Memory Swap

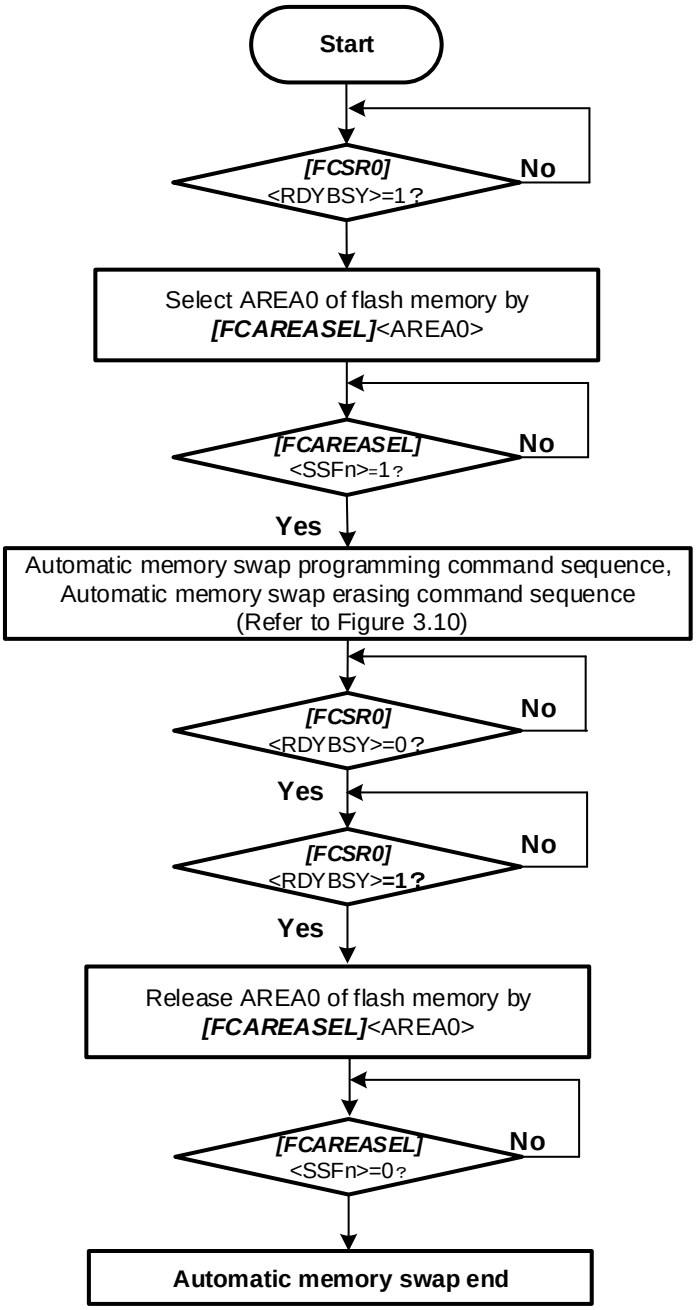

Figure 3.9 Flowchart of memory swap (1)

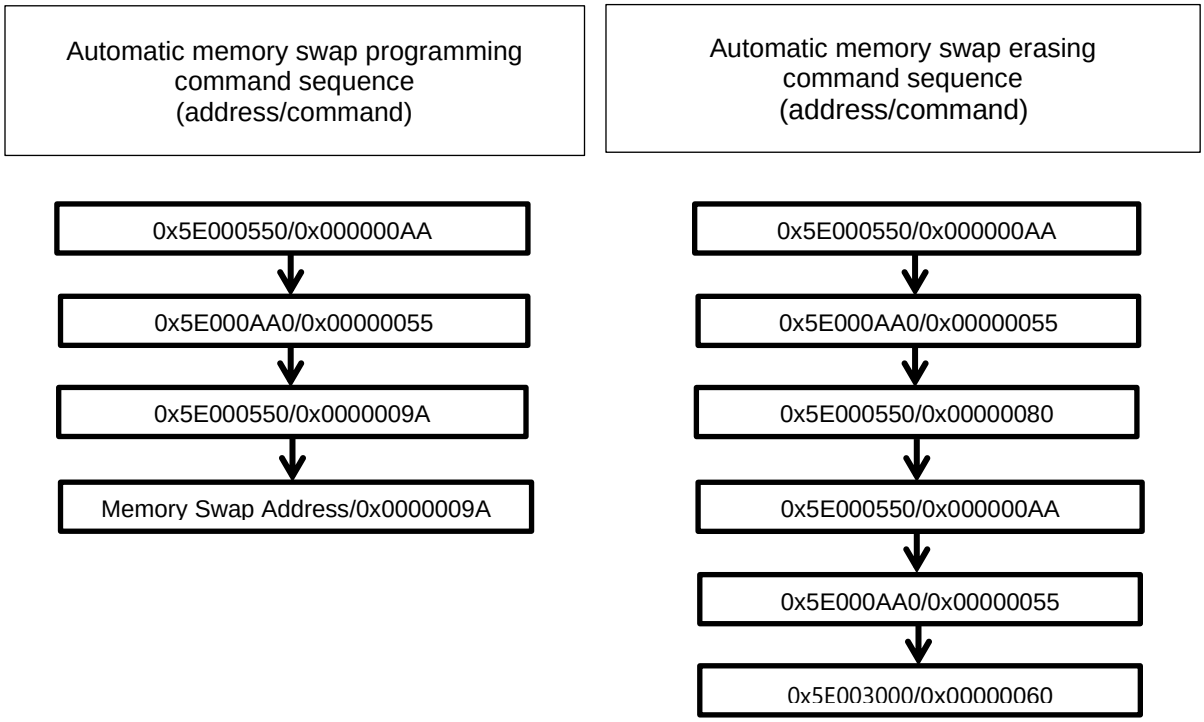

Figure 3.10 Flowchart of memory swap (2)

4. Details of Flash Memory

Flash memory is Programmed/erased data by executing a command in the control program. This programming/ erasing control program must be prepared by users in advance.

While a program is executing on a memory in area 0, another memory region (for example, <Area 4>: Data Flash) that is not operating can be erased or written and vice versa. This usage is called “dual mode” in this document.

4.1. Functions

Flash memory programming and erasing operation are generally compliant with the JEDEC standards commands except for some specific functions; however address assignment of an operational command is different from standard commands.

When programming/erasing operation is performed, a command is input to the flash memory with 32-bit (one word) store instruction. After the command is input, program or erase operation is internally automatically performed.

Table 4.1 Flash memory function

Main functions	Description
Automatic programming	Code flash: Program data in 4 words unit (16 bytes) automatically. Data flash: Program data in 1 word unit (4 bytes) automatically.
Automatic chip erasing	Erases the entire flash memory at one time automatically.(Note1)
Automatic code area erasing	Erases the flash memory in the code flash area automatically.
Automatic area erasing	Erases the flash memory in the unit of the area automatically.
Automatic block erasing	Erases the flash memory in the unit of the block automatically.(Note2)
Automatic page erasing	Erases the flash memory in the unit of the page automatically.
Automatic protect programming/erasing	Protects the flash memory from data program and erase operation.
Automatic security programming/erasing	Security setting to the flash memory and release security operation.
Automatic memory swap programming/erasing	Specifies memory swap, memory swap release, or swap size of the code flash area automatically.

Note1: Except user information area.
Note2: Block0 of code flash cannot be erased by one time. Please erase for every page by automatic page erasing command.

4.1.1. Operation Mode of the Flash Memory

The flash memory has three main operation modes:

- Read the memory data (Read mode)
- Input command for erasing/programming (Command sequence input mode)
- Erase/program data automatically (Automatic operation)

After power-on, or after reset, the flash memory or release area selection after normal end of automatic operation, enters read mode if the automatic operation is properly completed. Instructions described in the flash memory or data reading is executed in read mode.

The operation mode enters to Command sequence input mode after area setting. A command is inputted during this mode, the flash memory enters automatic operation mode. When a command processing is completed properly, the flash memory returns to read mode except the case that ID-Read command is handled. During the automatic operation mode, data reading or instruction on the flash memory cannot be executed.

4.1.2. Command Execution

A command is executed on the flash memory with the store instruction by inputting the command sequence after area setting. The flash memory executes an automatic operation command depending on the combination of input address and data. For details of command execution, refer to “4.1.3Command Description”.

A cycle where the store instruction is executed on the flash memory is called “bus write cycle”. Each command takes some bus write cycles. The flash memory executes automatic operation as long as the address and data in the bus write cycle are performed in the proper order. Otherwise, the flash memory aborts executing the command, and returns to read mode.

When the user attempts to cancel the command sequence in the middle of the process, or inputs the undefined command sequence, the flash memory executes the read/reset command to enter read mode. Then, tlash memory will return to read mode if area setting is released.

Note: Please perform cancellation until the 3rd bus cycle in an automatic program command, and until the last bus cycle in other commands.

When the command sequence is inputted completely, the flash memory starts the automatic operation and ***[FCSR0]***<RDYBSY>=0. When the automatic operation is completed properly, ***[FCSR0]***<RDYBSY> is set to "1"

Another command sequence is not accepted during automatic operation.
The following cautions should be exercised when executing a command.

1. Do not perform the operation below during the automatic operation:

   - Power shutdown
   - All exceptions (Recommend)

2. In order to recognize a command by the command sequencer, the flash memory must be in read mode before executing the command. Thus, confirm whether ***[FCSR0]***<RDYBSY>=1 before the flash memory entering command sequence input mode. And selecting area then execute the Read/Reset command.

3. Execute the following command sequences on the on-chip RAM.

   - Automatic chip erasing command
   - ID-Read command
   - Automatic security bit programming command
   - Automatic security bit erasing command
   - Automatic protect bit programming command
   - Automatic protect bit erasing command
   - Automatic memory swap command
   - Automatic memory swap erasing command

4. Set the area selection bit of the ***[FCAREASEL]*** register before executing each command. (Write "111" to <AREAn>).
   Note that when the following command is executed, set all area selection bits.

   - Automatic chip erasing command

5. Set each bus write cycle using consecutive 1-word (32-bit) data transfer instruction.

6. If an access is performed to the target Flash memory in each command sequence, a bus fault occurs.

7. When issuing commands, if wrong addresses or data are inputted, make sure to issue Read/Reset command, then return to command sequence input mode.

8. Confirmation procedure after each command completion is as follows:

   1) Execute the final bus write cycle
   2) Poll until ***[FCSR0]***<RDYBSY>=0(Busy).
   3) Poll until ***[FCSR0]***<RDYBSY>=1(Ready).

9. When data is read from the flash memory, clear the area selection bit of the ***[FCAREASEL]*** register. (Set <AREAn> to "000".)

When two or more flash memory areas are built-in, a command sequence other than the above can be used to write / erase in dual mode. For example, when there are area 0 and area 4, and the target flash memory to be programmed / erased is area 4, the program on the flash memory in area 0 can be executed to program / erase area 4(Reverse settings are possible).

In dual mode, interrupts can be used only when executing the instructions in area 0 to write / erase other areas.

4.1.3. Command Description

This section explains each command. For details of specific command sequences, refer to “3.1.1. Command Sequence” and “3.2.1. Command Sequence”.

4.1.3.1. Automatic Programming

(1) Operation

Code flash can be programmed in 4 words (16 bytes) unit with the automatic programming command sequence. Programming across 16 bytes is not possible. Data flash can be programmed in one word (four bytes) unit.

Programming data to flash memory means that data cells of “1” become those of “0”. It is not possible to become data cells of “1” from those of “0”. To become data cells of “1” from “0”, the erase operation is required.

The automatic programming command sequesnce is allowed only once to each programming address(4 words unit) already erased. Either data cells of “1” or “0” cannot be programmed data twice or more. If reprogramming to an address that has already been programmed once, the automatic program is needed to be set again after the automatic page erasing command sequesnce, automatic block erasing command sequesnce, or automatic chip erasing command sequesnce is executed.

Another command sequence is not accepted during automatic operation.
After programmed, flash memory returns to command sequence input mode.

Note1: Programming execute to the same programming unit twice or more without erasing operation may damage the data.
Note2: Programming/erasing to the protected block is not possible.

(2) How to set

The 1st to 3rd bus write cycles are the automatic programming command.
After the 4th bus write cycle, the first address and data are inputted. On and after 5th bus cycle, remaining data of four words will be inputted to code flash. Data flash is programmed in one word (32 bits) unit.

If a part of four words of code flash is used, program “0xFFFFFFFF” to the unused remaining part of four words.

If a part of one word of data flash is used, program “0xFF” to the unused remaining part of one word.

4.1.3.2. Automatic chip erasing

(1) Operation

Automatic chip erasing erases memory cells in all addresses. It erases in order of a data flash and a code flash. If protected pages or blocks are contained, the automatic chip erasing is performed on unprotected pages or blocks (Note1). After erased, flash memory returns to command sequence input mode.

Erasing target: Code Flash, Data Flash

Since protect bits are not erased, when erasing protect bits are required, please erase by an automatic protection bit erase command.

Another command sequence is not accepted during automatic operation. If the users attempt to stop the automatic chip erase, refer to “4.1.4Stopping Automatic Chip Erasing”. In this case, data may not be erased properly. Thus, the automatic chip erasing must be performed again.

(2) How to set

The 1st to 6th bus write cycles are the automatic chip erasing command sequences. After the command sequences are input, the automatic chip erasing starts.

Note 1: When there is the block or page protected, erasing operation is repeated per page inside a flash memory. It takes the time for the number of pages until erasing operation is completed.
Note 2: Automatic chip erasing cannot be performed continuously. When re-issuing the chip erasing command, a blank check is required.

4.1.3.3. to erased area

(1) Operation

The automatic area erasing command performs on the specified area. If protected pages or blocks are contained, the automatic area erasing is performed on un-protected pages or blocks (Note1). After erased, flash memory returns to command sequence input mode.

Another command sequence is not accepted during automatic operation.
After erased, flash memory returns to command sequence input mode.

(2) How to set

The 1st to 5th bus write cycles are the automatic area erasing command sequences. The area to be erased is specified in the 6th bus write cycle.
After the command sequences are input, the automatic area erasing starts.

Note 1: When there is the block or page protected, erasing operation is repeated per page inside a flash memory. It takes the time for the number of pages until erasing operation is completed.
Note 2: Automatic area erasing cannot be performed continuously. When re-issuing the chip erasing command, a blank check to erased area is required.

4.1.3.4. Automatic Block Erasing

(1) Operation

The automatic block erasing command performs on the specified block. When the specified block is included in the protected block, erasing is not executed and return to the command sequence input mode after the command sequence is input.

Another command sequence is not accepted during automatic operation.
After erased, flash memory returns to command sequence input mode.

(2) How to set

The 1st to 5th bus write cycles are the automatic block erasing command sequence. The block to be erased is specified in the 6th bus write cycle.
After the command sequences are input, the automatic block erasing starts.

4.1.3.5. Automatic Page Erasing

(1) Operation

The automatic page erasing command performs on the specified page. If protected page is contained, the automatic page erasing is not performed on this page. And flash memory returns to command sequence input mode.

Another command sequence is not accepted during automatic operation.
After erased, flash memory returns to command sequence input mode.

(2) How to set

The 1st to 5th bus write cycles are the automatic page erasing command sequences. The page to be erased is specified in the 6th bus write cycle.
After the command sequences are input, the automatic page erasing starts.

4.1.3.6. Automatic Protect Bit Programming

(1) Operation

The automatic protect bit programming sets the protect bit to “1” in the unit of bit. For clearing the protect bit to “0”, use the automatic protect bit erasing command.

For details of the protection function, refer to “4.1.6 Protection Function”.

Another command sequence is not accepted during automatic operation.
After programmed, flash memory returns to command sequence input mode.

(2) How to set

The 1st to 3rd bus write cycles are the automatic protect bit programming command sequences. The bit to be programmed is specified in the 4th bus write cycle.
After the command sequences are input, the automatic protect bit programming starts. Whether the protect bit is programmed normally, please check each bit of the ***[FCPSRn]***.

4.1.3.7. Automatic Protect Bit Erasing

(1) Operation

The automatic protect bit erasing command erases the protect bit regardless of the security state of the flash memory.

For details of the protection function, refer to “4.1.6Protection Function”.

Another command sequence is not accepted during automatic operation.
After erased, flash memory returns to command sequence input mode.

(2) How to set

Input a automatic protect bit erasing command sequence. After the command sequences are input, the automatic protect bit erasing starts.

All protect bits are erased at one time. Whether the protect bits are erased normally, please check the ***[FCPSRn]***.

4.1.3.8. Automatic Security Bit Programming

(1) Operation

The automatic security bit programming sets the security bit to “1”. For clearing the security bit to “0”, use the automatic security bit erasing command.

For details of the security function, refer to “4.1.7Security Function”.

Another command sequence is not accepted during automatic operation.
After programmed, flash memory returns to command sequence input mode.

(2) How to set

Input a security bit programming command sequence. After the command sequences are input, the automatic security bit programming starts. Security bit is enabled after system reset. When security is enabled, debugging tool cannot be connected.

4.1.3.9. Automatic Security Bit Erasing

(1) Operation

The operation of the automatic security bit erasing command varies depending on the security state of the flash memory.

- Non secured state (***[FCSBMR]*** <SMB> =0 and ***[FCSSR]*** <SEC> =1→0.)
  Erase the security bit to "0".

- Security state (***[FCSSR]***<SEC>=1)
  Erase all address of code flash and data flash, and erase security bit.

For details of the security function, refer to "4.1.7. Security Function".

Another command sequence is not accepted during automatic operation.
After erased, flash memory returns to command sequence input mode.

(2) How to set

Input security bit erasing command sequence. After the command sequences are input, the automatic security bit erasing starts.

In the case of a security state (***[FCSSR]*** <SEC>=1), in order to release security temporarily, clear ***[FCSBMR]*** <SMB> to "0". A security bit will be erased, when command sequence "automatic security bit erasing" is performed after checking that ***[FCSSR]***<SEC>= 0 is set. In order to check whether erasing has been performed normally, after a system reset, please set ***[FCSBMR]*** <SMB> =1 and read ***[FCSSR]*** <SEC>.

In security state, if the security bit erasing command sequenceis performed, data of all addresses of code flash, data flash and security bit are erased(note). In order to check whether erasing has been performed normally, after a system reset, please set ***[FCSBMR]*** <SMB> =1 and read ***[FCSSR]*** <SEC>. Please also check erasing the data of a code flash and a data flash. If necessary, execute the command sequence "Automatic protect bit erase" to erase protect bits.

Note: When performing the "Automatic security bit erase" command sequence, all areas must be selected with ***[FCAREASEL]***. If the all area are not specified, the "automatic security bit erase command sequence" will be ignored.

4.1.3.10. ID-Read

(1) Operation

The ID-Read command can read the information including the type of the flash memory. The information consists of a manufacturer code, device code, and macro code.

(2) How to set

The 1st to 3rd bus write cycles are the ID-Read command sequences. The ID address to be read is specified in the 4th bus write cycle. After the 4th bus write cycle, release area selection to read mode and input 5th bus cycle. Then, ID data is read from Flash.

If read other ID, input ID-read command sequence from 1st bus cycle again.

Note: After executed ID-read, the Read/Reset command must be executed.

4.1.3.11. Read/Reset Command

(1) Operation

This command is to enter the flash memory to command sequence input mode.

(2) How to set

The 1st bus write cycle is the Read/Reset command sequence. After the command sequence is executed, the flash memory returns to Command sequence input mode.

4.1.3.12. Automatic Memory Swap Programming

(1) Operation

The automatic memory swap sets each bit of ***[FCSWPSR]***<SWP0>, <SWP1> and <SIZE0> to <SIZE4> to "1" in the unit of bit. For clearing all bits to "0", use the automatic memory swap erasing command.

Another command sequence is not accepted during automatic operation.
After executed, flash memory returns to Command sequence input mode.

(2) How to set

The 1st to 4th bus write cycles are the automatic memory swap command sequences. After the command sequences are input, the designation bit of the ***[FCSWPSR]*** is set to "1". Whether the memory swap is programmed normally, please check each bit of the ***[FCSWPSR]***<SWP0>, <SWP1> and <SIZE0> to <SIZE4>.

4.1.3.13. Automatic Memory Swap Erasing

(1) Operation

The automatic memory swap erasing can erase ***[FCSWPSR]***<SWP0>, <SWP1> and <SIZE0> to <SIZE4> at one time.

Another command sequence is not accepted during automatic operation.
After executed, flash memory returns to command sequence input mode.

(2) How to set

Input a command sequence "Automatic memory swap erasing". After the command sequences are input, the automatic memory swap erasing starts. Whether the memory swap is erased normally, please check the ***[FCSWPSR]***<SWP0>, <SWP1> and <SIZE0> to <SIZE4>.

4.1.3.14. Precautions of executing automatic commands

Erasing/programming to multiple areas at the same time is prohibited. Similarly, the combination of protect bit and security bit is prohibited. Later commands will be ignored.

Example 1: Operation to program to code flash (area 0) at the same time while erasing data flash (area 4)

Example 2: Operation to program to the protect bit (area 0) of the code at the same time while erasing the data flash (area 4)

Example 3: Operation to erase data flash (area 4) at the same time while erasing code flash (area 0)

4.1.4. Stopping Automatic Chip Erasing

When the user attempts to cancel the automatic chip erasing in the middle of the process, cancel the automatic chip erasing as follows:

The flash memory returns to read mode.

1. Read ***[FCSR0]***<RDYBSY>.
2. If the result of Procedure 1 is “1” (Ready), end at Procedure 9. If the result is “0” (Busy), proceed to Procedure 3.
3. Write “0x7” to ***[FCCR]***<WEABORT>.
4. Write “0x0” to ***[FCCR]***<WEABORT>.
5. Poll until ***[FCSR0]***<RDYBSY>=1(Ready).
6. Read ***[FCSR1]***<WEABORT>
7. Issue the Read/reset command.
8. If the result of Procedure 6 is “0”, end at Procedure 9. If the result of Procedure 6 is “1”, perform the following operation to clear this flag:
    1) Write “0x7” to ***[FCSTSCLR]***<WEABORT>.
    2) Write “0x0” to ***[FCSTSCLR]***<WEABORT>.
    3) Poll until ***[FCSR1]***<WEABORT>=0.
9. End

Note**:** Before write to ***[FCCR]***, need to clear protection by ***[FCKCR]***.

4.1.5. Completion Detection of the Automatic Operation

The flash memory has an interrupt function to detect the completion of programming/erasing operation.

Table 4.2 Detection of Completion of programming/Erasing Flash

Item	Signal name	Interrupt name
Completion of the programming/erasing operation of a code flash	INTFLCRDY	Code FLASH Ready interrupt
Completion of the programming/erasing operation of a data flash	INTFLDRDY	Data FLASH Ready interrupt

When an automatic chip erasing command sequence is excecuted, INTFLDRDY is generated at the end of erasing the data flash first, and INTFLCRDY is generated at the end of erasing the code flash.

4.1.5.1. Procedure

The procedure (in the case of a data flash) which uses completion detection interrupt of automatic operation is as follows.

Please refer to chapter “Interrupts” of a reference manual “Exception” for the details of interrupt processing.

1. Enable INTFLDRDY interrupt.
2. After issued automatic programming or erasing command to a data flash, check under automatic operation (BUSY state) by ***[FCSR0]***<RDYBSY>.
3. An INTFLDRDY interrupt occurs after the end of automatic programming or erasing of data flash.
4. When you do not program in continuously, in an interrupt handler, disable INTFLDRDY interrupt, and perform return. When you program continuously, issue a new command sequence after INTFLDRDY interrupt without disable, and perform return.
5. When continuing program, repeat step3 to 4 in parallel performing a main process.

4.1.6. Protection Function

The protection function prohibits program/erase operation on the flash memory in the unit of block. The protection function is set for code flash and data flash separately.

In code flash, set the protection function to page 0 to 7 in the unit of page in block0. The remaining blocks are set in the unit of block. In data flash, the protection function is set in the unit of block.

Erasing protect setting, all protect bits are erased one time.

4.1.6.1. How to Set the Protection Function

In order to enable a protection function, a protect bit is set to “1” by a protect bit programming command.

The protection function is enabled under the condition below:

1. ***[FCPMRm]***<MSKn>=1 (Note)
2. Protect bit n=1

At this time, the block n is being protected from programming/erasing.
When check the status of protect bit, monitor ***[FCPSRm]*** after set ***[FCPMRm]***<MSKn>=1 .(Note)

Note: <MSKn> represents <PMn>, <MSKn>, and <DMSKn>.

4.1.6.2. Protection Release

Execute the protect bit erasing command, protect bits become “0” and being released block protection.

Note: All protect bits become “0” with the protect bit erasing command.

4.1.6.3. Protection Temporary Release Function

The protection function can be temporarilly released without erasing the protect bits.
Specified block can only be released.

When ***[FCPMRm]***<MSKn>=0, programming/erasing operation function is disabled regardless of the state of the protect bits.

For details of register settings, refer to ***[FCPMRm]*** in chapter "5.2 Detail of Register".

Note: <MSKn> represents <PMn>, <MSKn>, and <DMSKn>.

4.1.7. Security Function

The security function can disable data reading from the flash writer, and disable the debug function.

4.1.7.1. Security Setting

In order to enable a security function, a security bit is set to "1" by a security bit program command.
The security function is enabled under the following conditions:

1. ***[FCSBMR]***<SMB>=1
2. Security bit =1

When check the status of security bit, monitor ***[FCSSR]*** <SEC> after set ***[FCSBMR]***<SMB>=1.

Note: After security bit writing, security is enabled by system reset.

4.1.7.2. Security Setting Release

To release the security function, perform the procedure below:

1. ***[FCSBMR]***<SMB>=0
2. Set the security bit to "0" with the security bit erasing command.

While ***[FCSBMR]***<SMB>=1 and ***[FCSSR]***<SEC>=1, if the security bit erasing command is executed, the chip erasing function is executed, and then code flash, data flash, and security bits are erased.

Note: After security bit writing, security is enabled by system reset.

4.1.7.3. Operation

Table 4.3 shows the flash memory operation when the security function is enabled.

Table 4.3 Flash memory operation when the security function is enabled

Parameter	Description
Flash memory	Flash memory can be reading, programming by CPU.
Debug mode	Debugging is disabled.
Flash writer mode (Note)	Flash memory cannot be reading, programming.

Note: It is used by a gang writer etc. Specification is user nondisclosure.

4.1.8. Memory Swap Function

Application program reprogramming on the code flash may be suspended, for example, if the power becomes off after the program code is erased, application program reprogramming may not be continued. To avoid such a case, use this memory swap function to save your program.

4.1.8.1. Memory Swap Setting

A swap region starts from Address 0 and the same size next region. A swap size is determined by ***[FCSWPSR]*** <SIZE0> to <SIZE4>. To change the size, set the bit of corresponding size to "1" with the automatic memory swap programming command.

To perform memory swap, set ***[FCSWPSR]***<SWP0> to "1" with the automatic memory swap programming command. To release the swap condition, set ***[FCSWPSR]***<SWP1> to "1" with the automatic memory swap command or execute the automatic memory swap erasing command. A swap condition can be checked with ***[FCSWPSR]***<SWP0> and <SWP1>.

For details of the automatic memory swap command, refer to "4.1.3.12. Automatic Memory Swap Programming".

4.1.8.2. Memory Swap Operation

This section explains the basic operation flow of the memory swap. For the concrete example of the memory swap operation, refer to "6.8 How to Reprogram User Boot Program".

Release the protection function temporarily, when the protection function is valid.

For details of the protection function temporary release, refer to "4.1.6.3. Protection Temporary Release Function". If the protection function is not temporarily released, command execution is not performed in the procedure.

1. Check whether the area next to the area starting from Address 0 is blank. (The area starting from address 0 is called Page0, and the area following it is called Page1 to explain.) If not, erase the area.

   Page0: Old original data
   Page1: Blank

2. Program the original data starting from Address 0 to the next region. (Both regions have the same data.)

   Page0: Old original data
   Page1: Copied data (old original data)

3. Perform memory swap.

   Page0: Copied data (old original data)
   Page1: Old original data

4. Erase old original data to be blank.

   Page0: Copied data (Old original data)
   Page1: Blank

5. Program new data to the blank region.

   Page0: Copied data (Old original data)
   Page1: New original data

6. Release the swap state.

   Page0: New original data
   Page1: Copied data (Old original data)

7. Execute the automatic memory swap erasing command.

8. Options if required.

   - Erase copied data (old original data).
   - Reprogram the flash memory data except the swap regions.
   - Enable the protection function.
   - Enable the security function.

Procedure		1	2	3	4	5	6
On-chip RAM		Erase routine	Programming routine	Swap routine	Erase routine	Programming routine	Swap routine
Flash memory	Page0	Old original	Old original	Copy of old original	Copy of old original	Copy of old original	New original
	Page1	Blank	Copy of old original	Old original	Blank	New original	Copy of old original

Erase routine: A program is to erase Flash memory.
Programming routine: A program is to program Flash memory.
Swap routine: A program is to swap Flash memory.

Figure 4.1 Example of Procedure of Memory Swap

4.1.8.3. Erasing the Memory Swap Information

After the memory swap state is released, if the user attempts to perform memory swap again, initialize the all bits of the ***[FCSWPSR]*** register with the automatic memory swap erasing command.

4.1.9. User Information Area

Instructions cannot be executed in the user information area. Data reading can be instructed by the CPU.

Data becomes accessible on bank switching with ***[FCBNKCR]***. For address assignment, refer to "Table 2.6 User Information Area Configuration of Code Flash". After bank switching, do not access to code flash (Area 0).

Data in the user information area is not erased by the chip erasing command; therefore, it can be written the unique number for management.

User information area cannot be used with code flash (Area 0). Use this area exclusively.

4.1.9.1. Switching Procedure of the User Information Area

(1) Load the switching program on the RAM, and make Jump.
(2) Write "111" to ***[FCAREASEL]***<AREA0[2:0]> (Note)
(3) Write "111" to ***[FCBUFDISCLR]***<BUFDISCLR[2:0]>.
(4) Write "111" to ***[FCBNKCR]***<BANK0[2:0]>.
(5) Read ***[FCBNKCR]***<BANK0[2:0]> to confirm whether ***[FCBNKCR]***<BANK0[2:0]> is "111".
(6) Perform the following operation in the user information area:
Data reading, data programming, data erasing
(7) Write "000" to ***[FCBNKCR]***<BANK0[2:0]>.
(8) Read ***[FCBNKCR]***<BANK0[2:0]> to confirm whether ***[FCBNKCR]***<BANK0[2:0]> is "000".
(9) Write "000" to ***[FCBUFDISCLR]***<BUFDISCLR[2:0]>.
(10) Write "000" to ***[FCAREASEL]***<AREA0[2:0]> (Note)
(11) Return to the original program.

Note: When writing or erasing data, this procedure is necessary. And it is not necessary to read data.

4.1.9.2. Data programming Method for the User Information Area

Data on the user information area is programmed by same procedure of code flash (Area 0) by step (6) of "4.1.9.1".

4.1.9.3. Data Erasing Method for the User Information Area

Data on the user information area is erased by same procedure as page erase of code flash (Area 0) by step (6) of "4.1.9.1". All data are erased at one time.

4.1.10. Read buffer

The code flash has a built-in read buffer. The read buffer enables the code flash to be read at the fastest 1 clock.

The read buffer has a 256-bit length prefetch buffer: 2 stages, history buffer: 8 stages, and branch buffer: 32 stages.

4.1.10.1. Read buffer Operation

Figure 4.2 and Figure 4.3 show examples of operation when the read buffer is disabled and enabled, respectively.

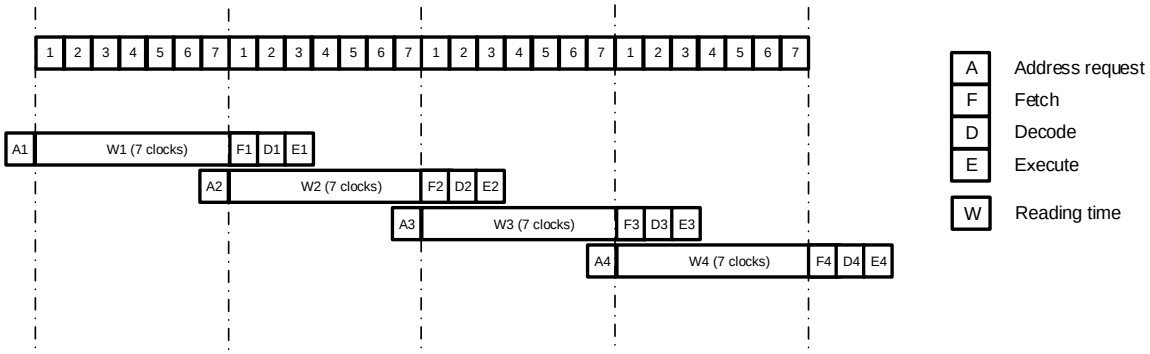

Figure 4.2 Example of operation without read buffer

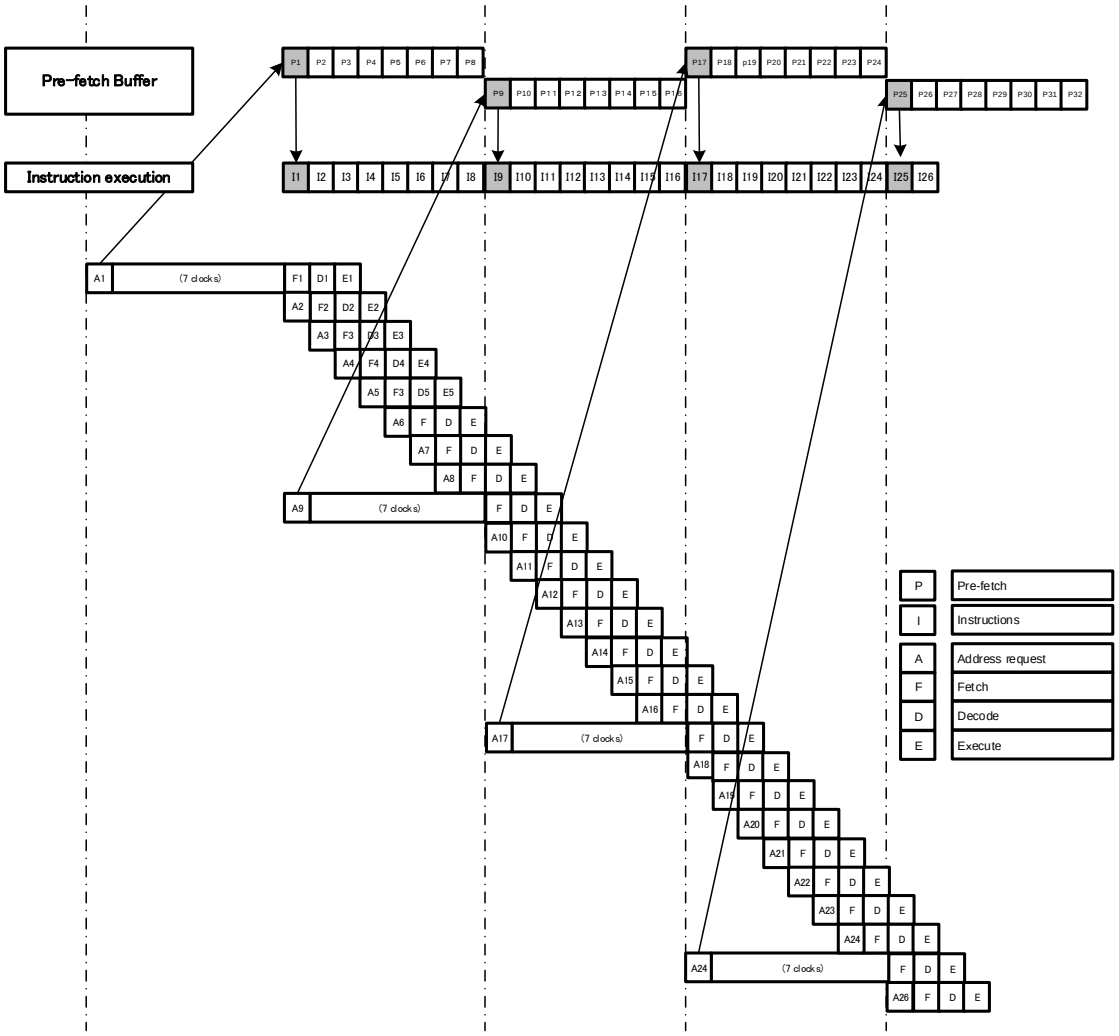

Figure 4.3 Example of operation with read buffer

5. Registers

5.1. Register List

The table below lists the registers related to flash memory.

Peripheral function		channel/unit	Base address
			Type 1
Flash Memory	FC	-	0x5DFF0000

Register name		Address (Base+)
Flash Security Bit Mask Register	***[FCSBMR]***	0x0010
Flash Security Status Register	***[FCSSR]***	0x0014
Flash Key Code Register	***[FCKCR]***	0x0018
Flash Status Register 0	***[FCSR0]***	0x0020
Flash Protect Status Register 0	***[FCPSR0]***	0x0030
Flash Protect Status Register 1	***[FCPSR1]***	0x0034
Flash Protect Status Register 6	***[FCPSR6]***	0x0048
Flash Protect Mask Register 0	***[FCPMR0]***	0x0050
Flash Protect Mask Register 1	***[FCPMR1]***	0x0054
Flash Protect Mask Register 6	***[FCPMR6]***	0x0068
Flash Status Register 1	***[FCSR1]***	0x0100
Flash Memory SWAP Status Register	***[FCSWPSR]***	0x0104
Flash Area Selection Register	***[FCAREASEL]***	0x0140
Flash Control Register	***[FCCR]***	0x0148
Flash Status Clear Register	***[FCSTSCLR]***	0x014C
Flash Bank Change Register	***[FCBNKCR]***	0x0150
Flash Access Control Register	***[FCACCR]***	0x0154
Flash Buffer Disable and Clear Register	***[FCBUFDISCLR]***	0x0158

Note: Do not access to the addresses where the registers are not assigned.

5.2. Detail of Register

5.2.1. *[FCSBMR]* (Flash Security Bit Mask Register)

Bit	Bit Symbol	After reset	Type	Function
31:1	-	0	R	Read as "0"
0	SMB	1	R/W	Security mask bit 1: Not masked 0: Masked (Security is temporarily released) When security is enabled (***[FCSSR]***<SEC>=1), if “0” is written to this register, security is temporarily released.

Note1: To rewrite this register, follow the procedure below:
1. Write the specific code (0xA74A9D23) to ***[FCKCR]***.
2. Rewrite the data of ***[FCSBMR]***<SMB> within 16 clocks after Procedure 1.

Note2: Do not rewrite this register while writing or erasing of flash memory.

Note3: This register is initialized by POR or PORF. For details of POR and PORF, refer to the “Reset and power control” chapter in the reference manual “Clock control and operation mode”.

5.2.2. *[FCSSR]* (Flash Security Status Register)

Bit	Bit Symbol	After reset	Type	Function
31:1	-	0	R	Read as “0”
0	SEC	0/1	R	Security status: Indicates security status. 1: Secured 0: Not secured The state of security is loaded by a system reset.

5.2.3. *[FCKCR]* (Flash Key Code Register)

Bit	Bit Symbol	After reset	Type	Function
31:0	KEYCODE	0x00000000	W	Locked register release key code When ***[FCSBMR]***, ***[FCPMRn]***, ***[FCCR]***, ***[FCAREASEL]*** are rewritten, write the specific code (0xA74A9D23) to this register. And then rewrite the value of the register within 16 clocks after the previous action. If valid data is written to this register within 16 clocks, released status is reset.

5.2.4. *[FCSR0]* (Flash Status Register 0)

Bit	Bit Symbol	After reset	Type	Function
31:11	-	0	R	Read as “0”
10	RDYBSY2	1	R	ReadyBusy flag of data flash area 0: In automatic operation 1: Completion of automatic operation
9	-	1	R	Read as “1”
8	RDYBSY0	1	R	ReadyBusy flag of code flash area 0: In automatic operation 1: Completion of automatic operation
7:1	-	0	R	Read as “0”
0	RDYBSY	1	R	ReadyBusy flag (all flash area) 0: In automatic operation 1: Completion of automatic operation ReadyBusy flag indicates automatic operation status when automatic programming command or automatic erasing command is executed. When this bit is “0”, it indicates that the flash memory is busy status where it is in automatic operation. When automatic operation is completed, this bit is set to “1”. It indicates ready status where the register can accept the next command.

5.2.5. *[FCPSR0]* (Flash Protect Status Register 0)

Bit	Bit Symbol	After reset	Type	Function
31:8	-	0	R	Read as “0”
7	PG7	0/1	R	Protect status of code flash. 1: Protected 0: Not protected This register indicates the protected status of each page from Page0 to Page7 (Block0). If one of bits is “1”, it indicates that the corresponding page is protected. Protected page cannot be erased or programmed. The state of protection is loaded by system reset.
6	PG6	0/1	R	
5	PG5	0/1	R	
4	PG4	0/1	R	
3	PG3	0/1	R	
2	PG2	0/1	R	
1	PG1	0/1	R	
0	PG0	0/1	R	

5.2.6. *[FCPSR1]* (Flash Protect Status Register 1)

Bit	Bit Symbol	After reset	Type	Function
31	BLK31	0/1	R	Protect status of code flash. 1: Protected 0: Not protected This register indicates the protected status of each block from Block1 to Block31. If one of bits is “1”, it indicates that the corresponding block is protected. Protected block cannot be erased or programmed. The state of protection is loaded by system reset.
30	BLK30	0/1	R	
29	BLK29	0/1	R	
28	BLK28	0/1	R	
27	BLK27	0/1	R	
26	BLK26	0/1	R	
25	BLK25	0/1	R	
24	BLK24	0/1	R	
23	BLK23	0/1	R	
22	BLK22	0/1	R	
21	BLK21	0/1	R	
20	BLK20	0/1	R	
19	BLK19	0/1	R	
18	BLK18	0/1	R	
17	BLK17	0/1	R	
16	BLK16	0/1	R	
15	BLK15	0/1	R	
14	BLK14	0/1	R	
13	BLK13	0/1	R	
12	BLK12	0/1	R	
11	BLK11	0/1	R	
10	BLK10	0/1	R	
9	BLK9	0/1	R	
8	BLK8	0/1	R	
7	BLK7	0/1	R	
6	BLK6	0/1	R	
5	BLK5	0/1	R	
4	BLK4	0/1	R	
3	BLK3	0/1	R	
2	BLK2	0/1	R	
1	BLK1	0/1	R	
0	-	0	R	Read as “0”

5.2.7. *[FCPSR6]* (Flash Protect Status Register 6)

Bit	Bit Symbol	After reset	Type	Function
31:8	-	0	R	Read as “0”
7	DBLK7	0/1	R	Protect status of data flash). 1: Protected 0: Not protected This register indicates the protected status of each block of data flash. If one of bits is “1”, it indicates that the corresponding block is protected. Protected block cannot be erased or programmed. The state of protection is loaded by system reset.
6	DBLK6	0/1	R	
5	DBLK5	0/1	R	
4	DBLK4	0/1	R	
3	DBLK3	0/1	R	
2	DBLK2	0/1	R	
1	DBLK1	0/1	R	
0	DBLK0	0/1	R	

5.2.8. *[FCPMR0]* (Flash Protect Mask Register 0)

Bit	Bit Symbol	After reset	Type	Function
31:8	-	0	R	Read as “0”
7	PM7	1	R/W	Protect mask status of code flash. 1: Not masked (Protected) 0: Masked (Not protected) This register masks each protected page from Page0 to Page7 (block0). This register is initialized by a system reset.
6	PM6	1	R/W	
5	PM5	1	R/W	
4	PM4	1	R/W	
3	PM3	1	R/W	
2	PM2	1	R/W	
1	PM1	1	R/W	
0	PM0	1	R/W	

Note1: To rewrite this register, follow the procedure below:
1. Write the specific code (0xA74A9D23) to ***[FCKCR]***.
2. Rewrite the data of ***[FCPMR0]***<PMn> within 16 clocks after Procedure 1.

Note2: Do not rewrite this register while writing or erasing of flash memory.

5.2.9. *[FCPMR1]* (Flash Protect Mask Register 1)

Bit	Bit Symbol	After reset	Type	Function
31	MSK31	1	R/W	Protect mask status of code flash. 1: Not masked (Protected) 0: Masked (Not protected) This register masks each protected block from Block 1 to Block 31 in the unit of block. This register is initialized by a system reset.
30	MSK30	1	R/W	
29	MSK29	1	R/W	
28	MSK28	1	R/W	
27	MSK27	1	R/W	
26	MSK26	1	R/W	
25	MSK25	1	R/W	
24	MSK24	1	R/W	
23	MSK23	1	R/W	
22	MSK22	1	R/W	
21	MSK21	1	R/W	
20	MSK20	1	R/W	
19	MSK19	1	R/W	
18	MSK18	1	R/W	
17	MSK17	1	R/W	
16	MSK16	1	R/W	
15	MSK15	1	R/W	
14	MSK14	1	R/W	
13	MSK13	1	R/W	
12	MSK12	1	R/W	
11	MSK11	1	R/W	
10	MSK10	1	R/W	
9	MSK9	1	R/W	
8	MSK8	1	R/W	
7	MSK7	1	R/W	
6	MSK6	1	R/W	
5	MSK5	1	R/W	
4	MSK4	1	R/W	
3	MSK3	1	R/W	
2	MSK2	1	R/W	
1	MSK1	1	R/W	
0	-	0	R	Read as “0”

Note1: To rewrite this register, follow the procedure below:
1. Write the specific code (0xA74A9D23) to ***[FCKCR]***.
2. Rewrite the data of ***[FCPMR1]***<MSKn> within 16 clocks after Procedure 1.

Note2: Do not rewrite this register while writing or erasing of flash memory.

5.2.10. *[FCPMR6]* (Flash Protect Mask Register 6)

Bit	Bit Symbol	After reset	Type	Function
31:16	-	0	R	Read as “0”
15:8	-	1	R/W	Write as “1”
7	DMSK7	1	R/W	Protect status of data flash. 1: Not masked (Protected) 0: Masked (Not protected) This register masks each protected block of data flash memory in the unit of block. This register is initialized by a system reset.
6	DMSK6	1	R/W	
5	DMSK5	1	R/W	
4	DMSK4	1	R/W	
3	DMSK3	1	R/W	
2	DMSK2	1	R/W	
1	DMSK1	1	R/W	
0	DMSK0	1	R/W	

Note1: To rewrite this register, follow the procedure below:
1. Write the specific code (0xA74A9D23) to ***[FCKCR]***.
2. Rewrite the data of ***[FCPMR6]***<DMSKn> within 16 clocks after Procedure 1

Note2: Do not rewrite this register while writing or erasing of flash memory.

5.2.11. *[FCSR1]* (Flash Status Register 1)

Bit	Bit Symbol	After reset	Type	Function
31:25	-	0	R	Read as “0”
24	WEABORT	0	R	When ***[FCCR]***<WEABORT>=111, this bit is set to “1”.
23:0	-	0	R	Read as “0”

5.2.12. *[FCSWPSR]* (Flash Memory SWAP Status Register)

Bit	Bit Symbol	After reset	Type	Function
31:13	-	0	R	Read as “0”
12	SIZE4	0/1	R	These bits indicate the setting of memory swap size. (Note3) Use one of the following settings. <SIZE0>: Page0 ←→ Page1 (4K bytes) <SIZE1>: Page0 to 1 ←→ Page2 to 3 (8K bytes) <SIZE2>: Page0 to 3 ←→ Page4 to 7 (16K bytes) <SIZE3>: Block0 ←→ Block1 (32K bytes) <SIZE4>: Area0 ←→ Area1 (512K bytes) (Note4) The state of memory swap size is loaded by system reset.
11	SIZE3	0/1	R	
10	SIZE2	0/1	R	
9	SIZE1	0/1	R	
8	SIZE0	0/1	R	
7:2	-	0	R	Read as “0”
1	SWP1	0/1	R	Swap setting <SWP0> and <SWP1> indicate the following states. <SWP1><SWP0> 00: Release the swap 01: Swap is ongoing 10: Prohibited 11: Release the swap The state of swap setting is loaded by system reset.
0	SWP0	0/1	R	

Note1: Perform memory swap on the program in the RAM.

Note2: To clear swap setting from <SWP1> <SWP0>=11 to 00, execute the automatic memory swap erase command. At this time, the swap size <SIZE0> to <SIZE4> is also cleared to “00000”. Perform this operation when the program is written in both of the memories to be swapped.

Note3: When changing the swap size <SIZE0> to <SIZE4> after setting, execute the automatic memory swap command to renew setting after the automatic memory swap Erase command is executed.

Note4: If the product memory size is 1MB, setting is allowed.

5.2.13. *[FCAREASEL]* (Flash Area Selection Register)

Bit	Bit Symbol	After reset	Type	Function
31	-	0	R	Read as “0”
30	SSF4	0	R	Selection of Area 4 1: Selects Area 4 (Data write mode) 0: Not select Area 4 (Data read mode)
29:28	-	0	R	Read as “0”
27	SSF1	0	R	Selection of Area 1 1: Selects Area 1 (Data write mode) 0: Not select Area 1 (Data read mode)
26	SSF0	0	R	Selection of Area 0 1: Selects Area 0 (Data write mode) 0: Not select Area 0 (Data read mode)
25:23	-	0	R	Read as “0”
22:20	-	000	R/W	Write as “000”
19	-	0	R	Read as “0”
18:16	AREA4[2:0]	000	R/W	Specify Area 4 of data flash as the target to enter to Command sequence input mode for data programming with flash memory operation commands. (Note1) 111: Selects Area 4. Others: Not select Area 4.
15	-	0	R	Read as “0”
14:12	-	000	R/W	Write as “000”
11	-	0	R	Read as “0”
10:8	-	000	R/W	Write as “000”
7	-	0	R	Read as “0”
6:4	AREA1[2:0]	000	R/W	Specify Area 1 of data flash as the target to enter to Command sequence input mode for data programming with flash memory operation commands. (Note1) 111: Selects Area 1 Others: Not select Area 1
3	-	0	R	Read as “0”
2:0	AREA0[2:0]	000	R/W	Specify Area 0 of code flash as the target to enter to Command sequence input mode for data programming with flash memory operation commands. (Note1) 111: Selects Area 0 Others: Not select Area 0

Note1: When rewrite <AREA0[2:0]>, <AREA1[2:0]> ,<AREA4[2:0]>, please perform the next operation the setting is reflected to the read data of <SSF0>,<SSF1>,<SSF4>.
Note2: Rewrite the contents of this register on the program code in the RAM.
Note3: To rewrite this register, follow the procedure below:
1. Write the specific code (0xA74A9D23) to ***[FCKCR]***.
2. Rewrite the data of ***[FCAREASEL]***<AREAn[2:0]> within 16 clocks after the previous action.
Note4: Do not rewrite this register while writing or erasing of flash memory.

5.2.14. *[FCCR]* (Flash Control Register)

Bit	Bit Symbol	After reset	Type	Function
31:3	-	0	R	Read as “0”
2:0	WEABORT[2:0]	000	R/W	Stops the automatic chip erasing. 111**:** Stops the automatic erasing operation. 000**:** Inactive Others: Prohibited

Note1: Rewrite the contents of this register on the program code in the RAM.

Note2: To rewrite this register, follow the procedure below:

1. Write the specific code (0xA74A9D23) to ***[FCKCR]***.
2. Rewrite data of ***[FCCR]***<WEABORT> within 16 clocks after Procedure 1.

5.2.15. *[FCSTSCLR]* (Flash Status Clear Register)

Bit	Bit Symbol	After reset	Type	Function
31:3	-	0	R	Read as “0”
2:0	WEABORT[2:0]	000	R/W	Clear ***[FCSR1]***<WEABORT> to “0” 111**:** Clears Others**:** Inactive

Note: Rewrite the contents of this register on the program code in the RAM.

5.2.16. *[FCBNKCR]* (Flash Bank Change Register)

Bit	Bit Symbol	After reset	Type	Function
31:7	-	0	R	Read as “0”
6:4	-	000	R/W	Write as “000”
3	-	0	R	Read as “0”
2:0	BANK0[2:0]	000	R/W	Aera “0x5E005000” to “0x5E005FFF” of code flash address change to the user information area. 111**:** User information area 000**:** Code Flash Others**:** Don’t care

Note1: Before and after BANK0 operation, code flash read buffer operation is required. For detail, refer to “5.2.18. ***[FCBUFDISCLR]*** (Flash Buffer Disable and Clear Register)”.

Note2: To set this register, write the value to the register, and confirm the written value by reading the register.

Note3: Rewrite the contents of this register on the program code in the RAM.

Note4: Do not access to code flash (Area0) except “0x5E005000” to “0x5E005FFF” while the user information area is being used.

Note5: Do not rewrite this register while writing or erasing of flash memory.

5.2.17. *[FCACCR]* (Flash Access Control Register)

Bit	Bit Symbol	After reset	Type	Function
31:11	-	0	R	Read as “0”
10:8	FDLC[2:0]	(Note3)	R/W	Read clock control for Data Flash 000: 1 clocks 001: 2 clocks 010: 3 clocks 011: 4 clocks 100: 5 clocks 101: 6 clocks 110: 7 clocks Others: Prohibited
7:3	-	0	R	Read as “0”
2:0	FCLC[2:0]	(Note3)	R/W	Read clock control for Code Flash 000: 1 clocks 001: 2 clocks 010: 3 clocks 011: 4 clocks 100: 5 clocks 101: 6 clocks 110: 7 clocks Ohters: Prohibited

Note1: Rewrite the contents of this register on the program code in the RAM.

Note2: To rewrite this register, follow the procedure below:

1. Write the specific code (0xA74A9D23) to ***[FCKCR]***.
2. Rewrite data of ***[FCACCR]***<FCLC[2:0]> within 16 clocks after Procedure 1.
3. After writing to the register, make sure that the written value can be read.

Note3: The initial value varies depending on the product. For details, refer to the reference manual "Product Information".

Note4: When using clock gear, set this register according to the maximum frequency in the application. Do not change the setting even if you lower the frequency with the clock gear.

Note5: Do not rewrite this register while writing or erasing of flash memory.

5.2.18. *[FCBUFDISCLR]* (Flash Buffer Disable and Clear Register)

Bit	Bit Symbol	After reset	Type	Function
31:3	-	0	R	Read as “0”
2:0	BUFDISCLR[2:0]	000	R/W	Stops the buffer of code flash, and clears the buffer. 111: Stops the buffer function and clears the buffer. 000: Start the buffer function. Others: Inactive When bank switch (***[FCBNKCR]***) is performed between code flash (Area 0) and user information area, make sure to stop and clear the buffer with this register before the switching starts. After the user information area is operated, make sure to write “000” to start the buffer operation.

Note1: When this register is set to the value, write the value to the register, and confirm the written value by reading the register.

Note2: Rewrite the contents of this register on the program code in the RAM.

Note3: Do not rewrite this register while writing or erasing of flash memory.

Note4: Do not excecute instruction on code flash under disable read buffer.

6. The programming method

6.1. Initialization

Before performing programming/erasing operation to a code flash or a data flash, an internal high speed oscillator1 (IHOSC1) must be oscillated. And, please operate flash memory after confirmin oscillation and ***[CGOSCCR]*** <IHOSC1F>=1. Also, And do not stop oscillation of internal oscillator1 (IHOSC1) while erasing/programming. Please refer to the reference manual “Clock Control and Operation Mode” for detail.

6.2. Mode Description

This device provides single chip mode and single boot mode. The single chip mode contains normal mode and dual mode. Please refer to Table 6.1 for detail.

Table 6.1 The mode and operation

Mode	Operation	
Single boot Mode	After reset is released, the built-in program of the Boot ROM (mask ROM) will be started. "The programming/erasing program code for a flash memory" can be downloaded from the host to on-chip RAM via UART of a communication function, and the “The programming/erasing program for a flash memory” can be run. Please refer to “6.6. How to Reprogram the Flash in Single Boot Mode”.	
Single chip Mode	Normal Mode	A user's application program is run. Moreover, an on-chip flash memory can be programed/erased a "flash memory programming/erasing program" in RAM. Although the operation can be applied to all the built-in flash memory, the user’s application program of the user on a flash memory cannot be run while programming/ erasing flash memory. Only this mode can be used when one area is built-in. Please refer to “6.5. How to Reprogram the Flash” for how to program/erase a flash memory.
	Dual Mode	While running a user's application program, erasing/programming the area different from the area on which the user's application program is running is also available. In case of built-in two or more areas of a code flash or data flash, this mode is available. Please refer to “6.7. How to Reprogram using Dual Mode” for how to program/erase a flash memory.

6.3. Mode Determination

The transition to the single chip and single boot modes is determined by the state of the BOOT_N pin when the reset is released by the RESET_N pin or Power On Reset (POR) is deasserted.

Table 6.2 Operation mode setting

Operation mode	Pin	
	RESET_N	BOOT_N
Single chip mode	0 → 1	1
Single boot mode	0 → 1	0
	(Note1)	0

Note1: Depending on the product, a power on reset (POR) can be used instead of the RESET_N pin. For details, refer to reference manual "Product Information" and section "Reset and Power Control" of "Clock Control and Operation Mode".
Note2: Refer to “6.6. How to Reprogram the Flash in Single Boot Mode” for setting, such as selection of UART in single boot mode.

6.4. Memory Map in Each Mode

Refer to “Figure 1.1 The example of a memory map (1024KB)”.

6.5. How to Reprogram the Flash

The user boot mode reprograms the flash memory using the program in the on-chip RAM on the user’s set. This mode is used when the data transfer bus for the flash memory program code on the user application is not use UART or use diffrent channel of UART in single boot. It operates in single chip mode; therefore, normal mode, in which user application is activated in single chip mode, needs to switch to user boot mode for programming flash memory. For that reason, the user is required to add a mode judgment routine to the reset service routine in the user application program.

This mode switch condition is required to be constructed according to the user system set condition. A flash memory programming routine, which is uniquely made by the user, needs to be installed in the new application. This routine is used for programming after being switched to the user boot mode. It is recommended that program/erase protection should be set to the necessary block to avoid accidental modification in single chip mode (normal operation mode) after reprogramming is completed. Make sure not to generate any exception in user boot mode.

The following section explains two procedures where the reprogramming routine stored in Flash memory (1-A) and the reprogramming routine is transferred from the external device (1-B). For details of the programming/erasing the flash memory, refer to “4 Details of Flash Memory”.

6.5.1. (1-A) Procedure that a Programming Routine Stored in Flash memory

6.5.1.1. Step-1

A user determines the conditions (e.g., pin status) to enter the user boot mode and the I/O to be used to transfer data. Then suitable circuit design and program are created. Before installing the device on a printed circuit board, program the following three program routines into an arbitrary flash block using programming equipment such as a flash writer.

(a) Mode determination routine: A program to determine to switch to user boot mode.
(b) Copy routine: A program to copy the data described in (c) to the on-chip RAM.
(c) Flash programming routine: A program to download new program from the external device and reprogram Flash memory.

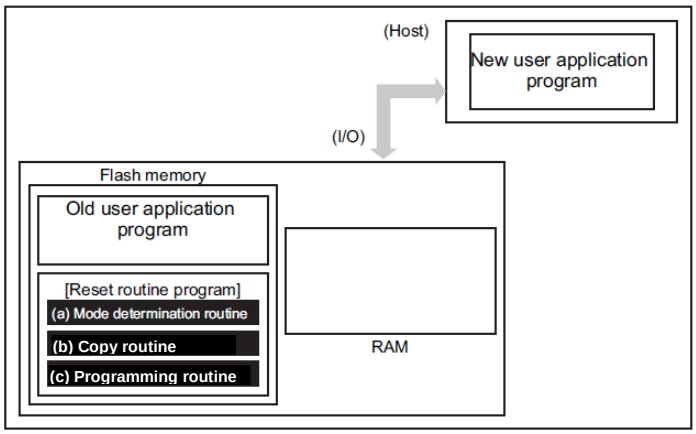

Figure 6.1 Procedure that a Programming Routine Stored in Flash memory (1)

6.5.1.2. Step-2

This section explains the case that a programming routine is stored in the reset service routine. First, the reset routine determines to enter the user boot mode. If mode switching conditions are met, the device enters the user boot mode to reprogram data. (Make sure not to generate any exception in user boot mode.)

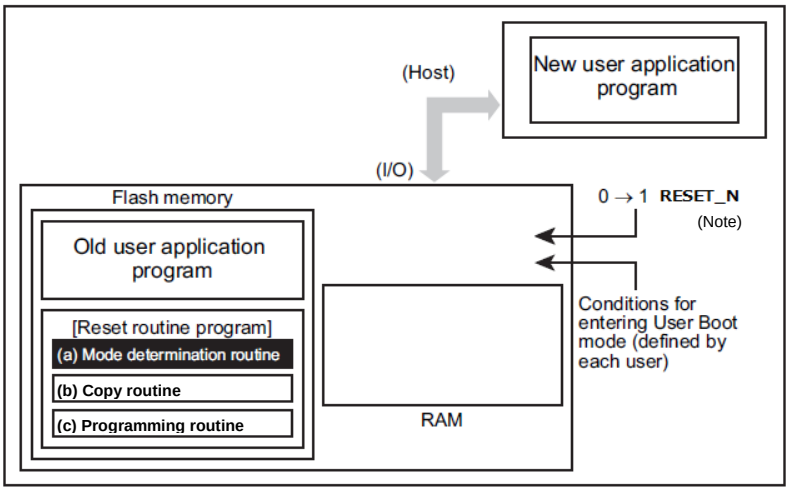

Figure 6.2 Procedure that a Programming Routine Stored in Flash memory (2)

Note: Depending on the product, a power on reset (POR) can be used instead of the RESET_N pin. For details, refer to reference manual "Product Information" and section "Reset and Power Control" of "Clock Control and Operation Mode".

6.5.1.3. Step-3

After the device enters the user boot mode, the device executes the copy routine (b) to download the flash programming routine (c) from the the flash memory to the on-chip RAM.

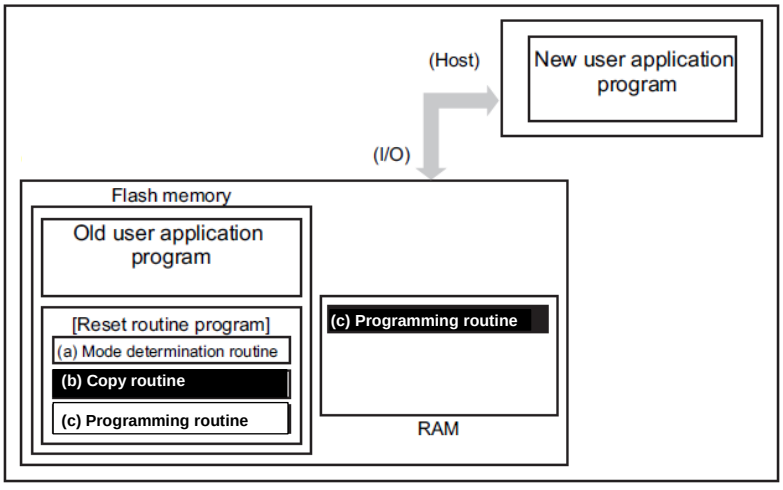

Figure 6.3 Procedure that a Programming Routine Stored in Flash memory (3)

6.5.1.4. Step-4

The device jumps to the programming routine (c) on the RAM to release the program/erase protection for the old application program, and to erase the flash (the units of erase is arbitrary size).

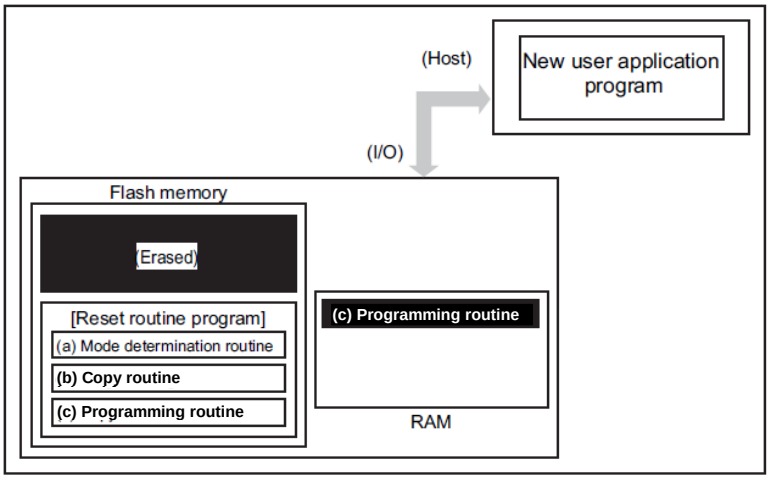

Figure 6.4 Procedure that a Programming Routine Stored in Flash memory (4)

6.5.1.5. Step-5

The device continues to execute the flash programming routine to download new program data from the host controller and program it into the erased flash block. When the programming is completed, set the program/erase protection of that user program area to ON.

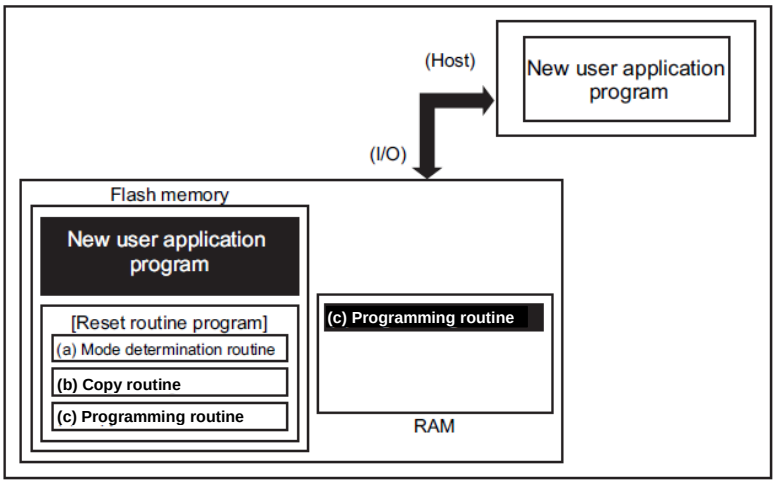

Figure 6.5 Procedure that a Programming Routine Stored in Flash memory (5)

6.5.1.6. Step-6

Upon reset, the flash memory is set to normal mode. After reset, the CPU will start operation along with the new application program.

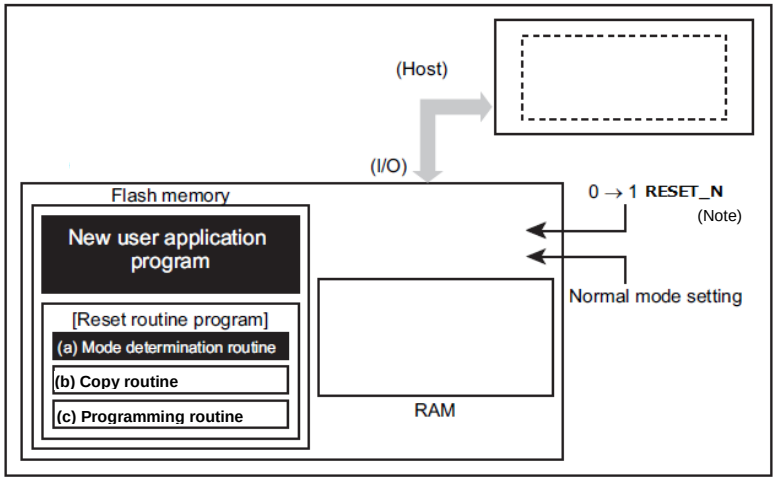

Figure 6.6 Procedure that a Programming Routine Stored in Flash memory (6)

Note: Depending on the product, a power on reset (POR) can be used instead of the RESET_N pin. For details, refer to reference manual "Product Information" and section "Reset and Power Control" of "Clock Control and Operation Mode".

6.5.2. (1-B) Procedure that a Programming Routine is Transferred from External Host

6.5.2.1. Step-1

The user determines the conditions (e.g., pin status) to enter user boot mode, and determines I/O used in data transfer. Then suitable circuit design and program are created. Before installing the device on a printed circuit board, program the following two program routines into an arbitrary flash block using programming equipment such as a flash writer.

(a) Mode determination routine: A program to determine to switch to reprogramming operation
(b) Transfer routine: A program to obtain a programming program (c) from the external device.

The programming routine shown below must be prepared on the host controller.

(c) Programming routine: A program to reprogramming data

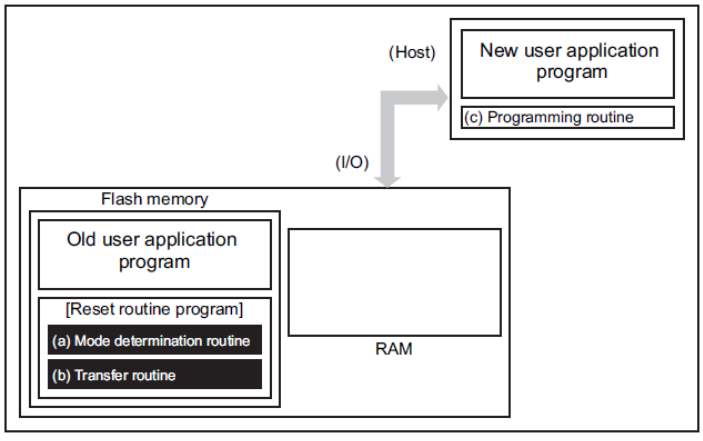

Figure 6.7 Procedure that a Programming Routine is Transferred from External Host (1)

6.5.2.2. Step-2

This section explains the case where a programming routine is stored in the reset service routine.

First, the reset service routine determines to enter user boot mode. If mode switching conditions are met, the device enters user boot mode to reprogram data. (Make sure not to generate any exception in user boot mode.)

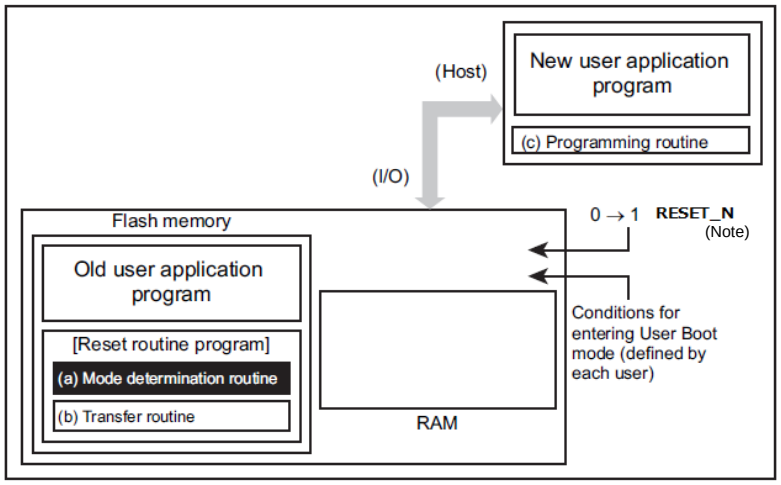

Figure 6.8 Procedure that a Programming Routine is Transferred from External Host (2)

Note: Depending on the product, a power on reset (POR) can be used instead of the RESET_N pin. For details, refer to reference manual "Product Information" and section "Reset and Power Control" of "Clock Control and Operation Mode".

6.5.2.3. Step-3

After the device enters user boot mode, the device executes the transfer routine (b) to download the flash programming routine (c) from the host controller to the on-chip RAM.

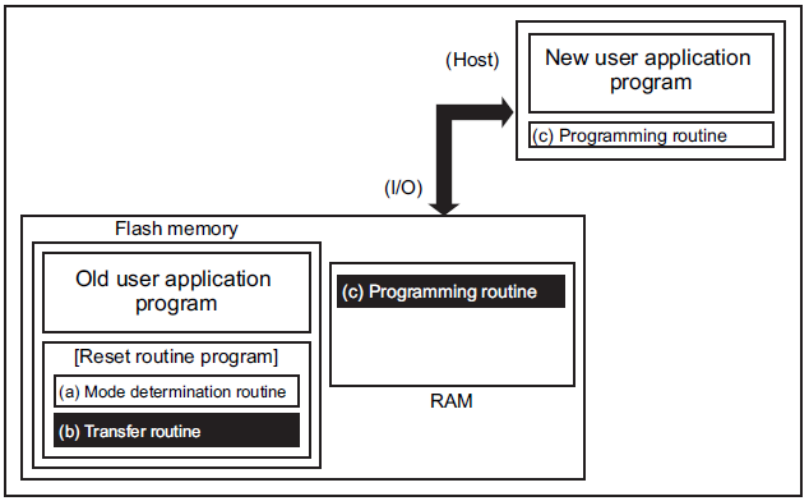

Figure 6.9 Procedure that a Programming Routine is Transferred from External Host (3)

6.5.2.4. Step-4

The device jumps to the programming routine on the RAM to release the program/erase protection for the old application program, and to erase the flash (the units of erase is arbitrary size).

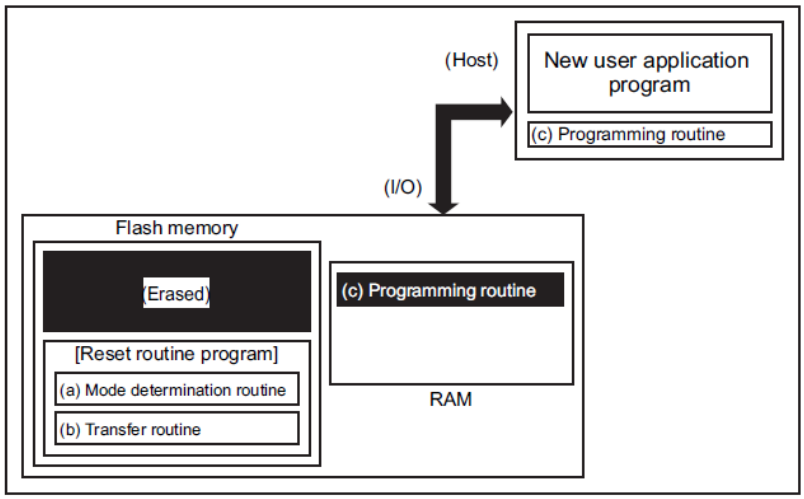

Figure 6.10 Procedure that a Programming Routine is Transferred from External Host (4)

6.5.2.5. Step-5

The device continues to execute the programming routine (c) on the RAM to download new program data from the host controller and programs it into the erased flash blocks. When the programming is completed, set the program/erase protection of that flash area in the user's program to ON.

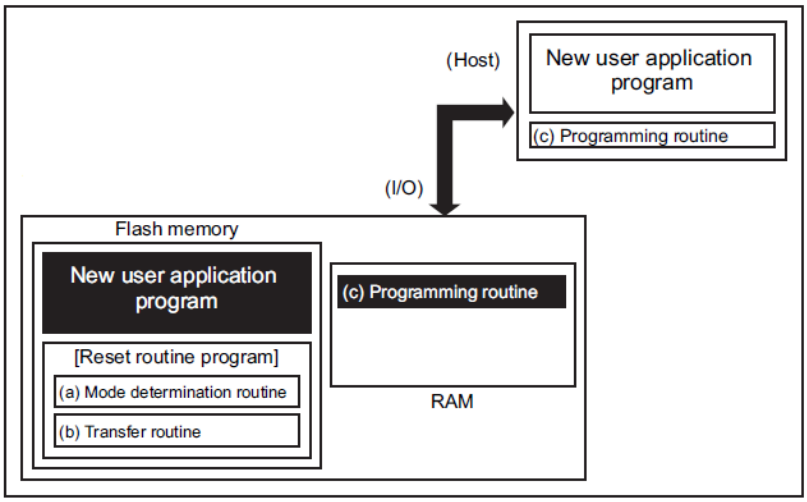

Figure 6.11 Procedure that a Programming Routine is Transferred from External Host (5)

6.5.2.6. Step-6

The flash memory is set to normal mode by reset. After reset, the CPU will start operation along with the new application program.

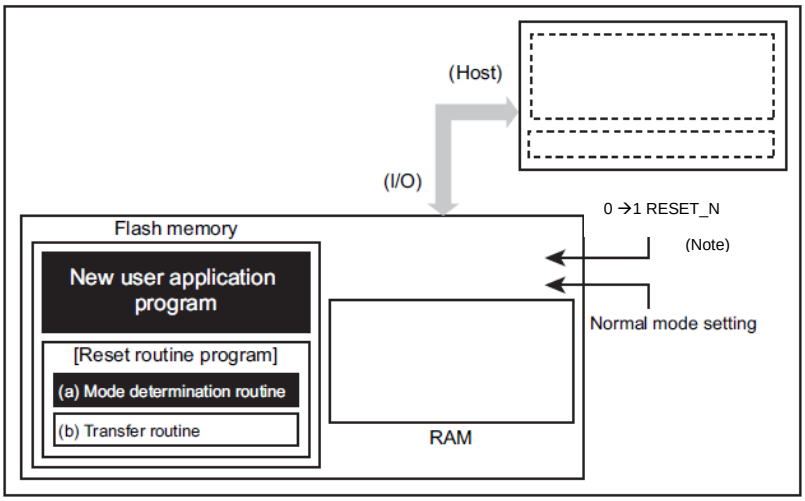

Figure 6.12 Procedure that a Programming Routine is Transferred from External Host (6)

Note: Depending on the product, a power on reset (POR) can be used instead of the RESET_N pin. For details, refer to reference manual "Product Information" and section "Reset and Power Control" of "Clock Control and Operation Mode".

6.6. How to Reprogram the Flash in Single Boot Mode

6.6.1. Single Boot Mode

The single boot mode utilizes a program contained in on-chip Boot ROM for reprogramming the flash memory. In this mode, the Boot ROM is mapped to the area containing interrupt vector tables, and the flash memory is mapped to another address area other than the Boot ROM area.

In the single boot mode, the flash memory is reprogrammed by the commands and data on serial transfer.

Table 6.3 Functions and Commands

Functions /Commands	Basic Operation	Description	Comment /Refer section
Communication function	Communication equipment	Use UART	
	Communication Rate	The signal sent at the rate beforehand decided from the external host controller is analyzed, and a communication rate is set up automatically.	"Table 6.7 Setting of baud rate in Single boot mode (fc=10MHz, No error)"
RAM Transfer Command	Transfer to on-chip RAM	Using communication function, a programming routine is copied from the external host device to the on-chip RAM. A programming routine on the RAM is executed to erase/ program the flash memory.	
	Password	Any data (255 bytes) in the flash memory can be used as a password. If password match fails, error is generated and RAM transfer stops.	A part of user memory is used for password.
Flash memory erasing command	Flash memory erasing	Erases on-chip flash memory except user information area, regardless of a program/ erase protect condition or security status, without a password.	Erasing for; Data Flash Code Flash Protect bits Memory swap bits Security bit

UART (Note) of a target (microcontroller) and the external host controller (hereafter controller) are connected. The "flash reprogramming program" sent from the controller is stored in on-chip RAM. The "flash reprogramming program" on RAM is run, and a flash memory is reprogrammed.

For the details of communication with the controller, see the below mentioned protocol.

In single boot mode, do not generate all exceptions to avoid abnormal program termination.

To protect the contents of the flash memory in single chip mode (normal operation mode), it is recommended to protect relevant flash blocks against accidental erasure after reprogramming is complete.

Note: For detail of UART, please refer to reference manual "Asynchronous Serial Communication Circuit".

6.6.2. Mode Setting

In order to execute the on-board programming, boot up this device in single boot mode. For details of single boot mode setting, refer to “6.3. Mode Determination” and “6.6.3. Interface Specifications”.

6.6.3. Interface Specifications

The single boot mode supports serial communication interface by UART.
Each interface specification is shown below.

6.6.3.1. Communicate by UART

Communication channel:	UART channel x (depends on the product)
Serial transfer mode:	UART (asynchronous communication) mode, half-duplex communication, LSB-first
Data length:	8 bits
Parity bit:	None
STOP bit:	1 bit
Baud rate:	Arbitrary baud rate (Table 6.7 Setting of baud rate in Single boot mode (fc=10MHz, No error))
WDT:	Stops

The clock/mode control block setting of the internal boot program operates on the initial settings(fc=10MHz, Clock is supplied to using function blocks).

A baud rate is determined by the timer counter mentioned in “6.6.7.1 Serial Operation Mode Determination”. At this time, a baud rate needs to be within the measurable range by the timer.

The pins used in the internal boot program are shown in “Table 6.4 Used pins (UART)”. Other pins are not operated in the boot program.

Table 6.4 Used pins (UART)

Category	Pin name	Setting
Mode setting pin	MODE	0
	BOOT_N	0
Reset pin	RESET_N	0→1
Communication pins	UTxTXD (Note1)(Note2)	-
	UTxRXD(Note1)(Note2)	-

Note1: Setting pins and UART channels to be used vary depending on the product. For details, refer to reference manual “Product Information”.

Note2: When two UART pins exist in the same channel and assigned both for single boot mode, either UART pin connected with the host device is automatically detected at start-up in single boot mode. The RXD pin not used in the channel is set to OPEN or fixed to “High” level. Do not connect both UART pins to the host device at the same time.

For details of UART assignment, refer to reference manual “Product Information”.

6.6.4. General flowchart of the internal boot program

The general flow chart of the internal boot program is shown.

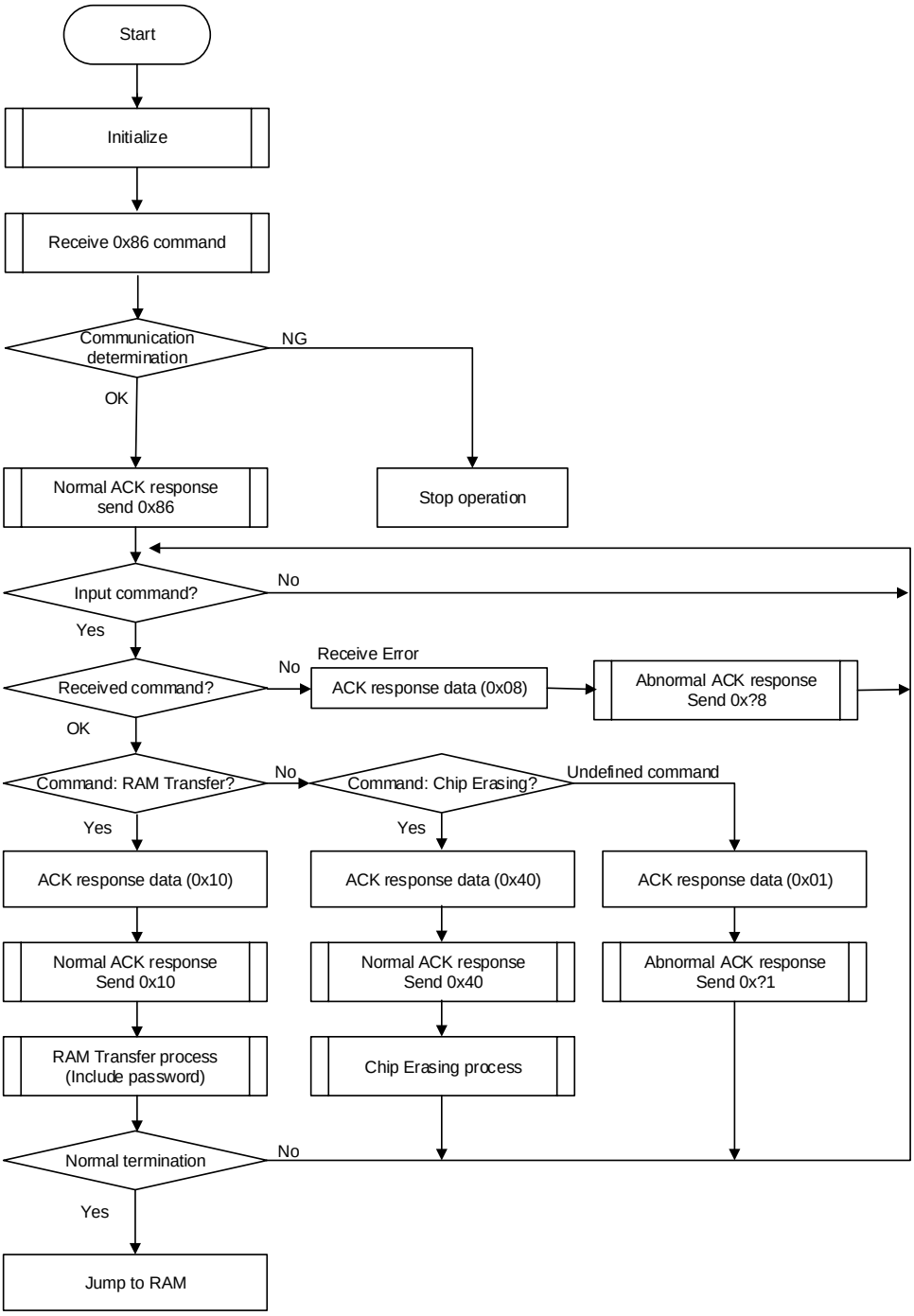

Figure 6.13 General flowchart of internal boot program

6.6.5. Restrictions on Memories

Note that the single boot mode places restrictions on the on-chip RAM and on-chip flash memory as shown in “Table 6.5 Restrictions on the memories in single boot mode”.

Table 6.5 Restrictions on the memories in single boot mode

Memory	Restrictions
On-chip RAM	Boot program uses the memory as a work area through “0x20000000” to “0x200003FF”. Store the program from “0x20000400” through the end address which can be transmitted. For the last transfer address available, refer to reference manual “Product Information”.
Internal flash memory	From “0x5E001000” up to the (maximum capacity) of Code flash can be used as the password area. Data flash cannot be used as the password area.

6.6.6. Operation Command

The boot program provides the following operation commands:

Table 6.6 Operation commands in single boot mode

Operation command data	Operation mode
0x10	RAM transfer
0x40	Flash memory erasing

6.6.6.1. RAM transfer

The RAM transfer is to store data from the controller to on-chip RAM. When the transfer is complete normally, a user program starts. The memory address of “0x20000400” or later can be used for a user program except “0x20000000” to “0x200003FF” where the addresses are used for the boot program. The execution start address means the start address to store data in the RAM.

This RAM transfer function can perform user's own on-board programming control. In order to execute the on-board programming by a user program, refer to “6.5. How to Reprogram the Flash”.

6.6.6.2. Flash Memory Erasing

The flash memory erasing command erases the entire blocks of the flash memory except the user information area. This command erases data flash, code flash, protect bits, and security bit regardless of a program/erase protect condition or security status, without a password.

A user information area cannot be erased by the flash memory erasing command. If a user would like to erase this area, execute this command and then perform the RAM transfer to execute the user information area erasing program.

6.6.7. Common Operation Regardless of the Command

This section describes common operation under the boot program execution condition.

6.6.7.1. Serial Operation Mode Determination

The controller must send “0x86” on the 1st byte at the desired baud rate in Table 6.7. If communication is impossible, please set lower baud rate.

Table 6.7 Setting of baud rate in Single boot mode (fc=10MHz, No error)

Baud Rate (Calculation)	<BRN>	<BRK>
9600 (9599)	65	57
19200 (19203)	32	29
38400 (38388)	16	46
57600 (57637)	10	10
62500 (62500)	9	0
76800 (76923)	8	55
115200 (115274)	5	37
128000 (127796)	4	7

6.6.7.2. Acknowledgement Response Data

The internal boot program shows processing states in specific codes and sends them to the controller. From “Table 6.8 ACK response data corresponding to serial operation determination data” to “Table 6.11 ACK response data corresponding to flash memory erasing operation”, ACK response data corresponding to each receive data is shown.

The upper four bits of ACK response data are equal to the upper four bits of the operation command data. The bit 3 indicates a receive error. The bit 0 indicates an invalid operation command error, a checksum error or a password error. The bit 1 and bit 2 are always “0”.

Table 6.8 ACK response data corresponding to serial operation determination data

Transmit data	Meaning
0x86	Determined that UART communication is possible. (Note)

Note: If it is determined that the UART baud rate cannot be set, the operation is stopped without sending anything.

Table 6.9 ACK response data corresponding to operation command data

Transmit data	Meaning
0x?8(Note)	A receive error occurs in the operation command data.
0x?1(Note)	An undefined operation command data is received normally.
0x10	Determined as a RAM transfer command.
0x40	Determined as a flash memory erasing command.

Note: The upper 4 bits of the ACK response data are the same as those of the previous command data.

Table 6.10 ACK response data corresponding to CHECKSUM data

Transmit data	Meaning
0xN8(Note)	A receive error occurred in the operation command data.
0xN1(Note)	A CHECKSUM error or password error occurred.
0xN0(Note)	The CHECKSUM value was determined as correct value.

Note: The upper 4 bits of the ACK response data are the same as the operation command data.

Table 6.11 ACK response data corresponding to flash memory erasing operation

Transmit data	Meaning
0x54	Determined as a flash memory erase command.
0x4F	Erase command completed.
0x4C	Erase command completed illegally.
0x47	Erase command was aborted.

6.6.7.3. Password

Any data (a part of user memory) in the flash memory can be used as a password. Once the password is set, RAM transfer command need password authentication.

(1) Mechanism of Password

Arbitrary data in the flash memory can be set as a password. And the password is authenticated by comparing the password string sent from the external controller with the TXZ + memory data string in which the password is specified.

(2) Password Communication Data Configuration

A password communication data is comprised of four elements: PLEN, PNSA, PCSA, and a password string (password). For detail, refer to “Figure 6.14 Password communication data configuration (Example of Transmission)”.

・PLEN (Password length data)

The length of a password is specified to “0xFF”.

・PNSA (Password length storage address)

The storage address of password length is specified in four bytes. Data of specified address is “0xFF”. A password error occurs when address data of PNSA is not “0xFF”.

・PCSA (Password compare start address)

The Password compare start address is specified in four bytes. Specified address is the start address to be compared with the password string. Specify PCSA so that sequential data of 255 bytes is in code flash area. If the specified address by PCSA is out of range from code flash, a password address error occurs.

・Password string

Use 255 bytes data. Memory data and password string are compared on the number of 255 bytes where the start address is specified by PCSA. If the comparison result is not matched, a password error occurs. And the same data over 3 bytes are sequentially detected, a password area error occurs.
The password is verified even when the security function is enabled.

・Password error

When it is determined that there is a password address error or password area error, "0x11" is sent for ACK regardless of the verification result of the password data. If it is judged as a password error, the ACK response will be a password error.
If a password error occurs, the external device will no longer be able to communicate with the TXZ+. To restart communication, reset from the reset pin (RESET_N) and restart single boot mode.

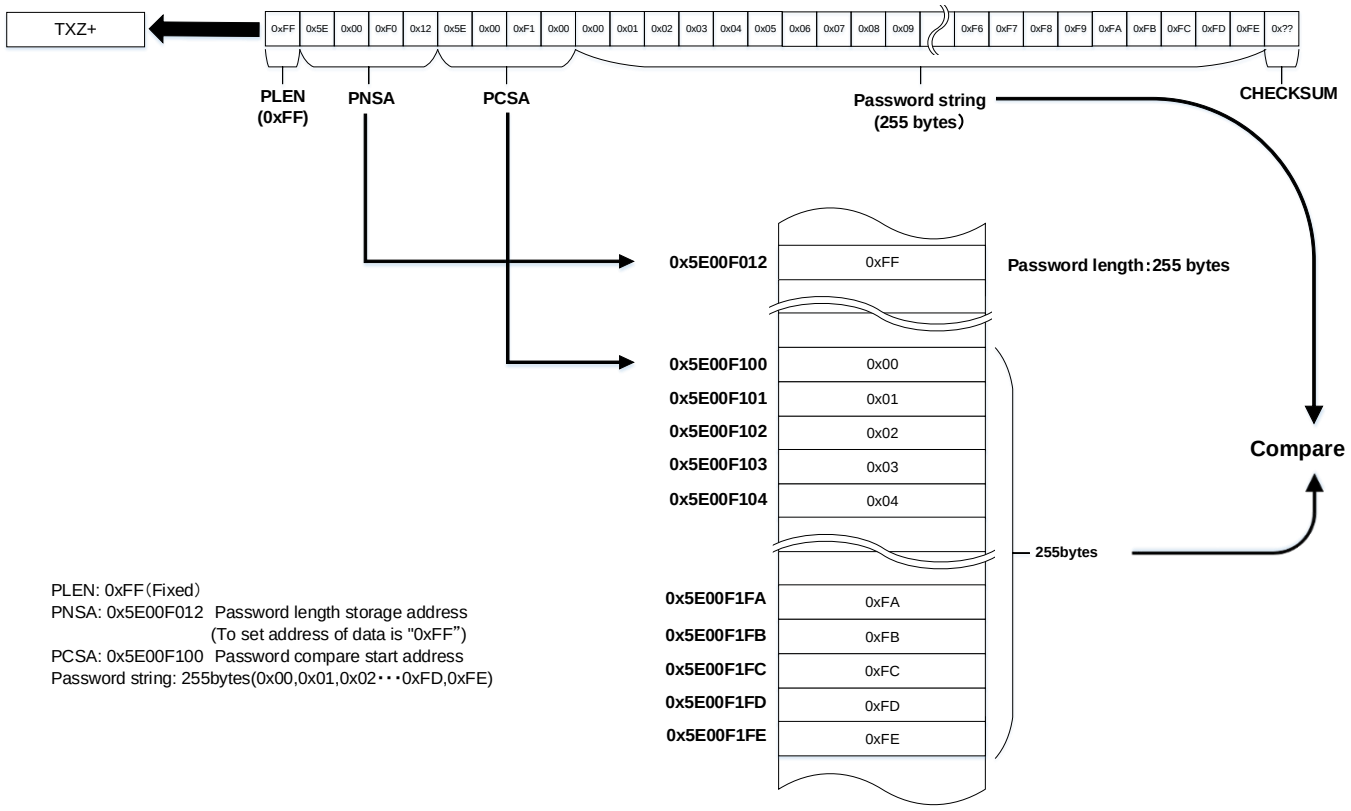

Figure 6.14 Password communication data configuration (Example of Transmission)

(3) Password Setting/Releasing/Verification

・Password setting

Password system uses a part of a user program. Therefore, special process is not required for password setting. At the time when a program is programmed to the code flash, a password is set.

・Password releasing

To release a password, chip erasing (entire erasing) of code flash (except user information area) and of data flash are required. A password is released at the time when the entire area of code and data flash are initialized to "0xFF".

・The case where password verification is unnecessary.

When the entire area of the code flash and data flash are "0xFF", the product is determined as a blank product. At this time, password verification is not performed.

For example, even if code flash area is all "0xFF" a password error occurs as long as data remains in data flash. In this case, perform chip erasing.

(4) Password Setting Values and Setting Ranges

A password must be set according to the condition described inTable 6.12. Unless the condition is met, a password error occurs.

Table 6.12 Password setting values and setting ranges

Password	Blank product	Non blank product
PNSA range (Address where the password length is stored)	Necessary (Note 2)	0x5E001000 ≤ PNSA ≤ Maximum memory address
PCSA range (Address where the start address used for password comparison)	Necessary (Note 2)	0x5E001000 ≤ PCSA ≤ Maximum memory address-254
Password length	Necessary (Note 2)	255
Password input (Note1)	Necessary (Note 2)	Necessary (Note 3)
Password range	N/A	0x5E001000 ≤ PNSA ≤ Maximum memory address

Note1: 255 bytes data must be sent when communication.

Note2: Please send the dummy PLEN, PNSA, PCSA and password string for blank products.

Note3: Over the three bytes consecutive and same data cannot be used as a password string.

6.6.7.4. CHECKSUM Calculation

The CHECKSUM is calculated by 8-bit addition (ignoring the overflow) to transmit data and taking the two's complement of the sum of lower 8 bits. Use this calculation when the controller transmits the CHECKSUM value.

Example calculation of CHECKSUM

To calculate the CHECKSUM for 2 bytes data ("0xE5" and "0xF6"), perform 8-bit addition without signed.

0xE5 + 0xF6 = 0x1DB

Take the two's complement of the sum to the lower 8-bit, and that is a checksum value. So, "0x25" is sent to the controller.

0 - 0xDB = 0x25

6.6.8. Communication Rules of RAM Transfer Command

This section shows communication rules of RAM transfer. Transfer directions in the table are indicated as follows:

Transfer direction (C→T): From Controller to target (TXZ+)
Transfer direction (T→C): From target (TXZ+) to Controller

Table 6.13 Communication Rules of RAM Transfer Command

No	Transfer direction	Transfer data	Description
1	C→T	Operation command data (0x10)	Controller transmits RAM transfer command data “0x10”.
2	T→C	ACK response to the operation command Normal: 0x10 Abnormal: 0x11 Communication error: 0x18	The target checks received data, and it sends ACK response data. If a receive error exists, the target sends ACK response data “0x18” indicating communication error, and then returns to the initial state waiting for operation command data. If a receive error does not exist, the target checks the data against operation command data described in “Table 6.6 Operation commands in single boot mode”. If checking is failed, the target sends ACK response data “0x11” indicating abnormal state, and then returns to the initial state waiting for operation command data. If checking is succeeded, the target sends ACK response data “0x10” indicating normal state, and then it waits for next data.
3	C→T	Password length (PLEN) (1 byte)	The controller transmits password length data “0xFF” of the code flash.
4	C→T	Password length store address (PNSA) (4 bytes)	The controller transmits the address data where the password length is stored.
5	C→T	Password store start address (PCSA) (4 bytes)	The controller transmits the start address where the password is stored.
6	C→T	Password string (255 bytes)	The controller transmits password data of the code flash. If it has been erased, the controller transmits dummy data.
7	C→T	CHECKSUM value of transmit data (No.3 to 6)	The controller calculates the CHECKSUM value of transmit data (No.3 to 6), and sends them. For details of CHECKSUM calculation, refer to “6.6.7.4. CHECKSUM Calculation”.
8	T→C	Password length error check, password store address error check, password verification, ACK response to CHECKSUM value. - Blank: 0x14 (Note1) - Normal: 0x10 - Abnormal: 0x11 - Communication error: 0x18	The target checks received data, and then it sends ACK response data. If a receive error exists, the target sends ACK response data “0x18” indicating communication error, and then returns to the initial state waiting for operation command data. If a receive error does not exist, the target checks a CHECKSUM value and password. For details of password verification, refer to “6.6.7.3. Password”. If password determination is failed, the target sends ACK response data "0x11" indicating abnormal state, and then returns to the initial state waiting for operation command data. If password determination is succeeded, the target sends ACK response data “0x10” indicating normal state, and then it waits for next transmit data. In the case of blank products, ACK response data"0x14" is replied (Note1), and it waits for next transmit data.

9	C→T	RAM store start address (31 to 24)	The controller transmits the RAM start address to be stored in RAM store data by dividing into 4 times as a next transmit data. Transmission order is as follows: 1st byte corresponds to bit 31 to bit 24 and 4th byte corresponds to bit 7 to bit 0 of transfer address. These addresses should be placed in "0x20000400" through the last address of RAM address. The target checks receive data. If a receive error exists, the target sends ACK response data "0x18" indicating communication error, and then returns to the initial state waiting for operation command data. If a receive error does not exist, the target transmits nothing, and waits for next transmit data.
10	C→T	RAM store start address (23 to 16)	
11	C→T	RAM store start address (15 to 8)	
12	C→T	RAM store start address (7 to 0)	
13	C→T	The number of bytes where the RAM stores data (15 to 8)	The controller transmits the number of bytes to be block-transferred. Transmission order is as follows: 1st byte corresponds to bit 15 to bit 8 and 2nd byte corresponds to bit 7 to bit 0 of transfer address. These addresses should be placed in "0x20000400" through the last address of RAM address. The target checks receive data. If a receive error exists, the target sends ACK response data "0x18" indicating communication error, and then returns to the initial state waiting for operation command data. If a receive error does not exist, the target transmits nothing, and waits for next transmit data.
14	C→T	The number of bytes where the RAM stores data (7 to 0)	
15	C→T	A CHECKSUM value of transmit data (No.9 to 14)	The controller transmits a CHECKSUM value of transmit data (No.9 to 14).
16	T→C	ACK response to a CHECKSUM value Normal: 0x10 Abnormal: 0x11 Communication error: 0x18	The target checks receive data, and it sends ACK response data. If a receive error exists, the target sends ACK response data "0x18" indicating communication error, and then returns to the initial state waiting for operation command data. If a receive error does not exist, the target checks a CHECKSUM value. If checking is failed, the target sends ACK response data "0x11" indicating abnormal state, and then returns to the initial state waiting for operation command data. If checking is succeeded, the target sends ACK response data "0x10" indicating normal state, and then it waits for next data.
17	C→T	RAM store data	The controller transmits data to be stored in RAM from the controller. The target receives data to be stored in RAM.
18	C→T	A CHECKSUM value of transmit data (No.17)	The controller transmits a CHECKSUM value of transmit data (No.17).
19	T→C	ACK response to CHECKSUM verification - Normal: 0x10 - Abnormal: 0x11 - Communication error: 0x18	The target checks receive data, and it sends ACK response data. If a receive error exists, the target sends ACK response data "0x18" indicating communication error, and then returns to the initial state waiting for operation command data. If a receive error does not exist, the target checks a CHECKSUM value. If checking is failed, the target responds ACK response data "0x11" indicating abnormal state, and then returns to the initial state waiting for operation command data. If checking is succeeded, the target sends ACK response data "0x10" indicating normal state and jumps to RAM store start address (No.9 to 12) as a branch address.(Note)

Note: A setup of the functions (a port, UART, a timer, RAM, etc.) which the Boot ROM program used is not initialized.

6.6.9. Communication Rules of Flash memory Erasing

This section shows a communication format of flash memory erasing command. Transfer directions in the table are indicated as follows:

Transfer direction (C→T): From Controller to Taeget(TXZ+)
Transfer direction (T→C): From Taeget(TXZ+) to Controller

Table 6.14 Communication Rules of Flash memory Erasing

No	Transfer direction	Transfer data	Description
1	C→T	Operation command data (0x40)	The controller transmits flash memory erasing command data “0x40”.
2	T→C	ACK response to operation command Normal: 0x40 Abnormal: 0x41 Communication error: 0x48	The target checks receive data, and it sends ACK response data. If a receive error exists, the target sends ACK response data “0x48” indicating communication error, and then returns to the initial state waiting for operation command data. If a receive error does not exist, the target checks a CHECKSUM value according to the operation commands shown in “Table 6.6 Operation commands in single boot mode”. If checking is failed, the target responds ACK response data “0x41” indicating abnormal state, and then returns to the initial state waiting for operation command data. If checking is succeeded, the target sends ACK response data “0x40” indicating normal state, and waits for next data.
3	C→T	Erase enable command data (0x54)	The controller transmits erase enable command data (0x54).
4	T→C	ACK response to erase enable command data - Normal: 0x54 - Abnormal: 0x51 - Communication error: 0x58	The target checks receive data and, it sends ACK response data. If receive error exists, the target sends ACK response data “0x58” indicating abnormal communication, and then returns to the initial state waiting for operation command data. If receive error does not exist, the target checks an erase enable command “0x54”. If checking is failed, the target responds ACK response data “0x51” indicating abnormal state, and then returns to the initial state waiting for operation command data. If checking is succeeded, the target sends ACK response data “0x54” indicating normal state, and performs chip erasing.
5	-	-	Chip erasing in progress.
6	T→C	ACK response to the checking for chip erasing - Erasing completed: 0x4F - Abnormal end (blank check error): 0x4C - Abnormal end (time-out error): 0x47	The target sends the result of chip erasing process. If no problems occur, the target sends ACK response data “0x4F” indicating normal state. If a blank check error occurs, the target sends ACK response data “0x4C” indicating abnormal state. If chip erasing command is aborted, the target sends ACK response data “0x47” indicating abort and then returns to the initial state waiting for operation command data.

6.6.10. Reprogramming Procedure of the Flash Using Reprogramming Algorithm in Boot ROM

This section describes the reprogramming procedure of the flash using reprogramming algorithm in the on-chip Boot ROM. (The Following example is using UART)

6.6.10.1. Step-1

The condition of the flash memory does not care whether a former user program has been programmed or erased. Since a programming routine and programming data are transferred via the UART, the UART of this device must be connected to an external host. A programming routine (a) is prepared on the host.

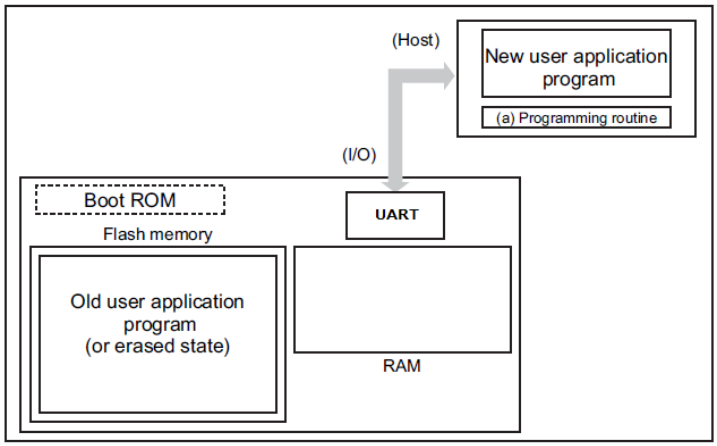

Figure 6.15 Procedure of Using Reprogramming Algorithm in Boot ROM (1)

6.6.10.2. Step-2

The user releases the reset by the pin condition setting for single boot mode and boots up on the Boot ROM. According to the procedure of single boot mode, the user transfers the programming routine (a) via the UART from the source (host). Password verification is performed against the password in the user application program first. For details, refer to "(4) Password Setting Values and Setting Ranges" in section "6.6.7.3. Password".

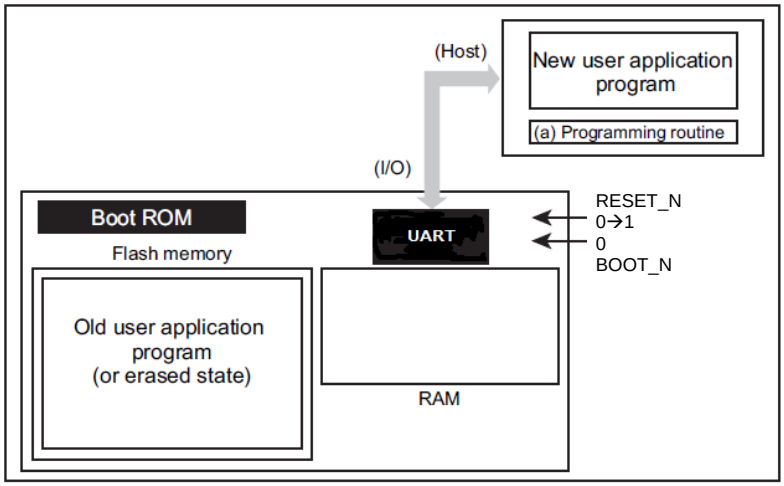

Figure 6.16 Procedure of Using Reprogramming Algorithm in Boot ROM (2)

Note: All products do not support the determination of the transition destination by the deassertion of Power On Reset (POR). For the details, refer to reference manual "Product Information".

6.6.10.3. Step-3

When the password verification is completed, the boot program transfers a programming routine (a) from the host into the on-chip RAM. The Boot ROM loads this routine to the on-chip RAM. The programming routine must be stored in the range from “0x20000400” to the end address which can be transmitted of the on-chip RAM.

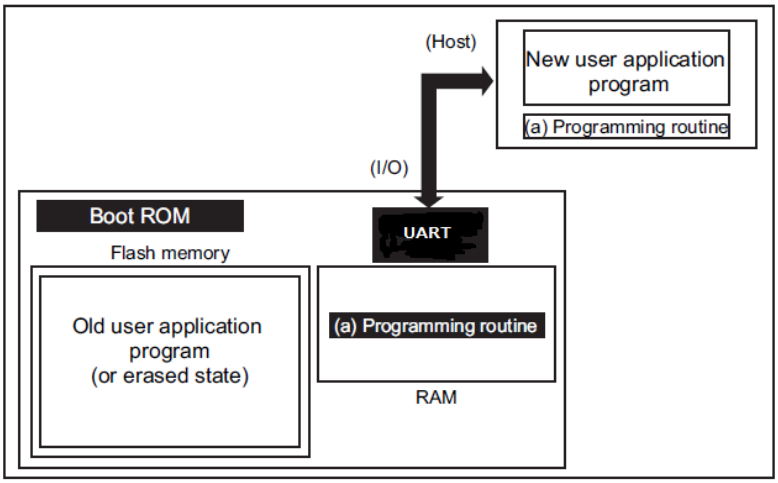

Figure 6.17 Procedure of Using Reprogramming Algorithm in Boot ROM (3)

6.6.10.4. Step-4

The boot program jumps to the programming routine (a) in the on-chip RAM to erase the flash block containing old application program codes (the units of erase is arbitrary size).

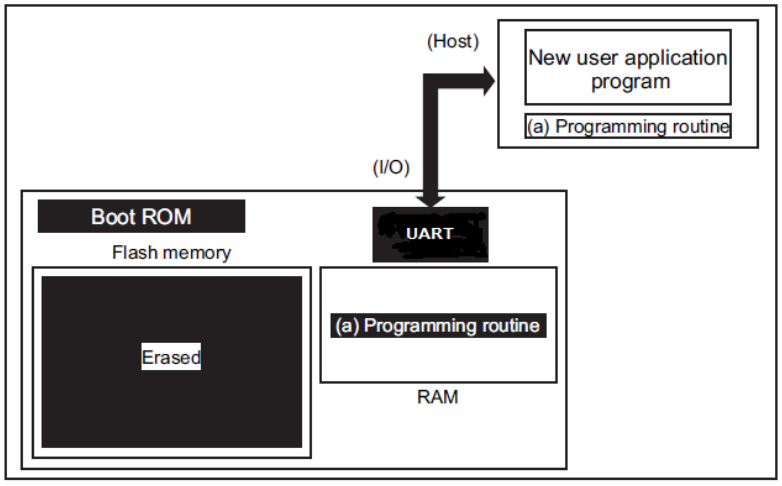

Figure 6.18 Procedure of Using Reprogramming Algorithm in Boot ROM (4)

6.6.10.5. Step-5

The boot program executes the programming routine (a) to download new application program codes from the host and programs it into the erased flash area. When the programming is completed, set the programming or erasing protection of that flash area in the user's program to ON.

In the example below, new program codes come from the same host via the same UART used when the programming routine has been transferred. However, once the programming routine starts operation, it is free to change the transfer path and the source of the transfer. The user can create a hardware board and programming routine to suit your particular needs.

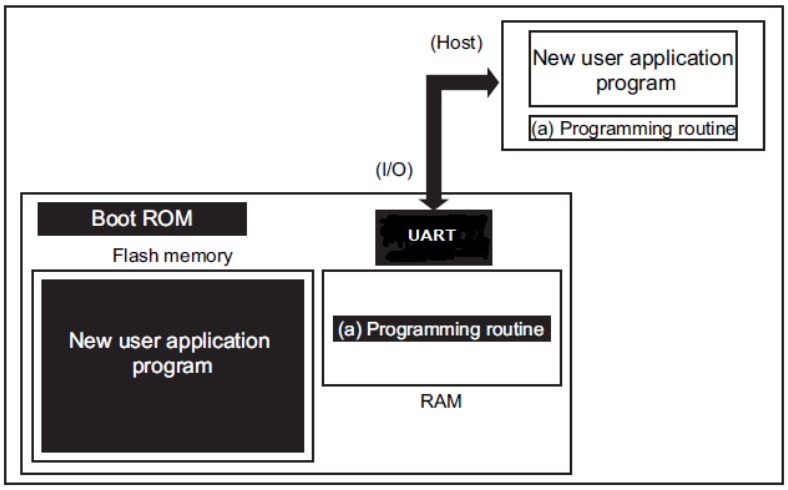

Figure 6.19 Procedure of Using Reprogramming Algorithm in Boot ROM (5)

6.6.10.6. Step-6

When programming of Flash memory is completed, the user shuts the power once and disconnects the cable connected with the host. The user then turns on the power again, so that the device re-boots in single-chip mode (normal mode) to execute the new program.

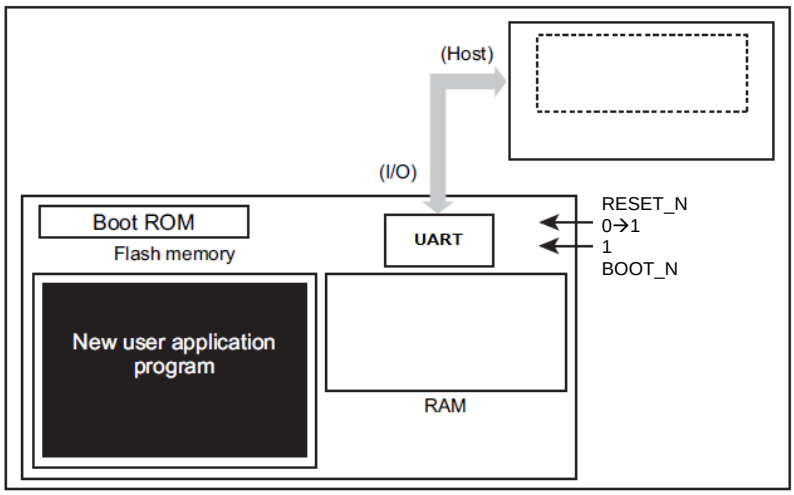

Figure 6.20 Procedure of Using Reprogramming Algorithm in Boot ROM (6)

Note: All products do not support the determination of the transition destination by the deassertion of Power On Reset (POR). For the details, refer to reference manual "Product Information".

6.7. How to Reprogram using Dual Mode

The dual mode executes flash reprogramming using the flash memory reprogramming routine located in specified block on the users' set.

While instructions are executing on area 0, another area (such as Area1:code flash (Note), Area 4: data flash) of the flash memory, on which instructions are not executed, can be programmed/erased. (The opposite case is also possible depending on the condition.)

Note: Area 1 may not be available depending on the product specifications.

When you use an exception in a dual mode, be careful not to mistakenly execute an instruction in the area for programming/ erasing the flash memory.

6.7.1. Example of Flash Memory Reprogramming Procedure

6.7.1.1. Step-1

A user determines the conditions (e.g., pin status) to enter the on-board programming and the target flash memory to be programmed or erased. Then suitable circuit design and program are created along to the users' conditions.

(a) Mode determination routine: A program to determine to switch to user boot mode
(b) Programming routine: A program to download new program from the host controller and reprogram Flash memory.

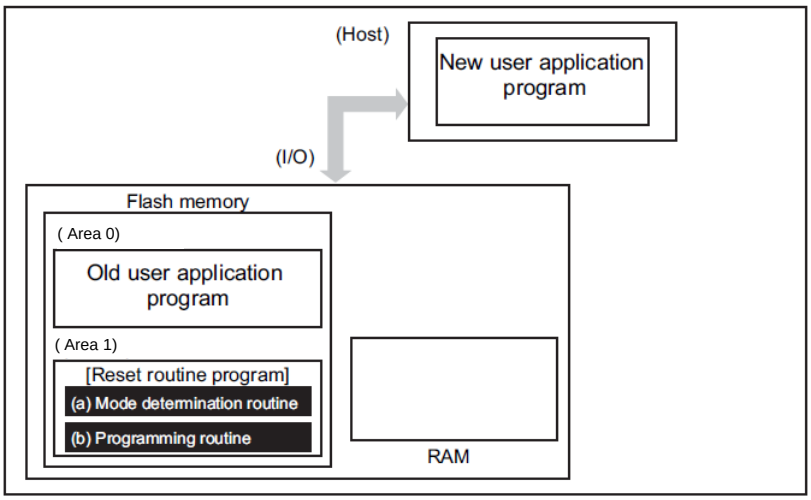

Figure 6.21 Reprogramming using Dual Mode (1)

6.7.1.2. Step-2

This section explains the case where a programming routine is stored in the reset routine. The reset routine determines to enter the dual mode. If mode switching conditions are met, the program jumps to the flash reprogramming routine to transfer to dual mode.

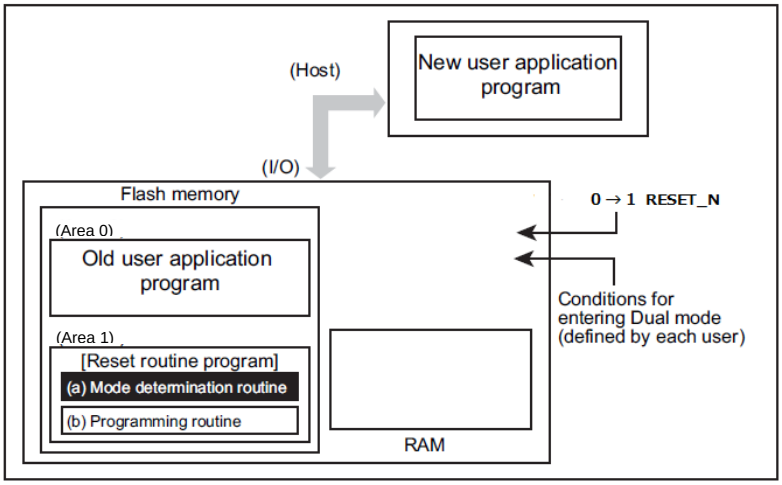

Figure 6.22 Reprogramming using Dual Mode (2)

6.7.1.3. Step-3

After the program jumps to the flash reprogramming routine, the program releases the program/erase protection in the old user program area and erases the areas in unit of the area, block, or page.

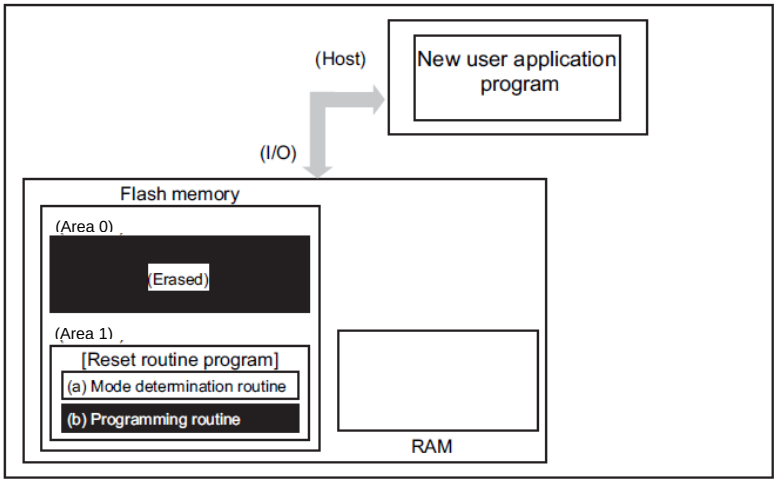

Figure 6.23 Reprogramming using Dual Mode (3)

6.7.1.4. Step-4

Subsequently, confirm whether the erased area of the flash is blank, and then download a new user's application program data from the transfer source (Host) to develop it on the RAM.

Developed data on the RAM is written to the erased area of the flash memory. When all data programming is completed, set the program/erase protection of that flash block in the user program area to ON.

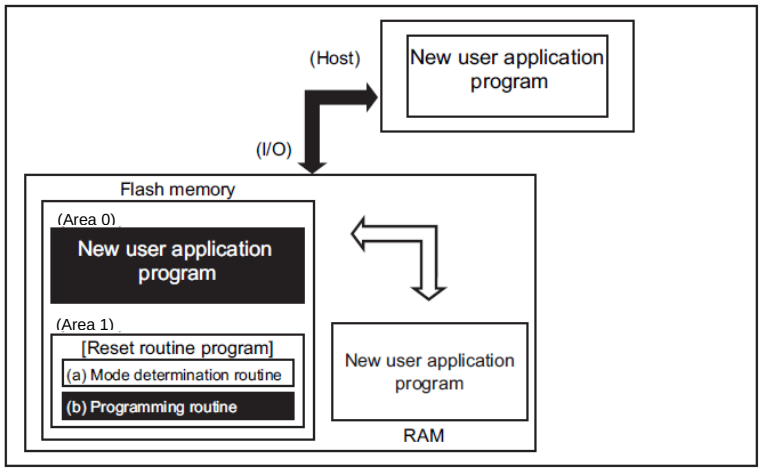

Figure 6.24 Reprogramming using Dual Mode (4)

6.7.1.5. Step-5

Upon reset, the flash memory is set to normal mode. After reset, the CPU will start operation along with the new application program.

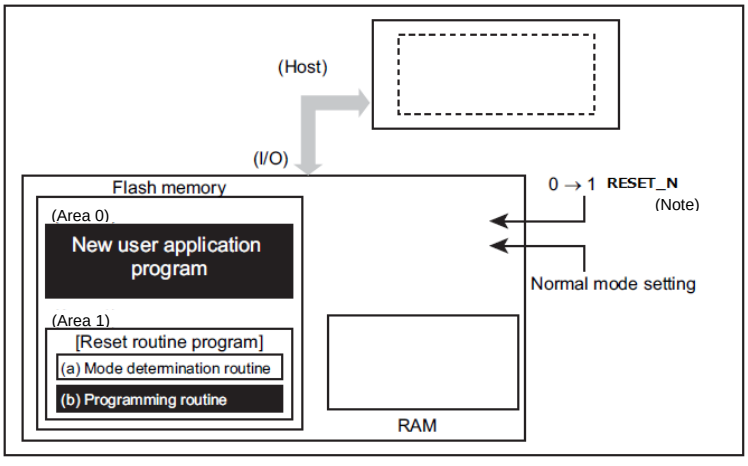

Figure 6.25 Reprogramming using Dual Mode (5)

Note: Depending on the product, a power on reset (POR) can be used instead of the RESET_N pin. For details, refer to reference manual "Product Information" and section "Reset and Power Control" of "Clock Control and Operation Mode".

6.8. How to Reprogram User Boot Program

This method switches the Page 0 to Page 1 area to hold a user boot program using the memory swap function when Flash memory is reprogrammed.

The following is an example of reprogramming procedure of user boot program.
(Assumed conditions: Swap size is 4K bytes. Page 1 program is copied from Page 0.)

6.8.1. Example of Flash Memory Reprogramming Procedure

6.8.1.1. Step-1

The user confirms whether "00" is read from ***[FCSWPSR]***<SWP1><SWP0>.

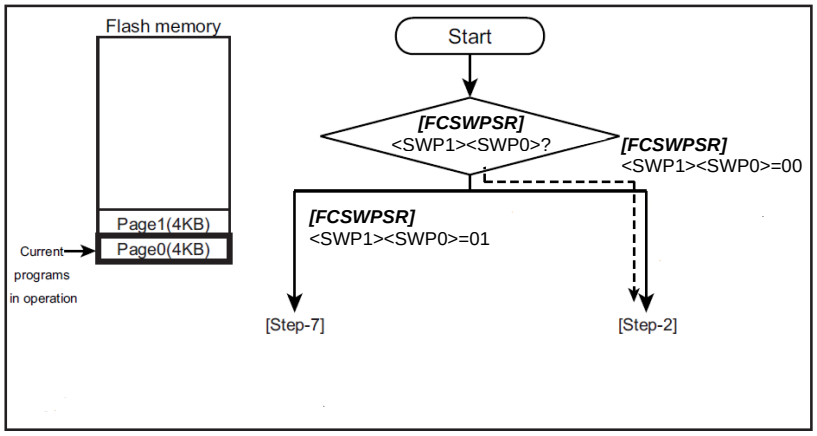

Figure 6.26 Reprogram by User Boot Program (1)

6.8.1.2. Step-2

The user checks ***[FCPSR0]***<PG1>=0. If protection status enabled then write "0" to ***[FCPMR0]***<PM1> for temporary release protection.

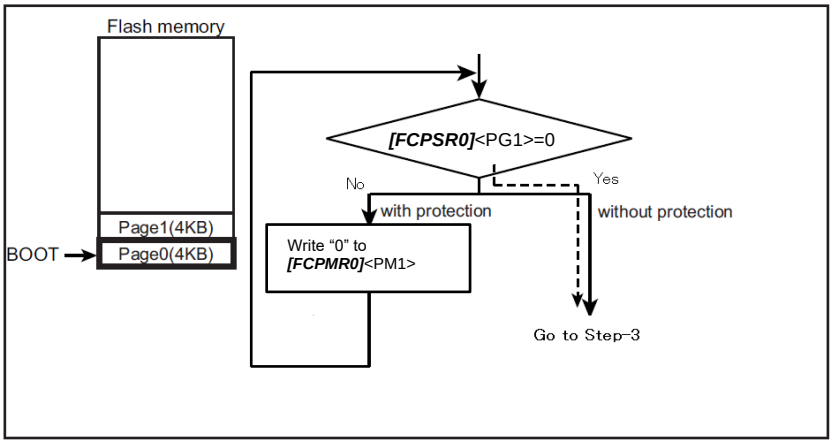

Figure 6.27 Reprogram by User Boot Program (2)

6.8.1.3. Step-3

The user transfers the reprogramming routine to the on-chip RAM, and moves the PC (Program Counter) to the transferred program.

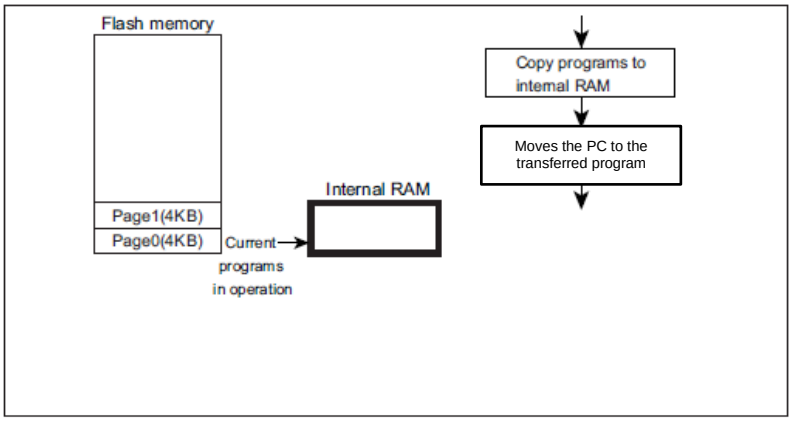

Figure 6.28 Reprogram by User Boot Program (3)

6.8.1.4. Step-4

The user erases Page 1, and then copies a program of Page 0 to Page 1.

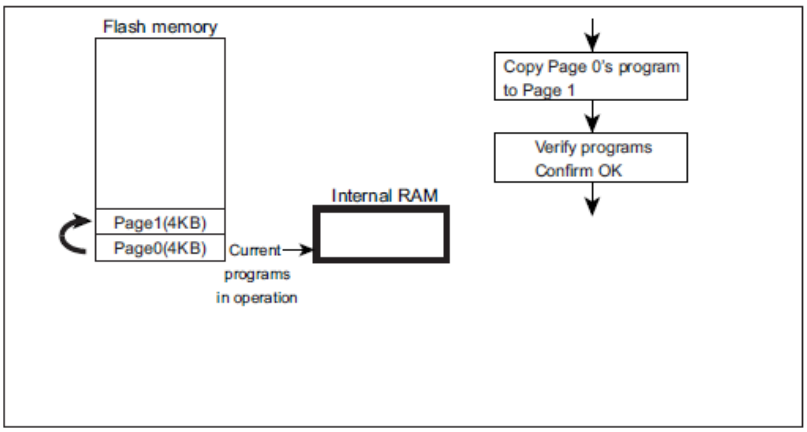

Figure 6.29 Reprogram by User Boot Program (4)

6.8.1.5. Step-5

The automatic memory swap command sets ***[FCSWPSR]***<SWP1><SWP0> to “01” swap Page 0 with Page 1.

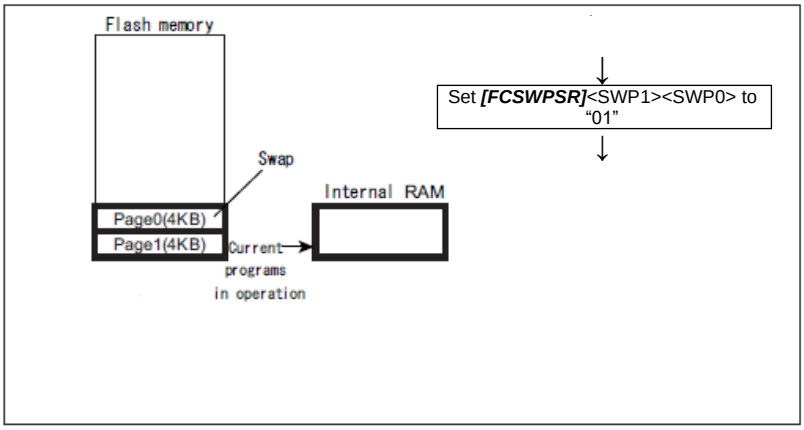

Figure 6.30 Reprogram by User Boot Program (5)

6.8.1.6. Step-6

The user performs a reset and releases a reset.
Page 1 is assigned to address 0 and the flash memory boots up at Page1.
A program branches to the conditioning routine where ***[FCSWPSR]***<SWP1><SWP0> is set to “01” (To [Step-7]).

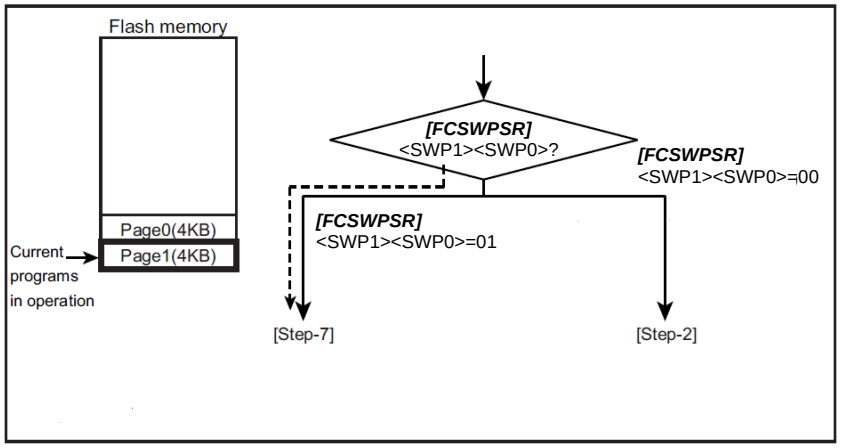

Figure 6.31 Reprogram by User Boot Program (6)

6.8.1.7. Step-7

The user checks ***[FCPSR0]***<PG1>=0. If protection status enabled then write ***[FCPMR0]***<PM1> to “0” for temporary release protection.

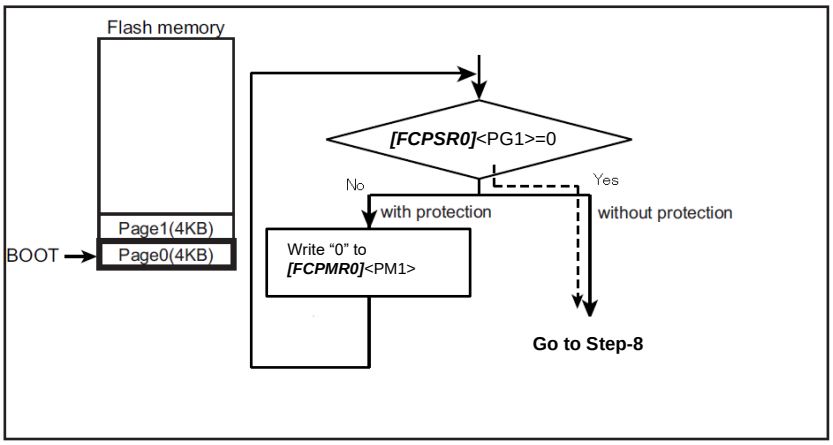

Figure 6.32 Reprogram by User Boot Program (7)

Note: Protection function performs to address.Then when memory swapped between Page0 and Page1, <PG0>/<PM0> is for Page1 and <PG1>/<PM1> is for Page0.

6.8.1.8. Step-8

The user transfers the flash reprogramming routine to the on-chip RAM, and moves the PC (Program Counter) to the transferred program.

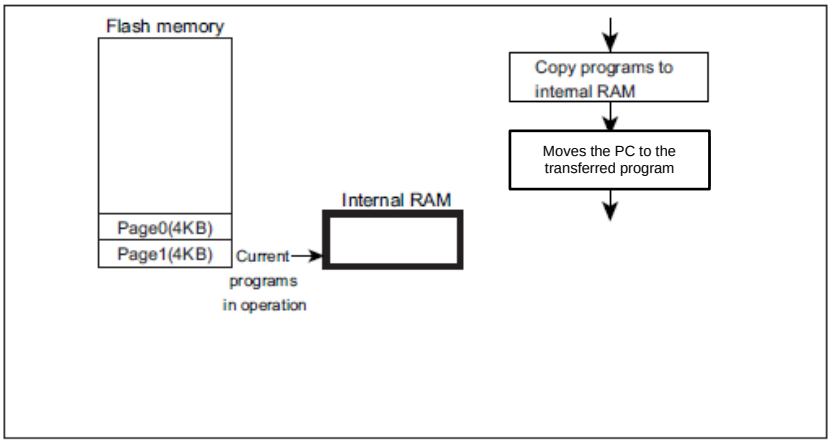

Figure 6.33 Reprogram by User Boot Program (8)

6.8.1.9. Step-9

The user programs a new boot program to Page 0.

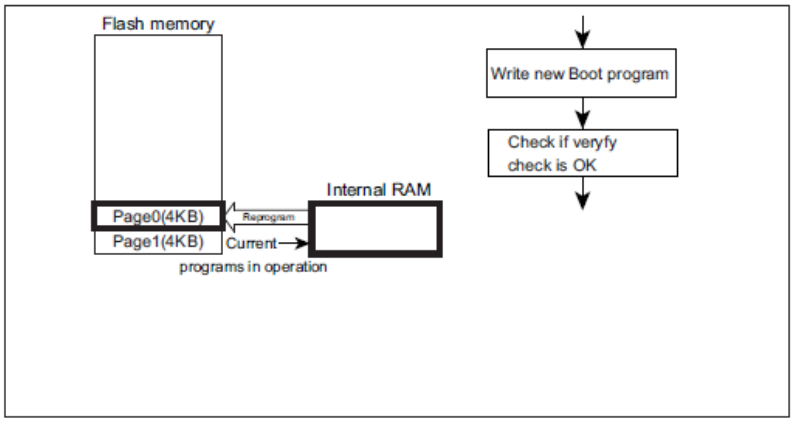

Figure 6.34 Reprogram by User Boot Program (9)

6.8.1.10. Step-10

Perform automatic memory swap erasing command (following figure) or set ***[FCSWPSR]***<SWP1><SWP0> to “11” with the automatic memory swap command to swap release Page 0 and Page 1.

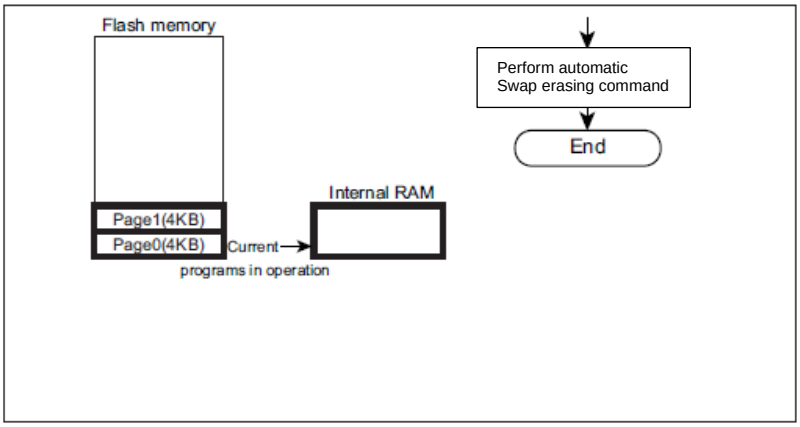

Figure 6.35 Reprogram by User Boot Program (10)

7. General Precautions

- Do not perform any operation that is not described in this document.
- Do not access the addresses that is not assigned to the registers in this document to the registers.
- It is recommended to confirm whether the programming/erasing was successfully completed by reading after command execution.

8. Revision History

Table 8.1 Revision history

Revision	Date	Description
1.0	2023-01-25	New Release

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