TB9032FNG
Application Note

INTRODUCTION

This material is a reference document that describes the technical information on TB9032FNG for engineers who use the product. This material mainly describes items and precautions that are useful when applying TB9032FNG. Always refer to the latest version of the TB9032FNG data sheet whenever using TB9032FNG.

Contents

1. PRODUCT OUTLINE

TB9032FNG is a driver/receiver IC that is compliant with ISO 20794-4 for CXPI (Clock Extension Peripheral Interface) communication. It can switch between commander and responder nodes using the external pin. When in Sleep Mode, it enters a standby state with low power consumption.
In addition, it is equipped with fault detection functions, including overheat detection and low voltage detection, and stops output when an abnormality is detected.

Always refer to the latest version of the TB9032FNG data sheet when using TB9032FNG. You can download it from the following website:

TB9032FNG | Automotive Devices | Toshiba Electronic Devices & Storage Corporation | Asia-English (semicon-storage.com)

Always comply with the contents described in the data sheet, including the notes.

2. POWER SUPPLY

2.1 Normal operating range and functional operation

・There are two power supply pins: the BAT pin and the VIO pin.
・Each power supply pin has a normal operating range and functional operation. Use them within normal operating range.
・The normal operating range and functional operation of BAT are as follows:
 ・Normal operating range $6\ V \leqq V_{BAT} \leqq 18\ V$
 ・Functional operation (BAT high voltage) $18\ V < V_{BAT} \leqq 27\ V$
 ・Functional operation (BAT low voltage) $V_{BAT\_UV} \leqq V_{BAT} < 6\ V$
・The normal operating range and functional operation of VIO are as follows:
 ・Normal operating range $4.5\ V \leqq V_{VIO} \leqq 5.5\ V$
 ・Functional operation (VIO low voltage) $V_{VIO\_UV} \leqq V_{VIO} < 4.5\ V$
・For details of functional operation, refer to “9. OPERATING RANGES” of the data sheet. Functional operation is a design guideline, and some of the electrical characteristics are not covered by warranty.
・For details of V_{BAT_UV} (BAT low voltage detection) and V_{VIO_UV} (VIO low voltage detection), refer to “Table 10.1 IC Characteristics” of the data sheet.
・For the absolute maximum ratings of the power supply voltage, refer to “8. ABSOLUTE MAXIMUM RATINGS” of the data sheet.

2.2 Power ON/OFF sequence

・For details of the power on/off sequence, refer to “7.2. OPERATION SEQUENCES” of the data sheet.

3. ABNORMALITY DETECTION FUNCTIONS

TB9032FNG has the following abnormality detection functions.

- ・BAT undervoltage (UVLO of BAT)
- ・VIO undervoltage (UVLO of VIO)
- ・VIO undervoltage (POR)
- ・Dominant timeout
- ・Overheat (TSD)

For details, refer to “7.1. Abnormality Detection Functions” of the data sheet.

4. EMC AND ESD

TB9032FNG is developed with EMI reduction, EMS resistance, and ESD resistance taken into consideration from the upstream process of product development.
Some of the reference parts and reference values shown in “7.2 Reference value for parts” in “7. APPLICATION CIRCUIT EXAMPLE” as described later are for EMI, EMS, and ESD countermeasures.
For mass production, contact us for more detailed information on EMC and ESD.

5. THERMAL RESISTANCE

The thermal resistance characteristics of the TB9032FNG’s package are as follows:

・Thermal resistance values that include the below board

・Θ_{JA} ・・・Between junction and ambient temperature

Θ_{JA} = 147.9 ℃/W

・Ψ_{JT} ・・・ Between junction and package upper surface center

Ψ_{JT} = 5.6 ℃/W

・Board conditions

・1-layer board

・Board size (FR-4) 114.3 mm × 76.2 mm × 1.57 mm t

1st layer Copper foil thickness: 70 µm

Copper foil area: 1L land pattern area：Cu 50 %, lead wires area：Cu 25 %

(Area of land pattern and lead wires is assumed.)

6. PIN FMEA

Table 6.1 shows the pin FMEA.

Table 6.1 Pin FMEA

Pin No.	Pin Name	Pin Description	Withstand Voltage (V)	I/O	5V-system Ground Fault	VBAT Ground Fault	GND Ground Fault	Adjacent Ground Fault	Pin Open
1	RXD	Output pin of CXPI signals received from BUS	6	O	No problems. IC is inoperative.	Destruction due to overvoltage.	No problems. IC is inoperative.	No problems. IC is inoperative.	No problems. IC is inoperative.
2	NSLP	Normal Mode: H Sleep Mode or Wakeup Transmission Mode: L	6	I	No problems. IC is partially inoperative.	Destruction due to overvoltage.	No problems. IC is partially inoperative.	No problems. IC is partially inoperative.	No problems. IC is partially inoperative.
3	VIO	5 V Interface	6	(Power Supply)	No problems.	Destruction due to overvoltage.	No problems. IC is inoperative.		No problems. IC is inoperative.
4	TXD	Input pin of CXPI signals to be transmitted to BUS	6	I	No problems. IC is inoperative.	Destruction due to overvoltage.	No problems. IC is inoperative.	No problems. IC is inoperative.	No problems. IC is inoperative.
5	GND	GND	-	(GND)	No problems. IC is inoperative.	No problems. IC is inoperative.	No problems.	No problems. IC is inoperative.	No problems. IC is inoperative.
6	BUS	CXPI communication BUS pin	40	I/O	No problems. IC is inoperative.	No problems. IC is inoperative.	No problems. IC is inoperative.	No problems. IC is inoperative.	No problems. IC is inoperative.
7	BAT	Connected to the battery	40	(Power Supply)	Destruction due to overvoltage.	No problems.	No problems. IC is inoperative.		No problems. IC is inoperative.
8	MS	Commander node: H Responder node: L	40	I	No problems. IC is partially inoperative.	No problems. IC is partially inoperative.	No problems. IC is partially inoperative.	No problems. IC is partially inoperative.	No problems. IC is partially inoperative.

No problem" in the table above includes the absence of ignition, smoke, destruction, and the like.

7. APPLICATION CIRCUIT EXAMPLE

7.1 Circuit diagram

・Figure 7.1 shows an application circuit example.

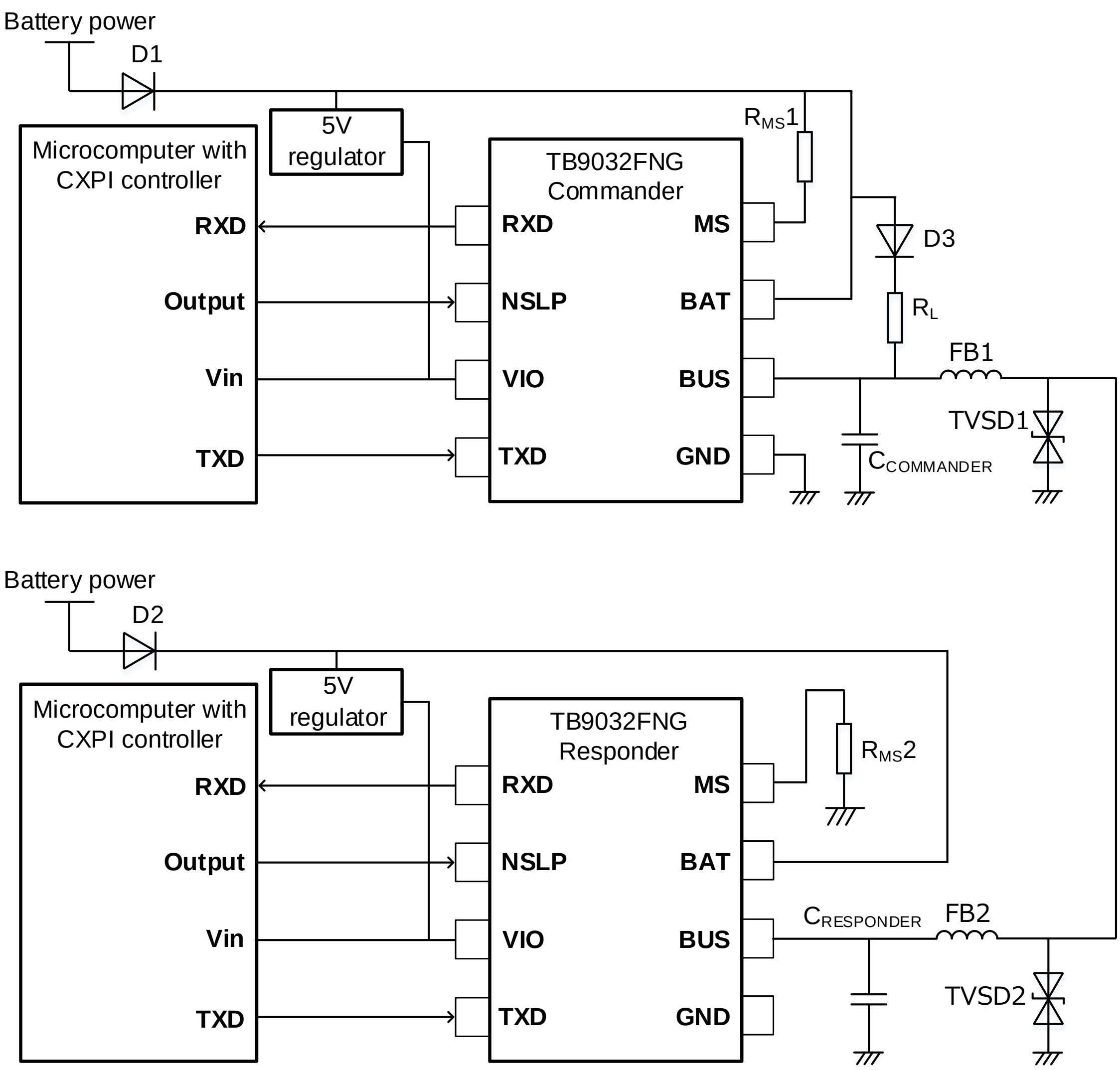

Figure 7.1 Application circuit example

7.2 Reference value for parts

・Table 7.2 shows the reference value for parts.

Table 7.2 Reference value for parts

Symbol	Reference part and reference value
D1	CRG09A
D2	CRG09A
D3	LL4148 V_F ≦ 1.0 V
$R_{MS}1$	10kΩ
$R_{MS}2$	10kΩ
R_L	1kΩ
$C_{COMMANDER}$	220pF
$C_{RESPONDER}$	220pF
FB1	BLM18AG601SH1
FB2	BLM18AG601SH1
TVSD1	DF2B29FU
TVSD2	DF2B29FU

The above values are recommended values for reference only; therefore, make decisions for mass production after sufficiently confirming the values on an actual circuit board.

7.3 Notes

・The circuit diagram on the previous page an application circuit example and cannot be guaranteed as a design for mass production.

・External parts are examples. External parts other than those shown in the above figure can also be chosen.

8. EVALUATION BOARD

8.1 Photograph of evaluation board

・Evaluation boards for checking the functions of the IC, shown in Figure 8.1, are available.

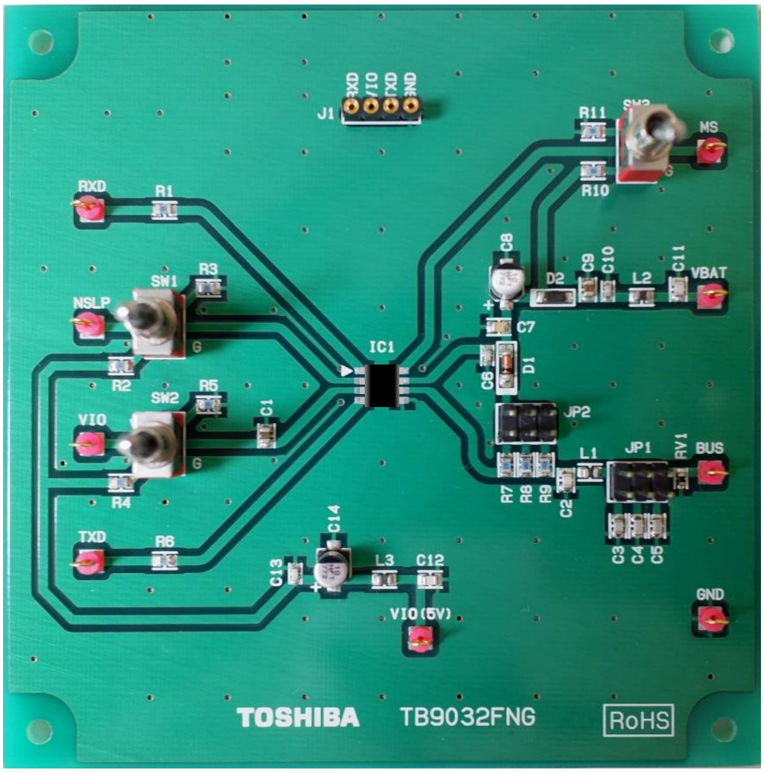

Figure 8.1 Evaluation board

8.2 Evaluation board circuit diagram

・Figure 8.2 shows the evaluation board circuit diagram.

R1	1kΩ
R2	1kΩ
R3	1kΩ
R4	1kΩ
R5	1kΩ
R6	1kΩ
R7	1kΩ
R8	660Ω
R9	500Ω
R10	10kΩ
R11	1kΩ

C1	100nF
C2	220pF
C3	820pF
C4	5nF
C5	10nF
C6	330pF
C7	56nF
C8	10μF
C9	0.1μF
C10	330pF
C11	1nF
C12	1nF
C13	330pF
C14	10μF

D1	LL4148
D2	CRG09A
L1	MMZ2012Y202B
L2	47μH
L3	47μH
RV1	AVRM1608C270KT221M

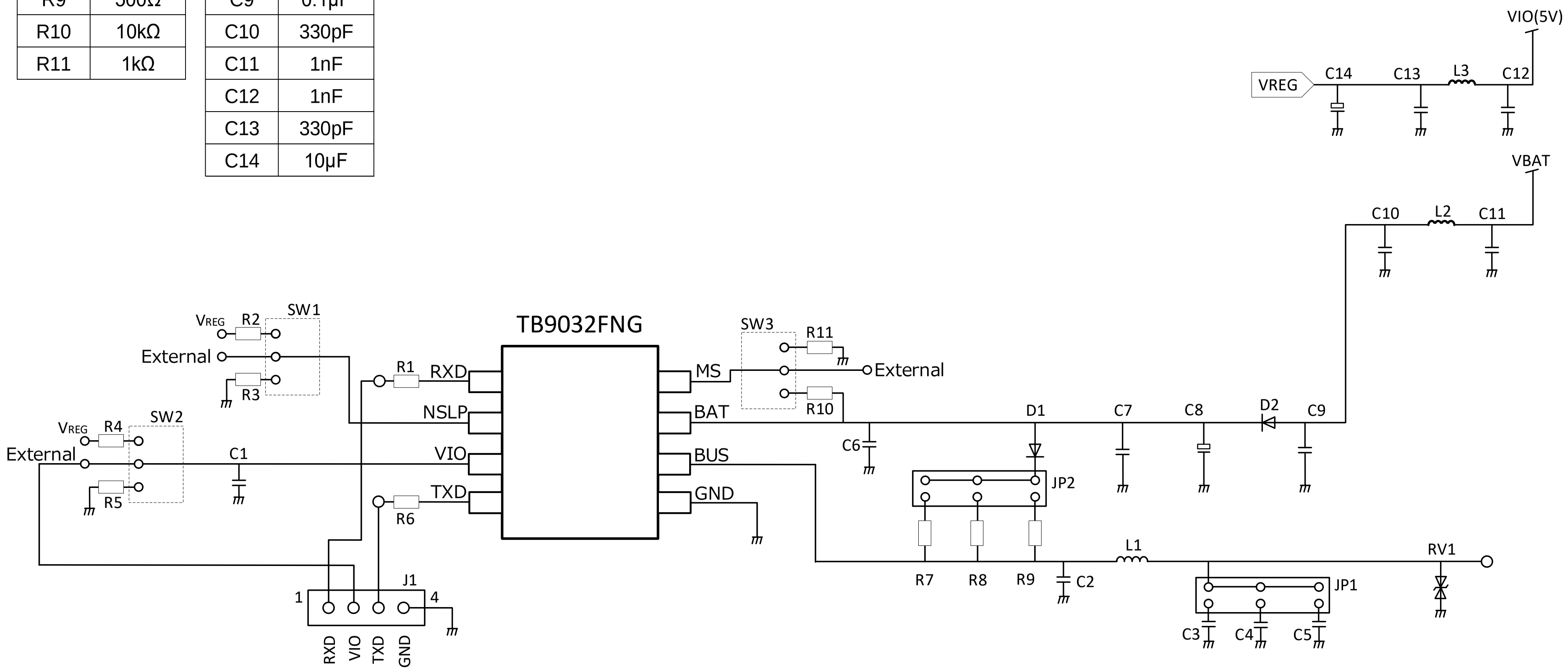

Figure 8.2 Evaluation board circuit diagram

9. LAND PATTERN

9.1 Land pattern diagram (for reference only)

・The reference land pattern for P-SOP8-0405-1.27-002 is available on our website below.

P-SOP8-0405-1.27-002 | Package & Packing Information | Toshiba Electronic Devices & Storage Corporation | Asia-English (semicon-storage.com)

・The figure is a reference land pattern. Please confirm the following 9.2 Precautions.

9.2 Notes

・All linear dimensions are given in millimeters unless otherwise specified.

・This drawing is based on JEITA ET-7501 Level3 and should be treated as a reference only. TOSHIBA is not responsible for any incorrect or incomplete drawings and information.

・You are solely responsible for all aspects of your own land pattern, including but not limited to soldering processes.

・The drawing shown may not accurately represent the actual shape or dimensions.

・Before creating and producing designs and using, customers must also refer to and comply with the latest versions of all relevant TOSHIBA information and the instructions for the application that Product will be used with or for.

10. PACKAGE MOUNTING GUIDE

・This section provides you with the reference material “Package Mounting Guide SOP/QFP”.

・To download this material, open the following website, scroll down, and click on “Package Mounting Guide SOP/QFP” in “Package Mounting Guide”.

https://toshiba.semicon-storage.com/ap-en/semiconductor/design-development/package.html

・This material describes circuit board design methods and mounting methods. Efficient heat dissipation on the mounting boards is important to bring out the full performance of the IC.

11. NOTES ON CONTENTS

1. Block diagram

Some of the functional blocks, circuits, or constants in the block diagram may be partially omitted or simplified to explain the functions.

2. Equivalent circuit

Equivalent circuits may be partially omitted or simplified to explain the circuits.

3. Timing chart

Timing charts may be simplified to explain functions and operations.

4. Application circuit example

The application circuit example is for reference purposes only. Conduct thorough evaluation when making designs for mass production. In addition, Toshiba does not grant any license to any industrial property rights by providing these examples of application circuits.

5. Test circuit diagram

Components in the test circuit are used only to obtain and confirm device characteristics. They are not guaranteed to prevent malfunction or failure in application equipment.

12. NOTES ON HANDLING OF ICS

(1) The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even momentarily. Do not exceed any of these ratings.
Exceeding rating(s) may cause device breakdown, damage, or deterioration, and may result in injury by explosion or combustion.

(2) Do not insert devices in the wrong orientation or incorrectly. Ensure that positive and negative pins of power supplies are connected properly. Otherwise, current or power consumption may exceed the absolute maximum rating and exceeding the rating(s) may cause the device breakdown, damage, or deterioration, and may result in injury by explosion or combustion. Also, do not ever use any device that was applied the current with inserting in the wrong orientation or incorrectly.

(3) Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over-current and/or IC failure. The IC may fully break down when used under conditions exceeding absolute maximum ratings, when wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and breakdown can lead smoke or combustion. To minimize effects of the flow of a large current in case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.

(4) The abnormality detection functions, which are designed to temporarily detect or avoid an abnormal state, do not guarantee that the IC will not be destroyed. In addition, operation outside the guaranteed range may make these functions inoperative, resulting in the destruction of the IC.

(5) The overheat detection circuit does not protect the IC in all cases. Immediately release the overheating state after operation.
Depending on usage and conditions, such as operation exceeding absolute maximum ratings, the overheat detection circuit may not operate properly or the IC may be destroyed before operation.
When using ICs with inflow and outflow of high currents, such as power amplifiers, regulators, and drivers, always design them to keep temperature below the specific junction temperature (Tj) by conducting appropriate heat dissipation. These ICs have self-heating functions during normal use.
An inadequate IC heat radiation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, design the device taking into consideration the effect of IC heat radiation on components used around the IC.

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