Toshiba BiCD Process Integrated Circuit Silicon Monolithic

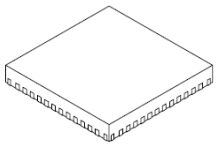
TB67S141FTG

Phase controlled Unipolar stepping motor driver

1. Description

The TB67S141FTG is a Phase controlled PWM chopping type 2 phase unipolar stepping motor driver. Using the BiCD process, the TB67S141 can be operated with VM voltage of 45 V, output voltage of 84 V, and output current of 3.0 A at max (absolute maximum ratings).

FTG



P-WQFN48-0707-0.50-003

Weight 0.1 g (typ.)

2. Features

- BiCD processed monolithic integrated circuit.
- Capable of operating one unipolar stepping motor.
- PWM controlled constant current drive.
- Full, half(a), and quarter step resolution.
- Low on resistance(0.25 Ω(typ.) output MOSFET.
- High voltage and current (For specification, please refer to the absolute maximum ratings and operating ranges).
- Brake mode function
- Standby (low power) mode function
- Error detect feedback signal output function (Over current/Thermal shutdown).
- Error detect function (Thermal shutdown(TSD), Over current(ISD), Low voltage(POR)).
- Built-in VCC regulator for internal circuit use.
- Fixed off time can be adjusted by external components.

Note: Please be careful about the thermal conditions during use.

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3. Block Diagram(Note)

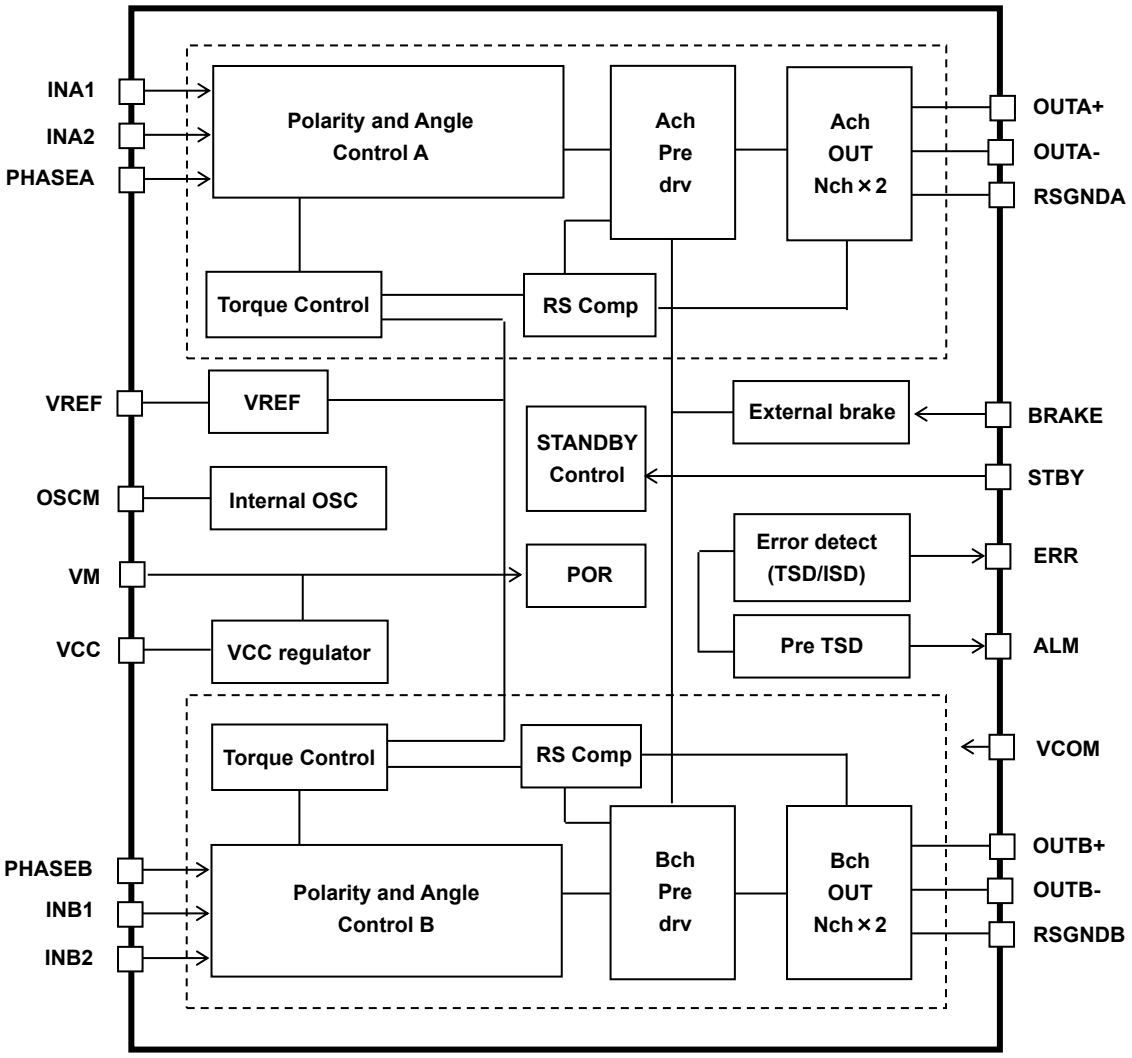


Figure 3.1 Block Diagram

Note: Functional blocks/circuits/constants in the block chart etc. may be omitted or simplified for explanatory purposes.

Note: All the grounding wires of the device must run on the solder mask on the PCB and be externally terminated at only one point. Also, a grounding method should be considered for efficient heat dissipation.
Careful attention should be paid to the layout of the output, VDD(VM) and GND traces, to avoid short circuits across output pins or to the power supply or ground. If such a short circuit occurs, the device may be permanently damaged.
Also, the utmost care should be taken for pattern designing and implementation of the device since it has power supply pins (VM, RSGND, OUT, GND) through which a particularly large current may run. If these pins are wired incorrectly, an operation error may occur or the device may be destroyed.
The logic input pins must also be wired correctly. Otherwise, the device may be damaged owing to a current running through the IC that is larger than the specified current.

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4. Pin Assignments

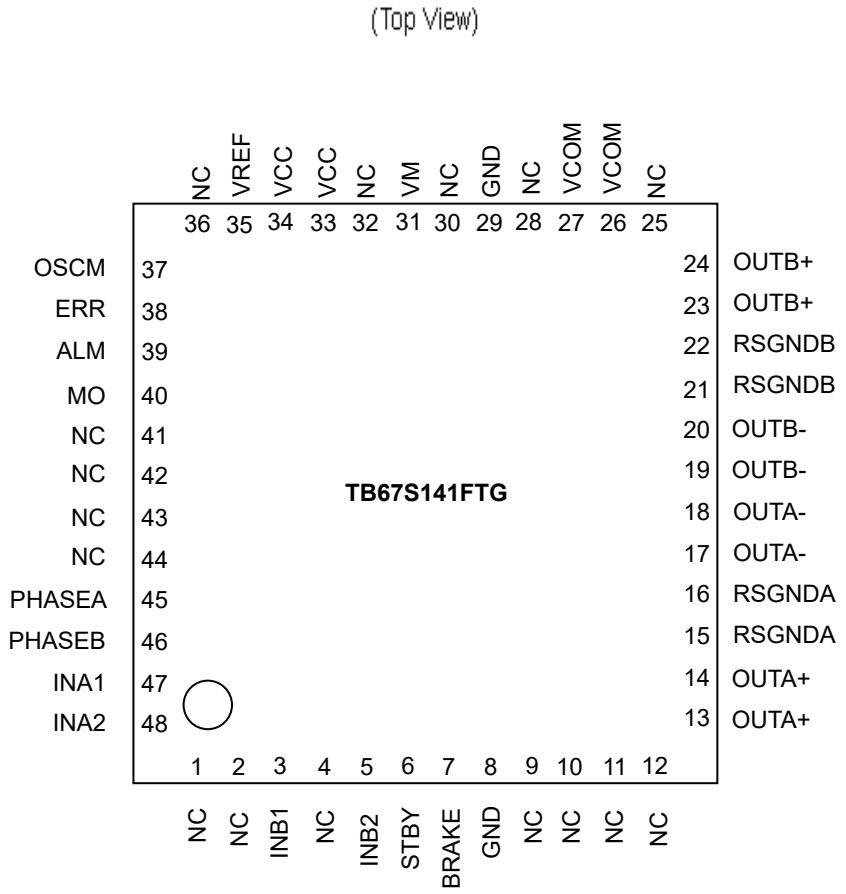


Figure 4.1 Pin Assignments (top view)

5. Pin Description

5.1. TB67S141FTG (WQFN48)

Table 5.1 Pin No.1 to 28

Pin No.	Pin Name	Function
1	NC	Non connection
2	NC	Non connection
3	INB1	Bch current setup 1
4	NC	Non connection
5	INB2	Bch current setup 2
6	STBY	Standby control pin
7	BRAKE	Brake control pin
8	GND	Ground pin
9	NC	Non connection
10	NC	Non connection
11	NC	Non connection
12	NC	Non connection
13	OUTA+	Motor output A+ pin
14	OUTA+	Motor output A+ pin
15	RSGNDA	Ach current sense ground pin
16	RSGNDA	Ach current sense ground pin
17	OUTA-	Motor output A- pin
18	OUTA-	Motor output A- pin
19	OUTB-	Motor output B- pin
20	OUTB-	Motor output B- pin
21	RSGNDB	Bch current sense ground pin
22	RSGNDB	Bch current sense ground pin
23	OUTB+	Motor output B+ pin
24	OUTB+	Motor output B+ pin
25	NC	Non connection
26	VCOM	Common pin
27	VCOM	Common pin
28	NC	Non connection

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Table 5.2 Pin No.29 to 48

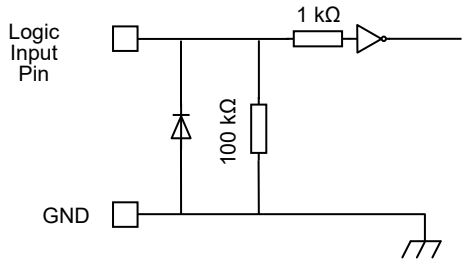
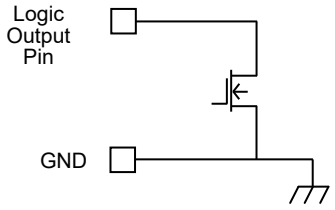
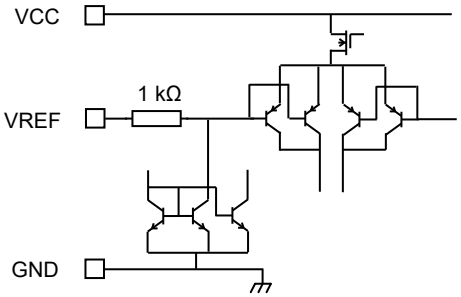
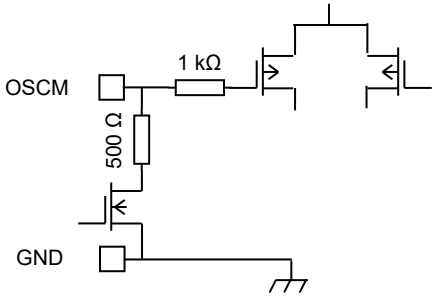
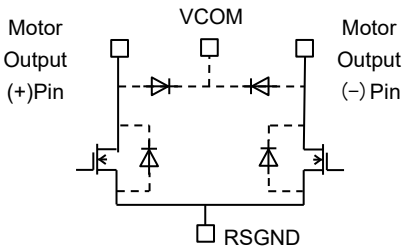
Pin No.	Pin Name	Function
29	GND	Ground pin
30	NC	Non connection
31	VM	VM power supply pin
32	NC	Non connection
33	VCC	Internal VCC regulator monitor pin
34	VCC	Internal VCC regulator monitor pin
35	VREF	Constant current threshold set pin
36	NC	Non connection
37	OSCM	Fixed off time set pin
38	ERR	Error detect feedback signal output pin
39	ALM	Thermal alarm output pin
40	NC	Non connection
41	NC	Non connection
42	NC	Non connection
43	NC	Non connection
44	NC	Non connection
45	PHASEA	Ach current phase setup pin
46	PHASEB	Bch current phase setup pin
47	INA1	Ach current setup 1
48	INA2	Ach current setup 2

Note: Please do not run patterns under NC pins.

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5.2. INPUT/OUTPUT Equivalent circuit

Table 5.3 INPUT/OUTPUT Equivalent circuit

Pin name	Input / Output	Equivalent circuit
PHASEA PHASEB INA1 INA2 INB1 INB2 STBY BRAKE	Logic input (VIH/VIL) VIH: 2.0 V(min) to 5.5 V(max) VIL: 0 V(min) to 0.8 V(max)	
ERR ALM	Logic output (VOH/VOL) (Pullup resistance:10 k to 100 kΩ)	
VCC VREF	VCC voltage range 4.75 V(min) to 5.0 V(typ.) to 5.25 V(max) VREF input voltage range 0 V to 4.0 V (Constant current control) VCC short(Constant current control: off)	
OSCM	OSCM frequency setup 0.82 MHz(min) to 3.2 MHz(typ.) to 8.2 MHz(max) (ROSCM=3.9 kΩ to 10 kΩ to 39 kΩ)	
OUT A+ OUT A- OUT B+ OUT B- RSGNDA RSGNDB VCOM	VM voltage range 10 V(min) to 40 V(max) Motor output pin voltage range 10 V(min) to 80 V(max)	

Note: The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

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6. Functional Description

The current is defined as ‘plus’ when the current flows from VM to OUT+ during charge status(OUT+ side MOSFET is turned on), and is defined as ‘minus’ when the current flows from VM to OUT- during charge status (OUT- side MOSFET is turned on).

6.1. Step resolution and current settings

6.1.1. Full step

Table 6.1 Step resolution of full step

Ach						Bch					
Logic signal			MOSFET		Current	Logic signal			MOSFET		Current
PHASEA	INA1	INA2	OUTA+	OUTA-	IOUT(A)	PHASEB	INB1	INB2	OUTB+	OUTB-	IOUT(B)
H	H	H	ON	OFF	+100 %	H	H	H	ON	OFF	+100 %
L	H	H	OFF	ON	-100 %	H	H	H	ON	OFF	+100 %
L	H	H	OFF	ON	-100 %	L	H	H	OFF	ON	-100 %
H	H	H	ON	OFF	+100 %	L	H	H	OFF	ON	-100 %

Note: About MOSFETs: motor output pin level will show ‘Low’ when ‘ON’, and pin level will show ‘Hi-Z’ when OFF.

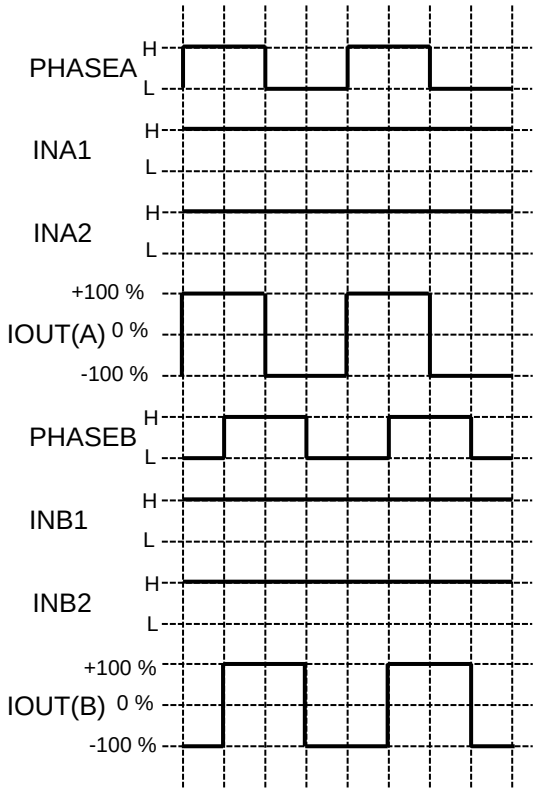


Figure 6.1 Full step timing chart

Note: Timing charts may be simplified for explanatory purpose.

6.1.2. Half step

Table 6.2 Step resolution of half step

Ach						Bch					
Logic signal			MOSFET		Current	Logic signal			MOSFET		Current
PHASEA	INA1	INA2	OUTA+	OUTA-	IOUT(A)	PHASEB	INB1	INB2	OUTB+	OUTB-	IOUT(B)
H	H	H	ON	OFF	+100 %	H	H	H	ON	OFF	+100 %
L or H	L	L	OFF	OFF	0 %	H	H	H	ON	OFF	+100 %
L	H	H	OFF	ON	-100 %	H	H	H	ON	OFF	+100 %
L	H	H	OFF	ON	-100 %	L or H	L	L	OFF	OFF	0 %
L	H	H	OFF	ON	-100 %	L	H	H	OFF	ON	-100 %
L or H	L	L	OFF	OFF	0 %	L	H	H	OFF	ON	-100 %
H	H	H	ON	OFF	+100 %	L	H	H	OFF	ON	-100 %
H	H	H	ON	OFF	+100 %	L or H	L	L	OFF	OFF	0 %

Note: About MOSFETs: motor output pin level will show ‘Low’ when ‘ON’, and pin level will show ‘Hi-Z’ when OFF.

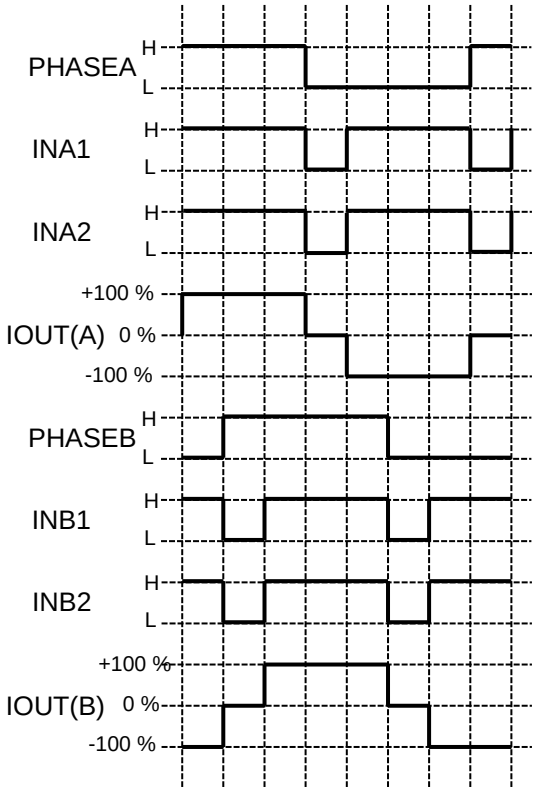


Figure 6.2 Half step timing chart

Note: Timing charts may be simplified for explanatory purpose.

6.1.3. Quarter step

Table 6.3 Step resolution of quarter step

Ach						Bch					
Logic signal			MOSFET		Current	Logic signal			MOSFET		Current
PHASEA	INA1	INA2	OUTA+	OUTA-	IOUT(A)	PHASEB	INB1	INB2	OUTB+	OUTB-	IOUT(B)
H	H	L	ON	OFF	+71 %	H	H	L	ON	OFF	+71 %
H	L	H	ON	OFF	+38 %	H	H	H	ON	OFF	+100 %
L or H	L	L	OFF	OFF	0 %	H	H	H	ON	OFF	+100 %
L	L	H	OFF	ON	-38 %	H	H	H	ON	OFF	+100 %
L	H	L	OFF	ON	-71 %	H	H	L	ON	OFF	+71 %
L	H	H	OFF	ON	-100 %	H	L	H	ON	OFF	+38 %
L	H	H	OFF	ON	-100 %	L or H	L	L	OFF	OFF	0 %
L	H	H	OFF	ON	-100 %	L	L	H	OFF	ON	-38 %
L	H	L	OFF	ON	-71 %	L	H	L	OFF	ON	-71 %
L	L	H	OFF	ON	-38 %	L	H	H	OFF	ON	-100 %
L or H	L	L	OFF	OFF	0 %	L	H	H	OFF	ON	-100 %
H	L	H	ON	OFF	+38 %	L	H	H	OFF	ON	-100 %
H	H	L	ON	OFF	+71 %	L	H	L	OFF	ON	-71 %
H	H	H	ON	OFF	+100 %	L	L	H	OFF	ON	-38 %
H	H	H	ON	OFF	+100 %	L or H	L	L	OFF	OFF	0 %
H	H	H	ON	OFF	+100 %	H	L	H	ON	OFF	+38 %

Note: About MOSFETs: motor output pin level will show ‘Low’ when ‘ON’, and pin level will show ‘Hi-Z’ when OFF.

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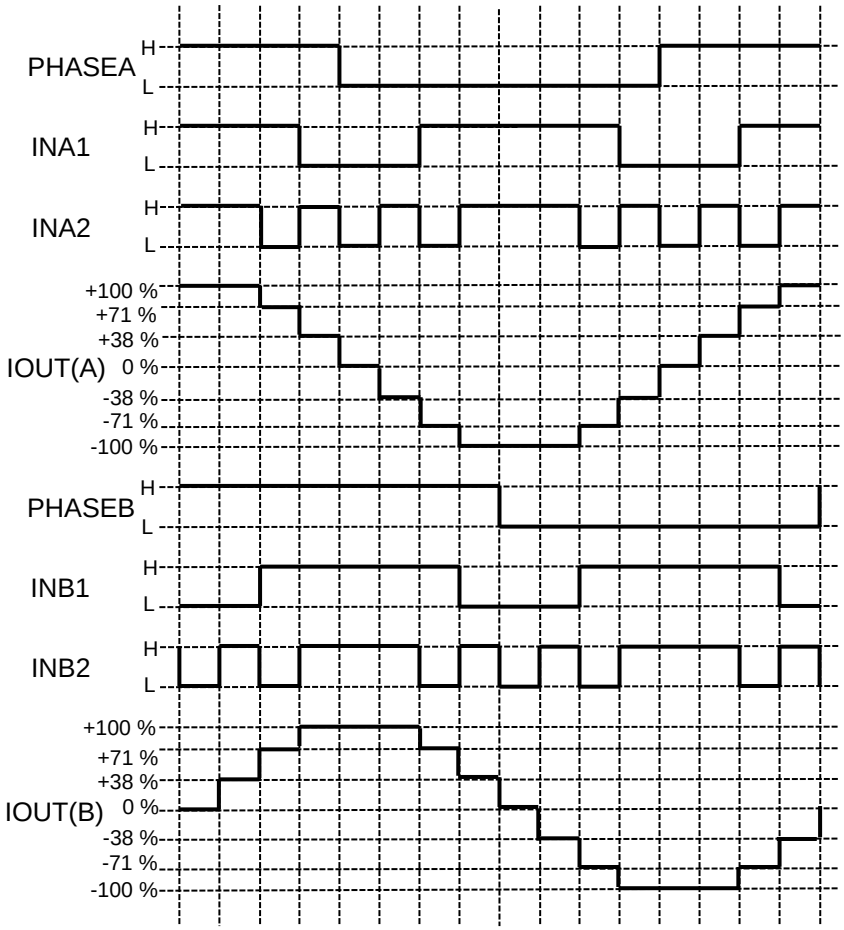


Figure 6.3 Quarter step timing chart

Note: Timing charts may be simplified for explanatory purpose.

6.2. BREAK mode function

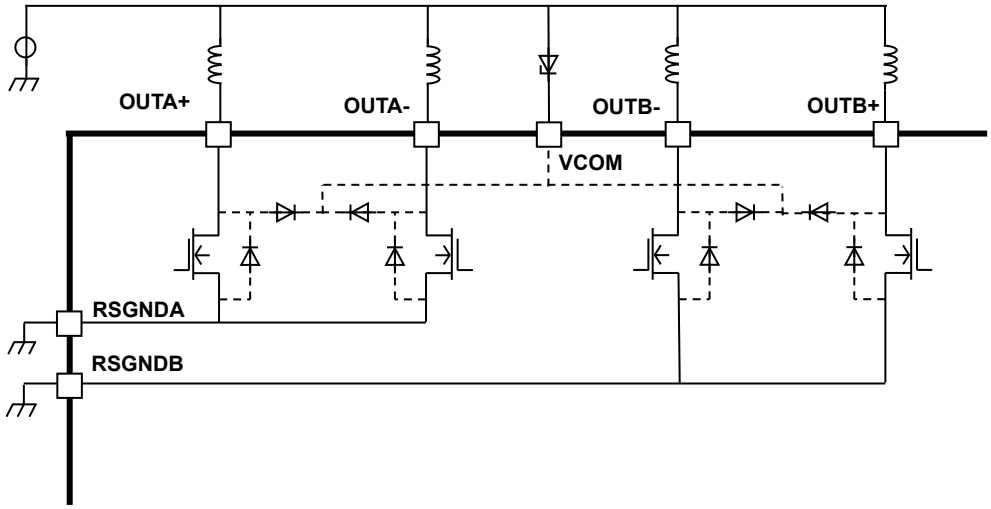


Figure 6.4 BREAK mode equivalent circuit

Equivalent circuit(s) may be omitted for explanatory purpose.

Table 6.4 BREAK mode function

BRAKE	Function
H	Brake mode: ON
L	Brake mode OFF (Normal operation)

(During Constant current control; VREF≤4.0V)

Phase status when BRAKE is set to 'High'	IOUT
PHASE=L	-100 %
PHASE=H	+100 %

Note: When the PHASE signal is switched during BRAKE=H, the current flow will also be switched, as shown in the table above. (For example, when PHASE is switched from 'Low' to 'High', the current control will be switched from OUT(-) side to OUT(+) side.)

Note: When BRAKE is set to High, the current setting will be set to 100 %; regardless of IN1 and IN2 input.

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(During Constant current control “off”; VREF-VCC direct connected)

When BRAKE is set to ‘High’; All four output MOSFETs(OUTA+,A-,B+,B-) will turn on.

Example: Relation between BRAKE mode and current setting
(BRAKE mode during Quarter step operation.)

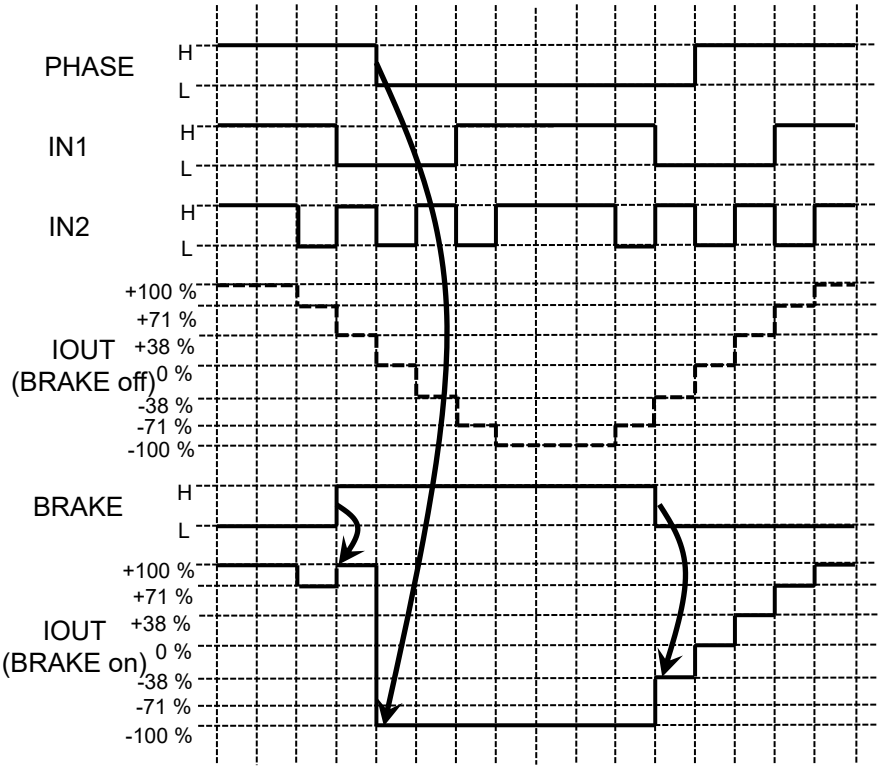


Figure 6.5 Relation between BRAKE mode and current setting

Note: Timing charts may be simplified for explanatory purpose.
When BRAKE is set to ‘High, the current will be determined by PHASE input. Also, the current setting will be set to 100 %; regardless of IN1 and IN2.

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6.3. Standby mode function

Setting the STBY pin will enable the device to be set to Standby mode (=Low power mode) which will cut all unnecessary internal bais current to reduce power consumption. The ISD(Over current)/TSD(Thermal shutdown) status can also be reseted by STBY.

Table 6.5 Standby mode function

STBY	Function
H	Standby mode: OFF(normal operation)
L	Standby mode: ON(Low power mode)

The ISD(Over current)/TSD(Thermal shutdown) status will be reseted when STBY is set to Low.

Note: After STBY is set to High, the internal circuit will restart from low power mode. Therefore don't input any logic signal for 10 μs, after the STBY is set to High. (If the logic signal is input to the device during wake-up period, the device may not be able to receive the signal correctly.)

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6.4. ERR pin functions (ERR feedback)

Table 6.6 ERR pin functions

ERR	Function
Hi-Z (Note)	Normal operation
Low	Error detected (TSD or ISD)

Note: The ERR pin is an open drain logic output. To use the function correctly, please make sure the ERR pin is connected to 3.3 V or 5.0 V with a pull-up resistance. During normal operation, the pin level will be Hi-Z (internal MOSFET:OFF) (it will show High level when pulled up), and once an error (TSD or ISD) has been detected, the pin level will be Low (internal MOSFET: ON).
Reasserting the VM power supply or using the STBY function, the ERR pin will return to the initial status (internal MOSFET: OFF).
ERR pin should be left open; when not using the ERR feedback function.

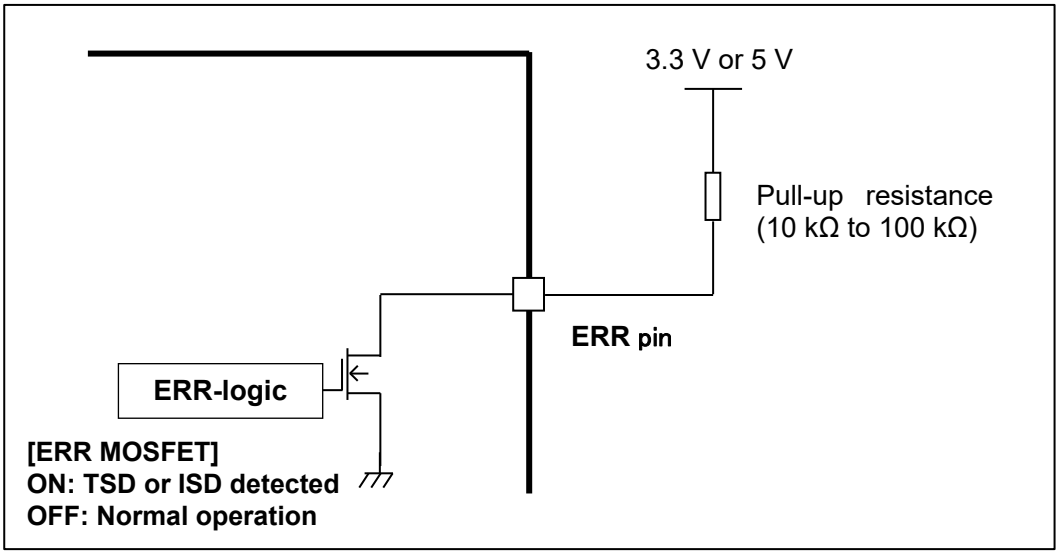


Figure 6.6 ERR pin equivalent circuit

Note: Equivalent circuit(s) may be omitted for explanatory purpose.

6.5. ALM pin functions (Thermal ALM feedback)

Table 6.7 ALM pin functions

ALM	Function
Hi-Z (Note)	Normal operation
Low	Thermal Alarm detected

Note: The ALM pin is an open drain logic output. To use the function correctly, please make sure the ALM pin is connected to 3.3 V or 5.0 V with a pull-up resistance. During normal operation, the pin level will be Hi-Z (internal MOSFET:OFF) (it will show High level when pulled up), and once the device detects a temperature rise, the pin level will be Low (internal MOSFET: ON).
The ALM is an auto recovery type output. Once the device reaches the ALM detect threshold(120 °C±15 °C), the pin level will show Low (internal MOSFET:ON), and after the device reaches the ALM release threshold ('detect threshold'-30 °C), the pin level will show Hi-Z (internal MOSFET:OFF) (it will show High level when pulled up)
ALM pin should be left open; when not using the thermal ALM feedback function.

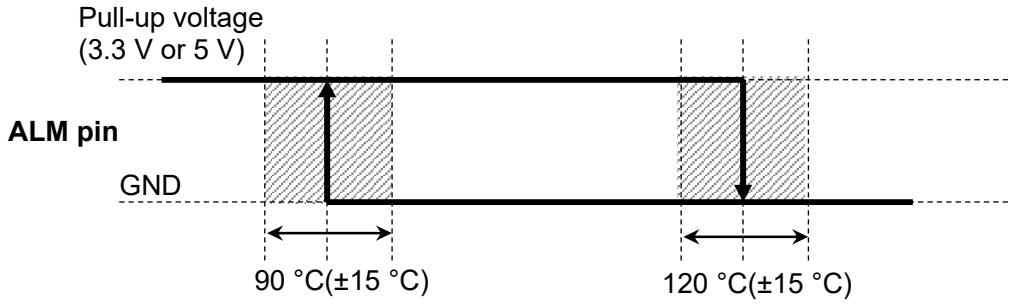


Figure 6.7 ALM pin setting

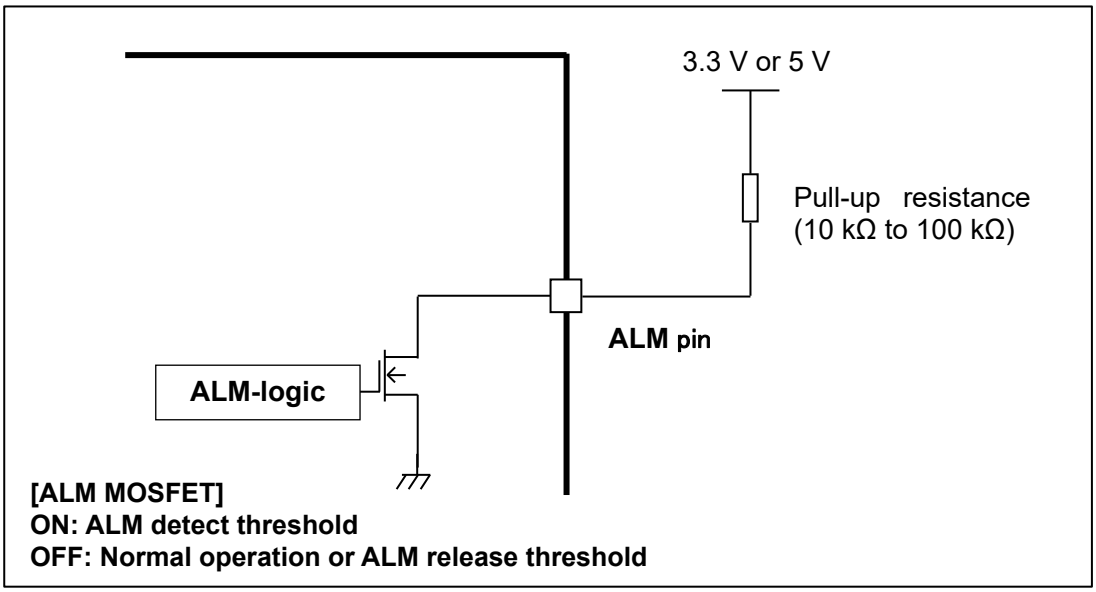


Figure 6.8 ALM pin equivalent circuit

Note: Timing charts may be simplified for explanatory purpose.
Equivalent circuit(s) may be omitted for explanatory purpose.

6.6. TB67S141FTG setup

6.6.1. Constant-current threshold setting

The constant-current threshold can be set by VREF voltage.

Iout(max)=VREF × 3/4

Example: Current setting 100 %, VREF=2.0 V: The constant current threshold(peak current) will be as shown below.

Iout = 2.0×3/4=1.5 A

To set the constant-current function ‘off’, connect the VCC and VREF pin directly (do not use any external power supply).

6.6.2. Fixed off time setting

To set the fixed off time for constant-current PWM control, please connect a pull-down resistance to the OSCM pin.
The relation between the pull-down resistance(ROSCM) and fixed off time is as shown below.

(For reference)

Table 6.8 Fixed off time setting

Pull-down resistance (ROSCM)	Fixed off time (toff)
3.9 kΩ	4.1 μs
4.7 kΩ	4.9 μs
5.6 kΩ	5.8 μs
6.8 kΩ	7.0 μs
8.2 kΩ	8.3 μs
10 kΩ	10 μs
15 kΩ	15 μs
18 kΩ	18 μs
22 kΩ	21 μs
27 kΩ	26 μs
39 kΩ	37 μs

Note: The value shown in the table above does not include any dispersion of the device / external components.

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6.6.3. OFF TIME for PHASE switching

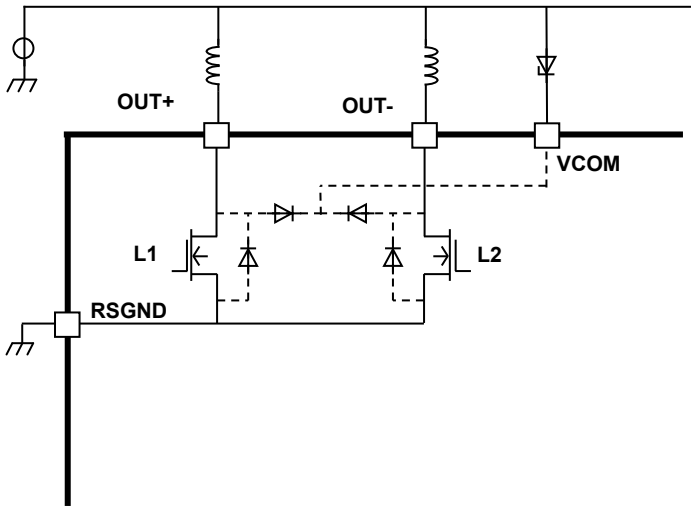


Figure 6.9 OFF TIME for PHASE switching equivalent circuit

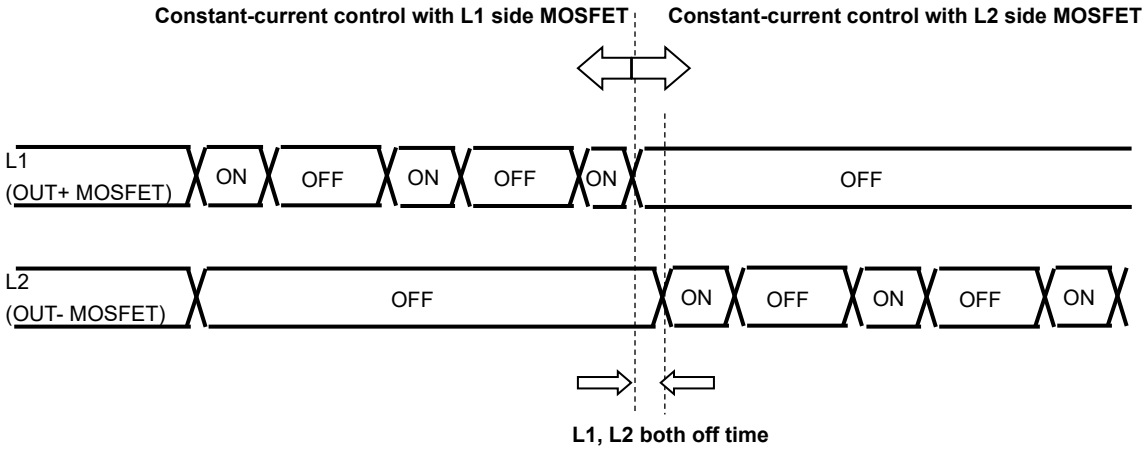


Figure 6.10 OFF TIME for PHASE switching timing chart

Note: Timing charts may be simplified for explanatory purpose.

When the PHASE signal is switched from Low to High or High to Low (the above timing chart is one example), there is an
off time, to avoid both OUT+ and OUT- MOSFET to turn ON at the same time.
Using the internal system oscillator (fOSCS=6.4 MHz), the switching time is about 3CLK (including the synchronous time
difference; 1+3CLK=4CLK at the most): the off time is about 470 to 625 ns.

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7. Absolute Maximum Ratings

Table 7.1 Absolute Maximum Ratings（Ta=25 °C）

Characteristics		Symbol	Rating	Unit
Motor power supply		VM(max)	45	V
VM-VCOM voltage differential		VDIFF(max)	45	V
Motor output voltage		VOUT(max)	84	V
Motor output current (per channel)		IOUT(max)	3.0	A
Internal logic power supply		VCC(max)	6.0	V
Logic input voltage		VIN(H)(max)	6.0	V
		VIN(L)(min)	-0.4	V
VREF input voltage		VREF(max)	6.0	V
Open drain output pin (ERR,ALM,MO) voltage		VOD(max)	6.0	V
Open drain output pin (ERR,ALM,MO) inflow current		IOD(max)	20	mA
Power dissipation	Device alone(Note1)	PD	1.3	W
	When mounted on a PCB(Note2)		4.1	W
Operating temperature		Topr	-20 to 85	°C
Storage temperature		Tstr	-55 to 150	°C
Junction temperature		Tj(max)	150	°C

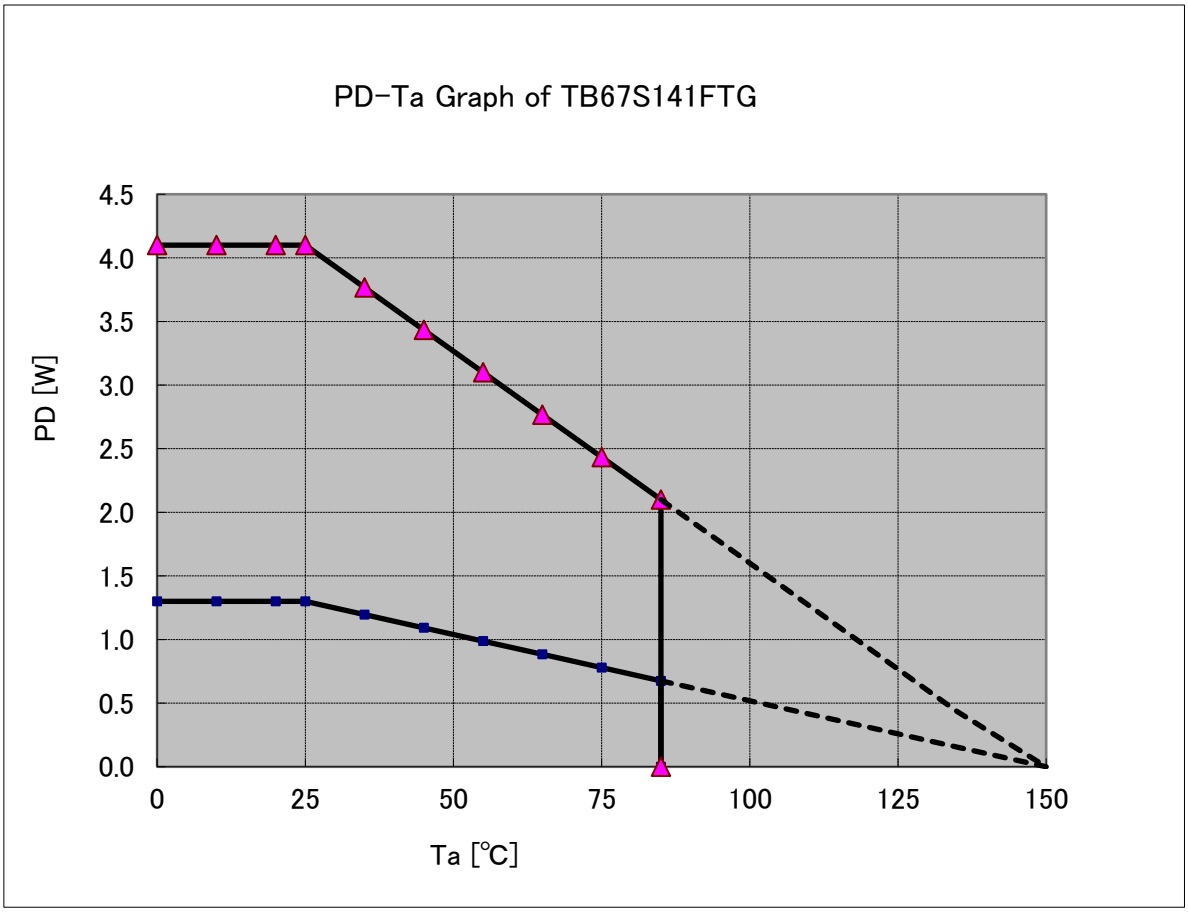
Note 1: Device alone. (Ta =25 °C)
If the ambient temperature is above 25 °C, the power dissipation must be de-rated by 10.4 mW/°C.
Note 2: When mounted on a specially designed PCB (4-layer, Ta =25 °C)
If the ambient temperature is above 25 °C, the power dissipation must be de-rated by 32.8 mW/°C.

Caution）Absolute maximum ratings

The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.
Exceeding the rating(s) may cause device breakdown, damage or deterioration, and may result in injury by explosion or combustion.
The value of even one parameter of the absolute maximum ratings should not be exceeded under any circumstances. The device does not have overvoltage detection circuit. Therefore, the device is damaged if a voltage exceeding its rated maximum is applied.
All voltage ratings, including supply voltages, must always be followed. The other notes and considerations described later should also be referred to.

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(For reference) PD-Ta graph



(1) … Device alone
(2) … When mounted to a 4 layer glass epoxy board (power dissipation example of Rth(j-a)=25 °C/W (when mounted); dependent on board and mount condition.)

Figure7 (For reference) PD-Ta graph

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8. Operating Ranges

Table 8.1 Operating Ranges

Characteristics	Symbol	Test condition	Min	Typ.	Max	Unit
Motor power supply	VM	-	10	-	40	V
Motor output voltage	VOUT	-	10	-	80	V
Motor output current (per channel)	IOUT	Ta=25 °C	-	1.5	3.0	A
Internal logic power supply	VCC	-	4.75	5.0	5.25	V
Logic input voltage	VIN(H)	Logic input high level	2.0	-	5.5	V
	VIN(L)	Logic input low level	0	-	0.8	V
VREF input voltage range	VREF(range)	-	GND	-	5.5	V
Open drain pin voltage range	VOD(range)	ERR,ALM,MO pin	3.0	-	5.5	V
Open drain pin inflow current range	IOD(range)	ERR,ALM,MO pin	-	-	10	mA
Internal oscillator frequency range	fOSCM(range)	-	820	3200	8200	kHz
Fixed off time range	tOFF(range)	-	5	10	40	μs

Note: The maximum current that can actually be used may be limited by the operating environment (operating conditions such as excitation mode and operating time, ambient temperature conditions, and heat generation conditions such as board conditions). Please confirm the maximum current value that can actually be used after thermal calculation under the operating environment.

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9. Electrical Characteristics

9.1. Electrical Characteristics 1 (Ta = 25 °C, VM = 24 V, unless otherwise specified)

Table 9.1 Electrical Characteristics 1

Characteristics		Symbol	Test condition	Min	Typ.	Max	Unit
Logic input voltage		VIH	Logic input pin High level (Note)	2.0	-	5.5	V
		VIL	Logic input pin Low level (Note)	GND	-	0.8	V
Logic input hysteresis voltage		VIN(HYS)	Logic input pin (Note)	100	-	300	mV
Logic input current	High	IIN(H)	Logic input voltage High level (VIN=VIH)	-	33	55	μA
	Low	IIN(L)	Logic input voltage Low level (VIN=VIL)	-	-	1	μA
Power consumption		IM1	Output pins=open, Standby mode	-	-	1.0	mA
		IM2	Output pins=open, Normal operation, Motor output section operation (Full step resolution)	-	3.0	5.0	mA
Open drain output pin voltage		VOD(L)	IOD=10 mA	0	-	0.5	V
Motor current channel differential		⊿IOUT1	Current differential between channels (IOUT=1.0 A)	-5	0	+5	%
Motor current setting accuracy		⊿IOUT2	IOUT=1.0 A	-6	0	+6	%
Source-drain diode forward voltage		VFN	IOUT=2.0 A	1.0	-	1.6	V
Motor output off leak current		Ileak	VOUT=80V, Output MOSFET:OFF	-	-	1	μA
Motor output ON-resistance (Low side)		RON(D-S)	IOUT=2.0 A	-	0.25	0.35	Ω

Note: VIN (H) is defined as the VIN voltage that causes the outputs (OUTA, OUTB) to change when a pin under test is gradually raised from 0 V. VIN (L) is defined as the VIN voltage that causes the outputs (OUTA, OUTB) to change when the pin is then gradually lowered. The difference between VIN (L) and VIN (H) is defined as VIN(HYS).

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9.2. Electrical Specifications 2 (Ta =25 °C, VM = 24 V, unless otherwise specified)

Table 9.2 Electrical Characteristics 2

Characteristics	Symbol	Test condition	Min	Typ.	Max	Unit
VCC regulator voltage	VCC	ICC=5.0 mA	4.75	5	5.25	V
VCC regulator current	ICC	4.75 V≤VCC≤5.25 V	-	2.5	5.0	mA
VREF input current	IREF	VREF=2.0 V	-	0	1.0	μA
Thermal shutdown(TSD） threshold (Note1)	TjTSD	-	140	155	170	°C
VCC recovery voltage	VCCR	-	3.5	4.0	4.5	V
VM recovery voltage	VMR	-	7.0	8.0	9.0	V
Over-current detection(ISD) threshold (Note2)	ISD	-	3.1	4.0	5.0	A

Note1: About Thermal shutdown (TSD)
When the junction temperature of the device reached the TSD threshold, the TSD circuit is triggered; the internal reset circuit then turns off the output transistors. Noise rejection blanking time is built-in to avoid misdetection. Once the TSD circuit is triggered; the detect latch signal can be cleared by reasserting the VM power source, or setting the device to standby mode. The TSD circuit is a backup function to detect a thermal error, therefore is not recommended to be used aggressively.

Note2: About Over-current detection (ISD)
When the output current reaches the threshold, the ISD circuit is triggered; the internal reset circuit then turnsoff the output transistors. Once the ISD circuit is triggered, the detect latch signal can be cleared by reasserting the VM power source, or setting the device to standby mode. For fail-safe, please insert a fuse to avoid secondary trouble.

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9.3. Electrical Specifications 3 (Ta =25 °C, VM = 24 V, unless otherwise specified)

Table 9.3 Electrical Characteristics 3

Characteristics	Symbol	Test condition	Min	Typ.	Max	Unit
Current ratio	-	IN1=H, IN2=H	-	100	-	%
		IN1=H, IN2=L	66	71	76	%
		IN1=L, IN2=H	33	38	43	%
		IN1=L, IN2=L	-	0	-	%

Back-EMF

While a motor is rotating, there is a timing at which power is fed back to the power supply. At that timing, the motor current recirculates back to the power supply due to the effect of the motor back-EMF.
If the power supply does not have enough sink capability, the power supply and output pins of the device might rise above the rated voltages. The magnitude of the motor back-EMF varies with usage conditions and motor characteristics. It must be fully verified that there is no risk that the device or other components will be damaged or fail due to the motor back-EMF.

Cautions on Over-current Detection (ISD) and Thermal Shutdown (TSD)

The ISD and TSD circuits are only intended to provide temporary protection against irregular conditions such as an output short-circuit; they do not necessarily guarantee the complete IC safety.
If the device is used beyond the specified operating ranges, these circuits may not operate properly: then the device may be damaged due to an output short-circuit.
The ISD circuit is only intended to provide a temporary protection against an output short-circuit. If such condition persists for a long time, the device may be damaged due to overstress. Over-current conditions must be removed immediately by external hardware.

IC Mounting

Do not insert devices incorrectly or in the wrong orientation. Otherwise, it may cause breakdown, damage and/or deterioration of the device.

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9.4. AC Electrical Specification (Ta =25 °C, VM = 24 V, unless otherwise specified)

Table 9.4 AC Electrical Characteristics

Characteristics	Symbol	Test condition	Min	Typ.	Max	Unit
CLK input frequency	fCLK	fOSCM=3200 kHz	-	-	400	kHz
Minimum CLK pulse width	tCLK(twp)	-	50	-	-	ns
	tCLK(twn)	-	50	-	-	ns
Output MOSFET switching specific (rise time, fall time)	tr	-	50	100	150	ns
	tf	-	50	100	150	ns
Output MOSFET switching specific (CLK-OUT response time)	tpLH(CLK)	CLK→OUT	200	700	1200	ns
	tpHL(CLK)	CLK→OUT	200	700	1200	ns
Analog noise blanking time	AtBLK	Analog tblank	250	400	550	ns
OSCM frequency	fOSCM	ROSCM=10 kΩ	2720	3200	3680	kHz
OSCS frequency	fOSCS	-	5120	6400	7680	kHz
Fixed off time	tOFF	fOSCM=3.2 MHz	8.5	10	11.5	μs
Over current (ISD) detect masking time	tISD(mask)	fOSCS=6.4 MHz,8clk	1.0	1.25	1.5	μs
Thermal shutdown (TSD) detect masking time	tTSD(mask)	fOSCS=6.4 MHz,32clk	4.0	5.0	6.0	μs
Thermal Alarm(ALM) detect masking time	tALM(mask)	fOSCS=6.4 MHz,16clk	2.0	2.5	3.0	μs

AC specification timing chart

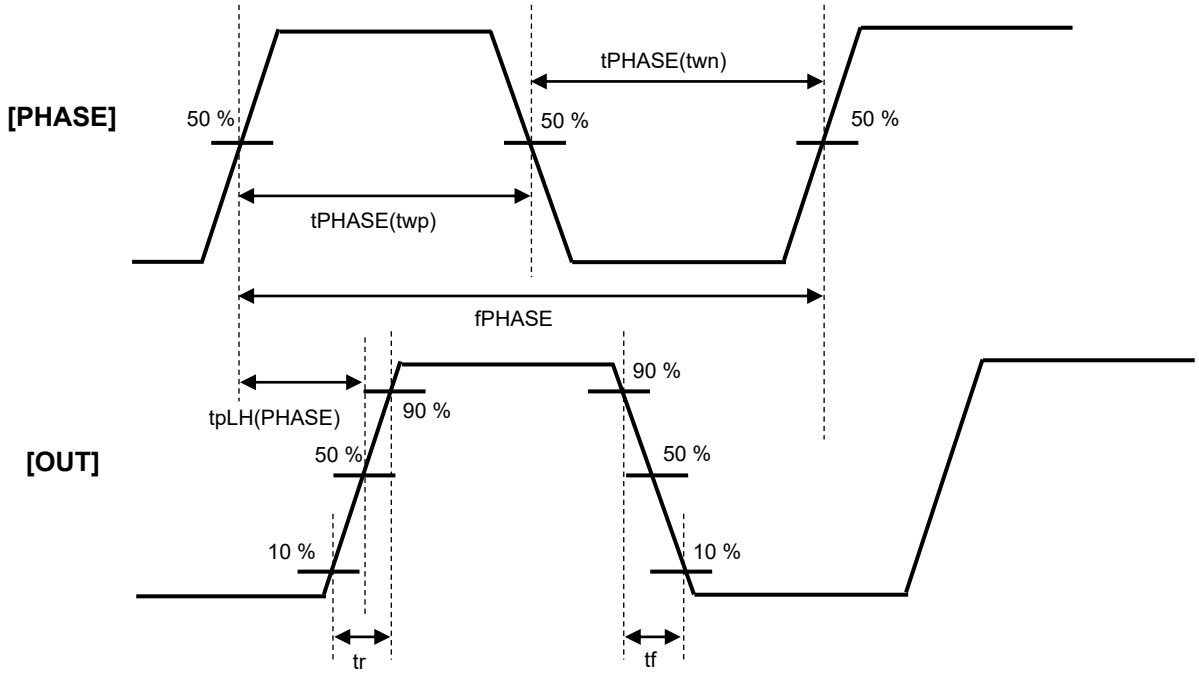


Figure 9.1 AC Timing chart

Note: Timing charts may be simplified for explanatory purpose.

10. Application Circuit Example

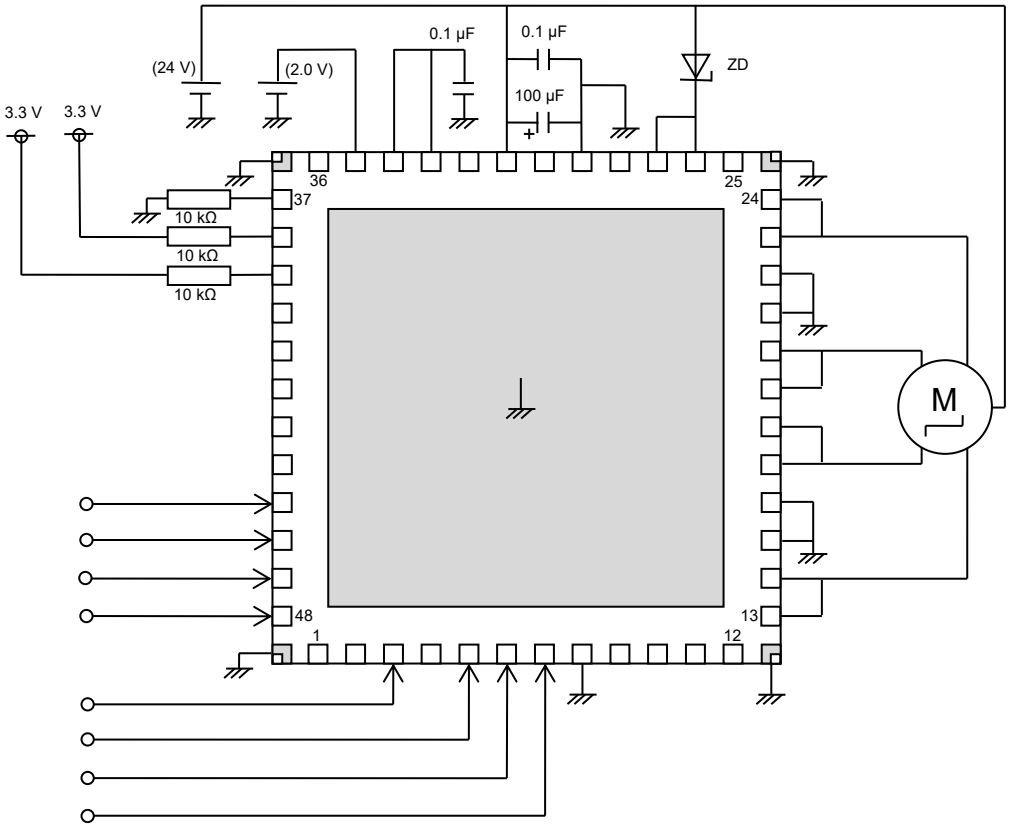


Figure 10.1 Application Circuit Example

Note: Please mount the four corner pins of the QFN package and the exposed pad to the GND area of the PCB.
The application circuit above is an example; therefore, mass-production design is not guaranteed.

Notes on Contents

Block Diagrams

Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

Equivalent Circuits

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

Timing Charts

Timing charts may be simplified for explanatory purposes.

Application Circuits

The application circuits shown in this document are provided for reference purposes only. Thorough evaluation is required, especially at the mass-production design stage.

Toshiba does not grant any license to any industrial property rights by providing these examples of application circuits.

Test Circuits

Components in the test circuits are used only to obtain and confirm the device characteristics. These components and circuits are not guaranteed to prevent malfunction or failure from occurring in the application equipment.

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11. IC Usage Considerations

11.1. Notes on Handling of ICs

(1) The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings. Exceeding the rating(s) may cause device breakdown, damage or deterioration, and may result in injury by explosion or combustion.

(2) Use an appropriate power supply fuse to ensure that a large current does not continuously flow in the case of over-current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead to smoke or ignition. To minimize the effects of the flow of a large current in the case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.

(3) If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition. Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.

(4) Do not insert devices in the wrong orientation or incorrectly. Make sure that the positive and negative terminals of power supplies are connected properly.
Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause device breakdown, damage or deterioration, and may result in injury by explosion or combustion.
In addition, do not use any device inserted in the wrong orientation or incorrectly to which current is applied even just once.

(5) Carefully select external components (such as inputs and negative feedback capacitors) and load components (such as speakers), for example, power amp and regulator.
If there is a large amount of leakage current such as from input or negative feedback condenser, the IC output DC voltage will increase. If this output voltage is connected to a speaker with low input withstand voltage, over-current or IC failure may cause smoke or ignition. (The over-current may cause smoke or ignition from the IC itself.) In particular, please pay attention when using a Bridge Tied Load (BTL) connection-type IC that inputs output DC voltage to a speaker directly.

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11.2. Points to Remember on Handling of ICs

Over-current detection Circuit

Over-current detection circuits (referred to as current limiter circuits) do not necessarily protect ICs under all circumstances. If the over-current detection circuits operate against the over-current, clear the over-current status immediately.Depending on the method of use and usage conditions, exceeding absolute maximum ratings may cause the over-current detection circuit to operate improperly or IC breakdown may occur before operation. In addition, depending on the method of use and usage conditions, if over-current continues to flow for a long time after operation, the IC may generate heat resulting in breakdown.

Thermal Shutdown Circuit

Thermal shutdown circuits do not necessarily protect ICs under all circumstances. If the thermal shutdown circuits operate against the over-temperature, clear the heat generation status immediately.
Depending on the method of use and usage conditions, exceeding absolute maximum ratings may cause the thermal shutdown circuit to operate improperly or IC breakdown to occur before operation.

Heat Radiation Design

When using an IC with large current flow such as power amp, regulator or driver, design the device so that heat is appropriately radiated, in order not to exceed the specified junction temperature (TJ) at any time or under any condition. These ICs generate heat even during normal use. An inadequate IC heat radiation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, when designing the device, take into consideration the effect of IC heat radiation with peripheral components.

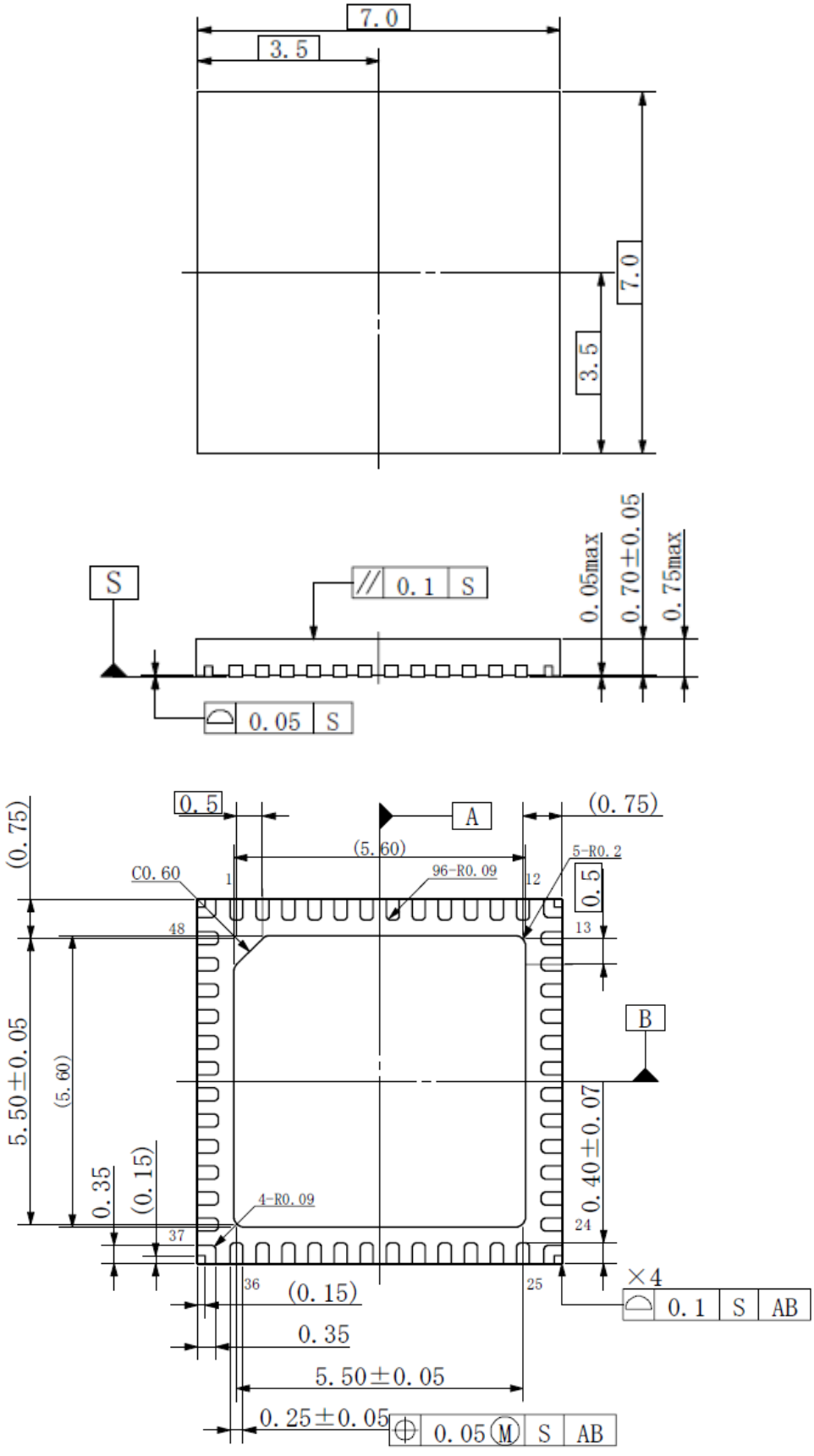
Back-EMF

When a motor reverses the rotation direction, stops or slows abruptly, current flows back to the motor's power supply owing to the effect of back-EMF. If the current sink capability of the power supply is small, the device's motor power supply and output pins might be exposed to conditions beyond the absolute maximum ratings. To avoid this problem, take the effect of back-EMF into consideration in system design.

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12. Package Information

12.1. Package Dimensions (Unit:mm): P-WQFN48-0707-0.50-003



Weight: 0.1 g (typ.)

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