TOSHIBA

© 2020 Toshiba Electronic Devices & Storage Corporation

RD Number: RD072

RD Title: TB67S213FTAG Evaluation circuit BOM

Item No.	Designator	Quantity	Value	Part Number	Manufacturer	Description	Package	Not Mount
1	IC1	1	TB67S213FTAG	TB67S213FTAG	TOSHIBA	Motor driver IC	QFN36	
2	C_VCC	1	0.1µF 25V	—	—	Chip capacitor	3.2mm×1.6mm	
3	C_VM2	1	0.1µF 50V	-	—	Chip capacitor	3.2mm×1.6mm	
4	C_VRFA	1	0.1µF 25V	_	_	Chip capacitor	3.2mm×1.6mm	
5	C_VRFB	1	0.1µF 25V	-	-	Chip capacitor	3.2mm×1.6mm	
6	C_OAP	0	0.1µF 25V	-	—	Chip capacitor	3.2mm×1.6mm	√
7	C_OAM	0	0.1µF 25V	-	-	Chip capacitor	3.2mm×1.6mm	√
8	C_OBM	0	0.1µF 25V	—	—	Chip capacitor	3.2mm×1.6mm	√
9	C_OBP	0	0.1µF 25V	-	-	Chip capacitor	3.2mm×1.6mm	√
10	C_VM1	1	100µF 50V	-	-	Electrolytic capacitor		
11		0	Socket pin	—	—	Socket pin		√
12	C_VDD	1	10µF 25V	-	—	Electrolytic capacitor		
13		0	Socket pin	-	-	Socket pin		√
14	C_OSCM	1	270pF 25V	—	—	Chip capacitor	3.2mm×1.6mm	
15		0	270pF 25V	-	-	Lead capacitor	2.54mm pitch	√
16		0	Socket pin	-	—	Socket pin		√
17	CON1	1	Connector	-	-	CONN HEADER VERT 4POS		
18	OSCM	1	Check terminal	-	—	Check terminal for oscilloscope		
19	OUT_A-	1	Check terminal	-	—	Check terminal for logic		
20	OUT_A+	1	Check terminal	-	-	Check terminal for logic		
21	OUT_B-	1	Check terminal	_	_	Check terminal for logic		
22	OUT_B+	1	Check terminal	_	_	Check terminal for logic		
23	RSA	0	Check terminal	_	—	Check terminal for oscilloscope		√
24	RSB	0	Check terminal	_	_	Check terminal for oscilloscope		√
25	VCC	1	Check terminal	-	_	Check terminal for oscilloscope		

-				1	1	1		r
26	VDD	1	Check terminal	—	—	Check terminal for logic		
27	VM	1	Check terminal	_	_	Check terminal for logic		
28	VREFA	1	Check terminal	_	_	Check terminal for oscilloscope		
29	VREFB	1	Check terminal	_	_	Check terminal for logic		
30	CW/CCW	1	Check terminal	—	—	Check terminal for oscilloscope		
31	МО	1	Check terminal	—	—	Check terminal for oscilloscope		
32	D_MODE1	1	Check terminal	_	—	Check terminal for oscilloscope		
33	D_MODE2	1	Check terminal	—	—	Check terminal for oscilloscope		
34	CLK	1	Check terminal	_	—	Check terminal for oscilloscope		
35	ENABLE	1	Check terminal	_	—	Check terminal for oscilloscope		
36	RESET	1	Check terminal	—	—	Check terminal for oscilloscope		
37	GND	1	Check terminal	—	—	Check terminal for logic		
38	GND	1	Check terminal	—	—	Check terminal for logic		
39	GND	0	Check terminal	_	—	Check terminal for logic		√
40	GND	0	Check terminal	—	—	Check terminal for logic		\checkmark
41	GND	0	Check terminal	_	—	Check terminal for logic		\checkmark
42	GND	0	Check terminal	—	—	Check terminal for logic		\checkmark
43	GND	0	Check terminal	—	—	Check terminal for logic		\checkmark
44	JP_VRF1	1	Pin header 2P	_	—	Single row plugs		
45		1	Jump socket	_	—	Position Shunt Connector		
46	JP_VRF2	1	Pin header 2P	—	—	Single row plugs		
47		1	Jump socket	—	—	Position Shunt Connector		
48	JP_VCC	1	Pin header 2P	—	—	Single row plugs		
49		1	Jump socket	_	—	Position Shunt Connector		
50	R_MOUT	0	100kΩ 0.25W	—	—	Leaded resistor	2.54mm pitch	\checkmark
51		0	Socket pin	_	—	Socket pin		\checkmark
52	R_OSCM	1	3.6kΩ	_	—	Chip resistor	3.2mm×1.6mm	
53		0	3.6kΩ	_	—	Leaded resistor	2.54mm pitch	\checkmark
54		0	Socket pin	_	_	Socket pin		\checkmark
55	R_VRF1	0	Socket pin	_	—	Socket pin		√
56		0	Not mount	_	—	Leaded resistor	2.54mm pitch	\checkmark
57	R_VRF2	0	Socket pin	_	_	Socket pin		√

58		0	Not mount	_	_	Leaded resistor	2.54mm pitch	√
59	R_RSA	1	0.22Ω 1W	—	—	Chip resistor	5.0mm×2.5mm	
60	R_RSB	1	0.22Ω 1W	—	—	Chip resistor	5.0mm×2.5mm	
61	SW1	0	Toggle Switch	—	-	SPDT Toggle Switch		\checkmark
62		1	Pin header 3P	—	—	Single row plugs		
63		1	Jump socket	—	—	Position Shunt Connector		
64	SW2	0	Toggle Switch	—	-	SPDT Toggle Switch		\checkmark
65		1	Pin header 3P	—	—	Single row plugs		
66		1	Jump socket	—	-	Position Shunt Connector		
67	SW3	0	Toggle Switch	—	-	SPDT Toggle Switch		√
68		0	Pin header 3P	—	—	Single row plugs		\checkmark
69		0	Jump socket	—	-	Position Shunt Connector		\checkmark
70	SW4	0	Toggle Switch	—	-	SPDT Toggle Switch		√
71		0	Pin header 3P	—	-	Single row plugs		\checkmark
72		0	Jump socket	—	—	Position Shunt Connector		\checkmark
73	SW5	0	Toggle Switch	—	-	SPDT Toggle Switch		√
74		1	Pin header 3P	—	-	Single row plugs		
75		1	Jump socket	—	—	Position Shunt Connector		
76	SW6	0	Toggle Switch	—	-	SPDT Toggle Switch		\checkmark
77		1	Pin header 3P	—	-	Single row plugs		
78		1	Jump socket	—	—	Position Shunt Connector		
79	SW7	0	Toggle Switch	—	-	SPDT Toggle Switch		√
80		1	Pin header 3P	—	-	Single row plugs		
81		1	Jump socket	_	—	Position Shunt Connector		

Terms of Use

This terms of use is made between Toshiba Electronic Devices and Storage Corporation ("We") and customers who use documents and data that are consulted to design electronics applications on which our semiconductor devices are mounted ("this Reference Design"). Customers shall comply with this terms of use. Please note that it is assumed that customers agree to any and all this terms of use if customers download this Reference Design. We may, at its sole and exclusive discretion, change, alter, modify, add, and/or remove any part of this terms of use at any time without any prior notice. We may terminate this terms of use at any time and for any reason. Upon termination of this terms of use, customers shall destroy this Reference Design. In the event of any breach thereof by customers, customers shall destroy this Reference Design, and furnish us a written confirmation to prove such destruction.

1. Restrictions on usage

1. This Reference Design is provided solely as reference data for designing electronics applications. Customers shall not use this Reference Design for any other purpose, including without limitation, verification of reliability.

2. This Reference Design is for customer's own use and not for sale, lease or other transfer.

3. Customers shall not use this Reference Design for evaluation in high or low temperature, high humidity, or high electromagnetic environments.

4. This Reference Design shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable laws or regulations.

2. Limitations

 We reserve the right to make changes to this Reference Design without notice.
This Reference Design should be treated as a reference only. We are not responsible for any incorrect or incomplete data and information.

3. Semiconductor devices can malfunction or fail. When designing electronics applications by referring to this Reference Design, customers are responsible for complying with safety standards and for providing adequate designs and safeguards for their hardware, software and systems which minimize risk and avoid situations in which a malfunction or failure of semiconductor devices could cause loss of human life, bodily injury or damage to property, including data loss or corruption. Customers must also

refer to and comply with the latest versions of all relevant our information, including without limitation, specifications, data sheets and application notes for semiconductor devices, as well as the precautions and conditions set forth in the "Semiconductor Reliability Handbook".

4. When designing electronics applications by referring to this Reference Design, customers must evaluate the whole system adequately. Customers are solely responsible for all aspects of their own product design or applications. WE ASSUME NO LIABILITY FOR CUSTOMERS' PRODUCT DESIGN OR APPLICATIONS.

5. No responsibility is assumed by us for any infringement of patents or any other intellectual property rights of third parties that may result from the use of this Reference Design. No license to any intellectual property right is granted by this terms of use, whether express or implied, by estoppel or otherwise.

6. THIS REFERENCE DESIGN IS PROVIDED "AS IS". WE (a) ASSUME NO LIABILITY WHATSOEVER, INCLUDING WITHOUT LIMITATION, INDIRECT, CONSEQUENTIAL, SPECIAL, OR INCIDENTAL DAMAGES OR LOSS, INCLUDING WITHOUT LIMITATION, LOSS OF PROFITS, LOSS OF OPPORTUNITIES, BUSINESS INTERRUPTION AND LOSS OF DATA, AND (b) DISCLAIM ANY AND ALL EXPRESS OR IMPLIED WARRANTIES AND CONDITIONS RELATED TO THIS REFERENCE DESIGN, INCLUDING WARRANTIES OR CONDITIONS OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, ACCURACY OF INFORMATION, OR NONINFRINGEMENT.

3. Export Control

Customers shall not use or otherwise make available this Reference Design for any military purposes, including without limitation, for the design, development, use, stockpiling or manufacturing of nuclear, chemical, or biological weapons or missile technology products (mass destruction weapons). This Reference Design may be controlled under the applicable export laws and regulations including, without limitation, the Japanese Foreign Exchange and Foreign Trade Law and the U.S. Export Administration Regulations. Export and re-export of this Reference Design are strictly prohibited except in compliance with all applicable export laws and regulations.

4. Governing Laws

This terms of use shall be governed and construed by laws of Japan.