

RD Number: RD107

RD Title: TB67S522FTAG Evaluation circuit BOM

Item No.	Designator	Quantity	Value	Part Number	Manufacturer	Description	Package	Not Mount
1	C_VCC	1	0.1μF 100V	—	—	Chip capacitor		
2	C_VM2	1	0.1μF 100V	—	—	Chip capacitor		
3	C_VRFA	1	0.1μF 100V	—	—	Chip capacitor		
4	C_VRFB	1	0.1μF 100V	—	—	Chip capacitor		
5	C_OAP	0	0.1μF 100V	—	—	Chip capacitor		✓
6	C_OAM	0	0.1μF 100V	—	—	Chip capacitor		✓
7	C_OBM	0	0.1μF 100V	—	—	Chip capacitor		✓
8	C_OBP	0	0.1μF 100V	—	—	Chip capacitor		✓
9	C_VM1	1	100μF 50V	—	—	Electrolytic capacitor		
10		0	Socket pin	—	—	Socket pin		✓
11	C_VDD	1	10μF 25V	—	—	Electrolytic capacitor		
12		0	Socket pin	—	—	Socket pin		✓
13	C_OSCM	1	270pF 1000V	—	—	Chip capacitor		
14		0	270pF	—	—	Ceramic capacitor		✓
15		0	Socket pin	—	—	Socket pin		✓
16	CON1	1	Connector 4P	—	—	Connector 4P-2.5		
17	OSCM	1	Check terminal	—	—	Check terminal		
18	OUT_A-	1	Check terminal	—	—	Logic pin		
19	OUT_A+	1	Check terminal	—	—	Logic pin		
20	OUT_B-	1	Check terminal	—	—	Logic pin		
21	OUT_B+	1	Check terminal	—	—	Logic pin		
22	RSA	1	Check terminal	—	—	Check terminal		
23	RSB	1	Check terminal	—	—	Check terminal		
24	VCC	1	Check terminal	—	—	Check terminal		
25	VDD	1	Check terminal	—	—	Logic pin		
26	VM	1	Check terminal	—	—	Logic pin		

27	VREFA	1	Check terminal	–	–	Check terminal		
28	VREFB	1	Check terminal	–	–	Logic pin		
29	CW/CCW	1	Check terminal	–	–	Check terminal		
30	MO	1	Check terminal	–	–	Check terminal		
31	D_MODE1	1	Check terminal	–	–	Check terminal		
32	D_MODE2	1	Check terminal	–	–	Check terminal		
33	CLK	1	Check terminal	–	–	Check terminal		
34	ENABLE	1	Check terminal	–	–	Check terminal		
35	RESET	1	Check terminal	–	–	Check terminal		
36	GND	1	Check terminal	–	–	Logic pin		
37	GND	1	Check terminal	–	–	Logic pin		
38	GND	1	Check terminal	–	–	Logic pin		
39	GND	1	Check terminal	–	–	Logic pin		
40	GND	1	Check terminal	–	–	Logic pin		
41	GND	1	Check terminal	–	–	Logic pin		
42	GND	1	Check terminal	–	–	Logic pin		
43	JP_VRF1	1	Pin header 2P	–	–	Jumper		
44		1	Jumper socket	–	–	Jumper Short		
45	JP_VRF2	1	Pin header 2P	–	–	Jumper		
46		1	Jumper socket	–	–	Jumper Short		
47	JP_VCC	1	Pin header 2P	–	–	Jumper		
48		1	Jumper socket	–	–	Jumper Short		
49	R_MOUT	0	100k $\Omega$ 0.25W	–	–	Leaded resistor		✓
50		0	Socket pin	–	–	Socket pin		✓
51	R_OSCM	1	5.1k $\Omega$ 0.25W	–	–	Chip resistor		
52		0	Not mount	–	–	Leaded resistor		✓
53		0	Socket pin	–	–	Socket pin		✓
54	R_VRF1	2	Socket pin	–	–	Socket pin		
55		0	Not mount	–	–	Leaded resistor		✓
56	R_VRF2	2	Socket pin	–	–	Socket pin		
57		0	Not mount	–	–	Leaded resistor		✓
58	R_RSA	1	0.22 $\Omega$ 1W	–	–	Chip resistor		
59	R_RSB	1	0.22 $\Omega$ 1W	–	–	Chip resistor		
60	SW1	1	Pin header 3P	–	–	Jumper		



## Terms of Use

This terms of use is made between Toshiba Electronic Devices and Storage Corporation ("We") and customers who use documents and data that are consulted to design electronics applications on which our semiconductor devices are mounted ("this Reference Design"). Customers shall comply with this terms of use. Please note that it is assumed that customers agree to any and all this terms of use if customers download this Reference Design. We may, at its sole and exclusive discretion, change, alter, modify, add, and/or remove any part of this terms of use at any time without any prior notice. We may terminate this terms of use at any time and for any reason. Upon termination of this terms of use, customers shall destroy this Reference Design. In the event of any breach thereof by customers, customers shall destroy this Reference Design, and furnish us a written confirmation to prove such destruction.

### 1. Restrictions on usage

1. This Reference Design is provided solely as reference data for designing electronics applications. Customers shall not use this Reference Design for any other purpose, including without limitation, verification of reliability.
2. This Reference Design is for customer's own use and not for sale, lease or other transfer.
3. Customers shall not use this Reference Design for evaluation in high or low temperature, high humidity, or high electromagnetic environments.
4. This Reference Design shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable laws or regulations.

### 2. Limitations

1. We reserve the right to make changes to this Reference Design without notice.
2. This Reference Design should be treated as a reference only. We are not responsible for any incorrect or incomplete data and information.
3. Semiconductor devices can malfunction or fail. When designing electronics applications by referring to this Reference Design, customers are responsible for complying with safety standards and for providing adequate designs and safeguards for their hardware, software and systems which minimize risk and avoid situations in which a malfunction or failure of semiconductor devices could cause loss of human life, bodily injury or damage to property, including data loss or corruption. Customers must also

refer to and comply with the latest versions of all relevant our information, including without limitation, specifications, data sheets and application notes for semiconductor devices, as well as the precautions and conditions set forth in the "Semiconductor Reliability Handbook".

4. When designing electronics applications by referring to this Reference Design, customers must evaluate the whole system adequately. Customers are solely responsible for all aspects of their own product design or applications. WE ASSUME NO LIABILITY FOR CUSTOMERS' PRODUCT DESIGN OR APPLICATIONS.
5. No responsibility is assumed by us for any infringement of patents or any other intellectual property rights of third parties that may result from the use of this Reference Design. No license to any intellectual property right is granted by this terms of use, whether express or implied, by estoppel or otherwise.
6. THIS REFERENCE DESIGN IS PROVIDED "AS IS". WE (a) ASSUME NO LIABILITY WHATSOEVER, INCLUDING WITHOUT LIMITATION, INDIRECT, CONSEQUENTIAL, SPECIAL, OR INCIDENTAL DAMAGES OR LOSS, INCLUDING WITHOUT LIMITATION, LOSS OF PROFITS, LOSS OF OPPORTUNITIES, BUSINESS INTERRUPTION AND LOSS OF DATA, AND (b) DISCLAIM ANY AND ALL EXPRESS OR IMPLIED WARRANTIES AND CONDITIONS RELATED TO THIS REFERENCE DESIGN, INCLUDING WARRANTIES OR CONDITIONS OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, ACCURACY OF INFORMATION, OR NONINFRINGEMENT.

### 3. Export Control

Customers shall not use or otherwise make available this Reference Design for any military purposes, including without limitation, for the design, development, use, stockpiling or manufacturing of nuclear, chemical, or biological weapons or missile technology products (mass destruction weapons). This Reference Design may be controlled under the applicable export laws and regulations including, without limitation, the Japanese Foreign Exchange and Foreign Trade Law and the U.S. Export Administration Regulations. Export and re-export of this Reference Design are strictly prohibited except in compliance with all applicable export laws and regulations.

### 4. Governing Laws

This terms of use shall be governed and construed by laws of Japan.