

TOSHIBA BiCD Integrated Circuit Silicon Monolithic

# TB6674FAG

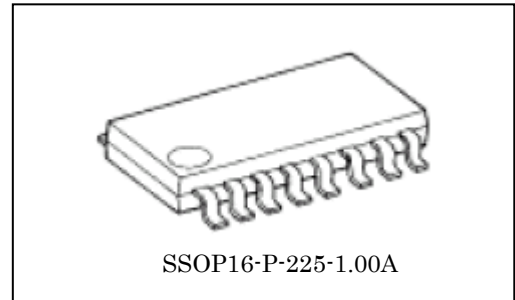
## Stepping Motor Driver IC

TB6674FAG is a stepping motor driver IC with MOS output transistors.

The IC can control two-phase stepping motor forward and reverse by bipolar driving. A power-saving circuit and a standby circuit are included.

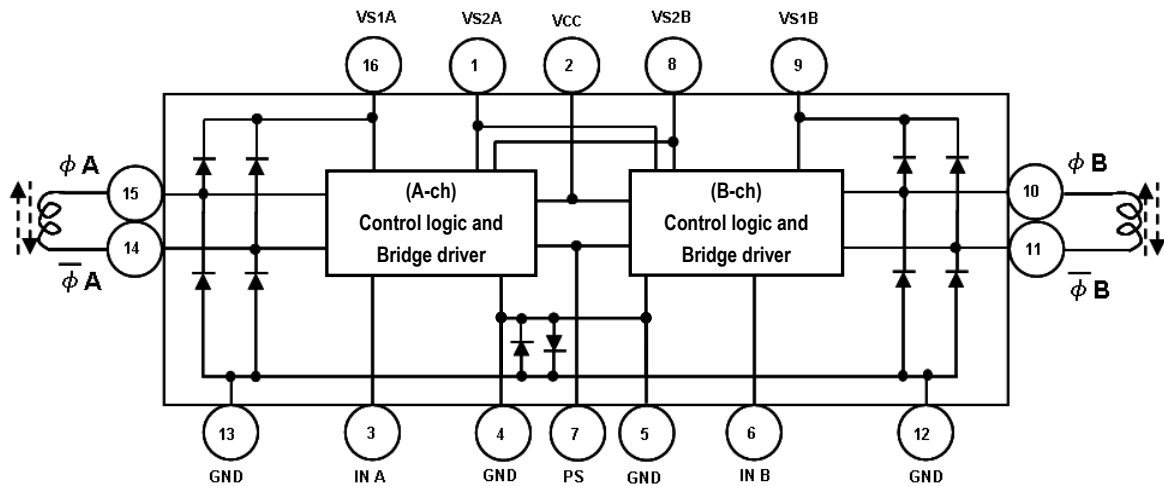
## Features

- One-chip two-phase bipolar stepping motor driver (including two bridge drivers)
- Power saving operation is available.
- Standby operation is available.  
Current consumption  $\leq 20 \mu\text{A}$  (typ.)
- Built-in punch-through current restriction circuit for system reliability and noise suppression.
- TTL-compatible inputs INA, INB, PS, and Vs2B terminals
- ON resistance PS = L :  $2.9 \Omega$  (Typ.)  
PS = H :  $7.9 \Omega$  (Typ.)
- High driving ability.  
: IO (START) 100 mA (MAX) : VS1 ENABLE  
: IO (HOLD) 50 mA (MAX) : VS2 ENABLE
- Typical PKG SSOP16 pin
- Over current shutdown circuit (ISD).
- Thermal shutdown circuit (TSD).
- Under voltage lockout circuit (UVLO).
- Pull-down resistance for input terminal (250 k $\Omega$ ).



Weight: 0.14 g (Typ.)

## Block Diagram



## Pin Description

Pin No.	Symbol	Functional Description
1	V <sub>S2A</sub>	Low-voltage power supply terminal
2	V <sub>CC</sub>	Power voltage supply terminal for control
3	IN A	A-ch forward rotation / reverse rotation signal input terminal, Truth Table 1
4	GND	GND terminal (Logic GND)
5	GND	GND terminal (Logic GND)
6	IN B	B-ch forward rotation / reverse rotation signal input terminal, Truth Table 1
7	PS	Power saving signal input terminal
8	V <sub>S2B</sub>	Standby signal input terminal, Truth Table 2
9	V <sub>S1B</sub>	High-voltage power supply terminal
10	Φ B	Output B
11	Φ B-bar	Output B-bar
12	GND	GND terminal (Power GND)
13	GND	GND terminal (Power GND)
14	Φ A-bar	Output A-bar
15	Φ A	Output A
16	V <sub>S1A</sub>	High-voltage power supply terminal.

**Truth Table 1.**

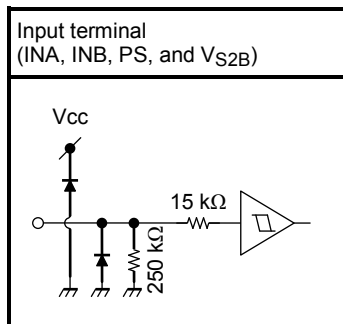
Input		Output		
PS	IN	$\Phi$	$\bar{\Phi}$	Mode
L	L	L	H	ENABLE $V_{S1}$
L	H	H	L	ENABLE $V_{S1}$
H	L	L	H	ENABLE $V_{S2}$ (Power saving)
H	H	H	L	ENABLE $V_{S2}$ (Power saving)

**Truth Table 2.**

$V_{S2B}$	Mode
L	POWER OFF (Standby mode)
H	OPERATION

Note: Apply 5 V to  $V_{S2A}$  as a supply terminal.

<Terminal circuit>



The diagram is partly-provided and omitted or simplified for explanatory purposes.

## Absolute Maximum Ratings (Ta = 25°C)

Characteristic	Symbol	Rating	Unit
Supply voltage	V <sub>CC</sub>	6.0	V
	V <sub>S1</sub>	24.0	
	V <sub>S2</sub>	Up to V <sub>CC</sub>	
Output current	I <sub>O</sub> (PEAK)	±200	mA
	I <sub>O</sub> (START)	±100	
	I <sub>O</sub> (HOLD)	±50	
Input voltage	V <sub>IN</sub>	Up to V <sub>CC</sub>	V
Power dissipation	P <sub>D</sub>	0.78 (Note)	W
Operating temperature	T <sub>opr</sub>	-30 to 75	°C
Storage temperature	T <sub>stg</sub>	-55 to 150	°C

Note: This value is obtained if mounting is on a 50 mm × 50 mm × 1.6 mm PCB, 40 % or more of which is occupied by copper.

## Operating Conditions (Ta = 25°C)

Characteristic	Symbol	Min	Typ.	Max	Unit
Supply voltage	V <sub>CC</sub>	4.5	—	5.5	V
	V <sub>S1</sub>	8.0	—	22.0	
	V <sub>S2A</sub>	2.7	—	5.5	
Output current	I <sub>O</sub>	—	—	±100	mA
Input voltage	V <sub>IN</sub>	0	—	V <sub>CC</sub>	V
Maximum frequency of input pulse	f <sub>IN</sub>	—	—	25	kHz
Minimum resolution of input pulse	t <sub>w</sub>	20	—	—	μs

Value of ON resistance tends to increase when the difference between Vs1 and Vs2A becomes 5 V or less.

Electrical Characteristics (Unless otherwise specified, Ta = 25°C, Vcc = 5 V, VS1 = 12 V, and VS2A = 5 V)

Characteristic		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit	
Supply current		I <sub>CC1</sub>	1	PS: H, VS2B: H	—	3	5	mA	
		I <sub>CC2</sub>		PS: L, VS2B: H	—	3	5		
		I <sub>CC3</sub>		VS2B: L	—	1	20	μA	
Input voltage	High	V <sub>INH</sub>	—	INA, INB, PS, VS2B	2.0	—	V <sub>CC</sub>	V	
	Low	V <sub>INL</sub>			-0.2	—	0.8		
Input hysteresis voltage*		V <sub>INHys</sub>			1		—	90	—
Input current		I <sub>IN (H)</sub>	1	INA, INB, PS, VS2B V <sub>IN</sub> = 5.0 V Built in pull-down resistance.	5	20	38	μA	
		I <sub>IN (L)</sub>		V <sub>IN</sub> = 0 V	—	—	1	μA	
Output ON resistance		R <sub>on 1H</sub>	2	PS: L, VS2B: H	I <sub>OUT</sub> = 200 mA	—	2	5	Ω
		R <sub>on 2H</sub>	3	PS: H, VS2B: H	I <sub>OUT</sub> = 50 mA	—	7	16	
		R <sub>on L</sub>	2	VS2B: H	I <sub>OUT</sub> = 200 mA	—	0.9	3.5	
Diode forward voltage		V <sub>FU</sub>	4	I <sub>F</sub> = 350 mA, PS = L	—	1.2	2.5	V	
		V <sub>FL</sub>			—	1.0	2.2		
Delay time		t <sub>pLH</sub>	—	IN - φ	—	0.5	—	μs	
		t <sub>pHL</sub>			—	0.5	—		
Thermal shutdown circuit*		TSD	—	(Design target only)	—	160	—	°C	
TSD hysteresis *		TSDhys	—	(Design target only)	—	20	—	°C	

\*: Toshiba does not implement testing before shipping.

## Under voltage Lockout Circuit (UVLO)

An under voltage lockout circuit is included.

Outputs are turned off (Hi-Z) under the conditions as follows:

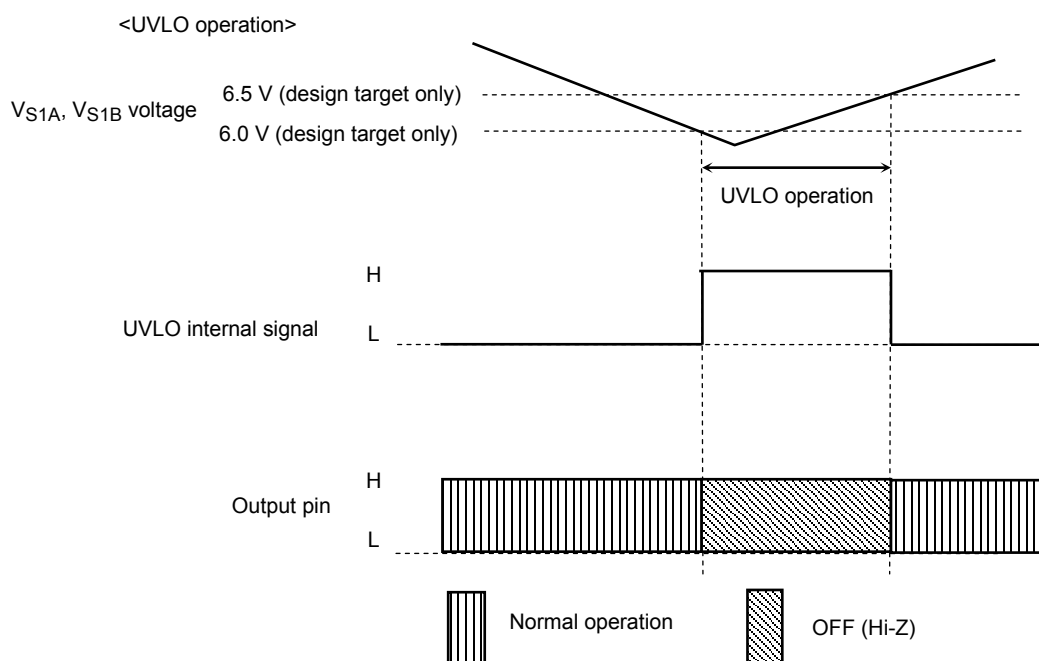
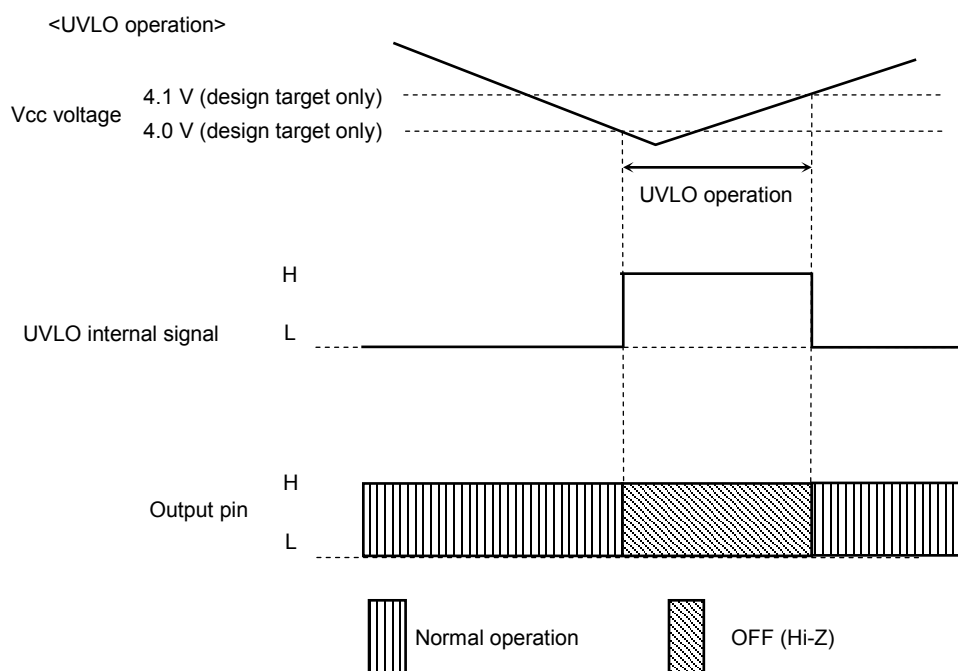
$V_{CC} \leq 4.0 \text{ V}$  (Design target) or

$V_{S1A} \leq 6.0 \text{ V}$  (Design target) and  $V_{S1B} \leq 6.0 \text{ V}$  (Design target) or

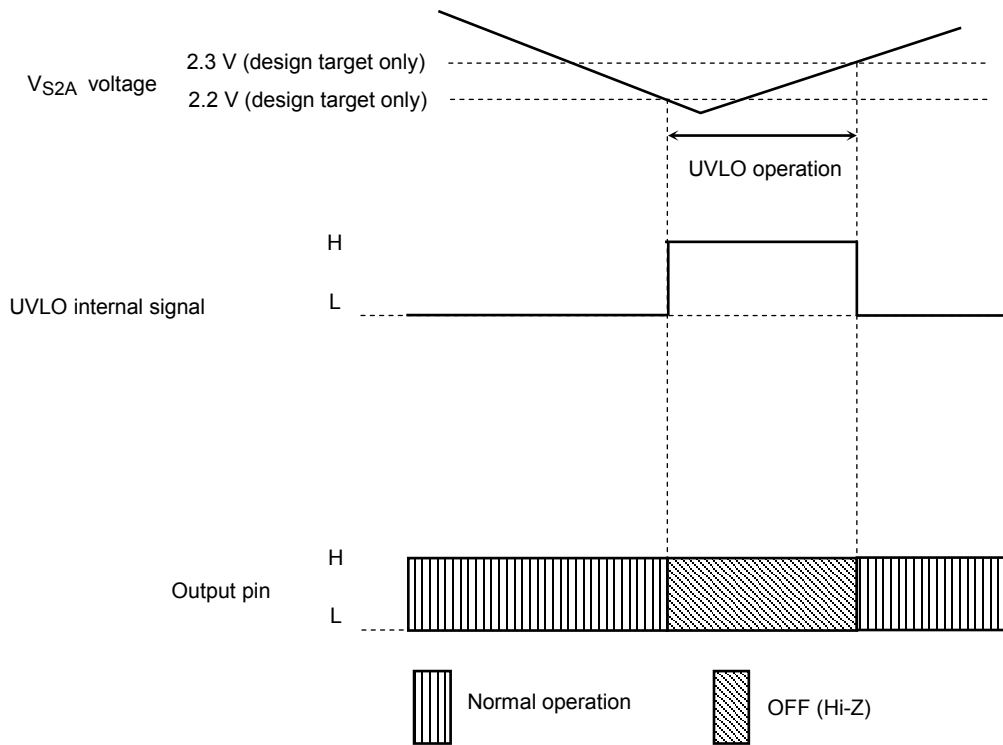
$V_{S2A} \leq 2.2 \text{ V}$  (Design target)

The UVLO circuit has a hysteresis and the function recovers under the conditions as follows:

$V_{CC} = 4.1 \text{ V}$  (Design target),  $V_{S1A}/V_{S1B} = 6.5 \text{ V}$  (Design target),  $V_{S2A} = 2.3 \text{ V}$  (Design target)



### <UVLO operation>



**Over Current Protection (ISD) Circuit**

The IC has the over current protection circuit that monitors the current flowing through each output power transistor. If a current, which is out of the detecting current, is sensed at any one of these transistors, all output transistors are turned off (Hi-Z). (However, ISD is not included in upper PchDMOS when PS is high level (Vs2A is 5 V usage) because ON resistance is large.

Masking time is 20 μs. The operation does not recover automatically (latch method). There are two recovery methods written below.

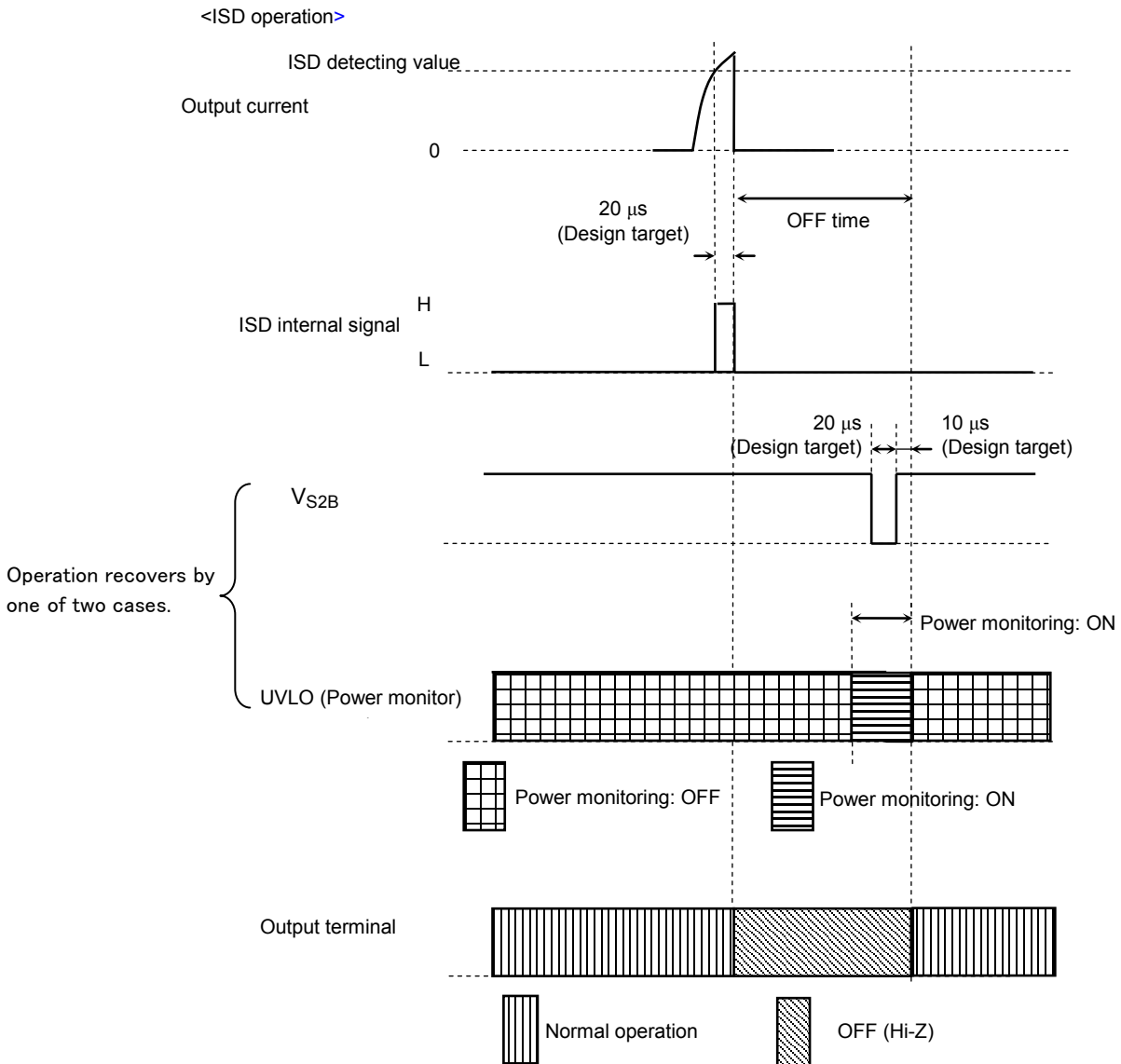
- (1) Power monitor turns on when any of the power supply decreases and reaches the specified voltage.
- (2) Vs2B is set low level for 20 μs or more and then set high. The operation recovers in 10 μs.

Reference design target of detecting current is as follows;

PS = L, VS1A (12 V) :PchDMOS = 1.1 A

PS = H/PS = L in common :Lower NchDMOS = 1.4 A

Please reduce the external noise to prevent malfunction for ISD.

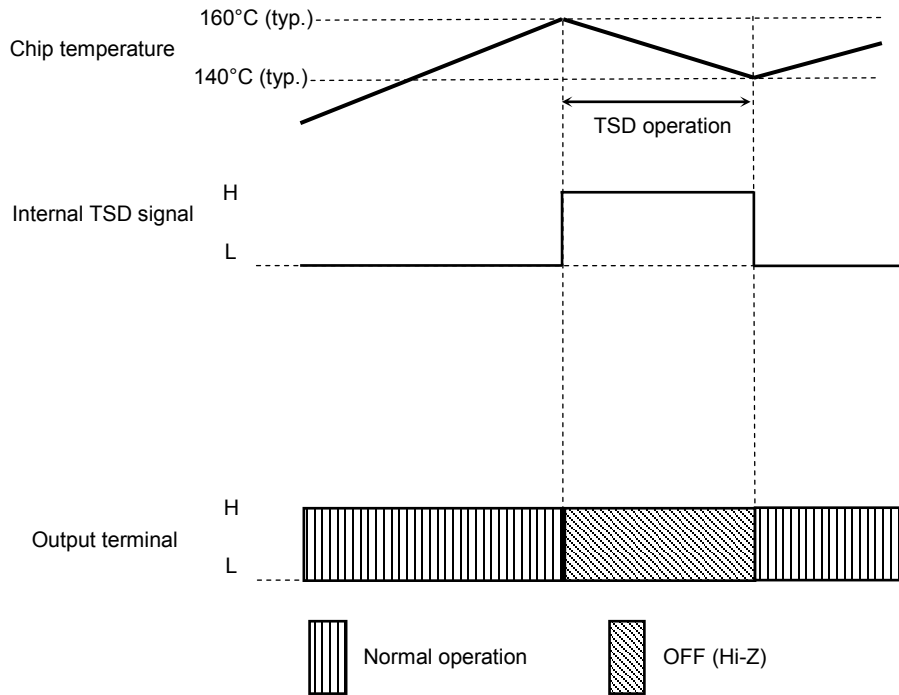


**Thermal Shutdown Circuit (TSD)**

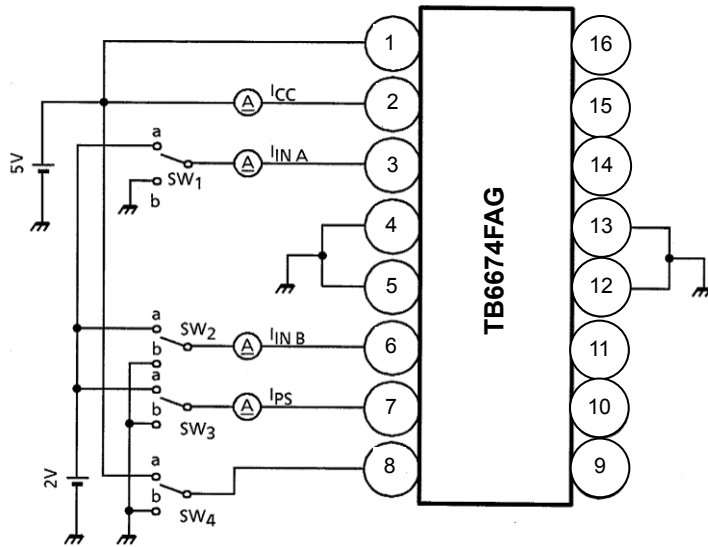
The TB6674FAG has a thermal shutdown circuit. If the junction temperature ( $T_j$ ) exceeds 160°C (design target only), all the outputs are tuned off (Hi-Z). It recovers automatically at 140°C. It has a hysteresis width of 20°C.

TSD = 160°C (design target only)

< TSD operation >



## Test Circuit 1. $I_{CC1}$ , $I_{CC2}$ , $I_{CC3}$ , $I_{IN A}$ , $I_{IN B}$ , and $I_{PS}$

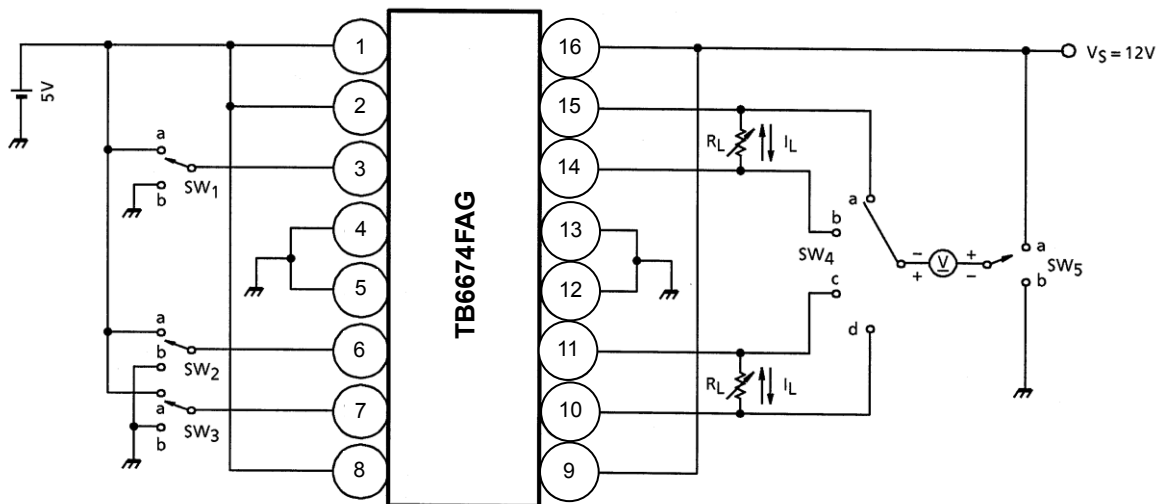


### Measuring method

Item	SW <sub>1</sub>	SW <sub>2</sub>	SW <sub>3</sub>	SW <sub>4</sub>
$I_{CC1}$	b	b	a	a
$I_{CC2}$	b	b	b	a
$I_{CC3}$	b	b	—	b
$I_{IN A}$	a	—	—	a
$I_{IN B}$	—	a	—	a
$I_{PS}$	—	—	a	a

All terminals of INA, INB, and PS should output low or be connected to the ground terminal in measuring  $I_{CC3}$ .

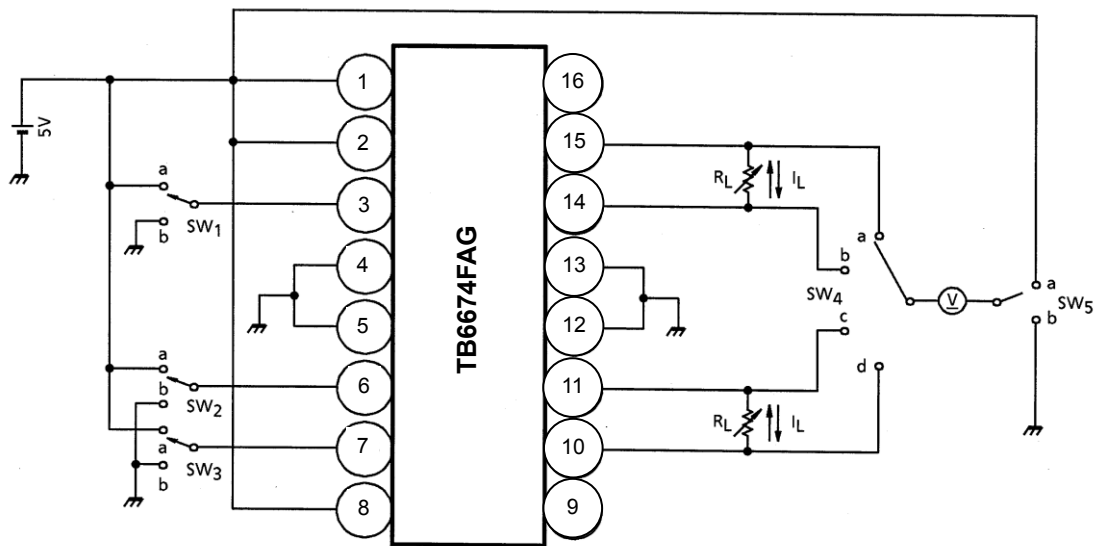
## Test Circuit 2. Ron 1H1, Ron 1H2, Ron L2, and Ron L3



\*: Adjust  $R_L$  to correspond to  $I_L$ .

Item	SW <sub>1</sub>	SW <sub>2</sub>	SW <sub>3</sub>	SW <sub>4</sub>	SW <sub>5</sub>	$I_L$ (mA)
$V_{SAT\ 1H1}$	a	—	b	a	a	100
	b	—		b		
	—	a		d		
	—	b		c		
$V_{SAT\ 1H2}$	a	—	b	a	a	400
	b	—		b		
	—	a		d		
	—	b		c		
$V_{SAT\ L2}$	a	—	—	b	b	100
	b	—		a		
	—	a		c		
	—	b		d		
$V_{SAT\ L3}$	a	—	b	b	b	400
	b	—		a		
	—	a		c		
	—	b		d		

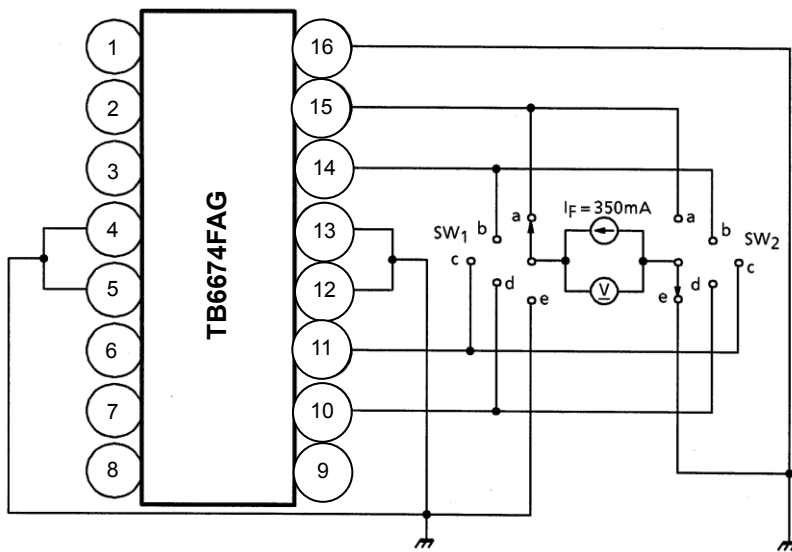
## Test Circuit 3. Ron 2H1, Ron 2H2, and Ron L1



\*: Adjust  $R_L$  to correspond to  $I_L$ .

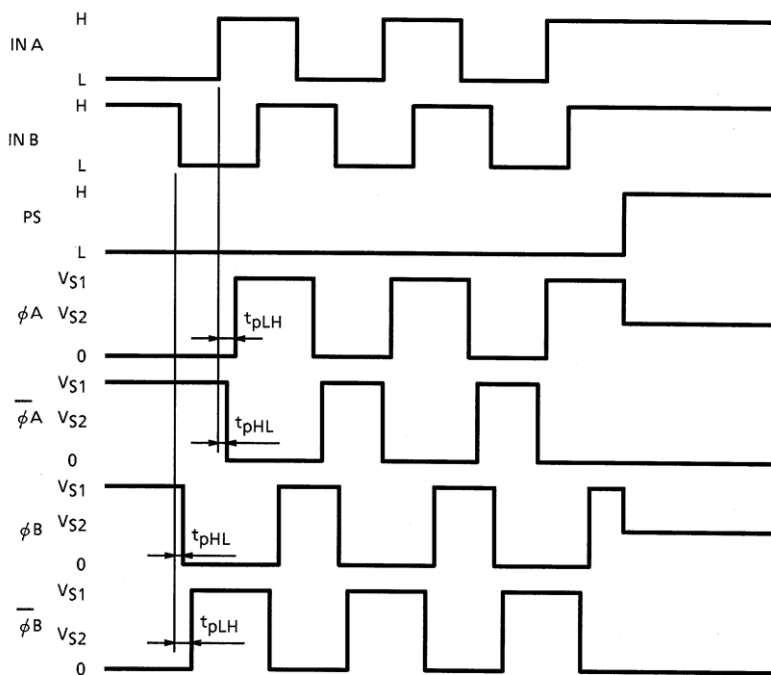
Item	SW <sub>1</sub>	SW <sub>2</sub>	SW <sub>3</sub>	SW <sub>4</sub>	SW <sub>5</sub>	$I_L$ (mA)
V <sub>SAT</sub> 2H1	a	—	a	a	a	20
	b	—		b		
	—	a		c		
	—	b		d		
V <sub>SAT</sub> 2H2	a	—	a	a	a	100
	b	—		b		
	—	a		c		
	—	b		d		
V <sub>SAT</sub> L1	a	—	a	b	b	20
	b	—		a		
	—	a		c		
	—	b		d		

## Test Circuit 4. $V_{FU}$ and $V_{FL}$



Item	SW <sub>1</sub>	SW <sub>2</sub>
$V_{FU}$	a	e
	b	
	c	
	d	
$V_{FL}$	e	a
		b
		c
		d

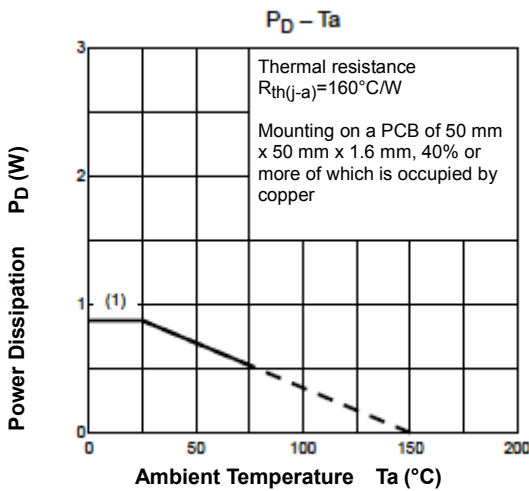
## Timing Chart (two-phase excitation)



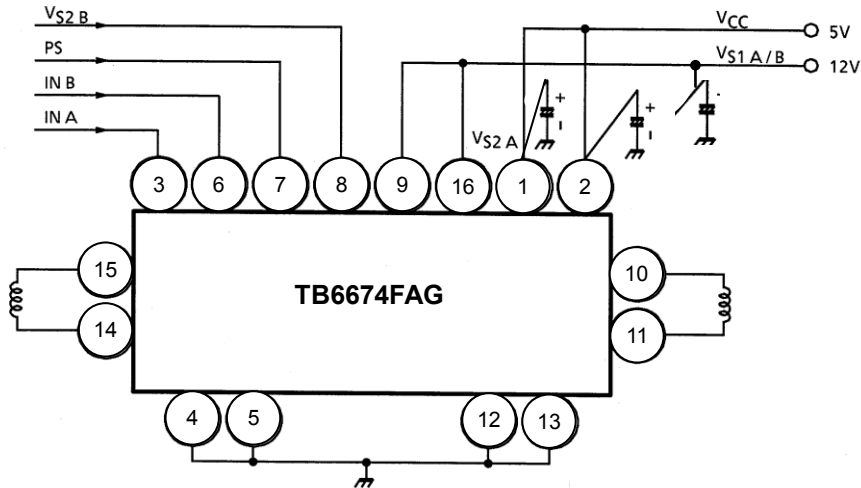
$t_{pLH}$  : 0.5 $\mu$ s (typ.)

$t_{pHL}$  : 0.5 $\mu$ s (typ.)

**Thermal Performance Characteristics**



**Application Circuit**

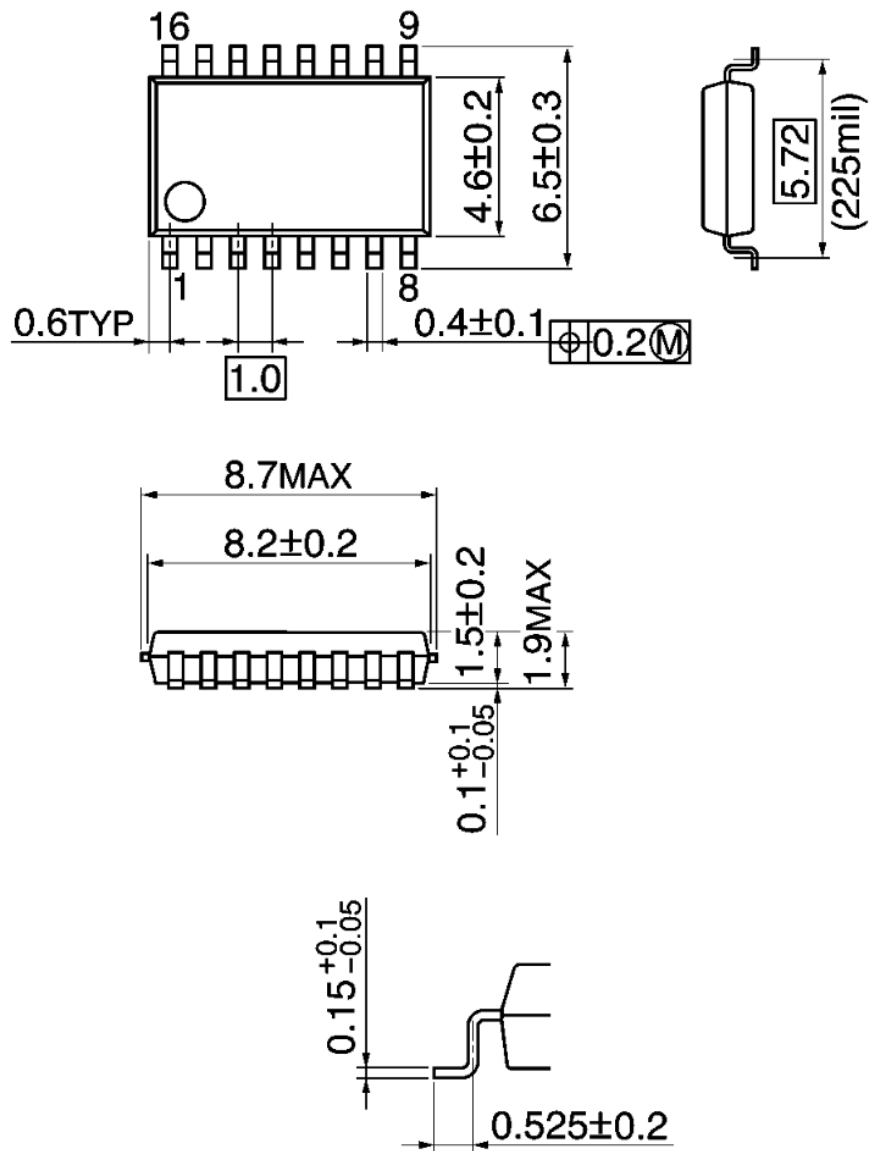


- Note 1: Connect the  $V_{S2A}$  terminal to the lower supply voltage (5 V).
- Note 2: Supply smoothing capacitor\* should be connected between each supply terminal ( $V_{CC}$ ,  $V_{S2A}$ , and  $V_{S1A/B}$ ) and GND terminal. \*: (Ex.): Capacitors of tens of  $\mu\text{F}$  and  $0.1 \mu\text{F}$  which are connected in parallel.
- Note 3: Utmost care is necessary in the design of the output,  $V_{CC}$ ,  $V_{S1A/B}$ , and GND lines since the IC may be destroyed by short-circuiting between outputs, air contamination faults, or faults due to improper grounding, or by short-circuiting between contiguous terminals.
- Note 4: By our short-circuited examination of neighboring terminals, when 9 and 10 terminals or 15 and 16 terminals are short-circuited, the TB6674FAG might to be destroyed and cause the trouble of smoking etc. Please use an appropriate fuse to the power supply line.
- Note 5: Connect  $V_{S1A}$  terminal and  $V_{S1B}$  terminal externally.
- Note 6: Connect each GND terminal externally.

## Package Dimensions

SSOP16-P-225-1.00A

Unit: mm



Weight: 0.14 g (Typ.)

## Notes on Contents

### 1. Block Diagrams

Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

### 2. Equivalent Circuits

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

### 3. Timing Charts

Timing charts may be simplified for explanatory purposes.

### 4. Application Circuits

The application circuits shown in this document are provided for reference purposes only. Thorough evaluation is required, especially at the mass production design stage.

Toshiba does not grant any license to any industrial property rights by providing these examples of application circuits.

### 5. Test Circuits

Components in the test circuits are used only to obtain and confirm the device characteristics. These components and circuits are not guaranteed to prevent malfunction or failure from occurring in the application equipment.

## IC Usage Considerations

### Notes on handling of ICs

- [1] The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.  
Exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.
- [2] Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead smoke or ignition. To minimize the effects of the flow of a large current in case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.
- [3] If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition.  
Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.
- [4] Do not insert devices in the wrong orientation or incorrectly.  
Make sure that the positive and negative terminals of power supplies are connected properly.  
Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.  
In addition, do not use any device that is applied the current with inserting in the wrong orientation or incorrectly even just one time.

**Points to remember on handling of ICs****(1) Heat Radiation Design**

In using an IC with large current flow such as power amp, regulator or driver, please design the device so that heat is appropriately radiated, not to exceed the specified junction temperature ( $T_j$ ) at any time and condition. These ICs generate heat even during normal use. An inadequate IC heat radiation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, please design the device taking into consideration the effect of IC heat radiation with peripheral components.

**(2) Back-EMF**

When a motor rotates in the reverse direction, stops or slows down abruptly, a current flows back to the motor's power supply due to the effect of back-EMF. If the current sink capability of the power supply is small, the device's motor power supply and output terminals might be exposed to conditions beyond absolute maximum ratings. To avoid this problem, take the effect of back-EMF into consideration in system design.

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