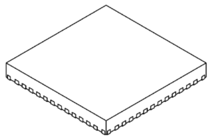
Toshiba BiCD Process Integrated Circuit Silicon Monolithic

TB67S105FTG

8bit Serial controlled bipolar stepping motor driver

1. Outline

The TB67S105FTG is a two phase bipolar stepping motor driver using a PWM chopper, controlled by 8-bit serial data.
Fabricated by the BiCD process, the TB67S105FTG is rated at 50 V/3.0 A.
The internal voltage regulator allows to control the device with a single VM power supply.



P-WQFN48-0707-0.50-003

Weight: 0.12 g (typ.)

2. Features

- BiCD process integrated monolithic IC.
- Capable of controlling one bipolar stepping motor.
- Low on-resistance MOSFET output stage.
- High voltage and current (for specification, please refer to the absolute maximum ratings and operation ranges).
- Built-in serial-parallel convert circuit (8bit shift register)
- 3-line (Data, Clock, Latch) serial output function for cascade connection
- PWM controlled constant-current drive.
- Allows full and half step operation
- 4 bit (16 steps) adjustable torque function (TRQ1, TRQ2, TRQ3, TRQ4).
- Built-in error detection circuits (Thermal shutdown (TSD), over current shutdown (ISD), and power on reset(POR)).
- Built-in VCC regulator for internal use.
- Chopping frequency of a motor can be customized by external resistor and capacitor.
- Package type: P-WQFN48-0707-0.50-003

Note: Please be careful about thermal conditions during use.

3. Pin assignment

(Top View)

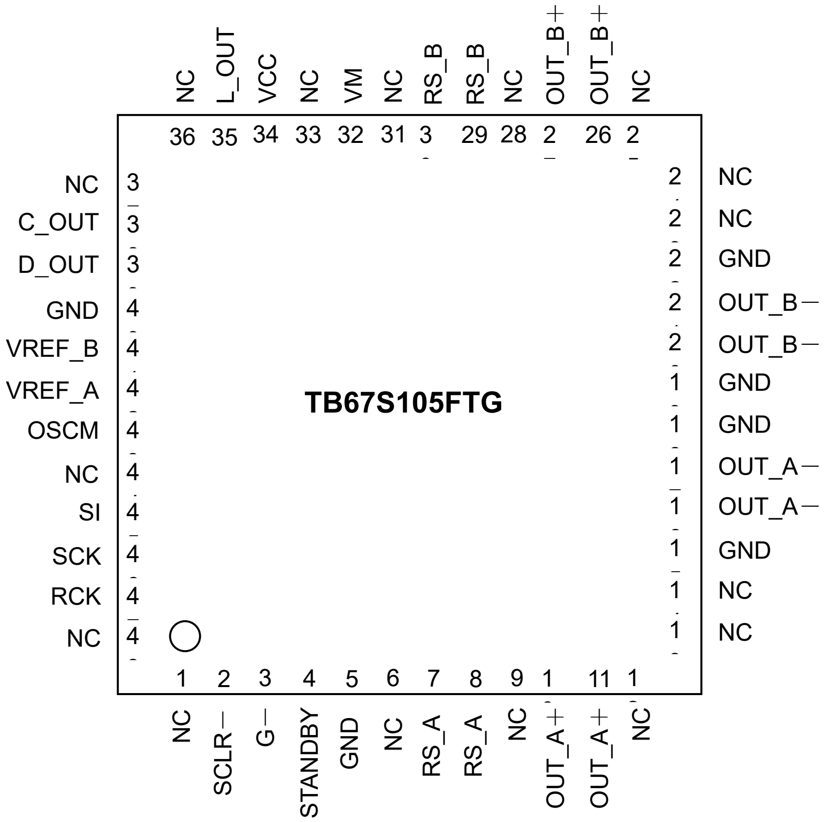


Figure3 Pin assignment

Note: Please solder the four corner pins of the QFN package and the exposed pad to the GND area of the PCB.

4. Pin explanations

Table4 Pin explanations

Pin No.1 to 28

Pin No.	Pin Name	Function
1	NC	Non-connection pin
2	SCLR−	Serial register clear pin (low active)
3	G−	Serial data select pin (low active)
4	STANDBY	Standby pin
5	GND	Ground pin
6	NC	Non-connection pin
7	RS_A(*)	Motor Ach current sense pin
8	RS_A(*)	Motor Ach current sense pin
9	NC	Non-connection pin
10	OUT_A+(*)	Motor Ach (+) pin
11	OUT_A+(*)	Motor Ach (+) pin
12	NC	Non-connection pin
13	NC	Non-connection pin
14	NC	Non-connection pin
15	GND	Ground pin
16	OUT_A−(*)	Motor Ach (-) pin
17	OUT_A−(*)	Motor Ach (-) pin
18	GND	Ground pin
19	GND	Ground pin
20	OUT_B−(*)	Motor Bch (-) pin
21	OUT_B−(*)	Motor Bch (-) pin
22	GND	Ground pin
23	NC	Non-connection pin
24	NC	Non-connection pin
25	NC	Non-connection pin
26	OUT_B+(*)	Motor Bch (+) pin
27	OUT_B+(*)	Motor Bch (+) pin
28	NC	Non-connection pin

Pin No.29 to 48

Pin No.	Pin Name	Function
29	RS_B(*)	Motor Bch current sense pin
30	RS_B(*)	Motor Bch current sense pin
31	NC	Non-connection pin
32	VM	Motor power supply pin
33	NC	Non-connection pin
34	VCC	Internal VCC regulator monitor pin
35	L_OUT	Serial ‘Latch’ output pin
36	NC	Non-connection pin
37	NC	Non-connection pin
38	C_OUT	Serial ‘Clock’ output pin
39	D_OUT	Shift register data output pin
40	GND	Ground pin
41	VREF_B	Motor Bch output current set pin
42	VREF_A	Motor Ach output current set pin
43	OSCM	Oscillating circuit frequency for PWM chopping set pin
44	NC	Non-connection pin
45	SI	Serial ‘Data’ input pin
46	SCK	Serial ‘Clock’ input pin
47	RCK	Serial ‘Latch’ input pin
48	NC	Non-connection pin

Note:
Please do not run patterns under NC pins.
Please connect the pins with the same pin name.

5. Block diagram

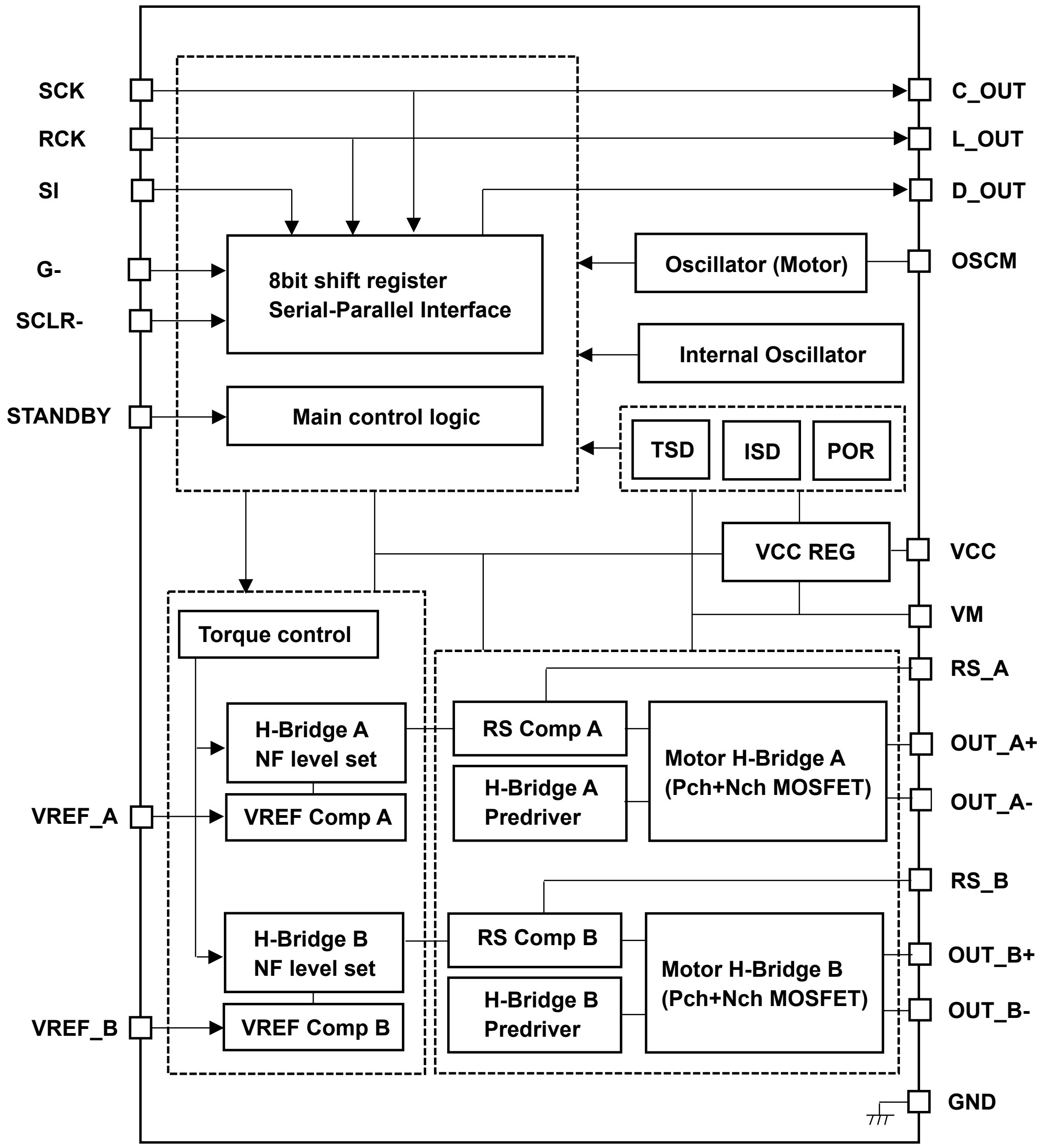


Figure5 Block diagram

Note: Functional blocks/circuits/constants in the block diagram may be omitted or simplified for explanatory purposes.

Note: All the grounding wires of the TB67S105FTG must run on the solder mask on the PCB, and be externally connected at a single point. Also, the grounding method should be considered for efficient heat dissipation.

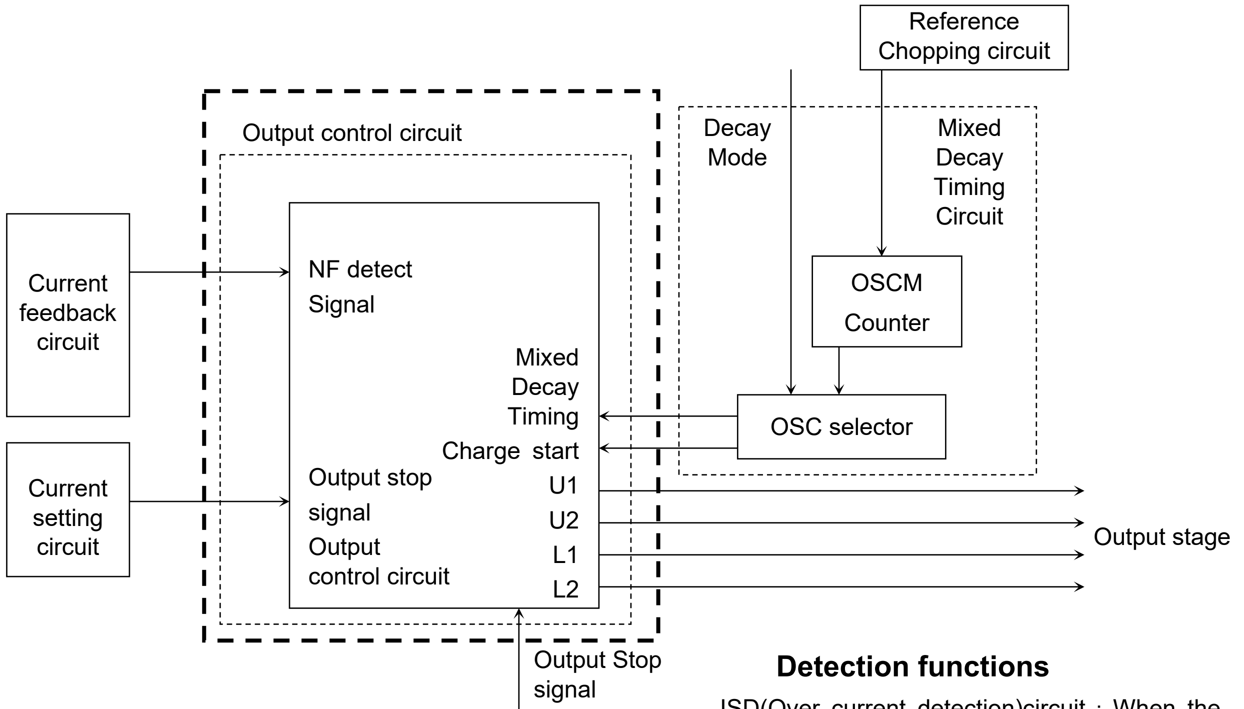
Careful attention should be paid to the layout of the output, VM and GND traces, to avoid short circuits across output pins or to the power supply or ground. If such a short circuit occurs, the device may be permanently damaged.

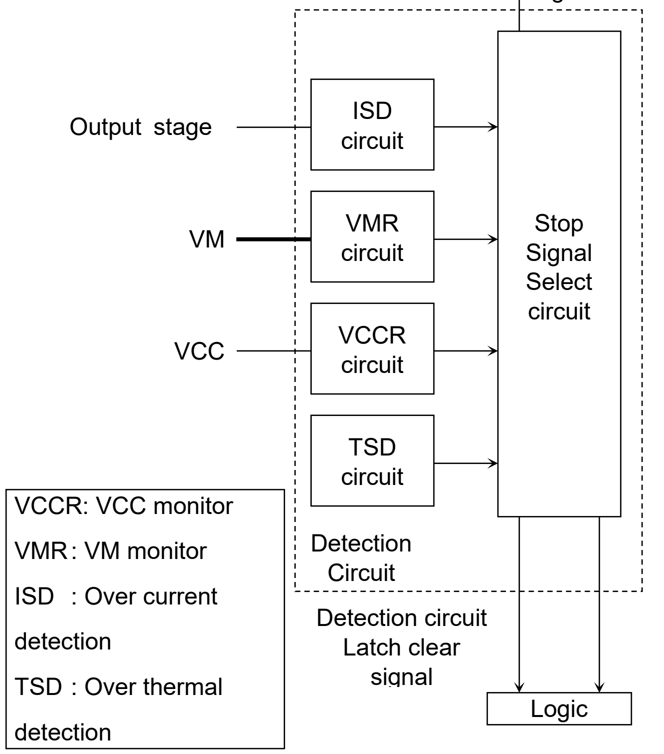
Also, the utmost care should be taken for pattern designing and implementation of the device since it has power supply pins (VM, RS_x+, RS_x-, OUT_x+, OUT_x-, GND (x=A or B)) through which a particularly large current may run. If these pins are wired incorrectly, an operation error may occur or the device may be destroyed.

The logic input pins must also be wired correctly. Otherwise, the device may be damaged owing to a current running through the IC that is larger than the specified current.

6. Output current feedback circuit, current setting circuit

Note: Logic pins are either pulled up or pulled down internally by 100 kohm resistor. Please refer to the equivalent circuit.)





Detection functions

ISD(Over current detection)circuit : When the current exceeds the threshold, the output stage will turn OFF. Reapplying the VM again from 0V or setting the STANDBY to H→L→H will reset the ISD.

TSD(Over temperature detection)circuit: When the temperature of the IC exceeds the threshold, the output stage will turn OFF. Reapplying the VM again from 0V or setting the STANDBY to H→L→H will reset the TSD.

VMR(VM monitor)circuit: Detects H when VM is above the threshold, and detects L when VM is below the threshold.

VCCR(VCC monitor)circuit: Detects H when VCC is above the threshold, and detects L when VCC is below the threshold.

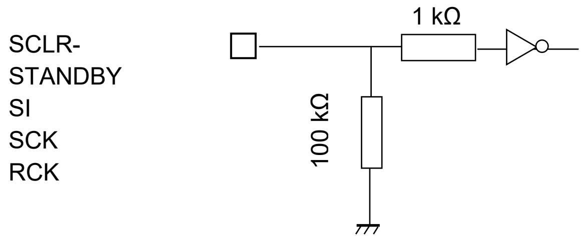
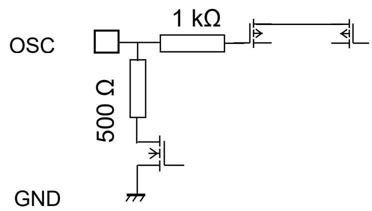
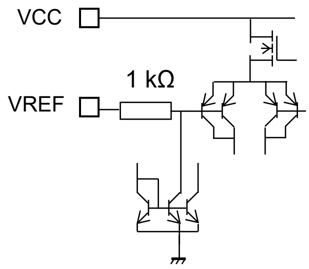
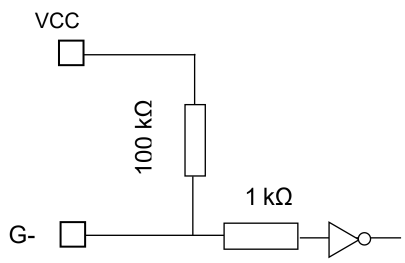
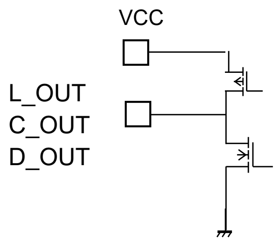
POR(Power On Reset)circuit: When both VMR and VCCR is above the threshold the logic becomes active. When both or either VMR or VCCR is below the threshold, the logic is stopped.

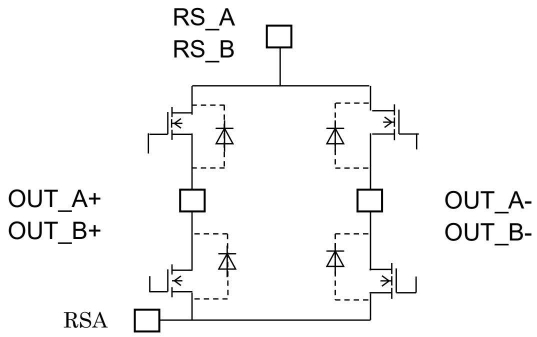
Figure6 Output control circuit current value feedback circuit, current value setting circuit

Note: Functional blocks/circuits/constants in the block diagram may be omitted or simplified for explanatory purposes.

7. INPUT/OUTPUT equivalent circuit

Table7 INPUT/OUTPUT equivalent circuit

Pin Name	Input/output equivalent circuit
SCLR- STANDBY SI SCK RCK	
OSCM	
VREF_A VREF_B	
G-	
L_OUT C_OUT D_OUT	

Pin Name	Input/output equivalent circuit
OUT_A+ OUT_A- OUT_B+ OUT_B- RS_A RS_B	 Note: OUTB1, OUTB2 are the same.

Note: The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

8. Control mode/Function explanation

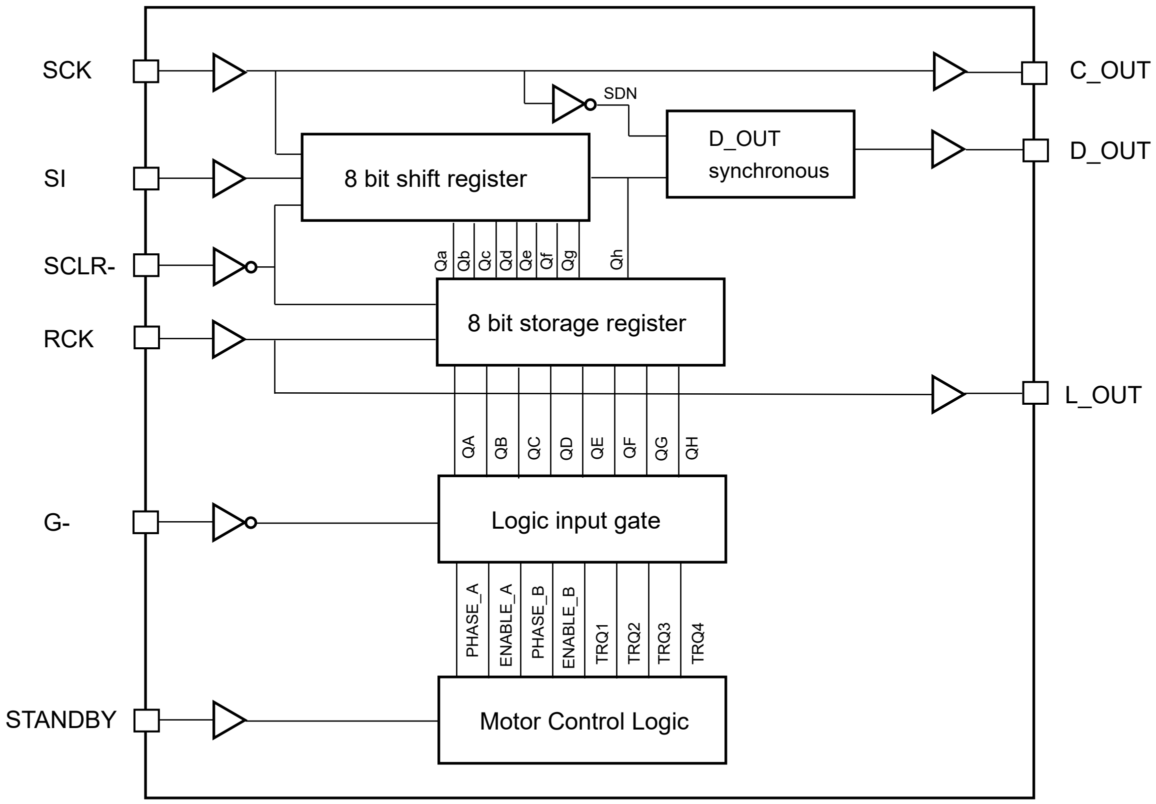


Figure8 Serial control interface (8 bit shift register+8bit storage register)

Note: The block diagram and equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

If the logic signal is not asserted, the initial status of the logic pins will be as shown below.

SCK: Low
SI: Low
SCLR-: Low (shift register and storage register are at the initial status.)
RCK: Low
G-: High (PHASE_A, ENABLE_A, PHASE_B, ENABLE_B, TRQ1, TRQ2, TRQ3, TRQ4=Disable)
STANDBY: Low (Standby mode)

Table8 Truth table

Input					Function
SI	SCK	SCLR-	RCK	G-	
X	X	X	X	H	PHASE_A, ENABLE_A, PHASE_B, ENABLE_B, TRQ1, TRQ2, TRQ3, TRQ4=Disable
X	X	X	X	L	PHASE_A, ENABLE_A, PHASE_B, ENABLE_B, TRQ1, TRQ2, TRQ3, TRQ4=Enable
X	X	L	X	X	Shift register and storage register are initialized
L	↑	H	X	X	The first data of the shift register is L, and the other register will be stored with the data before.
H	↑	H	X	X	The first data of the shift register is H, and the other register will be stored with the data before.
X	↓	H	X	X	The shift register data will maintain its status. The data after the shift register(Qh) will be output from D_OUT pin.
X	X	H	↑	X	Shift register data will be stored to the storage register.
X	X	H	↓	X	(The storage register data will maintain its status.)

X: Don't care
Note) To send the logic output data correctly to the next IC, please make sure to end the SCK data transfer with a Low signal.

8.1. Function explanation

The motor current is defined as plus when the current flows from OUT_X+ to OUT_X-, and defined minus when the current flows from OUT_X- to OUT_X+.

Table8.1 Function explanation

Signal	H	L	
ENABLE_X	OUTPUT: ON	OUTPUT: OFF	When ENABLE_X is set to L, no matter what the PHASE status are, the corresponding output stage will be set OFF(Hi-z).
PHASE_X	OUT_X+: H OUT_X-: L	OUT_X+: L OUT_X-: H	When set to H, the current will flow from OUT_X+ to OUT_X- at charge status.
STANDBY	Motor operational	Standby mode	When STANDBY is set to L, the internal OSC circuit as well as output stage is set OFF; therefore the motor will not operate.

(X=A or B)

8.2. Internal signal and current ratio

Table8.2.1 Full step

Ach			Bch		
Internal signal		Output	Internal signal		Output
PHASE_A	ENABLE_A	IOUT_A	PHASE_B	ENABLE_B	IOUT_B
H	H	+100 %	H	H	+100 %
L	H	-100 %	H	H	+100 %
L	H	-100 %	L	H	-100 %
H	H	+100 %	L	H	-100 %

Table8.2.2 Half step

Ach			Bch		
Internal signal		Output	Internal signal		Output
PHASE_A	ENABLE_A	IOUT_A	PHASE_B	ENABLE_B	IOUT_B
H	H	+100 %	H	H	+100 %
X	L	0 %	H	H	+100 %
L	H	-100 %	H	H	+100 %
L	H	-100 %	X	L	0 %
L	H	-100 %	L	H	-100 %
X	L	0 %	L	H	-100 %
H	H	+100 %	L	H	-100 %
H	H	+100 %	X	L	0 %

X: Don’t care

Table8.2.3 TRQ function: Current Ratio

TRQ1	TRQ2	TRQ3	TRQ4	Current Ratio(%)
L	L	L	L	0
L	L	L	H	5
L	L	H	L	10
L	L	H	H	15
L	H	L	L	25
L	H	L	H	29
L	H	H	L	38
L	H	H	H	43
H	L	L	L	52
H	L	L	H	60
H	L	H	L	67
H	L	H	H	74
H	H	L	L	80
H	H	L	H	86
H	H	H	L	94
H	H	H	H	100

9. Absolute Maximum Ratings (T_a = 25 °C)

Table9 Absolute Maximum Ratings

Characteristics	Symbol	Rating	Unit	Note
Motor power supply	V_M	50	V	-
Motor output voltage	V_{OUT}	50	V	-
Motor output current	I_{OUT}	3	A	Note 1
Internal VCC voltage	V_{CC}	6	V	Note 2
Logic input voltage	V_{IH}	6	V	-
Logic output current	I_{OH}	-7	mA	-
	I_{OL}	7	mA	-
VREF input voltage	V_{REF}	5	V	-
Power dissipation	P_D	1.3	W	Note 3
Operating temperature	T_{opr}	-20 to 85	°C	-
Storage temperature	T_{stg}	-55 to 150	°C	-
Junction temperature	T_j	150	°C	-

Note 1: Usually the maximum current value should be controlled below 80 % or less of the absolute maximum ratings for a standard based on thermal rating. The maximum output current may be further limited due to thermal considerations, depending on ambient temperature and board conditions.
Note 2: V_{CC} is an internal voltage regulator and regulates 4.75 V≤V_{CC}≤5.25 V in a normal condition. The above rating shows the pin tolerance.
Note 3: Device alone. (T_a =25 °C)
If the ambient temperature is above 25 °C, the power dissipation must be de-rated by 10.4 mW/°C.

T_a: Ambient temperature
T_{opr}: Ambient temperature while the device is active
T_j: Junction temperature while the device is active. The maximum junction temperature is limited by the thermal shutdown(TSD) circuitry. It is advisable to keep the maximum current below a certain level so that the maximum junction temperature, $T_{j(max)}$, will not exceed 120 °C.

Caution) Absolute maximum ratings

The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings. Exceeding the rating(s) may cause device breakdown, damage or deterioration, and may result in injury by explosion or combustion. The value of even one parameter of the absolute maximum ratings should not be exceeded under any circumstances. The device does not have overvoltage detection circuit. Therefore, the device is damaged if a voltage exceeding its rated maximum is applied. All voltage ratings, including supply voltages, must always be followed. The other notes and considerations described later should also be referred to.

10. Operating Range (T_a=0 to 85 °C)

Figure10 Operating Range

Characteristics	Symbol	Min	Typ.	Max	Unit	Note
Motor power supply	V_M	10	24	40	V	-
Motor output current	I_{OUT}	-	1.0	2.4	A	Note
Logic input voltage	$V_{IN(H)}$	3.0	-	5.5	V	Logic H level
	$V_{IN(L)}$	0	-	2.0	V	Logic L level
Chopping frequency set range	$f_{chop(range)}$	40	100	150	kHz	-
VREF input voltage	V_{REF}	GND	3.0	3.6	V	-

Note: Maximum current for actual usage may be limited by the operating circumstances such as operating conditions (exciting mode, operating time, etc), ambient temperature, and heat conditions (board condition and so on).

11. Electrical Specifications1 (T_a = 25 °C, V_M = 24 V, unless otherwise specified)

Table11 Electrical Specifications1

Characteristics		Symbol	Test conditions	Min	Typ.	Max	Unit
Logic input voltage	HIGH	$V_{IN(H)}$	Logic input pin (Note1)	3.0	-	5.5	V
	LOW	$V_{IN(L)}$		0	-	2.0	V
Logic input hysteresis		$V_{IN(HYS)}$		0.3	-	0.5	V
Logic input current	HIGH	$I_{IN(H)}$	Logic input voltage:3.3 V	-	33	50	μA
	LOW	$I_{IN(L)}$	Logic input voltage:0 V	-	-	1	μA
Logic output pin voltage	HIGH	$V_{OH(LO)}$	$I_{OH(LO)}$=-3 mA, VCC based	-0.41	-0.34	-0.27	V
	LOW	$V_{OL(LO)}$	$I_{OL(LO)}$=3 mA, GND based	0.20	0.25	0.30	V
Power consumption		I_{M1}	Output pins=open, STANDBY=L	-	2	3.5	mA
		I_{M2}	Output pins=open, STANDBY=H, ENABLE=L	-	3.5	5.5	mA
		I_{M3}	Output pins=open, (Full step)	-	5.5	7	mA
Output leakage current	High side	I_{OH}	V_M=RS=50 V, V_{OUT}=0 V	-	-	1	μA
	Low side	I_{OL}	V_M=RS=V_{OUT}=50 V	1	-	-	μA
Motor current channel differential		ΔI_{OUT1}	Current differential between Ach and Bch	-5	0	5	%
Motor current setting accuracy		ΔI_{OUT2}	I_{OUT}=1 A (Note2)	-5	0	5	%
RS pin current		I_{RS}	V_M=RS=24 V	0	-	10	μA
Output MOSFET On resistance (High+Low side)		$R_{ds(on)}$	I_{OUT}=2.4 A, T_j=25 °C, Forward direction, (High side + Low side)	-	0.6	0.8	Ω

Note1: $V_{IN (H)}$ is defined as the V_{IN} voltage that causes the outputs (OUT_A, OUT_B) to change when a pin under test is gradually raised from 0 V. $V_{IN (L)}$ is defined as the V_{IN} voltage that causes the outputs (OUT_A, OUT_B) to change when the pin is then gradually lowered. The difference between $V_{IN (H)}$ and $V_{IN (L)}$ is defined as the $V_{IN (HYS)}$.

Note2: When using the internal V_{CC} regulator and for V_{REF} input voltage with a resistance divider; taking V_{CC} accuracy and V_{REF} ratio into consideration, the motor current setting accuracy specification will be ±8%.

Note: When the logic signal is applied to the device whilst the V_M power supply is not asserted; the device is designed not to function, but for safe usage, please apply the logic signal after the V_M power supply is asserted and the V_M voltage reaches the proper operating range.

12. Electrical Specifications2 (T_a=25 °C, V_M=24 V, unless otherwise specified)

Table12 Electrical Specifications2

Characteristics	Symbol	Test conditions	Min	Typ.	Max	Unit
VREF input voltage	V_{REF}	V_M=24 V, V_{CC}=5 V	GND	3.0	3.6	V
VREF input current	I_{REF}	V_{REF}=3 V	-	0	1	μA
VCC pin voltage	V_{CC}	I_{CC}=5 mA	4.75	5	5.25	V
VCC pin current	I_{CC}	V_{CC}=5 V	-	2.5	5	mA
VREF ratio	$V_{REF(gain)}$	V_{REF}=2 V	1/5.2	1/5	1/4.8	-
Thermal shutdown threshold	T_{SD}	Note 1	140	150	170	°C
VM POR threshold	V_{MR}	-	7	8	9	V
Over-current detection threshold	I_{SD}	Note 2	3.6	4.6	5.6	A

Note 1: About Thermal shutdown (TSD)
When the junction temperature of the device reaches the TSD threshold, the TSD circuit is triggered; the internal reset circuit then turns off the output transistors. Noise rejection blanking time is built-in to avoid misdetection.
Once the TSD circuit is triggered; the detect latch signal can be cleared by reasserting the VM power source, or setting the device to standby mode. The TSD circuit is a backup function to detect a thermal error, therefore is not recommended to be used aggressively.

Note 2: About Over-current detection (ISD)
When the output current reaches the threshold, the ISD circuit is triggered; the internal reset circuit then turns off the output transistors. Once the ISD circuit is triggered, the detect latch signal can be cleared by reasserting the VM power source, or setting the device to standby mode. For fail-safe, please insert a fuse to avoid secondary trouble.

12.1. Back-EMF

While the motor is rotating, there is a timing at which power is fed back to the power supply. At that timing, the motor current recirculates back to the power supply due to the effect of the motor back-EMF.
If the power supply does not have enough sink capability, the power supply and output pins of the device might rise above the rated voltages. The magnitude of the motor back-EMF varies with usage conditions and motor characteristics. It must be fully verified that there is no risk that the device or other components will be damaged or fail due to the motor back-EMF.

12.2. Cautions on Overcurrent Shutdown (ISD) and Thermal Shutdown (TSD)

The ISD and TSD circuits are only intended to provide temporary protection against irregular conditions such as an output short-circuit; they do not necessarily guarantee the complete IC safety. If the device is used beyond the specified operating ranges, these circuits may not operate properly: then the device may be damaged due to an output short-circuit.
The ISD circuit is only intended to provide a temporary protection against an output short-circuit. If such condition persists for a long time, the device may be damaged due to overstress. Overcurrent conditions must be removed immediately by external hardware.

12.3. IC Mounting

Do not insert devices incorrectly or in the wrong orientation. Otherwise, it may cause breakdown, damage and/or deterioration of the device.

13. Electrical Specification(T_a=25 °C, V_M=24 V, 6.8 mH/5.7 Ω unless otherwise specified)

Table13 AC Electrical Specification

Characteristics	Symbol	Test conditions	Min	Typ.	Max	Unit
Minimum pulse width (SCK,RCK,SI)	$t_{w(H)}$	f_{OSCM}=1600 kHz	100	-	-	ns
	$t_{w(L)}$	f_{OSCM}=1600 kHz	100	-	-	ns
Minimum setup time	t_{set1}	SCLR-→SCK	50	-	-	ns
	t_{set2}	SI→SCK	50	-	-	ns
	t_{set3}	SCK→RCK	50	-	-	ns
Minimum clock signal cycle(SCK,RCK)	t_{cyc}	f_{OSCM}=1600 kHz	200	-	-	ns
Minimum hold time	t_{hold1}	SCK→SI	50	-	-	ns
	t_{hold2}	SCLR-→Data	50	-	-	ns
Output transistor switching time	t_r	Motor output	70	120	170	ns
	t_f	Motor output	100	150	200	ns
Analog noise blanking time	At_{BLK}	V_M=24 V, I_{OUT}=1 A Analog t_{BLK}	250	400	550	ns
OSCM frequency	f_{OSCM}	C_{OSC}=270 pF, R_{OSC}=3.6 kΩ	1360	1600	1840	kHz
Chopping frequency	f_{chop}	Output:Active(I_{OUT}=1 A), f_{OSCM}= 1600 kHz	-	100	-	kHz

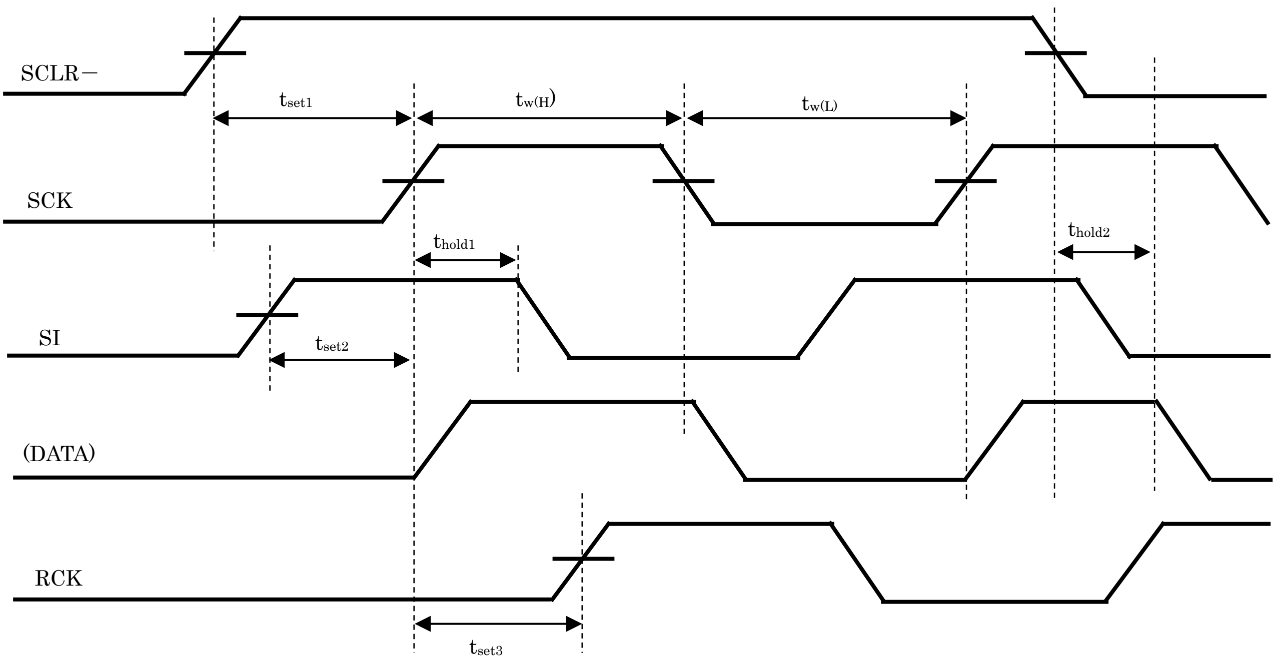


Figure13 AC Electrical Specification Timingchart

Timing charts may be simplified for explanatory purpose.

·Application Notes

14. Mixed Decay Mode waveform and settings

During constant current control, the rate of the Mixed decay mode which determines the current ripple is fixed to 37.5 %.

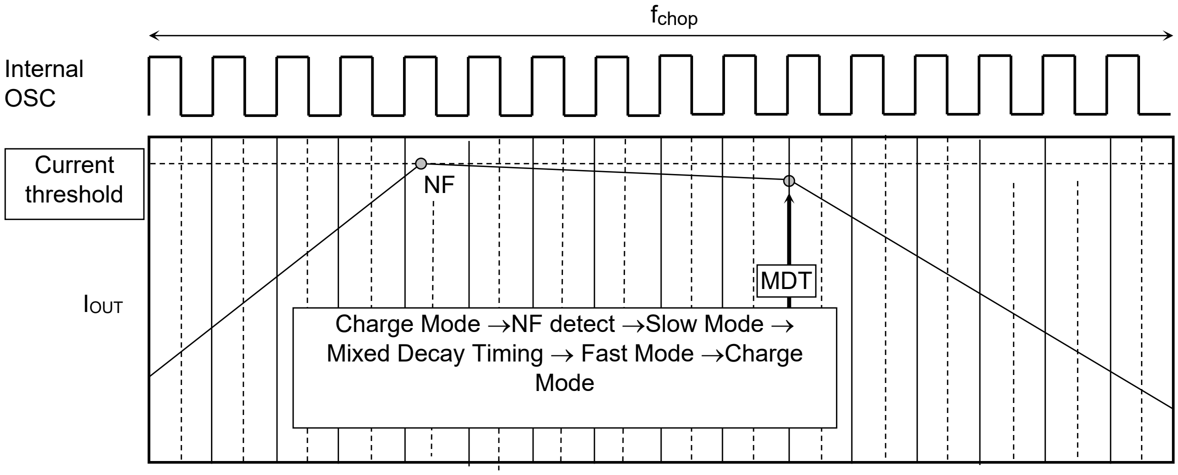
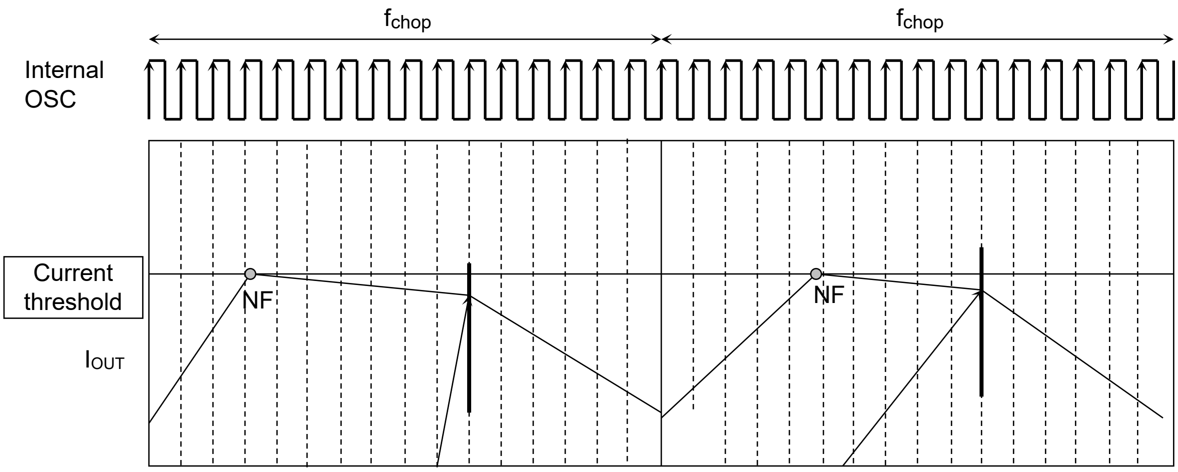


Figure14 Mixed Decay Mode waveform and settings

14.1. Mixed Decay Mode waveform (Current waveform)



MDT (Mixed Decay Timing) : 37.5 % (fixed)

Figure 14.1 Mixed Decay Mode waveform (Current waveform)

Timing charts may be simplified for explanatory purpose.

14.2. Mixed (Slow + Fast) Decay Mode current waveform

○ When the current value increases (Mixed Decay Mode is fixed to 37.5 %)

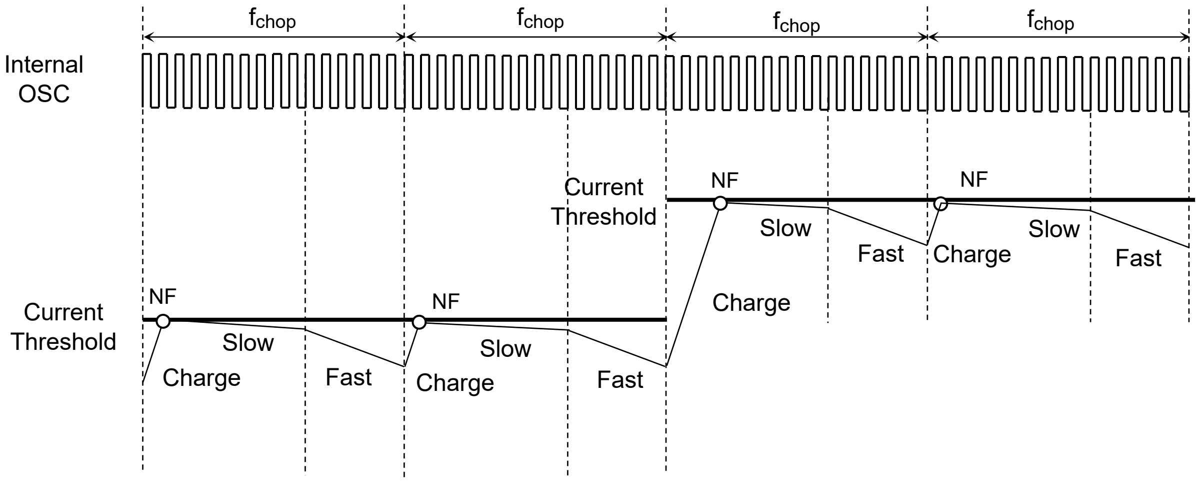


Figure14.2.1 When the set current value is in the increasing direction

○ When the current value decreases (Mixed Decay Mode is fixed to 37.5 %)

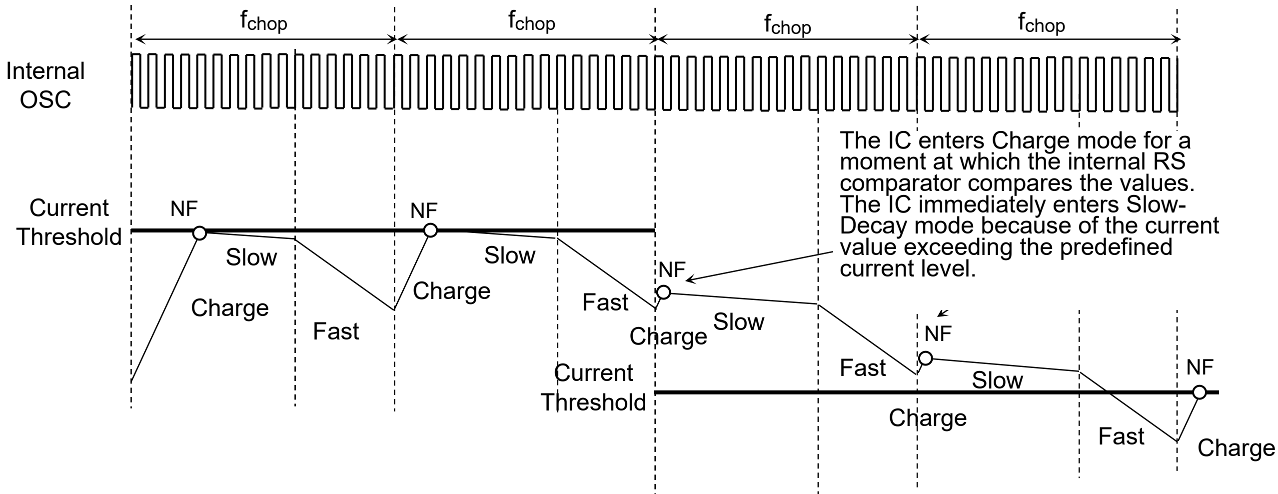


Figure14.2.2 When the set current value is in the decreasing direction

Note: Timing charts may be simplified for explanatory purpose.
Note: These figures are intended for illustrative purposes only. If designed more realistically, they would show transient response curves.

The Charge period starts as the internal oscillator clock starts counting. When the output current reaches the predefined current level, the internal RS comparator detects the predefined current level (NF); as a result, the IC enters Slow-Decay mode.
The device transits from Slow-Decay mode to Fast-Decay mode at the point 37.5% of a PWM frequency (one chopping frequency) remains in a whole PWM frequency period (on the rising edge of the 11th clock of the OSCM clock).
When the OSCM pin clock counter clocks 16 times, the Fast-Decay mode ends; and at the same time, the counter is reset, which brings the device into Charge mode again.

15. PHASE signal and internal OSC - output current waveform (Full step mode)

Note: Timing charts may be simplified for explanatory purpose.

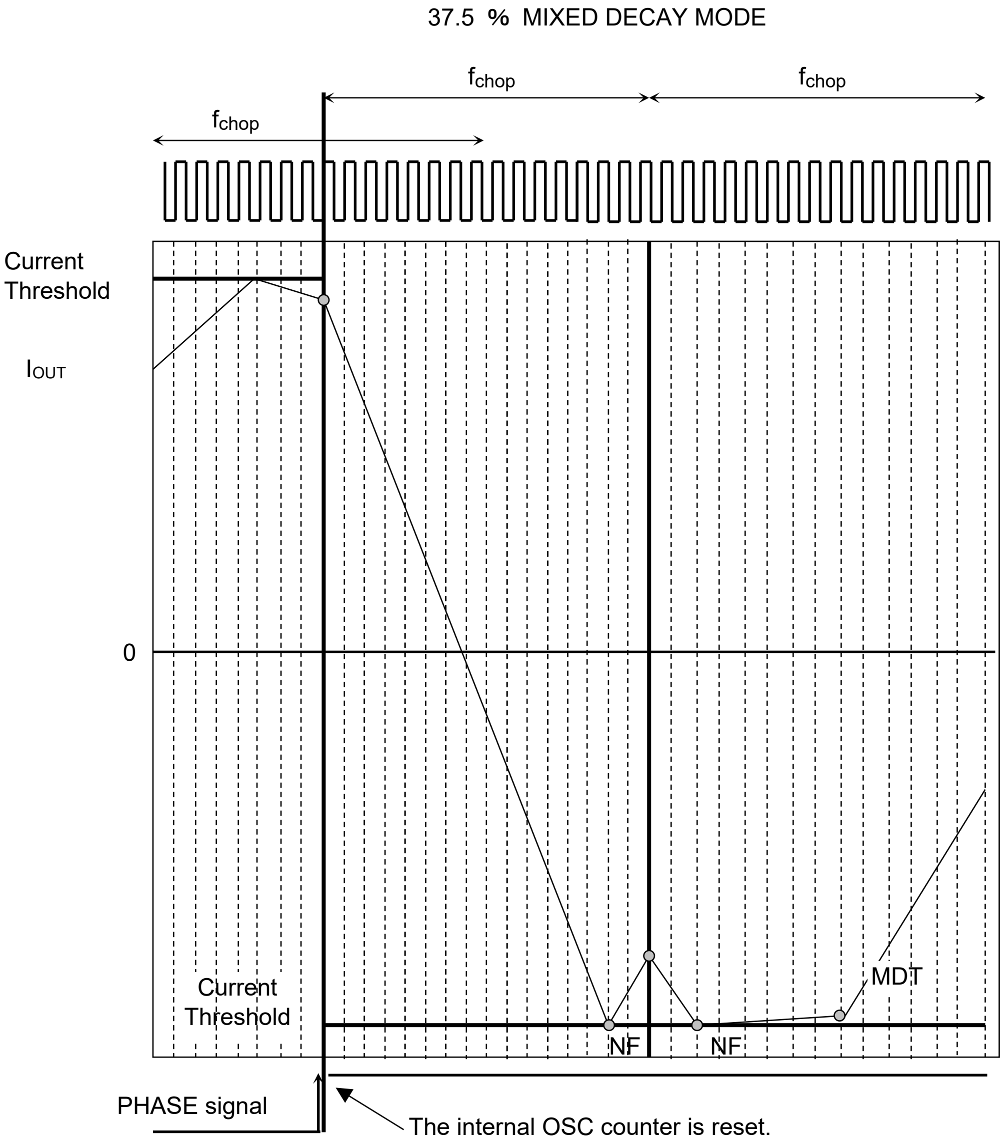
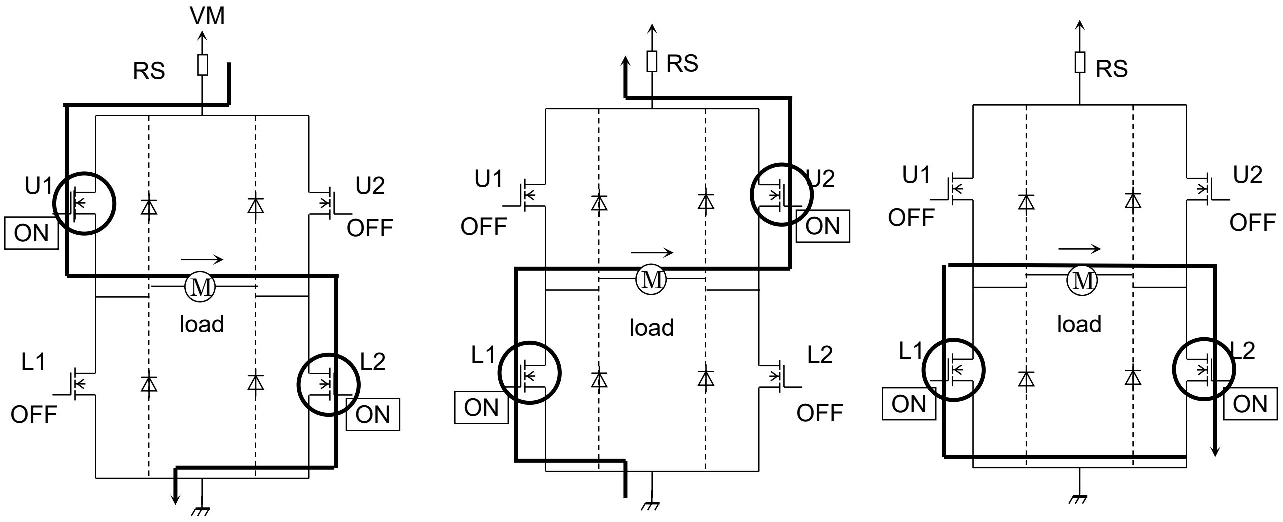


Figure15 PHASE signal and internal CR CLK and output current waveforms

16. Motor output function



Charge mode
Flows the current
into the load.

Slow mode
Circulates the current
within the device and

Fast mode
Recirculates the energy back
to the power supply.

Figure16 Motor output MOSFET operation mode

Note: The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

16.1. Motor output function

Table16.1 At positive current

Mode	U1	U2	L1	L2
CHARGE	ON	OFF	OFF	ON
SLOW	OFF	OFF	ON	ON
FAST	OFF	ON	ON	OFF

Note: The table above is an example when the current flow in the direction shown in the figure above.
The table below shows when it is in reverse.

Table16.2 At negative current

Mode	U1	U2	L1	L2
CHARGE	OFF	ON	ON	OFF
SLOW	OFF	OFF	ON	ON
FAST	ON	OFF	OFF	ON

This device controls each mode automatically to achieve the constant current drive.
The device has a dead time to avoid shoot-through current during the mode changes.

17. Current threshold calculation

The peak current (current threshold) is set by current sense resistor (R_S) and reference voltage (V_{REF}).

$$I_{OUT(max)} = V_{REF(gain)} \times \frac{V_{REF}(V)}{R_S(\Omega)}$$

$V_{REF(gain)}$: $V_{REFgain}$ is rated at 1 / 5.0 (typ.).

Example) When current ratio is 100 %,

When V_{REF} = 3.0 V, Torque = 100 %, R_S = 0.51 Ω is applied

the current threshold (peak current) is calcculated as below;

I_{OUT} = 3.0 V / 5.0 / 0.51 Ω= 1.18 A

18. OSCM frequency calculation

The approximation of the OSCM frequency (f_{OSCM}) and chopping frequency (f_{chop}) can be calculated by below.

f_{OSCM}=1/[0.60x{Cx(R_1+500)}]
………C,R_1 : OSCM resistor and capacitor value (e.g. C=270 pF , R_1=3.6 kΩ)

f_{chop} = f_{OSCM} / 16

Increasing the chopping frequency will decrease the current ripple, which will lead to a better waveform quality. But it will also increase the gate loss, leading to an increase in heat generation.
Decreasing the chopping frequency will most likely lower the heat generation, but will also lead to an increase in the current ripple.
Therefore, as a reference the chopping frequency should be set to 70 kHz first, then be adjusted between the range of 50 kHz to 100 kHz, depending on each customer’s usage conditions.

19. Power consumption

The power consumed within the device is mainly separated into two groups; the output power stage and the internal logic.

19.1. Motor output power consumption ($R_{ds(on)}$= 0.6 Ω)

The power consumption of the output stage is mainly due to the H-Bridges.

The power consumption within the two H-Bridges can be calculated as below.

$P_{(out)} = 2\ \text{(H-Bridge)} \times I_{OUT}\ (A) \times V_{DS}\ (V) = 2\ \text{(H-Bridge)} \times I_{OUT}\ (A)^2 \times R_{ds(on)}\ (\Omega)$ ...... (1)

Controlling the motor in full step mode ideally will make the motor current to a trapezoidal waveform. In this case, the average power consumption can be calculated as shown below.

Example:
$R_{ds(on)} = 0.6\ \Omega$, $I_{OUT\ (peak:\ Max)} = 1.0\ A$, $V_M = 24\ V$
$P_{(out)} = 2\ \text{(H-Bridge)} \times 1.0\ (A)^2 \times 0.6(\Omega)$ ....(2)
$= 1.2\ (W)$

19.2. Internal logic power consumption

There are two states in which the internal logic power consumption can be considered.

$I_{(IM3)} = 5.5$ mA (typ.) : When motor is in operation.
$I_{(IM2)} = 3.5$ mA (typ.) : When motor is stopped.

The output is connected to the V_M(24 V); therefore, the power consumed should be multiplied by the VM and IM.

The power consumption in this case can be calculated as below.

$P_{(IM3)} = 24\ (V) \times 0.0055\ (A)$ .... (3)
$= 0.132\ (W)$

The power consumption can also be calculated when the motor is not in operation.

$P_{(IM2)} = 24\ (V) \times 0.0035\ (A) = 0.084\ (W)$

19.3. Total power consumption

As a result from (2) and (3) above, the total power consumption can be calculated as shown below.

$P = P_{(out)} + P_{(IM)} = 1.332\ (W)$

Note that the calculation is just a reference and the margin for PCB design should be considered based on evaluation and consideration under the actual usage conditions.

20. OSCM-Charge DELAY:

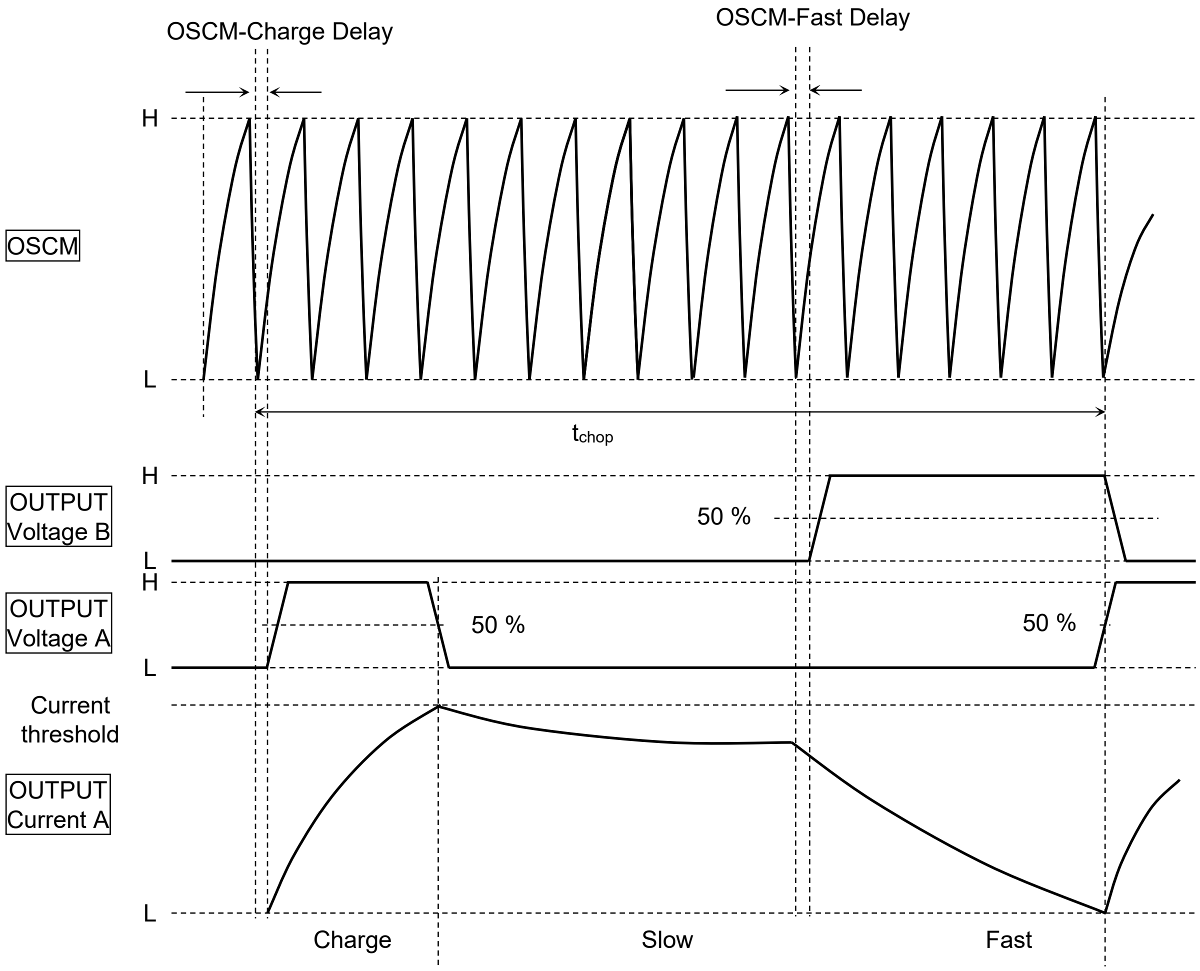


Figure20.1 OSCM-Charge DELAY

Note: Timing charts may be simplified for explanatory purpose.

When transferring the OSCM waveform into the internal OSC, there will be some delay due to the level determination of the OSCM waveform. The maximum delay between the OSCM and the internal OSC is nearly 1 µs (f_{OSCM} = 1600 kHz).

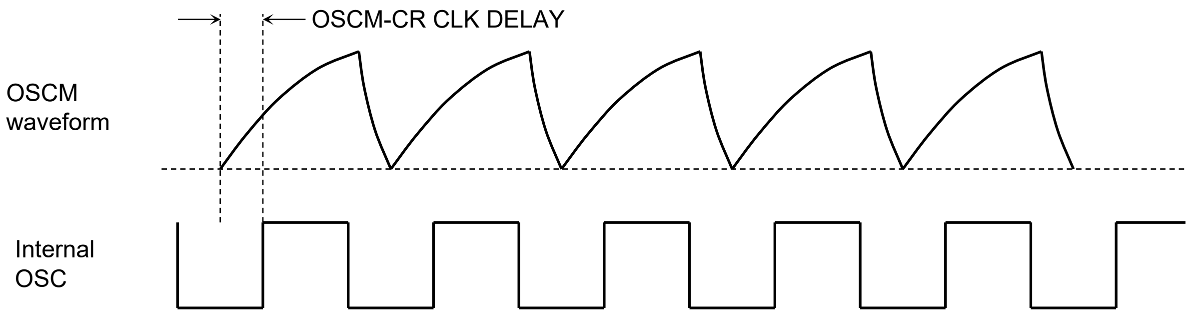


Figure20.2 Timing charts of the OSCM and the internal OSC waveform

Note: Timing charts may be simplified for explanatory purpose.

21. Step resolution sequence

21.1. Full step resolution sequence

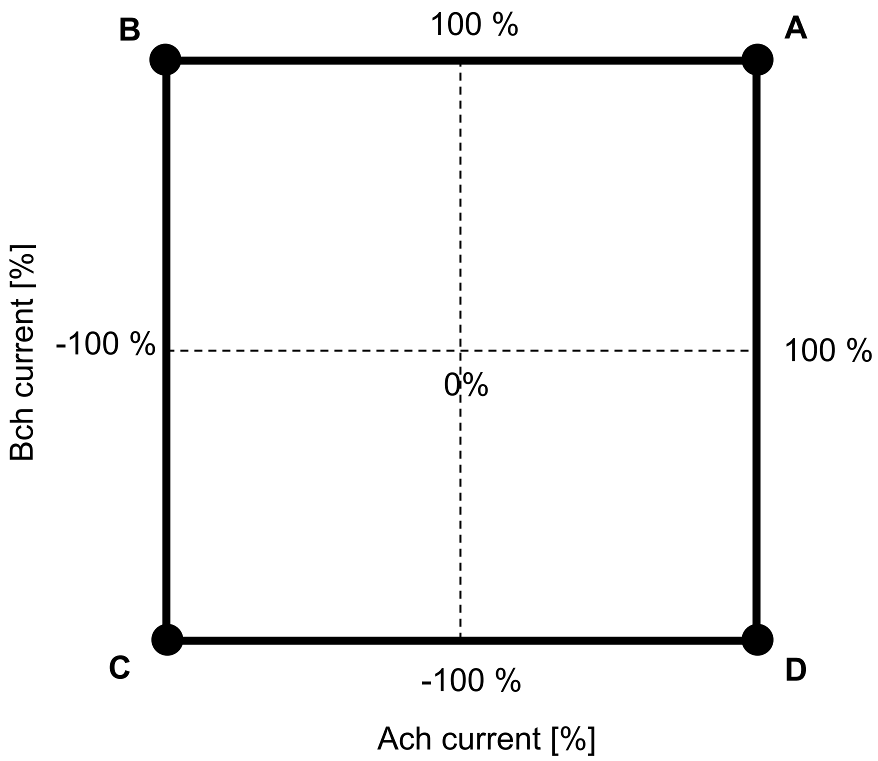


Figure21.1.1 Full step resolution sequence

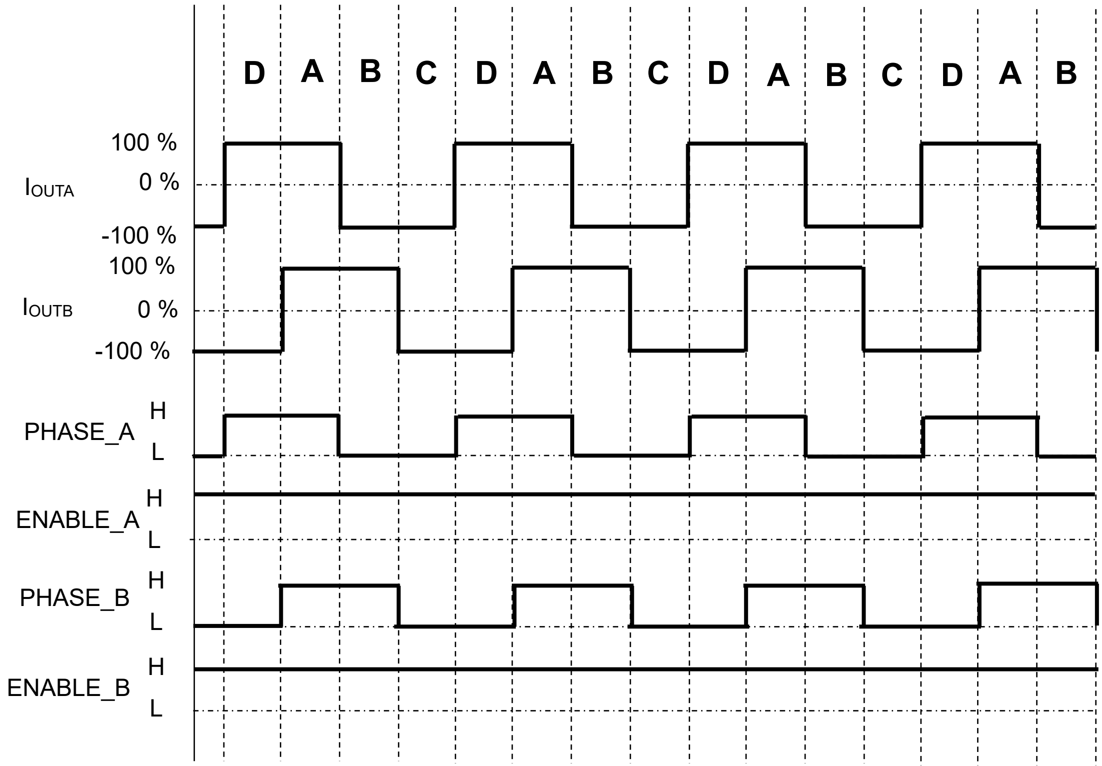


Figure21.1.2 Full step resolution sequence timing chart

Note: Timing charts may be simplified for explanatory purpose.

21.2. Half step resolution sequence

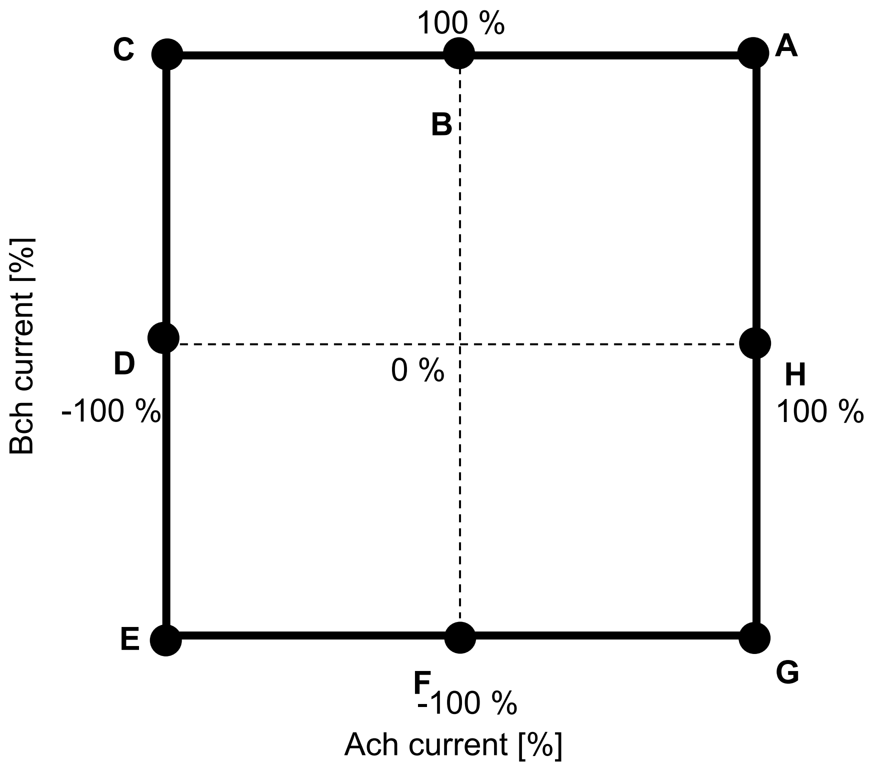


Figure21.2.1 Half step resolution sequence

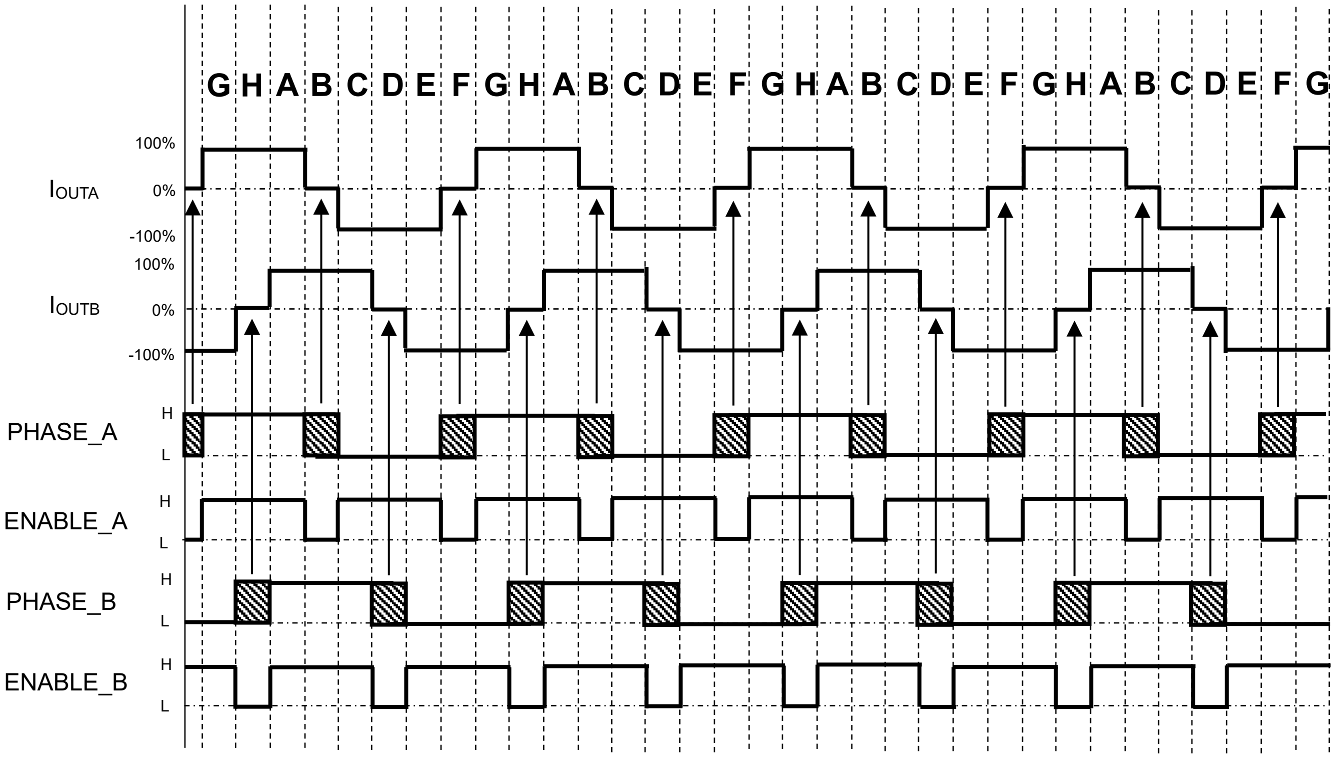


Figure21.2.2 Half step resolution sequence timing chart

Note: Timing charts may be simplified for explanatory purpose.

22. Step resolution sequence

22.1. Full step sequence(TRQ1/TRQ2,TRQ3,TRQ4 settings)

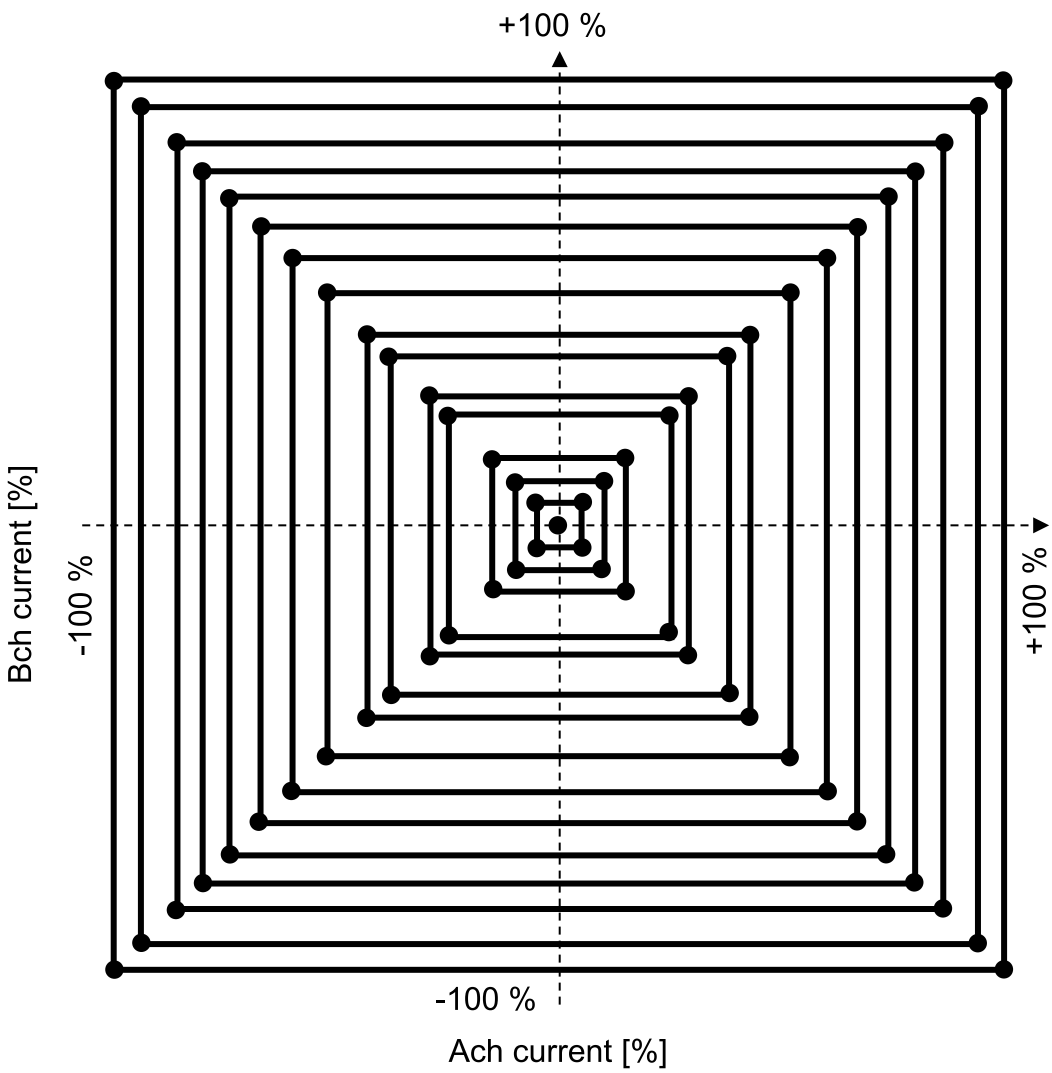


Figure22.1 Full step sequence

Figure22.1.1 (Example) <Full step>（TRQ1,TRQ2,TRQ3,TRQ4=H,H,H,H=100 %）

Ach			Bch		
Input		Output	Input		Output
PHASE_A	ENABLE_A	$I_{OUT(A)}$	PHASE_B	ENABLE_B	$I_{OUT(B)}$
H	H	+100 %	H	H	+100 %
L	H	-100 %	H	H	+100 %
L	H	-100 %	L	H	-100 %
H	H	+100 %	L	H	-100 %

Figure22.1.2 (Example) <Full step> （TRQ1,TRQ2,TRQ3,TRQ4=H,L,L,H=60 %）

Ach			Bch		
Input		Output	Input		Output
PHASE_A	ENABLE_A	$I_{OUT(A)}$	PHASE_B	ENABLE_B	$I_{OUT(B)}$
H	H	+60 %	H	H	+60 %
L	H	-60 %	H	H	+60 %
L	H	-60 %	L	H	-60 %
H	H	+60 %	L	H	-60 %

22.2. Half step sequence(TRQ1/TRQ2,TRQ3,TRQ4 settings)

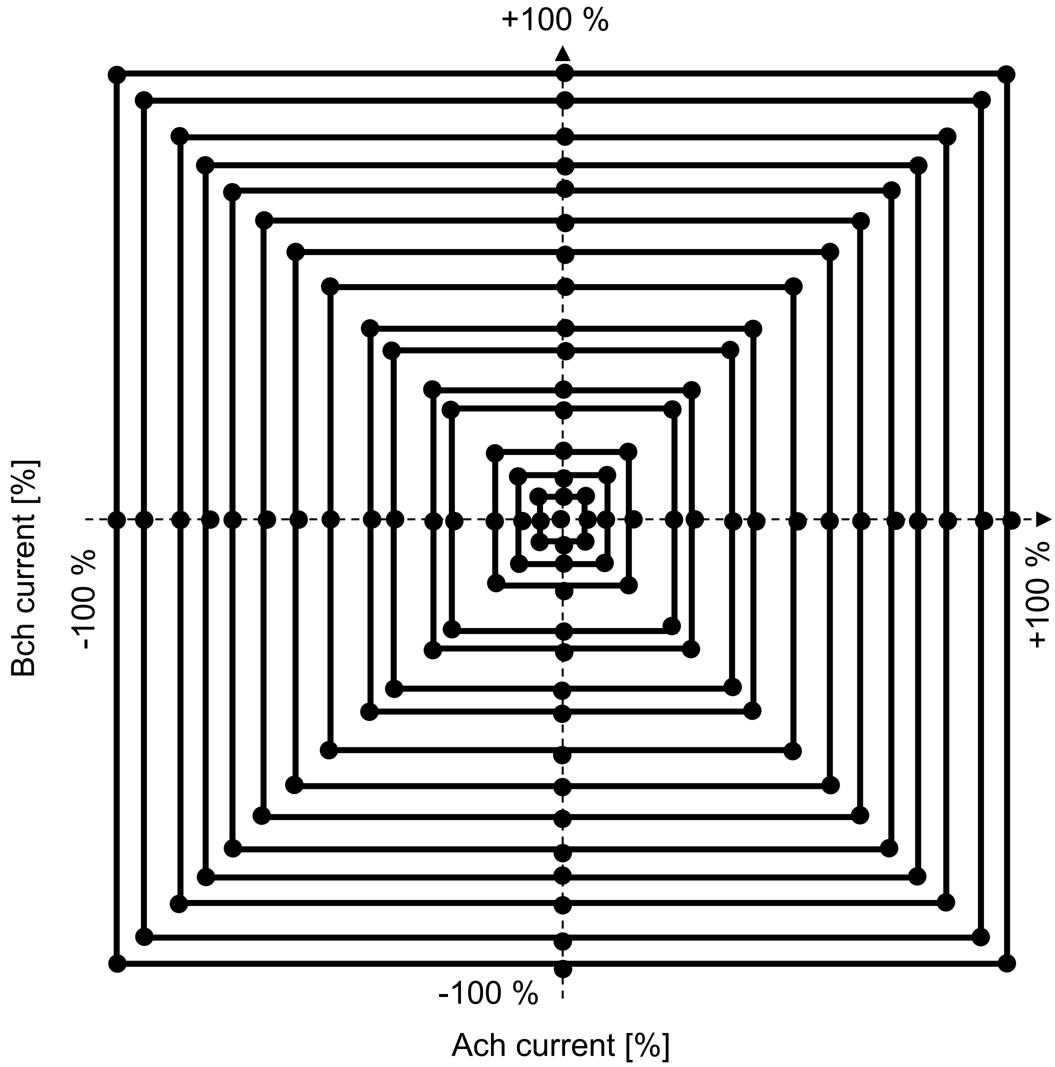


Figure22. 2 Half step sequence

Figure22.2.1 (Example) <Half step(a)> （TRQ1,TRQ2,TRQ3,TRQ4=H,H,H,H=100 %）

Ach			Bch		
Input		Output	Input		Output
PHASE_A	ENABLE_A	IOUT (A)	PHASE_B	ENABLE_B	IOUT (B)
H	H	+100 %	H	H	+100 %
X	L	0	H	H	+100 %
L	H	-100 %	H	H	+100 %
L	H	-100 %	X	L	0
L	H	-100 %	L	H	-100 %
X	L	0	L	H	-100 %
H	H	+100 %	L	H	-100 %
H	H	+100 %	X	L	0

X: Don’t care

Figure22.2.2 (Example) <Half step(a)>　(TRQ1,TRQ2,TRQ3,TRQ4=L,H,L,L=25 %)

Ach			Bch		
Input		Output	Input		Output
PHASE_A	ENABLE_A	$I_{OUT\ (A)}$	PHASE_B	ENABLE_B	$I_{OUT\ (B)}$
H	H	+25 %	H	H	+25 %
X	L	0	H	H	+25 %
L	H	-25 %	H	H	+25 %
L	H	-25 %	X	L	0
L	H	-25 %	L	H	-25 %
X	L	0	L	H	-25 %
H	H	+25 %	L	H	-25 %
H	H	+25 %	X	L	0

x: Don’t care

23. Blanking time for over current detection

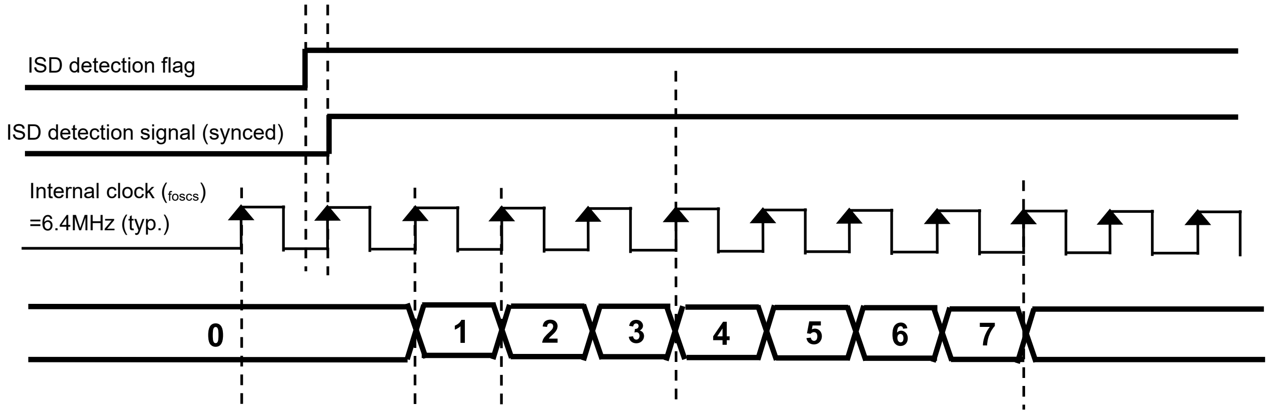


Figure23 Blanking time for over current detection timing chart

Note: Timing charts may be simplified for explanatory purpose.

To avoid misdetecting the ISD which may be caused by external noise or switching spikes, the ISD circuit has a blanking
time. This blanking time is counted up by the internal system clock(6.4 MHz (typ.)).

※f_{oscs}=6.4MHz(typ.) internal clock
1/f_{oscs}×7 to 8 clk (1.09 μs to 1.25 μs)

Note: that this blanking time is just a designed value and only for reference. It does not guarantee that the ISD will be detected in the ideal way when used in the actual conditions. Therefore, for safety measures, please insert a protective fuse in the VM power line. The optimum value of the fuse will change in each customer's usage conditions, so please select a fuse with enough margin to operate correctly and safely.

24. Blanking time for over thermal detection

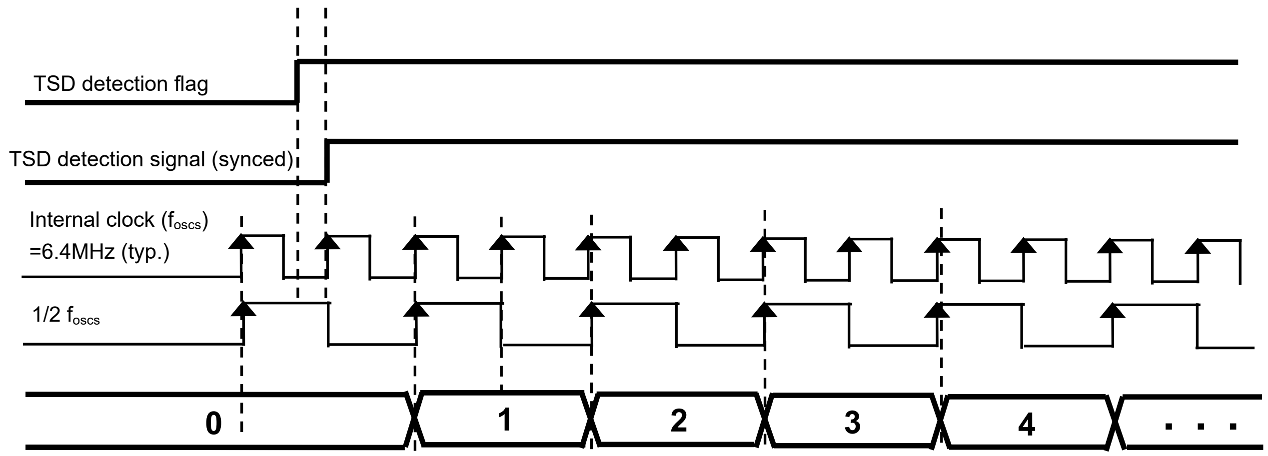


Figure24 Blanking time for over thermal detection timing chart

Note: Timing charts may be simplified for explanatory purpose.
To avoid misdetecting the TSD, the TSD circuit has a blanking time. This blanking time is counted up by the internal system
clock(6.4 MHz (typ.)).

Note: f_{oscs}=6.4 MHz(typ.) internal clock
1/(f_{oscs}/2)×7 to 8 clk=1/f_{oscs}×14 to 16 clk (2.18 μs to 2.5 μs)

25. (For reference) PD-Ta graph

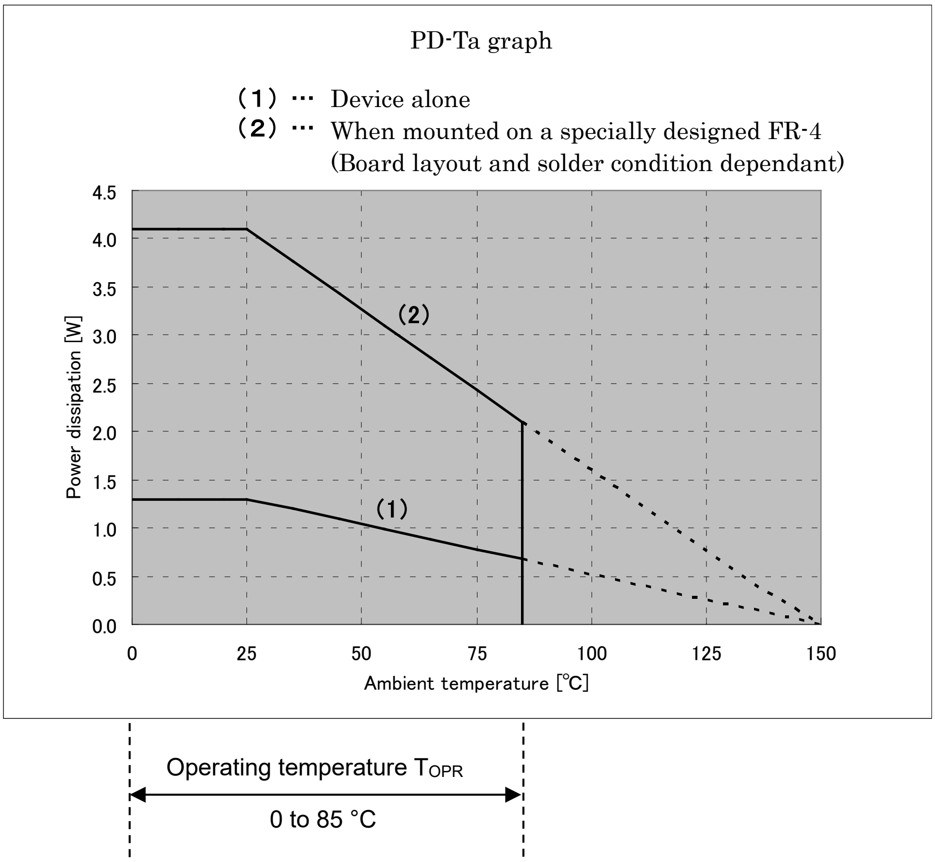


Figure25 (For reference) PD-Ta graph

(1) Rth(j-a) Device alone (96 °C /W)

(2) When mounted on a specially designed FR-4 PCB (100 mm × 200 mm × 1.6 mm: 30 °C /W : reference value)

Device alone(T_a = 25 °C)

If the T_a exceeds above 25 °C, de-rate by 10.4 mW/°C

When mounted on a specially designed FR4(T_a = 25 °C)

If the T_a exceeds above 25 °C, de-rate by 33.3 mW/°C

26. TB67S105FTG application circuit

(Values of the components are for reference.)

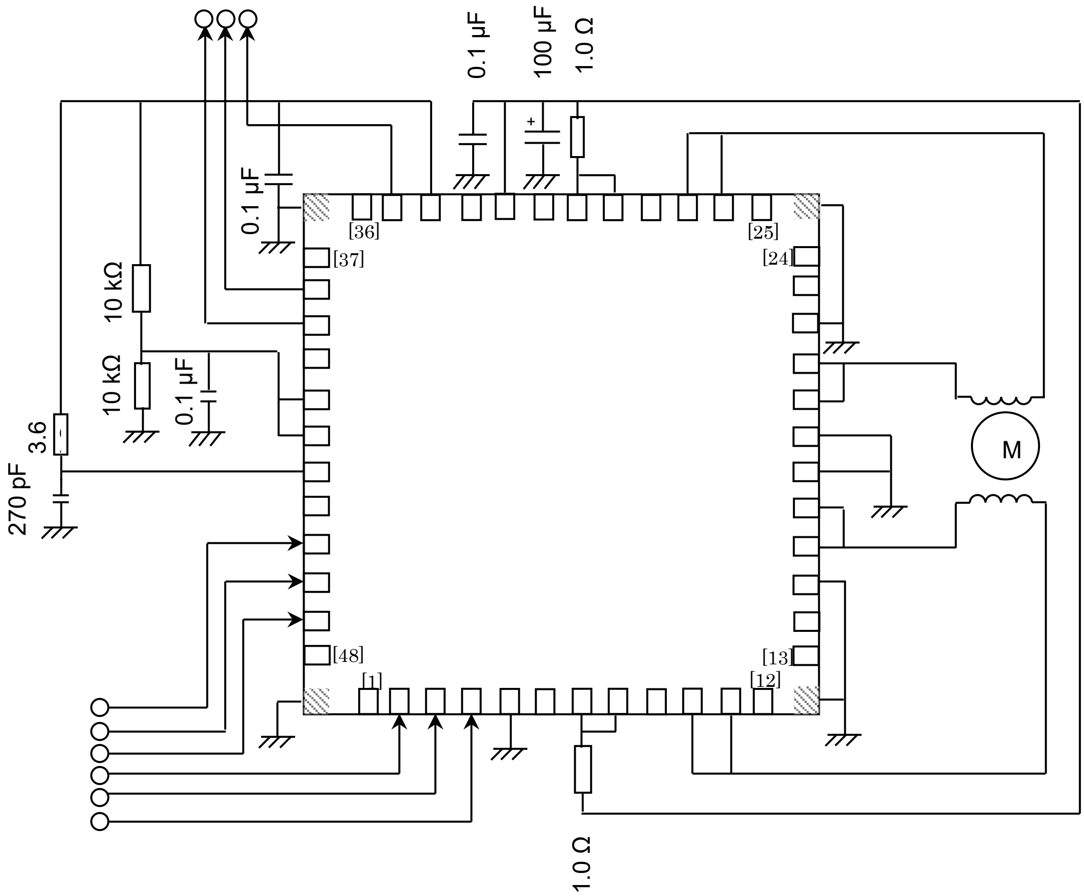


Figure26 TB67S105FTG application circuit

Note that the shaded area shown above is either the GND pins or GND area, and shown in gray is the NC pins.
Note: Please consider adding capacitors if needed. Also make sure that the GND pattern is connected to each other.
For RS_A, RS_B, OUT_A+, OUT_A-, OUT_B-, and OUT_B+; there are two pins so please tie the same pins together when using the device.
Note: Solder/mount the four corner pads and the exposed pad to the GND area of the board.
Note: The application circuit above is an example; therefore, mass-production design is not guaranteed.

27. Package dimensions

P-WQFN48-0707-0.50-003

Unit: mm

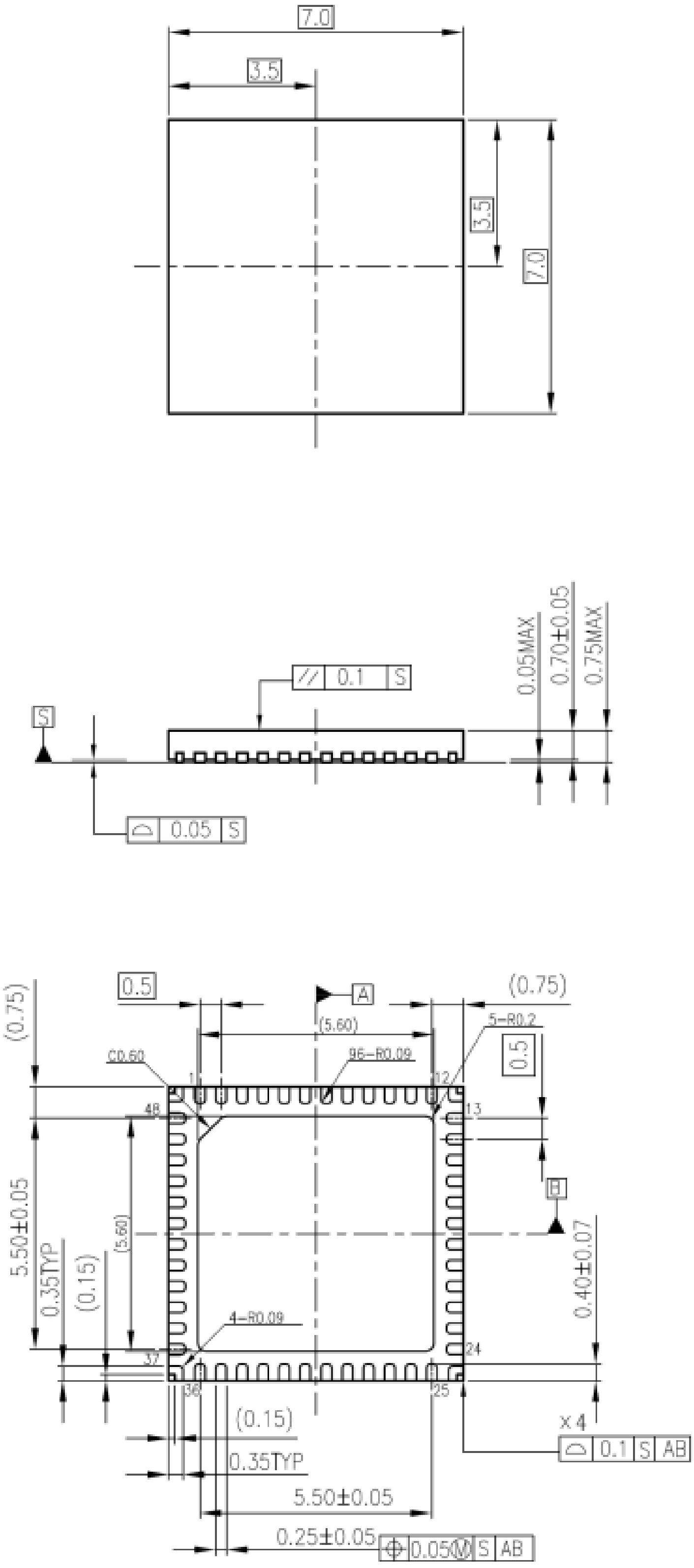


Figure27 Package dimensions

28. Notes on Contents

Block Diagrams
Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

Equivalent Circuits
The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

Timing Charts
Timing charts may be simplified for explanatory purposes.

Application Circuits
The application circuits shown in this document are provided for reference purposes only. Thorough evaluation is required, especially at the mass production design stage.
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Test Circuits
Components in the test circuits are used only to obtain and confirm the device characteristics. These components and circuits are not guaranteed to prevent malfunction or failure from occurring in the application equipment.

29. IC Usage Considerations

29.1. Notes on handling of ICs

(1) The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.
Exceeding the rating(s) may cause the device breakdown, damage, or deterioration, and may result injury by explosion or combustion.

(2) Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead smoke or ignition. To minimize the effects of the flow of a large current in case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.

(3) If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke, or ignition.
Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke, or ignition.

(4) Do not insert devices in the wrong orientation or incorrectly.
Make sure that the positive and negative terminals of power supplies are connected properly. Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.
In addition, do not use any device that is applied the current with inserting in the wrong orientation or incorrectly even just one time.

29.2. Points to remember on handling of ICs

(1) Over Current Protection Circuit

Over current protection circuits (referred to as current limiter circuits) do not necessarily protect ICs under all circumstances. If the Over current protection circuits operate against the over current, clear the over current status immediately.
Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the over current protection circuit to not operate properly or IC breakdown before operation. In addition, depending on the method of use and usage conditions, if over current continues to flow for a long time after operation, the IC may generate heat resulting in breakdown.

(2) Thermal Shutdown Circuit

Thermal shutdown circuits do not necessarily protect ICs under all circumstances. If the thermal shutdown circuits operate against the over temperature, clear the heat generation status immediately.
Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the thermal shutdown circuit to not operate properly or IC breakdown before operation.

(3) Heat Radiation Design

In using an IC with large current flow such as power amp, regulator, or driver, please design the device so that heat is appropriately radiated, not to exceed the specified junction temperature (T_j) at any time and condition. These ICs generate heat even during normal use. An inadequate IC heat radiation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, please design the device taking into considerate the effect of IC heat radiation with peripheral components.

(4) Back-EMF

When a motor rotates in the reverse direction, stops, or slows down abruptly, a current flow back to the motor's power supply due to the effect of back-EMF. If the current sink capability of the power supply is small, the device's motor power supply and output pins might be exposed to conditions beyond absolute maximum ratings. To avoid this problem, take the effect of back-EMF into consideration in system design.

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