MOSFETs Silicon P-Channel MOS

# SSM3J65CT

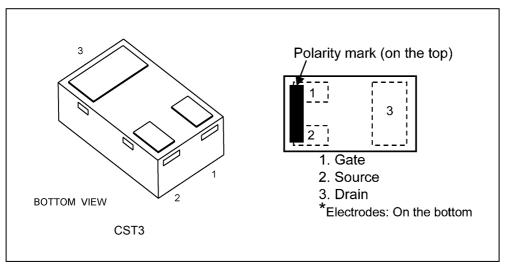
#### 1. Applications

Power Management Switches

#### 2. Features

- (1) 1.2 V drive
- (2) Low drain-source on-resistance
  - $\begin{array}{l} : {\rm R}_{\rm DS(ON)} = 1110 \mbox{ m}\Omega\ ({\rm typ.})\ (@V_{\rm GS} = -1.2 \mbox{ V}) \\ {\rm R}_{\rm DS(ON)} = 780 \mbox{ m}\Omega\ ({\rm typ.})\ (@V_{\rm GS} = -1.5 \mbox{ V}) \\ {\rm R}_{\rm DS(ON)} = 650 \mbox{ m}\Omega\ ({\rm typ.})\ (@V_{\rm GS} = -1.8 \mbox{ V}) \\ {\rm R}_{\rm DS(ON)} = 510 \mbox{ m}\Omega\ ({\rm typ.})\ (@V_{\rm GS} = -2.5 \mbox{ V}) \\ {\rm R}_{\rm DS(ON)} = 400 \mbox{ m}\Omega\ ({\rm typ.})\ (@V_{\rm GS} = -4.5 \mbox{ V}) \end{array}$

#### 3. Packaging and Pin Assignment



#### 4. Absolute Maximum Ratings (Note) (Unless otherwise specified, $T_a = 25$ °C)

Characteristics		Symbol	Rating	Unit
Drain-source voltage		V <sub>DSS</sub>	-20	V
Gate-source voltage		V <sub>GSS</sub>	±10	
Drain current (DC)	(Note 1)	I <sub>D</sub>	-700	mA
Drain current (pulsed)	(Note 1)	I <sub>DP</sub>	-1400	
Power dissipation	(Note 2)	PD	500	mW
Channel temperature		T <sub>ch</sub>	150	°C
Storage temperature		T <sub>stg</sub>	-55 to 150	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Ensure that the channel temperature does not exceed 150 °C.

Note 2: Device mounted on a 25.4 mm × 25.4 mm × 1.6 mm FR4 glass epoxy board (Cu pad: 645 mm<sup>2</sup>)

Note: This transistor is sensitive to electrostatic discharge and should be handled with care.

- Note: The MOSFETs in this device are sensitive to electrostatic discharge. When handling this device, the worktables, operators, soldering irons and other objects should be protected against anti-static discharge.
- Note: The channel-to-ambient thermal resistance, R<sub>th(ch-a)</sub>, and the drain power dissipation, P<sub>D</sub>, vary according to the board material, board area, board thickness and pad area. When using this device, be sure to take heat dissipation fully into account.

#### 5. Electrical Characteristics

#### 5.1. Static Characteristics (Unless otherwise specified, T<sub>a</sub> = 25 °C)

Characteristics		Symbol	Test Condition	Min	Тур.	Max	Unit
Gate leakage current		I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±8 V	_	—	±1	μA
Drain cut-off current		I <sub>DSS</sub>	V <sub>DS</sub> = -20 V, V <sub>GS</sub> = 0 V	_	_	-1	
Drain-source breakdown voltage		V <sub>(BR)DSS</sub>	I <sub>D</sub> = -1 mA, V <sub>GS</sub> = 0 V	-20		_	V
Drain-source breakdown voltage	(Note 1)	V <sub>(BR)DSX</sub>	I <sub>D</sub> = -1 mA, V <sub>GS</sub> = 5 V	-15	_	_	
Gate threshold voltage	(Note 2)	V <sub>th</sub>	V <sub>DS</sub> = -3 V, I <sub>D</sub> = -1 mA	-0.3	—	-1.0	
Drain-source on-resistance	(Note 3)	R <sub>DS(ON)</sub>	I <sub>D</sub> = -10 mA, V <sub>GS</sub> = -1.2 V	—	1110	11300	mΩ
			I <sub>D</sub> = -50 mA, V <sub>GS</sub> = -1.5 V	—	780	1550	
			I <sub>D</sub> = -100 mA, V <sub>GS</sub> = -1.8 V	_	650	1070	
			I <sub>D</sub> = -300 mA, V <sub>GS</sub> = -2.5 V	_	510	700	
			I <sub>D</sub> = -500 mA, V <sub>GS</sub> = -4.5 V	_	400	500	
Forward transfer admittance	(Note 3)	Y <sub>fs</sub>	V <sub>DS</sub> = -3 V, I <sub>D</sub> = -700 mA	_	2.2	_	S

Note 1: If a reverse bias is applied between gate and source, this device enters V<sub>(BR)DSX</sub> mode. Note that the drainsource breakdown voltage is lowered in this mode.

Note 3: Pulse measurement.

#### 5.2. Dynamic Characteristics (Unless otherwise specified, $T_a = 25$ °C)

Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Input capacitance	C <sub>iss</sub>	V <sub>DS</sub> = -10 V, V <sub>GS</sub> = 0 V,	_	48	—	pF
Reverse transfer capacitance	C <sub>rss</sub>	f = 1 MHz	_	4.6	—	
Output capacitance	C <sub>oss</sub>		_	8.9	_	
Switching time (turn-on time)	t <sub>on</sub>	$V_{DD}$ = -10 V, I <sub>D</sub> = -100 mA, V <sub>GS</sub> = 0 to -4.5 V, R <sub>GS</sub> = 50 Ω		130		ns
Switching time (turn-off time)		Duty $\leq$ 1 %, V <sub>IN</sub> : t <sub>r</sub> , t <sub>f</sub> < 5 ns, Common source, See Chapter 5.3.		1075	_	

#### 5.3. Switching Time Test Circuit

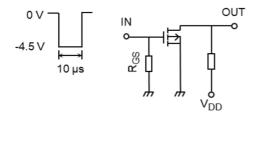


Fig. 5.3.1 Switching Time Test Circuit

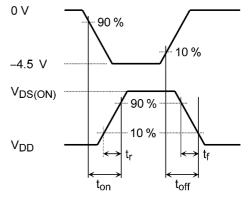


Fig. 5.3.2 Input Waveform/Output Waveform

#### 5.4. Source-Drain Characteristics (Unless otherwise specified, $T_a = 25$ °C)

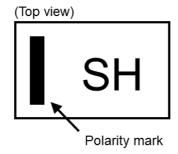
Characteristics		Symbol	Test Condition	Min	Тур.	Max	Unit
Diode forward voltage	(Note 1)	$V_{DSF}$	I <sub>D</sub> = 700 mA, V <sub>GS</sub> = 0 V	_	0.94	1.2	V
Note 1: Pulse measurement.							

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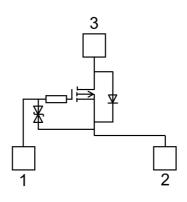
Note 2: Let  $V_{th}$  be the voltage applied between gate and source that causes the drain current (I<sub>D</sub>) to below (-1 mA for this device). Then, for normal switching operation,  $V_{GS(ON)}$  must be higher than  $V_{th}$ , and  $V_{GS(OFF)}$  must be lower than  $V_{th}$ . This relationship can be expressed as:  $V_{GS(OFF)} < V_{th} < V_{GS(ON)}$ . Take this into consideration when using the device.



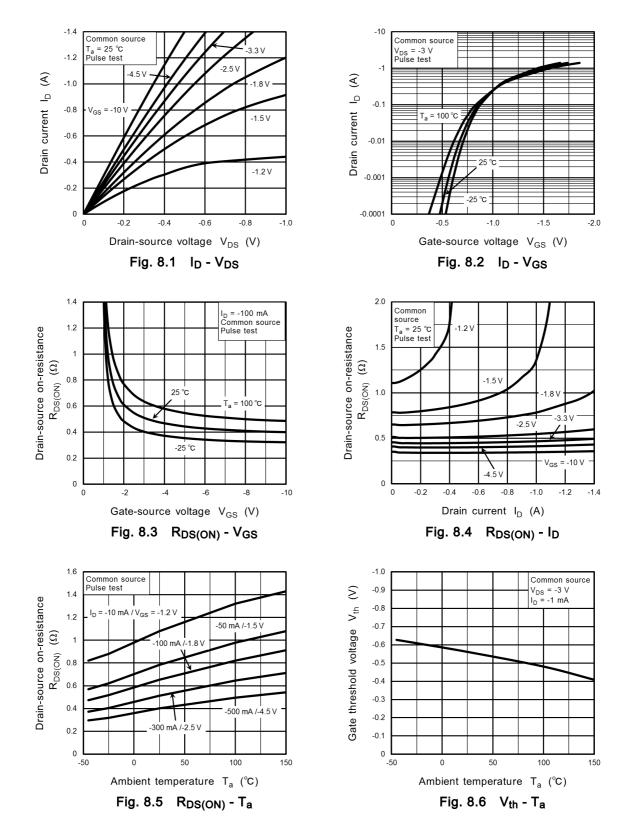
#### 6. Marking

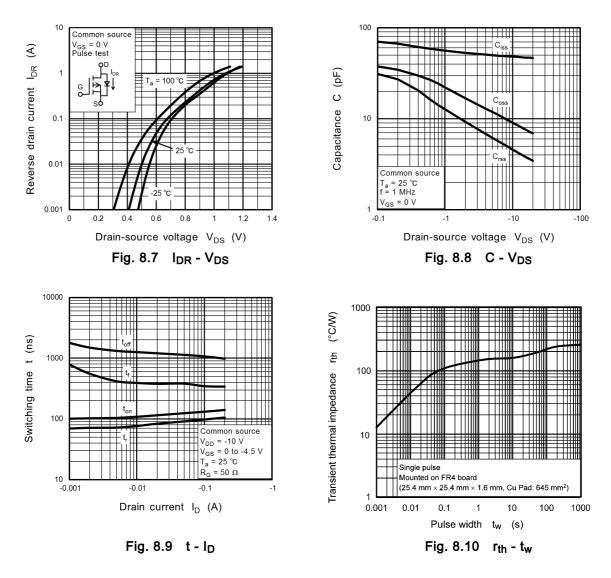


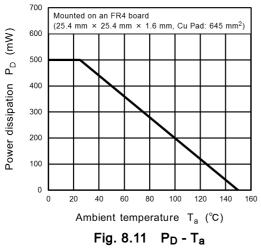
7. Equivalent Circuit



#### 8. Characteristics Curves (Note)





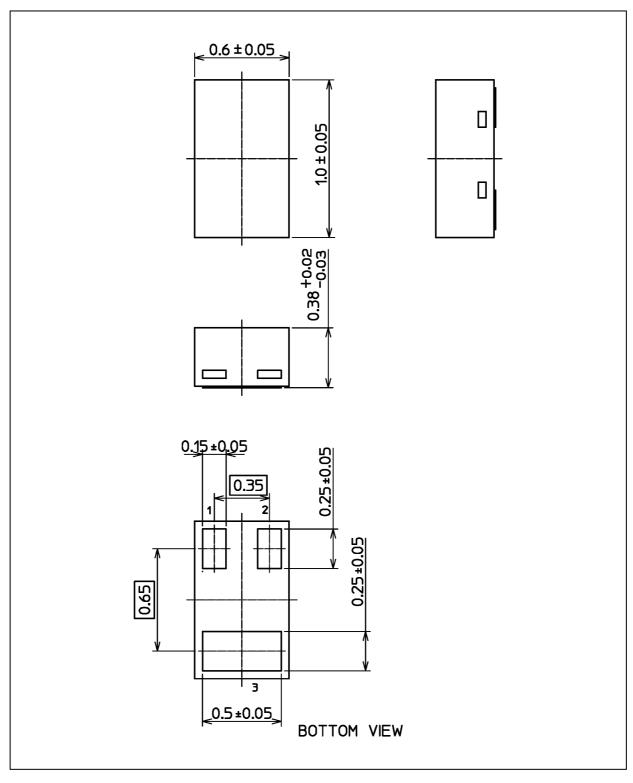




### SSM3J65CT

#### **Package Dimensions**

Unit: mm





Package Name(s)

Nickname: CST3

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