

TOSHIBA Digital Integrated Circuit Silicon Monolithic

T3GE9WBG

Dual Supply Bus Transceiver for SD Card

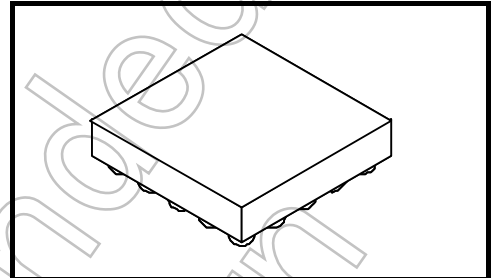
The T3GE9WBG is a dual supply, advanced high-speed CMOS dual supply voltage interface bus transceiver fabricated with silicon gate CMOS technology.

Designed for use as an interface between a 1.8-V bus and a 2.9-V bus in mixed 1.8-V/2.9-V supply systems.

The A-port interfaces with the 1.8-V bus, the B-port with the 2.9-V bus.

The direction of data transmission is determined by the level of the DIR input.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.



Weight: 0.006 g (typ.)

Features

Bidirectional interface between 1.8-V and 2.9-V buses.

High-speed operation : $t_{pd} = 8.5 \text{ ns (max)}$ ($V_{CCA} = 1.8 \pm 0.15 \text{ V}$, $V_{CCB} = 2.9 \pm 0.1 \text{ V}$)

Output current : $I_{OHB}/I_{OLB} = \pm 6 \text{ mA (min)}$ ($V_{CCB} = 2.8 \text{ V}$)
 $I_{OHA}/I_{OLA} = \pm 6 \text{ mA (min)}$ ($V_{CCA} = 1.65 \text{ V}$)

Regulator output current: 200mA (min)

Integrated EMI filter on B-port

Integrated Pull-up and Pull-down resistors on B-port

Latch-up performance : $\pm 200 \text{ mA}$

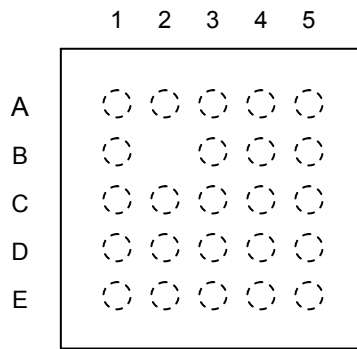
ESD performance : Machine model $> \pm 200 \text{ V}$
 Human body model $> \pm 2000 \text{ V}$

IEC61000-4-2 Level 4 (Contact) $> \pm 8000 \text{ V}$ (SD card side)

Ultra-small package : WCSP24

Start of commercial production
2008-07

Pin Assignment (top view)



(Top view)

	1	2	3	4	5
A	Dat2.h	CMD-dir	Dat0-dir	V _{Batt}	Dat2-B
B	Dat3.h	--	V _{CCA}	V _{CCB} O/P	Dat3-B
C	Clk.h	Enable	GND	GND	CLK-B
D	Dat0.h	CMD.h	CD	CMD-B	Dat0-B
E	Dat1.h	Clk-f	Dat123-dir	WP	Dat1-B

Truth Table

Input	Outputs	
Clk.h	Clk-f	CLK-B
L	L	L
H	H	H

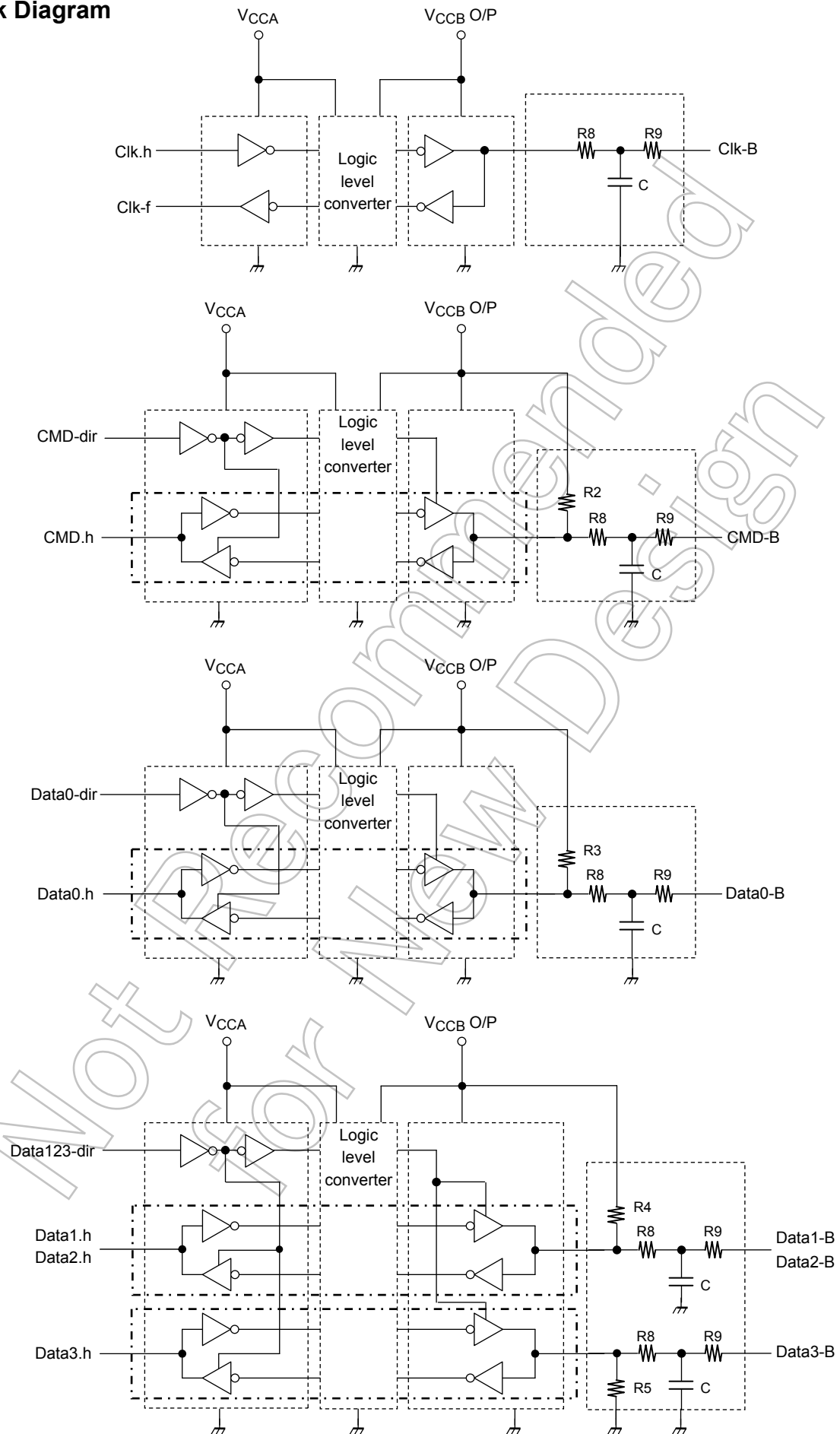
Inputs	Function		Outputs
CMD-dir	CMD.h	CMD-B	
L	Output	Input	CMD.h = CMD-B
H	Input	Output	CMD-B = CMD.h

Inputs	Function		Outputs
Dat0-dir	Dat0.h	Dat0-B	
L	Output	Input	Dat0.h = Dat0-B
H	Input	Output	Dat0-B = Dat0.h

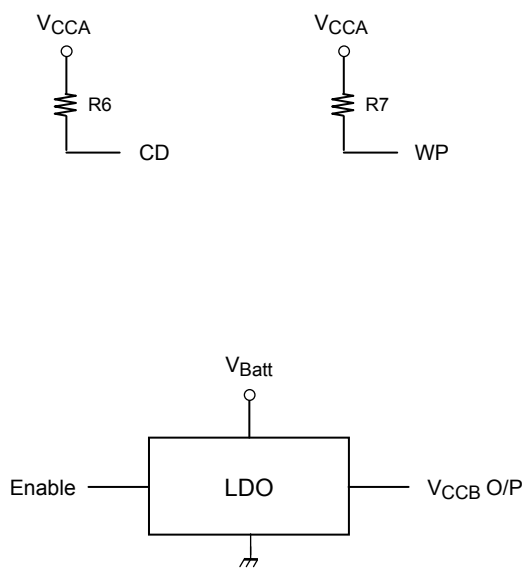
Inputs	Function		Outputs
Dat123-dir	Dat1.h – Dat3.h	Dat1-B – Dat3-B	
L	Output	Input	Datn.h = Datn-B
H	Input	Output	Datn-B = Datn.h

Input	Output
Enable	Regulator
L	OFF
H	ON

Block Diagram



Block Diagram



Symbol	Value (typ)
R3, R4	70k Ω
R2	15k Ω
R5	470k Ω
R6, R7	100k Ω
R8	5 Ω
R9	35 Ω
C	35pF

Absolute Maximum Ratings (Note 1)

Characteristics		Symbol	Rating	Unit
Power supply voltage		V_{CCA}	-0.5 to 3.0	V
		V_{Batt}	5.5	
DC input voltage	DIR, Clk.h	V_{IN}	-0.5 to $V_{CCA} + 0.5$	V
	Enable		-0.5 to 5.5	
DC bus I/O voltage		$V_{I/OA}$	-0.5 to $V_{CCA} + 0.5$ (Note 2)	V
		$V_{I/OB}$	-0.5 to $V_{CCB} + 0.5$ (Note 2)	
Input diode current	DIR, Clk.h	I_{IK}	± 25	mA
	Enable		-25	
Output diode current		$I_{I/OK}$	± 25 (Note 3)	mA
DC output current		I_{OUTA}	± 25	mA
		I_{OUTB}	± 25	
DC V_{CC} /ground current per supply pin		I_{CCA}	± 50	mA
Power dissipation		P_D	400	mW
Storage temperature		T_{stg}	-55 to 150	$^{\circ}\text{C}$

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Note 2: High or Low stats. I_{OUT} absolute maximum rating must be observed.

Note 3: $V_{OUT} < \text{GND}$, $V_{OUT} > V_{CC}$

Operating Range (Note 1)

Characteristics		Symbol	Rating	Unit
Power supply voltage		V_{CCA}	1.65 to 1.95	V
		V_{Batt}	3.2 to 5.0	
Input voltage	DIR, Clk.h	V_{IN}	0 to V_{CCA}	V
	Enable		0 to 5.0	
Bus I/O voltage		$V_{I/OA}$	0 to V_{CCA} (Note 2)	V
		$V_{I/OB}$	0 to V_{CCB} O/P (Note 2)	
Output current		I_{OUTA}	± 6 (Note 3)	mA
		I_{OUTB}	± 6 (Note 4)	
Operating temperature		T_{opr}	-30 to 85	$^{\circ}\text{C}$
Input rise and fall time		dt/dv	0 to 10 (Note 5)	ns/V

Note 1: The operating range is required to ensure the normal operation of the device. Unused inputs and bus inputs must be tied to either V_{CC} or GND. Please connect both bus inputs and the bus outputs with V_{CC} or GND when the I/O of the bus terminal changes by the function. In this case, please note that the output is not short-circuited.

Note 2: High or low state

Note 3: $V_{CCA} = 1.65$ to 1.95 V

Note 4: $V_{CCB} = 2.8$ to 3.0 V, V_{CCB} is supplied from the built-in LDO.

Note 5: $V_{CCA} = 1.65$ V, $V_{CCB} = 2.8$ V

Not Recommended for New Design

Electrical Characteristics

DC Characteristics (1.65 V ≤ V_{CCA} ≤ 1.95 V, 2.8 V ≤ V_{CCB} ≤ 3.0 V)

Characteristics	Symbol	Test Condition	V _{CCA} (V)	V _{CCB} (V)	Ta = -30 to 85°C		Unit	
					Min	Max		
H-level input voltage	V _{IHA}	DIR, An (Note 1)	1.65 to 1.95	2.8 to 3.0	V _{CCA} × 0.65	—	V	
	V _{IHB}	Bn (Note 1)	1.65 to 1.95	2.8 to 3.0	2.0	—		
L-level input voltage	V _{ILA}	DIR, An (Note 1)	1.65 to 1.95	2.8 to 3.0	—	V _{CCA} × 0.35	V	
	V _{ILB}	Bn (Note 1)	1.65 to 1.95	2.8 to 3.0	—	0.8		
H-level output voltage	V _{OHA}	V _{IN} = V _{IH} or V _{IL}	I _{OHA} = -100 μA	1.65 to 1.95	2.8 to 3.0	V _{CCA} - 0.2	—	V
			I _{OHA} = -6 mA	1.65	2.8 to 3.0	1.15	—	
	V _{OHB}		I _{OHB} = -100 μA	1.65 to 1.95	2.8 to 3.0	V _{CCB} - 0.2	—	
			I _{OHB} = -6 mA	1.65 to 1.95	2.8	2.2	—	
L-level output voltage	V _{OLA}	V _{IN} = V _{IH} or V _{IL}	I _{OLA} = 100 μA	1.65 to 1.95	2.8 to 3.0	—	0.2	V
			I _{OLA} = 6 mA	1.65	2.8 to 3.0	—	0.3	
	V _{OLB}		I _{OLB} = 100 μA	1.65 to 1.95	2.8 to 3.0	—	0.2	
			I _{OLB} = 6 mA	1.65 to 1.95	2.8	—	0.4	
Input leakage current	I _{IA}	V _{INA} = V _{CCA} or GND DIR = HIGH V _{CD} = V _{WP} = V _{CCA}	1.65 to 1.95	2.8 to 3.0	—	±5.0	μA	
	I _{IB}	V _{CMD-B} , DAT0, DAT1, DAT2 = V _{CCA} V _{DAT3} = GND DIR = LOW V _{CD} = V _{WP} = V _{CCA}	1.65 to 1.95	2.8 to 3.0	—	±5.0		
Quiescent supply current	I _{CCA}	V _{INA} = V _{CCA} or GND DIR = HIGH V _{CD} = V _{WP} = V _{CCA}	1.65 to 1.95	2.8 to 3.0	—	20	μA	

Note 1: An is a host side signal. Bn is a card side signal.

Note: V_{CCB} is supplied from the built-in LDO.

AC Characteristics (Ta = -30 to 85°C, Input: tr = tf = 2.0 ns)

VCCA = 1.8 ± 0.15 V, VCCB = 2.9 ± 0.1 V

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Propagation delay time (Bn → An)	tpLH tpHL	Figure 1, Figure 2	1.0	—	8.5	ns
Propagation delay time (An → Bn)	tpLH tpHL	Figure 1, Figure 2	1.0	—	8.5	ns
Propagation delay time (Clk.h → Clk-f)	tpLH tpHL	Figure 1, Figure 2	1.0	—	14	ns
Output Transition Time (An)	tTLH tTHL	Figure 1, Figure 2	—	1.5	—	ns
Output Transition Time (Bn)	tTLH tTHL	Figure 1, Figure 2	—	1.5	—	ns
Output to output skew	tosLH tosHL	(Note 1)	—	—	0.5	ns

Note 1: Parameter guaranteed by design. (tosLH = |tpLHm - tpLHn|, tosHL = |tpHLm - tpHLn|)

Note: An is a host side signal. Bn is a card side signal.
VCCB is supplied from the built-in LDO.

Dynamic Switching Characteristics (Ta = 25°C, Input: tr = tf = 2.0 ns, CL = 15 pF)

Characteristics	Symbol	Test Condition	VCC (V)		Typ.	Unit
			VCCA	VCCB		
Quiet output maximum dynamic VOL	A → B	VIH = VCC, VIL = 0 V (Note 2)	1.8	2.9	0.35	V
	B → A		1.8	2.9	0.25	
Quiet output minimum dynamic VOL	A → B	VIH = VCC, VIL = 0 V (Note 2)	1.8	2.9	-0.35	V
	B → A		1.8	2.9	-0.25	
Quiet output maximum dynamic VOH	A → B	VIH = VCC, VIL = 0 V (Note 2)	1.8	2.9	3.25	V
	B → A		1.8	2.9	2.05	
Quiet output minimum dynamic VOH	A → B	VIH = VCC, VIL = 0 V (Note 2)	1.8	2.9	2.55	V
	B → A		1.8	2.9	1.55	

Note 2: Parameter guaranteed by design.

Note: An is a host side signal. Bn is a card side signal.

Capacitive Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Circuit	VCC (V)		Typ.	Unit
			VCCA	VCCB		
Power dissipation capacitance (Note 3)	CPDA	A → B (DIR = "H")	1.8	2.9	24	pF
		B → A (DIR = "L")	1.8	2.9	22	
	CPDB	A → B (DIR = "H")	1.8	2.9	76	
		B → A (DIR = "L")	1.8	2.9	28	

Note 3: CPD is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

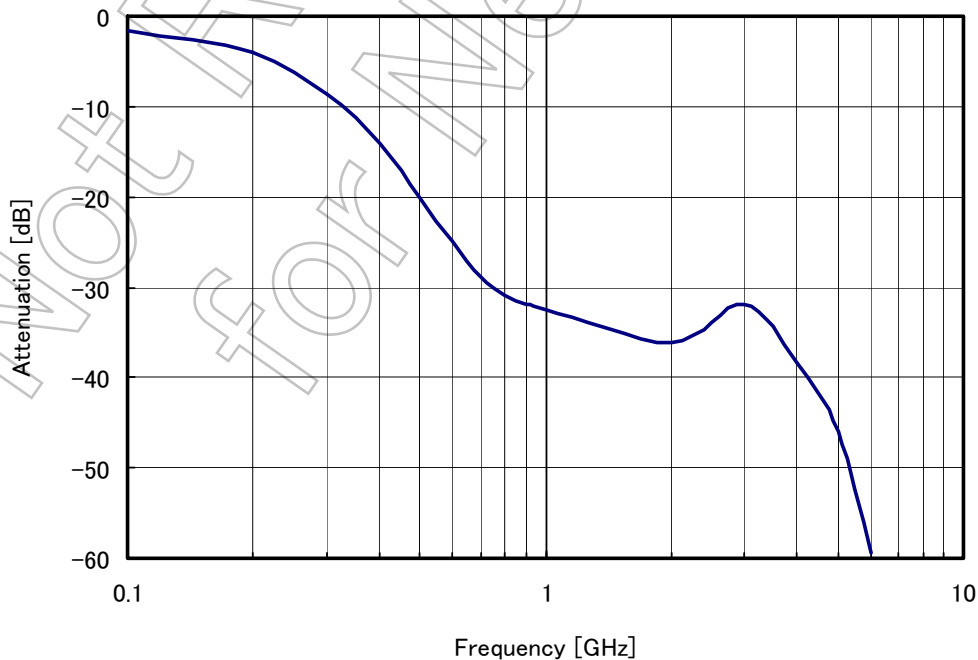
$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/6 \text{ (per bit)}$$

Regulator Section

Electrical Characteristics (unless otherwise specified, $V_{IN} = V_{OUT} + 1\text{ V}$, $I_{OUT} = 1\text{ mA}$, $C_{IN} = 0.1\text{ }\mu\text{F}$, $C_{OUT} = 2.2\text{ }\mu\text{F}$, $T_j = 25^\circ\text{C}$)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Input voltage	V_{IN}	—	3.2	—	5.0	V
Output voltage	$V_{CCB\ O/P}$	—	2.8	2.9	3.0	V
Line regulation	Reg·line	$V_{OUT} + 0.5\text{ V} \leq V_{IN} \leq 5.0\text{ V}$, $I_{OUT} = 1\text{ mA}$	—	3	15	mV
Load regulation	Reg·load	$1\text{ mA} \leq I_{OUT} \leq 200\text{ mA}$	—	—	150	mV
Quiescent current	I_{B1}	$I_{OUT} = 0\text{ mA}$	—	40	80	μA
	I_{B2}	$I_{OUT} = 100\text{ mA}$	—	45	85	
Stand-by current	$I_{B(OFF)}$	$V_{CT} = 0\text{ V}$	—	0.1	1.0	μA
Output noise voltage	V_{NO}	$V_{IN} = V_{OUT} + 1\text{ V}$, $I_{OUT} = 10\text{ mA}$, $10\text{ Hz} \leq f \leq 100\text{ kHz}$, $T_a = 25^\circ\text{C}$	—	140	—	μV_{rms}
Temperature coefficient	T_{CVO}	$-40^\circ\text{C} \leq T_{opr} \leq 85^\circ\text{C}$	—	100	—	ppm/ $^\circ\text{C}$
Ripple rejection	R.R.	$V_{IN} = V_{OUT} + 1\text{ V}$, $I_{OUT} = 10\text{ mA}$, $f = 1\text{ kHz}$, $V_{Ripple} = 500\text{ mV}_{p-p}$, $T_a = 25^\circ\text{C}$	—	40	—	dB
Control voltage (ON)	$V_{CT(ON)}$	—	1.5	—	V_{IN}	V
Control voltage (OFF)	$V_{CT(OFF)}$	—	0	—	0.25	V
Control current (ON)	$I_{CT(ON)}$	$V_{CT} = 1.5\text{ V}$	—	—	0.1	μA
Control current (OFF)	$I_{CT(OFF)}$	$V_{CT} = 0\text{ V}$	—	—	0.1	μA
Peak output current	$I_{outpeak}$	—	200	—	—	mA

EMI Filter Response (Typical Performance)



AC Test Circuit

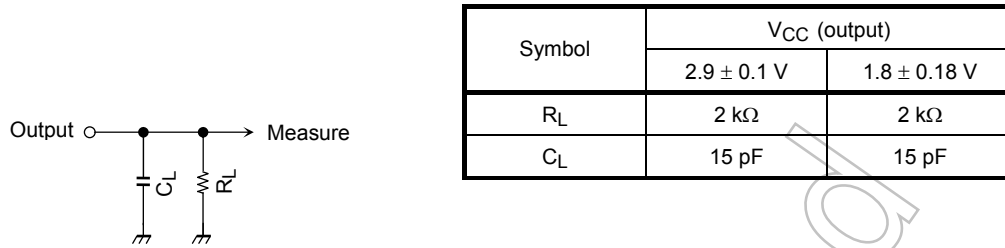


Figure 1

AC Waveform

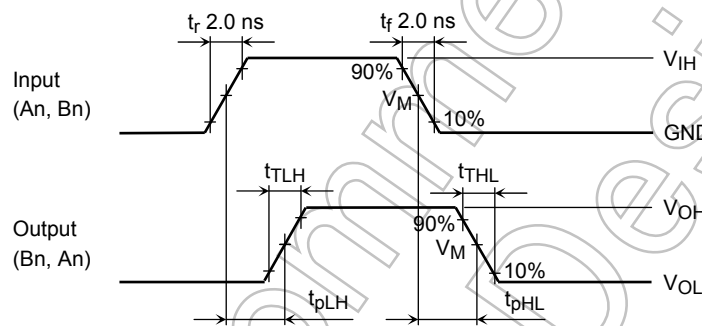


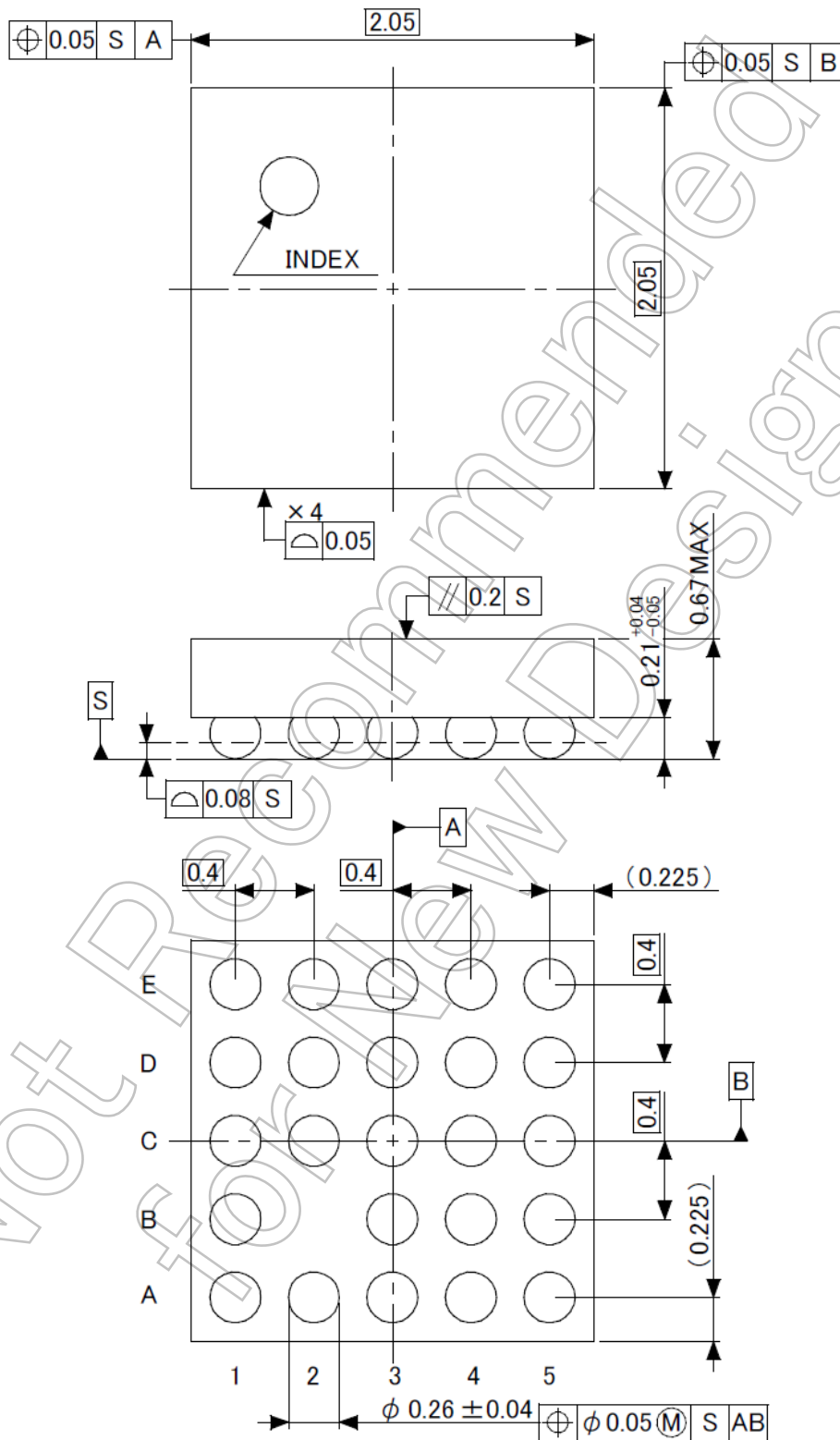
Figure 2 t_{pLH}, t_{pHL}, t_{tLH}, t_{tHL}

Symbol	V _{CC}	
	2.9 ± 0.1 V	1.8 ± 0.18 V
V _{IH}	V _{CC}	V _{CC}
V _M	V _{CC} /2	V _{CC} /2

Package Dimensions

S-WFBGA24-0303-0.40A02

Unit: mm



Weight: 0.006 g (typ.)

The resin used in this product includes no flame retardants.

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