1.6 kW Server Power Supply (Upgraded)

Design Guide

RD240-DGUIDE-01

Toshiba Electronic Devices & Storage Corporation

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1. Introduction

This Design Guide describes how to design power 1.6 kW Server Power Supply (Upgraded) (hereafter referred to as this power supply). Refer to the reference guide for the specifications, operation check procedure, characteristics, etc. of this power supply.

This power supply takes input of AC 90 to 264 V and output DC 12 V (Max. 1.6 kW) by using a semi-bridgeless PFC circuit and a phase-shift full-bridge (Phase Shift Full Bridge: PSFB) circuit. ORing output-circuit enables redundant operation. It also has a built-in auxiliary power supply circuit that is required to supply power for the operation of this circuit. Components for mounting on the board are selected considering the height, and they can be applied to 1U server power supply applications.

The power MOSFET TK125N60Z1 (under development) and SiC schottky barrier diode (SBD) TRS6E65H are used for semi-bridgeless PFC in this power supply. PSFB circuit uses the high-speed diode-type power MOSFET TK095N65Z5 in the primary-side full-bridge section, the power MOSFET TPH2R408QM in the secondary-side synchronous rectifier section, and the digital isolator DCL540C01 for isolated gate-signal transmission from the secondary-side controller. In addition, the power MOSFET TPHR6503PL1 is used in the ORing output-circuit. By using these latest Toshiba devices, this upgraded power supply has better efficiency and compact size compared to the existing reference design (1.6kW, 80Plus Platinum Class, High efficiency Server AC-DC Power supply), even though both of them uses the same circuit topology.

1.1. Outline of This Power Supply

Fig. 1.1 shows a block diagram of this power supply. The circuit consists of AC Input, Semi-bridgeless PFC, and Phase Shift Full-Bridge (PSFB) converter circuit. To use Toshiba's latest power MOSFET, SiC SBD and digital isolater on each portion of this power supply improves the efficiency.

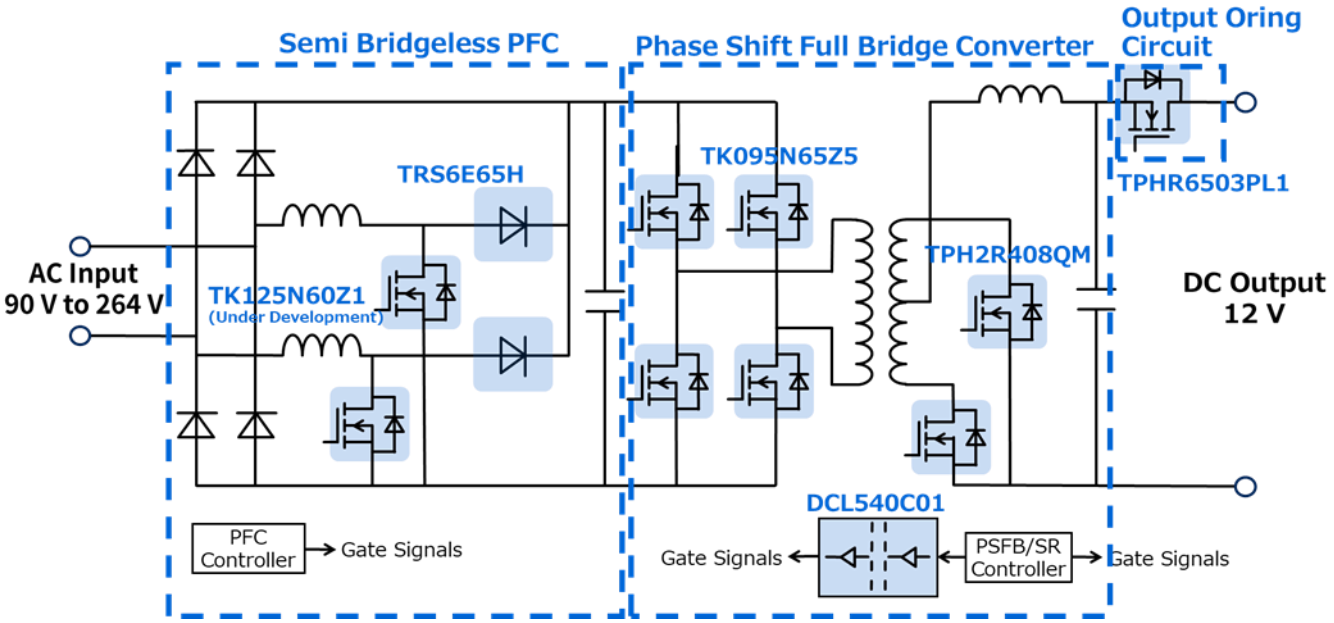


Fig. 1.1 Block Diagram

2. Main Components

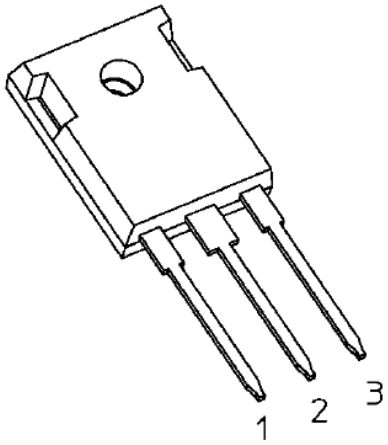
2.1. Power MOSFET TK125N60Z1 (Under Development)

The power MOSFET TK125N60Z1 is used as a switching device for the semi-bridgeless PFC circuit. The main features of TK125N60Z1 are as follows.

Features

- Low drain-source on-resistance: $R_{DS(ON)}$ = 0.105 Ω (Typ.)
- High speed switching properties with lower capacitance.
- Enhancement mode: V_{th} = 3 to 4 V (V_{DS} = 10 V, I_D = 0.73 mA)

External Appearance and Internal Circuit Configuration Diagram



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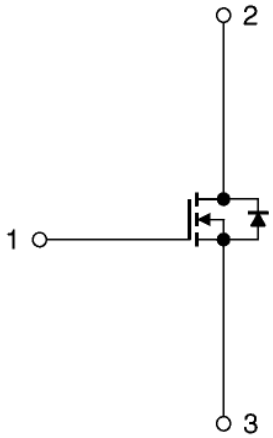


1: Gate
2: Drain (heatsink)
3: Source

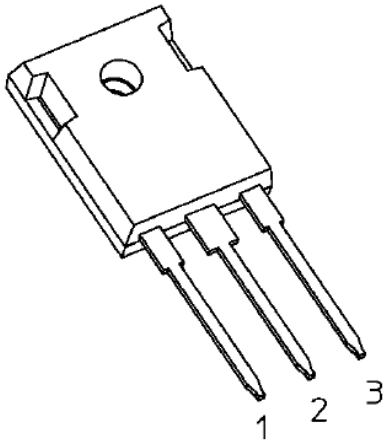
2.2. Power MOSFET TK095N65Z5

The power MOSFET TK095N65Z5 is used on the primary-side of the PSFB circuit. The main features of TK095N65Z5 are as follows.

Features

- Fast reverse recovery time: t_{rr} = 115 ns (Typ.)
- Low drain-source on-resistance: $R_{DS(ON)}$ = 0.079 Ω (Typ.)
- High speed switching properties with lower capacitance.
- Enhancement mode: V_{th} = 3.5 to 4.5 V (V_{DS} = 10 V, I_D = 1.27 mA)

External Appearance and Internal Circuit Configuration Diagram



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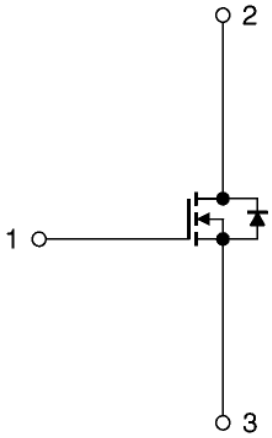


1: Gate
2: Drain (heatsink)
3: Source

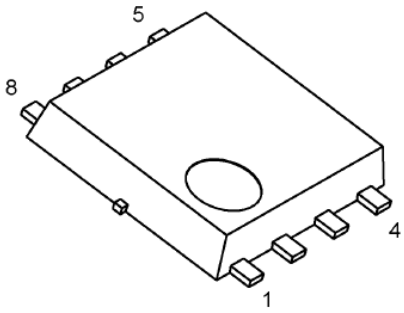
2.3. PowerMOSFET TPH2R408QM

The power MOSFET TPH2R408QM is used in the secondary-side synchronous rectifier section of the PSFB circuit. The main features of TPH2R408QM are as follows.

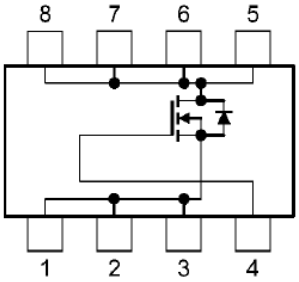
Features

- High speed switching
- Small gate gate charge: Q_{SW} = 28 nC (Typ.)
- Small output charge: Q_{oss} = 90 nC (Typ.)
- Low drain-source on resistance: $R_{DS(ON)}$ = 1.9 mΩ (Typ.) (V_{GS} = 10 V)
- Low leakage current: I_{DSS} = 10 μA (Max.) (V_{DS} = 80 V)
- Enhancement mode: Vth = 2.5 to 3.5 V (V_{DS} = 10 V, ID = 1.0 mA)

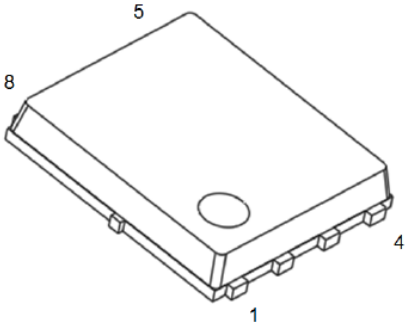
External Appearance and Internal Circuit Configuration Diagram



SOP Advance



1, 2, 3: Source
4: Gate
5, 6, 7, 8: Drain



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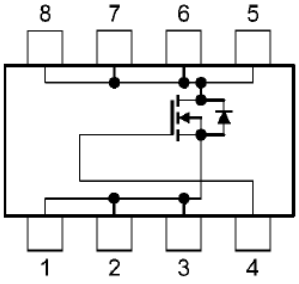


1, 2, 3: Source
4: Gate
5, 6, 7, 8: Drain

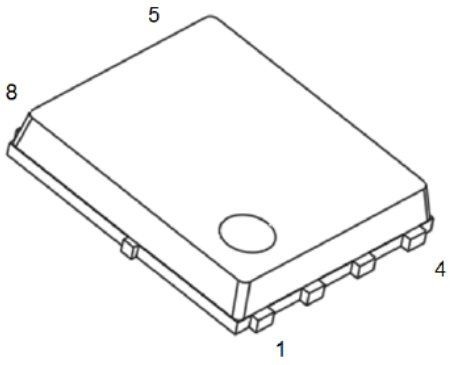
2.4. Power MOSFET TPHR6503PL1

The power MOSFET TPHR6503PL1 is used in the output Oring circuit. The main features of TPHR6503PL1 are as follows.

Features

- High speed switching
- Small gate charge: Q_{SW} = 30 nC (Typ.)
- Small output charge: Q_{oss} = 81.3 nC (Typ.)
- Low drain-source on resistance: $R_{DS(ON)}$ = 0.41 mΩ (Typ.) (V_{GS} = 10 V)
- Low leakage current: I_{DSS} = 10 μA (Max.) (V_{DS} = 30 V)
- Enhancement mode: V_{th} = 1.1 to 2.1 V (V_{DS} = 10 V, I_D = 1.0 mA)

External Appearance and Internal Circuit Configuration Diagram



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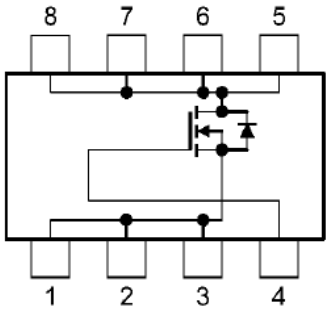


1, 2, 3: Source
4: Gate
5, 6, 7, 8: Drain

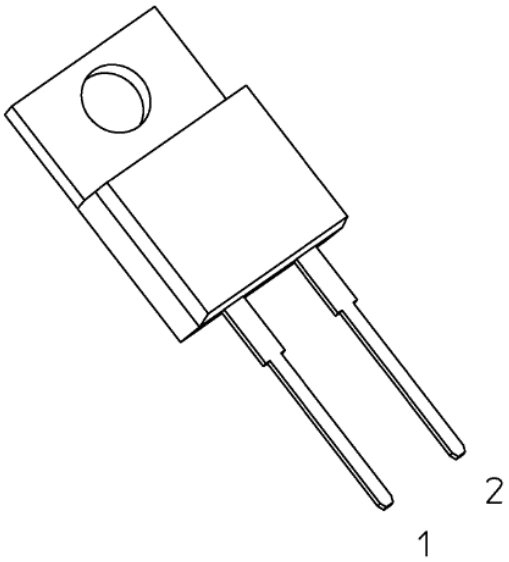
2.5. SiC Schottky Barrier Diode TRS6E65H

The SiC Schottky barrier diode TRS6E65H is used in the boosting section of semi-bridgeless PFC circuit. The main features of TRS6E65H are as follows.

Features

- Chip design of 3rd generation
- Low forward voltage: V_F = 1.2 V (Typ.)
- Low total capacitance charge: Q_c = 17 nC (Typ.)
- Low reverse current: I_R = 1.1 μA (Typ.)

External Appearance and Internal Circuit Configuration Diagram



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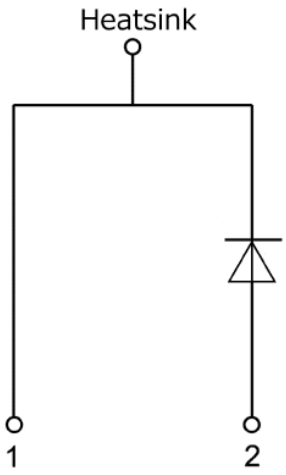


1: Cathode
2: Anode

2.6. Digital Isolator DCL540C01

The 4-channel digital isolator DCL540C01 is used for transferring signal between the primary and secondary-sides of the PSFB circuit. The main features of DCL540C01 are as follows.

Features

- Data-rate: Up to 150 Mbps
- Supply voltage: 2.25 V to 5.5 V
- Temperature range: –40 °C to 110 °C
- Propagation delay: 10.9 ns (Typ.)
- Default output: Low
- CMTI (Min.): ±100 kV/μs
- Withstand voltage: 5 kVrms
- Safety-related certification:

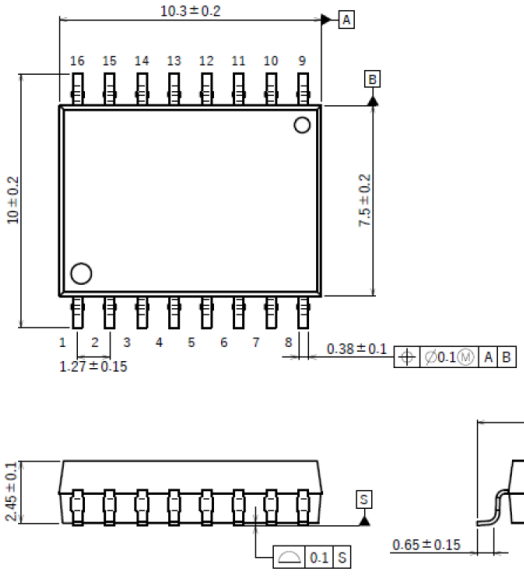
  UL : UL1577, File No. E519997

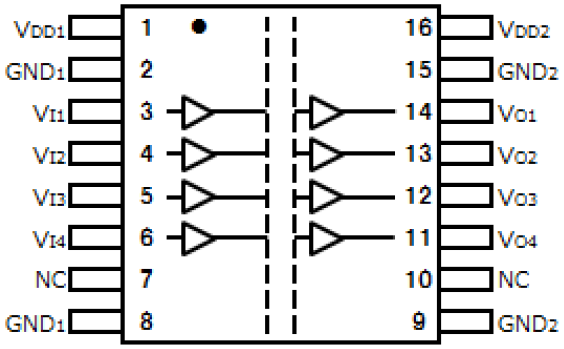
  cUL : CSA Component Acceptance Service Notice No. 5A, File No. E519997

  VDE : DIN VDE V 0884-11(VDE V 0884-11) Certificate No. 40055132

  CQC : GB 4943.1-2022 Certificate No. CQC22001345018

External Appearance and Internal Circuit Configuration Diagram





16 pin SOIC Wide body

3. Circuit Design

This section describes the points of the circuit design of this power supply.

3.1. AC Line Circuit

This section describes how to design AC line Circuit of this power supply. AC line circuit of this power supply is as follows.

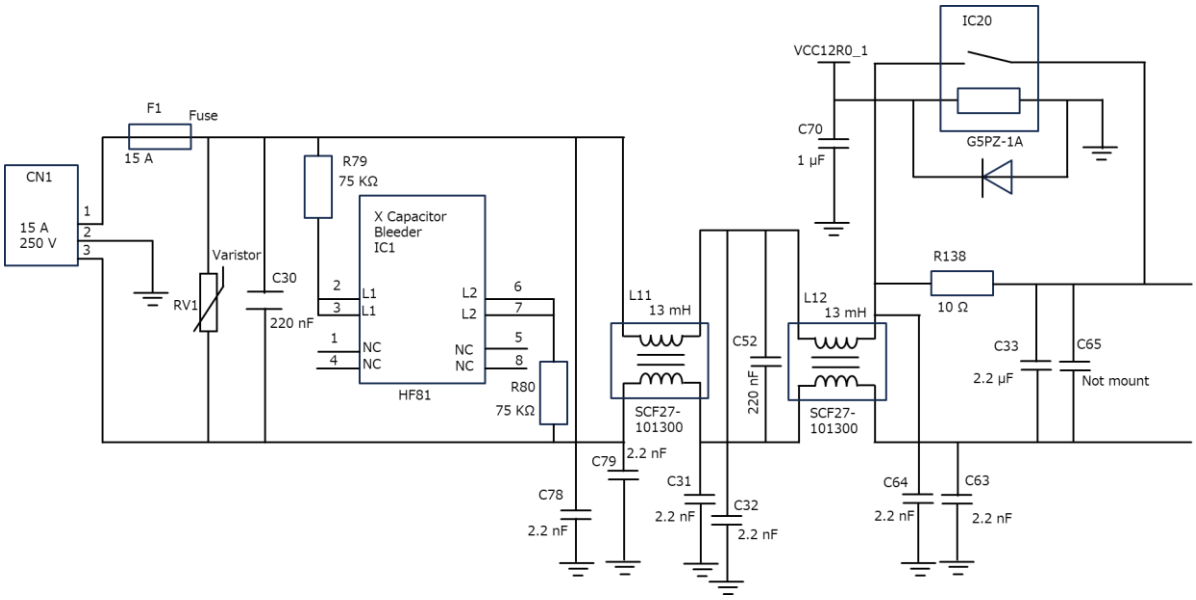


Fig. 3.1 AC Line Circuit

Fuse

A fuse (F1) is installed to shut off AC line when abnormally high current flows through the line. Select a fuse according to the maximum current value of AC line. The rms value of the max. AC line input current is calculated by the following equation.

max. AC line input current

= max. power ÷ efficiency ÷ power factor ÷ effective input Voltage (Min.)

This power supply is designed to have 1.6 kW output when the input is AC 200 V, and 0.8 kW output when the input is AC 100 V. If the power-supply efficiency of PFC does not change according to the input voltage, the maximum AC line input current will be the same regardless of the input voltage. However, the power supply efficiency of PFC is generally low when the input voltage is low. Therefore, when calculating the max. AC line current, consider the minimum input voltage of 90 V for 100 V system.

Assuming that, the input-voltage (Min. rms value) = 90 V, maximum power = 0.8 kW, power efficiency = 90 %, and power factor = 0.99, AC line-maximum current value of this power supply is approximately 10 A. Thus, a 15 A fuse is used in this power supply after taking margins into account. When selecting a fuse, in addition to the above max. current, it is also necessary to consider the inrush current when AC power supply is turned on, and whether the product meets the applicable safety standards.

Varistor

A ceramic varistor (RV1) is installed to protect the system when surge voltage is applied to the AC line due to induced lightning. The varistor is selected based on AC line-voltage used. For this power supply, the maximum voltage of AC line is 264 V in rms value and 373 V in instantaneous value. Therefore, considering the margins for these voltages, the maximum allowable circuit voltage is 350 V (AC) and the varistor of voltage 560 V is used. When selecting a varistor, surge current tolerance, energy tolerance, etc. must be considered in addition to the above voltage ratings. In addition, since the varistor failure mode is often a short mode, it is recommended to install a fuse to the first stage (AC input side) when mounting the varistor.

X Capacitor Discharging IC

When AC input is disconnected, the charges stored in the X capacitors Note 3-1 (C30, C33, C52) must be discharged quickly to avoid the risk of electric shock. In this power supply, a HF81 (IC1) is mounted as an IC for discharging the X capacitors. This IC cuts off the discharging path when AC power is supplied, thus realizing power saving. When AC power supply is lost, IC and the external resistors (R79, R80) of IC make it possible to discharge the X capacitor so that the voltage of the X capacitor is less than 37 % of the default voltage in one second. Since this power supply is equipped with an X capacitor of approximately 3 μF, it is equipped with an external resistor (75 kΩ × 2 pieces) required to discharge 3 μF. Note that the external resistor connected to this IC may need to be changed when changing the X capacitor for noise-suppression. IC can also be changed to a resistor for discharging to reduce costs. However, when AC is connected, the power dissipation due to the constantly discharging resistor will occur. Therefore, it is necessary to check whether the system's power saving requirements are satisfied.

EMI Suppression Components

As a countermeasure against common mode noise, Y capacitors Note 3-1 (C31, C32, C78, C79, C63, C64) and common mode chokes (L11, L12) are mounted. And X capacitors (C30, C33, C52) are mounted as a countermeasure against differential noise. The noise level is affected by the BOARD layout and chassis design. Change, delete, or add the above components as necessary. Incidentally, increasing the capacitance of the Y capacitor will increase the leakage current, so it is necessary to check whether the system satisfies the required safety standards.

Note 3-1: Y capacitor, X capacitor

The X capacitor reduces noise by short-circuiting the line at high frequency with the capacitor connected between the lines of the power supply line. The Y capacitor is connected between the power line and the reference ground. Prevents noise from flowing toward the power line.

Inrush Current Suppression Components

A built-in resistor (R138) and a relay (IC20) are installed to suppress inrush current when AC power is turned on. If this power supply is started in the correct manner, the relay-circuit is off when AC power supply is turned on, and the current flows through the built-in fuse resistor (10 Ω). Therefore, the inrush current can be suppressed. After AC power is turned on, the relay-circuit detects the primary 12 V power supplied from the outside and turns on. When the relay circuit is turned on, the current flows through the relay with lower resistance, thus reducing power loss during operation. The conditions and timing for turning the relay on and off must be checked to ensure that the required specifications of the system are met.

3.2. PFC Circuit

3.2.1 Semi-Bridgeless PFC Circuit

Before explaining this power supply circuit, outline of the operation of the semi-bridgeless PFC circuit is explained. In a typical power supply circuit, the AC input is rectified and then passed through a smoothing capacitor to generate DC output. The AC input current flows only when the voltage is higher than the smoothing capacitor voltage and does not become sinusoidal. PFC circuit brings the input current closer to the sine wave, and therefore eliminates the phase difference between the input voltage and current generated by the power supply circuit, and thus brings the power factor closer to unity. The bridgeless PFC circuit integrates the functions of the bridge diode section and PFC in order to reduce loss in the bridge diode section which performs full wave rectification of AC input.

Fig. 3.2 shows the basic configuration of the bridgeless PFC and the current path for each half-cycle of the AC input. When L_a side of the AC input is positive half-cycle, Q_a switches and D_a performs PFC operation as its output diode. At this time, Q_b operates in the synchronous rectification mode for the half-cycle of this commercial power supply and performs rectification of the AC input. On the other hand, during the negative half-cycle, Q_b and D_c perform switching operations, and Q_a performs rectification operation.

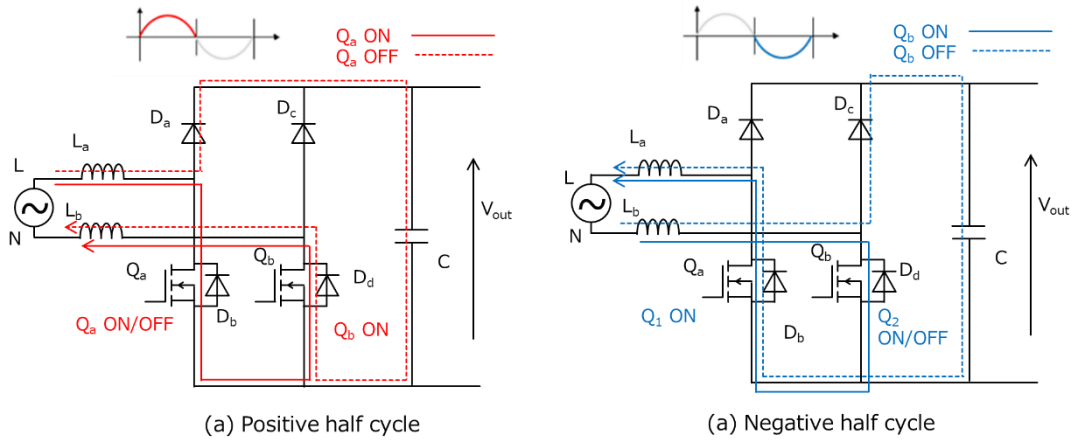


Fig. 3.2 Bridgeless PFC Circuit Operation

Fig. 3.3 shows the operation of the semi-bridgeless PFC circuit adopted by this power supply. This is a bridgeless PFC with a diode-added on the AC power supply side. The two diodes (D_{aa} and D_{bb}) connect PFC output ground through D_{aa} and D_{bb} to the input line, and the input line voltage is not floating but is the normal ground reference. Therefore, the input-voltage of PFC circuit is a rectified sine wave referenced to ground. Consequently, the above-mentioned bridgeless PFC circuit can suppress problematic noises.

D_{cc} and D_{dd} are inrush diodes for peak-charging the capacitor C during the initial startup. It does not contribute to the operation after the capacitor is peak charged and the converter begins to operate. As shown in Fig. 3.3, the current passes through D_{aa} and D_{bb} back to the input.

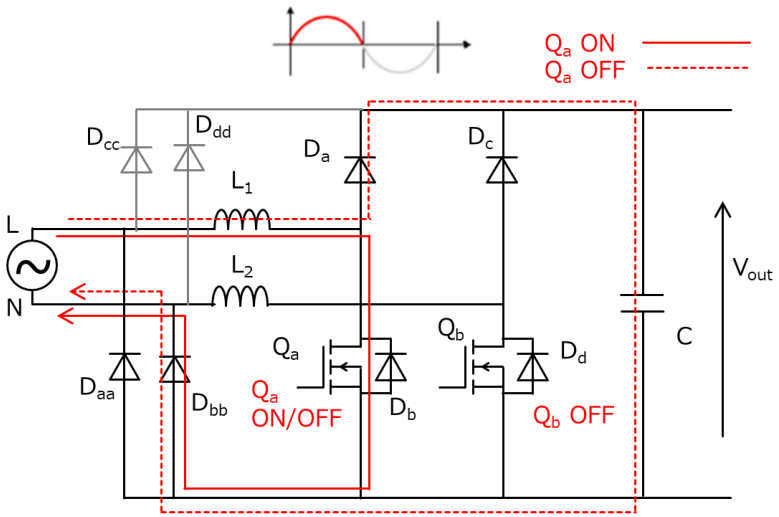


Fig. 3.3 Operation of Semi-Bridgeless PFC

3.2.2 PFC Circuit of This Power Supply

This power supply employs a semi-bridgeless PFC circuit using a controller UCC28070A (IC3 manufactured by Texas Instruments, hereinafter referred to as PFC controller). The basic design of different parts of the semi-bridgeless PFC of this power supply are described below. For detailed designs of the controller peripherals, refer to UCC28070A datasheet and related documents.

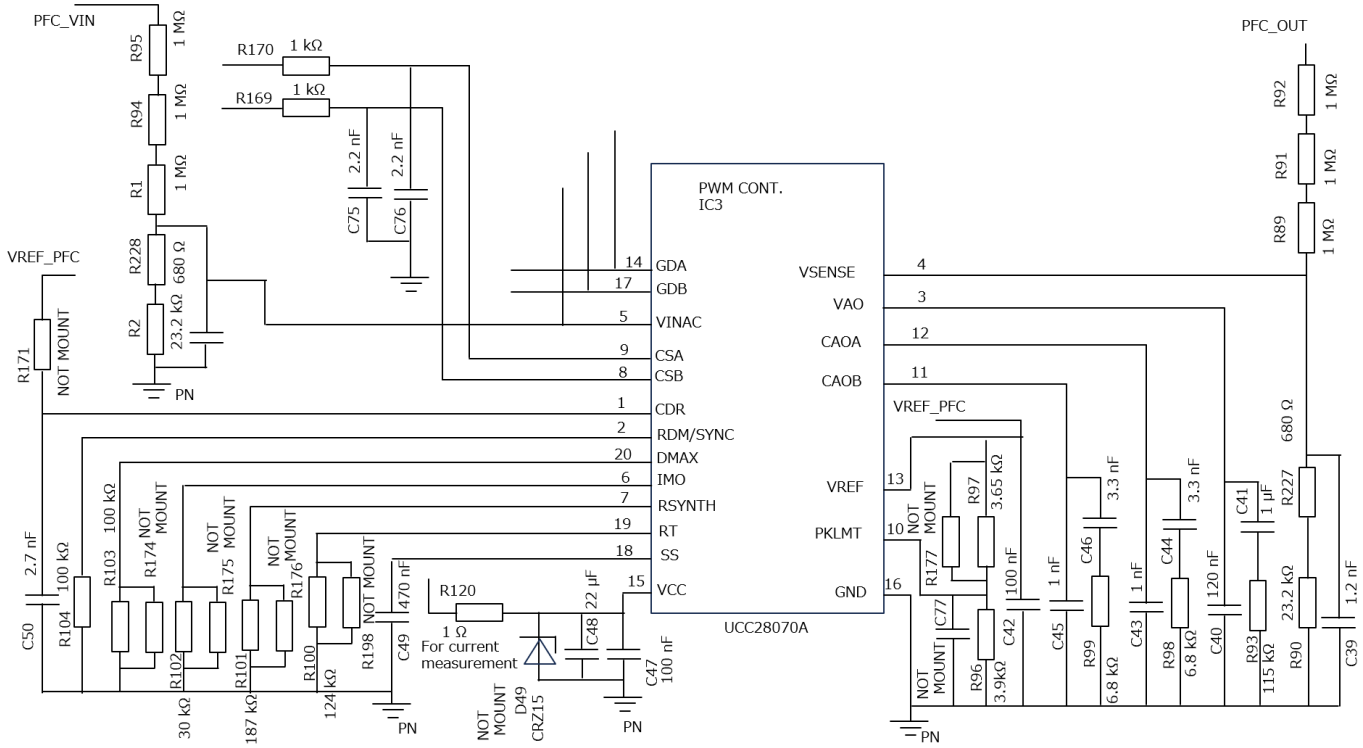


Fig. 3.4 PFC Circuit 1 (Around PFC Controller)

Output Voltage

The output voltage PFC_OUT of PFC circuit can be set by the external resistors (R89, R90, R91, R92, R227). The output voltage is controlled by comparing the sense pin voltage VSENSE (obtained from the resistors above) with the internal reference voltage (3.0 V) of PFC controller. The output voltage setting value is calculated by the following formula.

$$PFC\_OUT(V) = \frac{3.0 \times (R89+R91+R92+R90+R227)}{(R90+R227)}$$

When changing PFC output voltage, R1, R2, R94, R95, R228 resistors for measuring AC line voltage must also be changed accordingly. PFC circuit is initially set as R90 = R2 = 23.2 kΩ, R227 = R228 = 680 Ω, and R1 = R89 = R91 = R92 = R94 = R95 =1 MΩ, which is approximately 380 V. Change the above resistance value as necessary to set the desired output voltage value.

Switching Frequency

The switching-frequency f_{PWM} of PFC circuit can be set using an external resistor R100 connected to RT terminal of PFC controller. The switching frequency is calculated by the following formula.

$$f_{PWM}(kHz) = \frac{7500}{R100(k\Omega)}$$

The default switching frequency is set with R100=124 kΩ, which is approximately 60 kHz. Change the resistor value of R100 as needed to set the desired frequency.

Soft Start

The soft-start duration of PFC circuit can be set by an external capacitor C49 connected to SS pin of PFC controller. The setting value is calculated by the following equation.

$$T_{SS}(s) = C49 \times \frac{2.25(V)}{10(\mu A)}$$

The default soft start time is set with C49 = 470 nF, which is approximately 106 ms. Change the capacitance of C49 as needed to set the desired soft-start duration. It must be verified that the current limiter does not operate during the soft-start period and that the output voltage recovers to the normal range at the restart after the hold-up period.

Current Limiter

The current limiter of the PFC in Fig. 3.5 can be set by the current transformers (T2, T3), the current sense resistors (R7, R8), and the threshold setting resistors (R96, R97) connected to V_{REF} of PFC controller. The sensed value is input to PFC controller's CSA, CSB, and when the current reaches the threshold, PFC controller disables the gate drive signals (GDA, GDB) input to INA, INB of the gate driver UCC27524AD. The current limit level is calculated by the following equation.

$$I\_limit = \left(\frac{POUT \times \sqrt{2}}{efficiency, \eta(\%) \times VinAC} + \Delta I \right) \times Margin$$

The default current limit level is 19.6 A for V_{inAC} = 90 V when P_{OUT} = 800 W, efficiency η = 90 % and ΔI = 4.7 A, Margin = 1.2. Change the above values as necessary to set the desired current value.

Gate Drive Circuit

Design of gate-drive circuit affects power supply efficiency and EMI noises. Generally, there is a trade-off between power supply efficiency and EMI noise. Therefore, a balanced design should be used. For reducing EMI, it is recommended that you change the Gate-Series resistors (R72, R74, R108, R109) to a larger number to check for noise. The gate-drive circuit of this power supply has a circuit configuration that allows the turn-on speed and turn-off speed of FET to be individually adjusted. If the preliminary check shows that the noise source is occurring during the FET turn-on period or turn-off period, then all resistors need not be changed. Changing R72,R74 if the noise at turn-on is a problem and R108,R109 if the noise at turn-off is a problem may reduce EMI noise. If the gate-series resistor is changed to a larger value, the switching speed of FET will be reduced, which may result in a power supply inefficiency. When changing the gate series resistance, it is necessary to confirm that the power supply efficiency performance and heat dissipation performance required for the system are satisfactory. Also, if EMI noise can be suppressed by only adjusting either of turn-on or turn-off, there is a possibility that the adverse effect on the power supply efficiency of the system can be reduced compared to adjusting both.

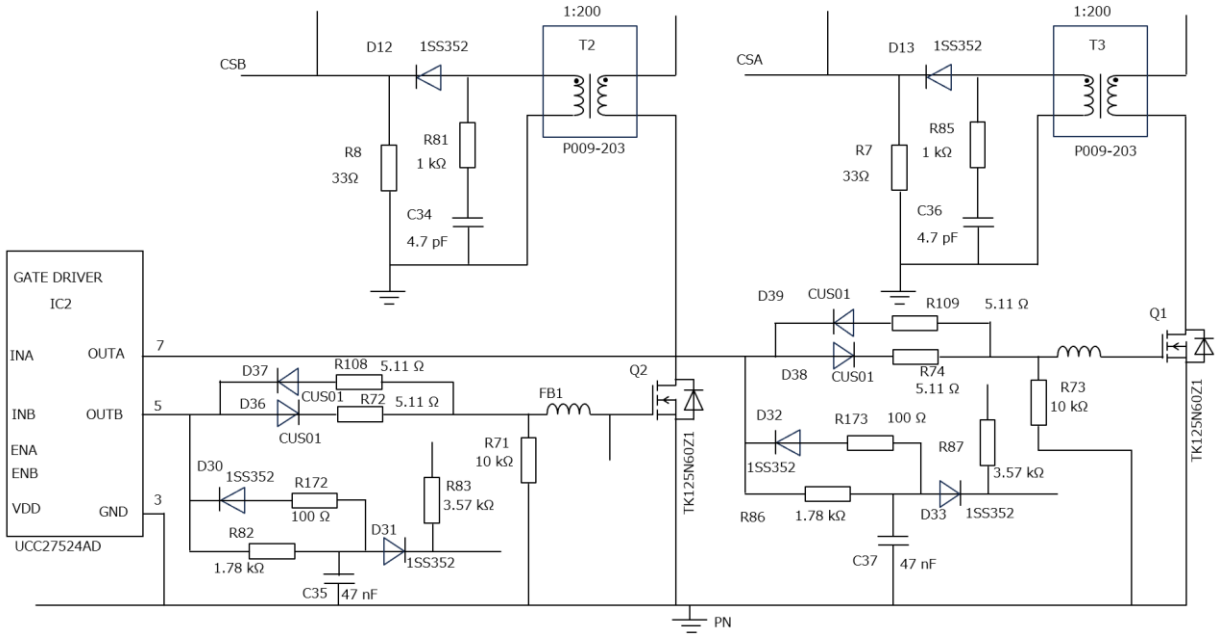


Fig. 3.5 PFC Circuit 2 (Around Power MOSFET)

Bridge diode

The rectifier diode uses a bridge diode (D3). Since this power supply has a semi-bridgeless PFC circuit, the diode between pin1 and pin2, and the diode between pin3 and pin2 of this bridge diode (D3) contribute only to the rectification operation during the start-up of this power supply and does not contribute to subsequent operations. This bridge diode (D3) can also be changed to a half-bridge diode and a surface-mount diode. When using a surface mount diode, it is necessary to select a product with a rating that can support inrush current.

Output capacitor

The capacitance of the output capacitors (C_1, C_7) is calculated based on the hold-up time requirement. The hold-up time Thold is calculated by the equation below, when the capacitance of the output capacitors is C_{out} (C_1+C_7), the output voltage is V_{out}_PFC, the lower limit of the output voltage is V_{min}.

$$Thold = Cout \times \frac{(Vout\_PFC^2 - Vmin^2)}{2 \times Pout}$$

By default, C_{out} = 660 μF, V_{out_PFC} = 380 V, Vmin = 280 V, P_{out} = 1777 W and the hold-up time is 12.3 ms. Adjust the capacitance of the output capacitor to satisfy the holdup time required for the system. In addition, when the output ripple specification is required, the capacitance required to satisfy the output ripple specification must be calculated and compared with the capacitance that satisfies the hold-up time, and a larger capacitance value must be used. Tolerances and aging must also be considered when selecting capacitors.

Inductors

To select the inductors (L_1, L_2) shown in Fig. 3.6, the ripple current of the inductor ΔI is set to 30% of the peak input current value (AC_{in_peak}) of AC line. When the input voltage is V_{inAC}, the PFC output voltage is Vout_PFC, the switching frequency is F, and the efficiency of PFC is η, the following formula is completed.

$$ACin\_peak = \frac{Pout \times \sqrt{2}}{VinAC \times \eta}$$

$$\Delta I = ACin\_peak \times 30\%$$

The value of the inductance L is expressed by the maximum voltage applied when the PFC switching element (MOSFET) is turned on, the on-time (T×D) and current change ΔI. (T: Switching period, D: On Duty)

$$L = V \times \frac{dt}{di} = \sqrt{2} \times VinAC \times \frac{T \times D}{\Delta I}$$

Here, T is expressed as MOSFET switching frequency F as follows.

$$T = \frac{1}{F}$$

In addition, the duty of PFC circuit is expressed by the following equation.

$$D = \frac{Vout\_PFC - VinAC}{Vout\_PFC}$$

Substituting the formulas of T and D into the formulas of the inductor L, the following formula can be obtained.

$$L = \sqrt{2} \times VinAC \times \frac{(Vout\_PFC - VinAC)}{Vout\_PFC \times \Delta I \times F}$$

In this power supply, if VinAC = 90 V, Vout_PFC = 380 V, F = 60 kHz, Pout = 888 W, η = 90 %, then L = 344 μH, so 350 μH is used. In addition, the peak current I_{L_peak} flowing through the inductor can be calculated as follows.

$$IL\_peak = ACin\_peak + \frac{\Delta I}{2}$$

Since AC_{in_peak} = 15.7 A, ΔI = 4.7 A, I_{L_peak} becomes 18.1 A. Therefore, an inductor that can allow a current of more than 18.1 A should be selected.

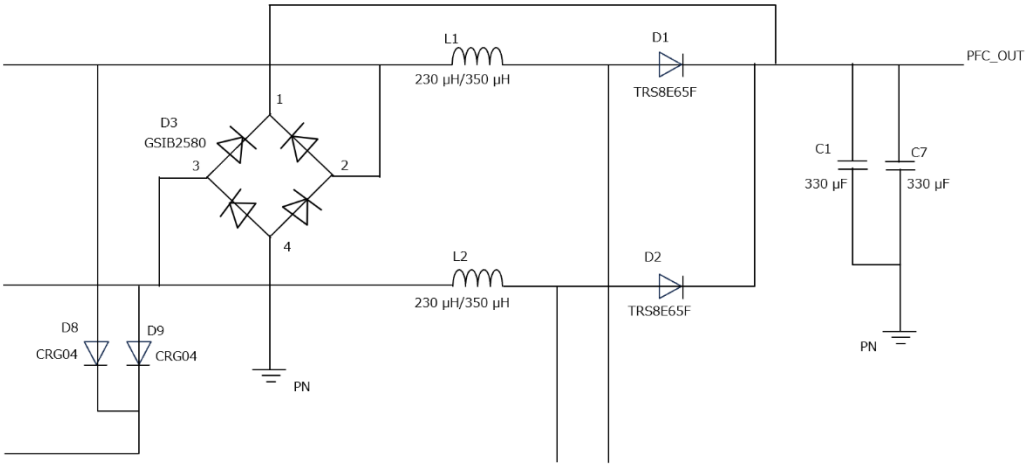


Fig. 3.6 PFC Circuit 3 (Around Bridge Diode, Inductor)

3.3. Phase-Shift Full-Bridge (PSFB) Circuit

3.3.1. PSFB Circuit

Fig. 3.7 shows the block diagram of PSFB circuit. The primary-side of the transformer T is formed by a full bridge circuit. Q_{AH} and Q_{BL} are switched with a duty ratio of 50 % and a phase difference of 180 degrees, respectively. Q_{CH} and Q_{DL} are similar. The basic operation is to swap the on/off states of Q_{AH} and Q_{BL} and then the on/off states of Q_{CH} and Q_{DL} with a certain phase delay. The amount of phase-shift determines the amount of energy transmitted to the secondary by the amount of overlap between Q_{AH} and Q_{DL}, Q_{BL} and Q_{CH} that are diagonally positioned. On the secondary-side, the voltage is output by the current doubler rectifier circuit. The output voltage is expressed by the following equation. Generally, Q_{AH} and Q_{BL} legs are called "forward legs" and Q_{CH} and Q_{DL} legs are called "late legs". PSFB circuit can handle greater power because switching losses can be significantly reduced by the switching elements operating at zero-voltage switching (ZVS).

$$V_{out} = \frac{n_2}{n_1} V_{in} \alpha$$

V_{out}: Output voltage [V]　　V_{in}: Input voltage [V]

n_1: Transformer primary turns　　n_2: Transformer secondary turns

α: Phase shift rate T1/ (T1+T2)　T_1: Q_{AH}, Q_{DL} simultaneous on-time

T_2: Q_{BL}, Q_{DL} simultaneous on-time

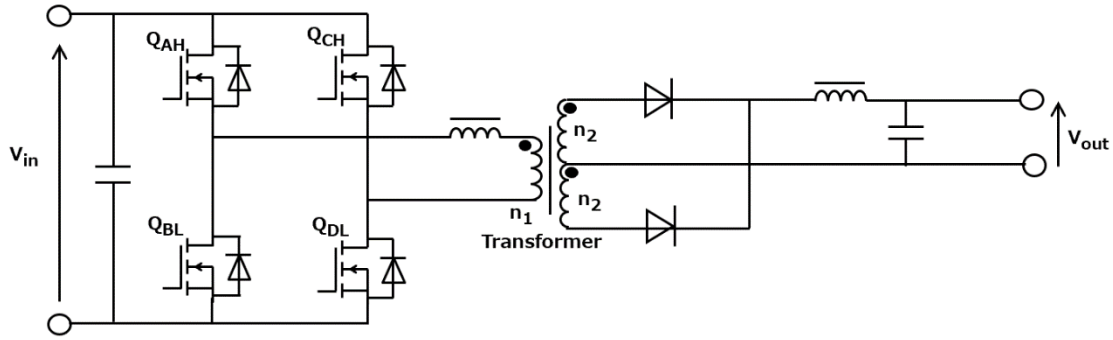


Fig. 3.7 PSFB Circuit

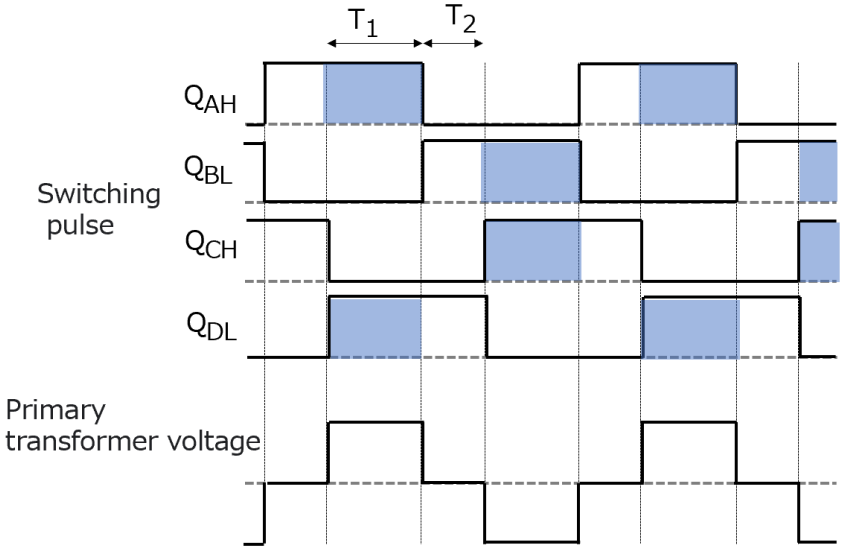


Fig. 3.8 PSFB Waveform

3.3.2. PSFB Circuit of This Power Supply

In this power supply, 12 V is generated after the semi-bridgeless PFC circuit. High efficiency is achieved by using a controller UCC28950 (IC10 manufactured by Texas Instruments that is capable of Zero Volt Switching (ZVS) operation over a wide range of loads, hereinafter referred to as PSFB controller). The basic designs of PSFB circuit of this power supply are described below. For detailed designs around the controller, refer to UCC28950 datasheet and related documents. Refer to the Reference Guide for the detailed specifications of this power supply.

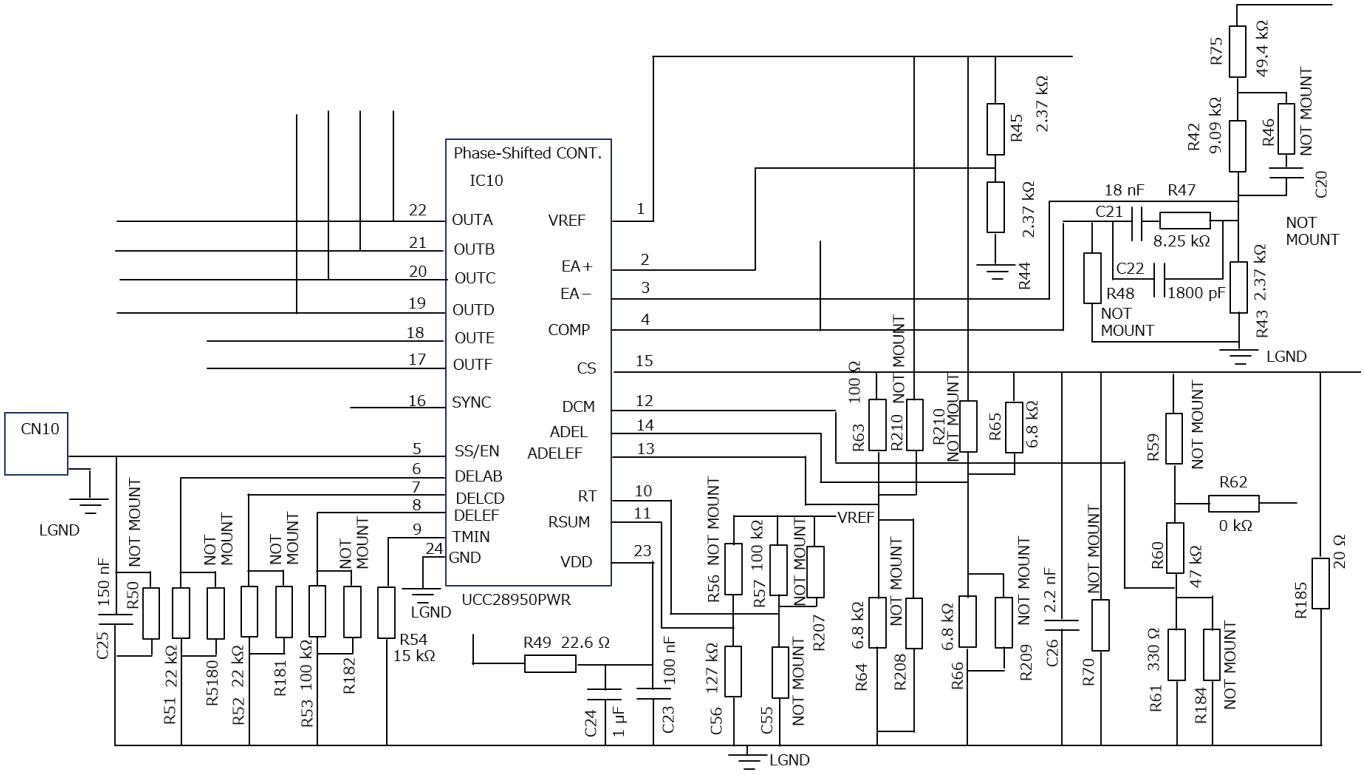


Fig. 3.9 PSFB Circuit 1 (Around PSFB controller)

Output Voltage

The output-voltage V_{OUT} of PSFB circuit can be set using the external resistors (R42, R43, R44, R45, R75) shown in Fig. 3.9. The setting is calculated by the following equation based on the above resistors and the internal voltage (VREF = 5.0 V) used to set the voltage of PSFB controller.

$$V_{OUT}(V) = \frac{VREF(V) \times R45 \times (R43 + R42 + R75)}{(R44 + R45) \times R43}$$

The default output-voltage setting for PSFB with R42 = 9.09 kΩ, R43 = R44 = R45 = 2.37 kΩ, R75 = 49.9 Ω is 12.14 V. Change the above resistance value as necessary to set the desired output voltage value.

Switching Frequency

The switching-frequency f_{PWM} of PSFB circuit can be set by the external resistor R57 between RT and VREF terminals of IC. The switching frequency is calculated by the following formula.

$$f_{PWM}(kHz) = \frac{2.5 \times 10^3}{\left(\frac{R57(k\Omega)}{VREF(V) - 2.5} + 1\right)}$$

In this equation, the unit of R57 is kΩ, VREF is V, and f_{PWM} is kHz. This equation is an empirical approximation, and the units are not matched. The default switching frequency with R57 = 100 kΩ is 60.98 kHz. Change the above resistance value as necessary to set the desired frequency.

Soft Start

The soft-start duration of PSFB circuit can be set by an external capacitor C25 connected between SS/EN pin and ground, and an internal charging current of 25 μA (Typ.). The setting value can be calculated by the following equation. 0.55 V is SS/EN pin voltage. VNI is EA + pin voltage.

$$T_{SS}(s) = \frac{C25 \times (VNI + 0.55)}{25\ \mu A} = \frac{C25 \times \left(\frac{VREF(V) \times R45}{R44 + R45} + 0.55\right)}{25\ \mu A}$$

R44 and R45 are 2.37 kΩ, V_{REF} is 5 V, and the default soft start time is 18.3 ms with C25 =150 nF. Change the capacitance of C25 as needed to set the desired soft-start duration. It is necessary to confirm that the current limiter does not operate during the soft-start period.

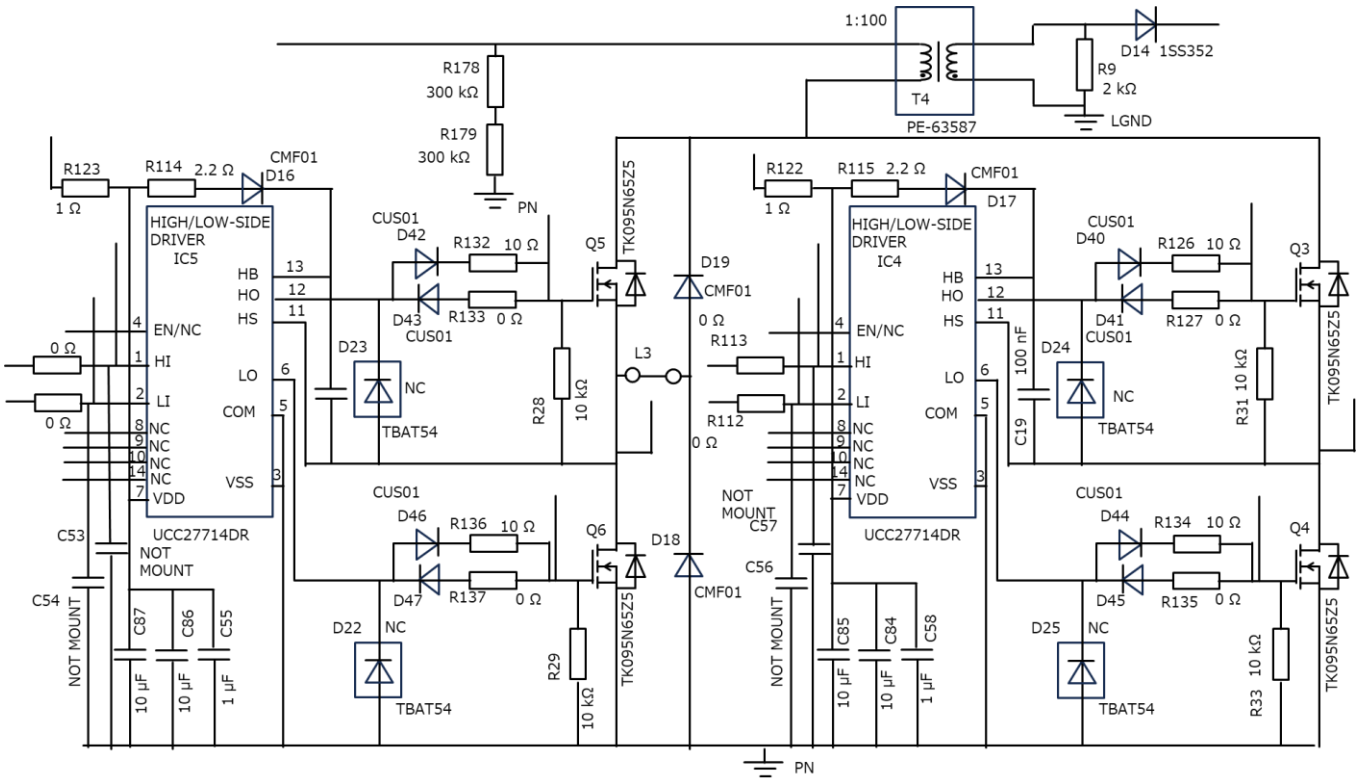


Fig. 3.10 PSFB Circuit 2 (Around Primary MOSFET)

Current Limiter

The current limiter of PSFB circuit can be set by the current transformer (T4) shown in Fig. 3.10, the current sense resistor (R185) connected between CS terminal of PSFB controller and GND in the Fig. 3.9, and the current limit threshold (2 V). When the current reaches the threshold, PSFB controller restricts MOSFET driving for MOSFET control on the primary-side to prevent abnormal current from flowing on the secondary-side. The current limit level is calculated by the following formula.

$$I\_limit = \frac{2.0}{R185 \times transfomer\ turns\ ratio}$$

The default setting of the current limiter with R185 = 20 Ω and the number of turns of 100:1, is 10 A. Change the above value as necessary to set the desired current value.

Gate Drive Circuit

Designing gate-drive circuit affects power supply efficiency and EMI noises. Generally, there is a trade-off between power supply efficiency and EMI noise. Therefore, a balanced design should be used. Although PSFB has implemented Zero Voltage Switching (ZVS), but if a hard switching region exists and is the cause of EMI noise, it is recommended to change the gate-series resistors (R126, R127, R132-R137) of the corresponding MOSFETs (Q3-Q6) to a large number. As with PFC gate-drive circuits, the circuit configuration allows independent adjustment during turn-on and turn-off. Therefore, if only one of these adjustments is used for adjustment, then it is possible to reduce the adverse effects on the power supply efficiency of the system.

Transformer

PSFB2 secondary circuit is shown in Fig. 3.11. The secondary-side synchronous circuit is a two-parallel circuit with transformer T5 and T6. Fig. 3.11 shows only T6 circuit.

When On Duty of the synchronous rectifier side of PSFB is set to 60 %, and the output-voltage is 12 V, a square wave of about 20 V is required on the secondary-side. Because PFC power supply is 380 V, the transformers (T5, T6) turn ratio should be 20:1:1 (center-tapped). This creates a 19 V square waveform on the secondary. In addition, it is necessary to fully consider the dielectric strength between primary and secondary, winding temperature increase, magnetic flux saturation, core loss, etc. Please refer to BOM for the specifications of the transformer used in this power supply.

In addition, this power supply uses the transformer leakage inductance to perform Zero Volt Switching (ZVS). If there is insufficient resonance due to leakage inductance, ZVS cannot be realized, and problems such as power supply efficiency degradation and increase in EMI noise may occur. When changing the transformer, it must be ensured that it is ZVS over a wide range of loading areas. If resonance is insufficient due to change of transformer and ZVS is not carried out, please mount a L3 additionally for resonance and adjust it to be ZVS over a wide range of loads. This power supply is initially designed for ZVS due to the transformer leakage inductance and for terminals for L3 on the PCB are shortened, because a resonant coil is not necessary.

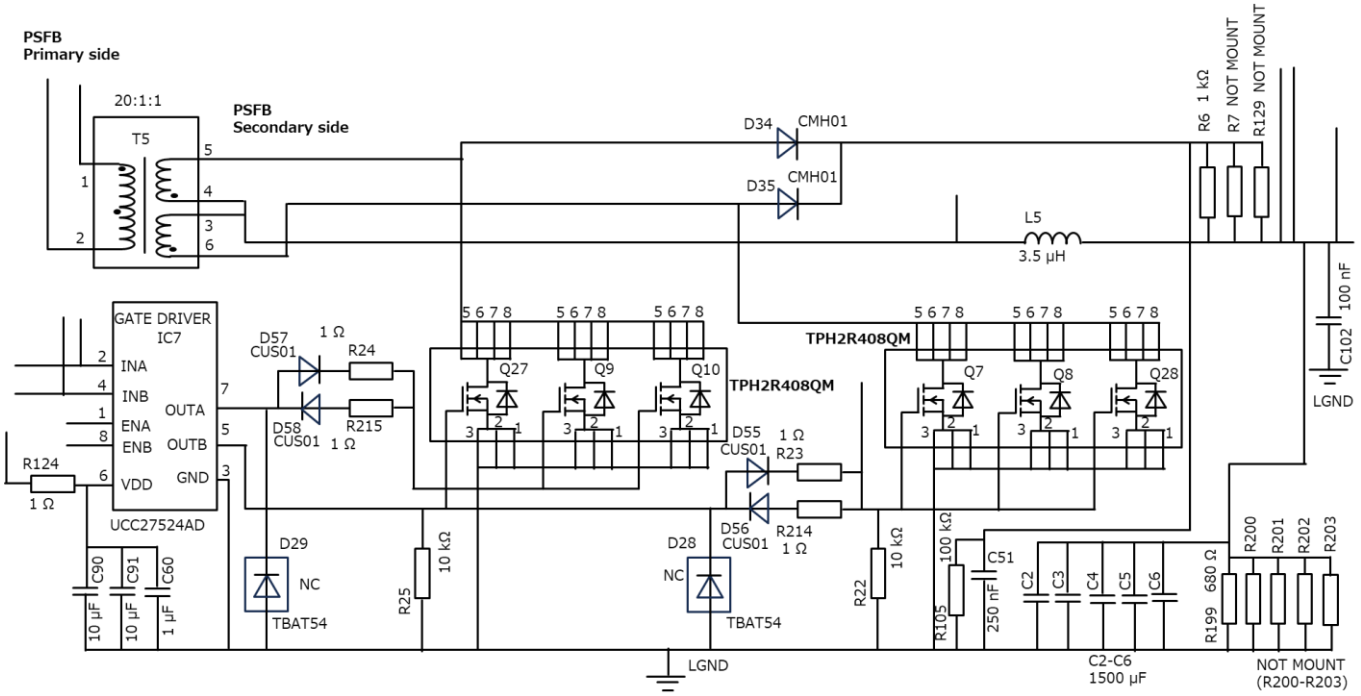


Fig. 3.11 PSFB Circuit 3 (Around Secondary MOSFET)

Output Capacitor

The output capacitors must be checked to ensure that the output voltage ripple is within the range required by the system. The output voltage ripple Vripple is a composite waveform including the ripple current ΔI generated by switching, and each voltage generated by ESR, capacitance (Cap), and ESL of the output capacitor. When the voltage of switching is V_{sw} and the output voltage is V_{out}, the switching frequency is F, the voltage generated by ESR, Cap, ESL is calculated by the following equation.

$$Vripple\_ESR = \Delta I \times ESR$$

$$Vripple\_Cap = \frac{\Delta I}{8 \times Cout \times F \times 2}$$

$$Vripple\_ESL = \frac{Vsw \times ESL}{L}$$

Here,

$$\Delta I = \frac{(Vsw - Vout) \times Vout}{Vsw \times F \times 2 \times L \times 2(phases)}$$

If V_{sw} = 19 V, V_{out} =12.14 V, F = 60.98 kHz, L = 3.5 µH, then ΔI is 20.5 A. The default values of the output ripple voltage generated by each element are: Vripple_ESR = 82 mV, Vripple_Cap = 2.8 mV, Vripple_ESL = 5.4 mV when C_{out} = 1500 µF x 5 pcs, ESR = 20 mΩ, ESL = 5 nH, L = 3.5 µH. The voltage generated by Cap is out of phase with the voltage generated by ESR, ESL, so a simple sum cannot be obtained originally. However, since the voltage generated by Cap is low, a simple sum can be used as a guideline. Adjust the capacitance of the output capacitor to satisfy the ripple voltage required for the system. It is also necessary to confirm that the undershoot or overshoot that occurs in the output when the load changes suddenly is within the specified voltage range, and that the allowable ripple current of the output capacitor can be maintained.

3.3.3. Communicaton Between Primary-side and Secondary-side in PSFB

As shown in Fig. 3.12, a 4-channel digital isolator DCL540C01 is used to isolate the primary-side and secondary-side transmission signals of PSFB circuit. MOSFET drive signals of the primary-side full-bridge circuit, which is output from PSFB controller located on the secondary-side, are transmitted through DCL540C01.

A photocoupler has a light-emitting element (LED) and a light-receiving element in the same package, electrically insulated by a light-transmitting plastic, and transmits signals by turning LED on/off. On the other hand, a digital isolator has a chip for modulating and demodulating in the same package and transmits signals by magnetic field or magnetic coupling.

DCL540C01 uses our proprietary magnetically coupled isolated transmission method to achieve a high CMTI of [Note 3-2] 100 kV/μs (Min.), which contributes to stable operation of equipment because it is less likely to malfunction even when affected by noises. In addition, it is suitable for high-speed communication applications because it realizes low-pulse-width distortion of 3.0 ns (Max.) and high-speed transmission rate of 150 Mbps (Max.).

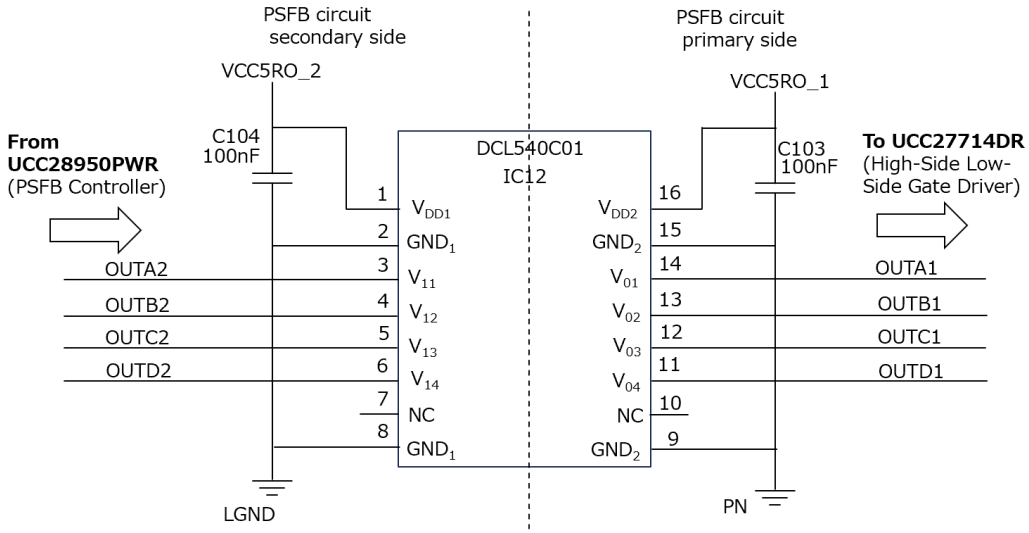


Fig. 3.12 Digital Isolator (TCL540C01)

Note 3-2: Common-mode transient immunity (CMTI)
Common-mode (common-mode) noise is noise that is superimposed on both signal-and GND lines. Current flows in the same direction. A digital isolator is used to perform signal transmission while electrically isolating circuits driven by independent power supplies. However, in such a case, if one potential fluctuates, common mode noise is generated. If this common mode noise causes the displacement current flowing through the coupling capacitance between the primary-side (input side) and secondary-side (output side) inside the standard digital isolator reaches a certain level, it will cause malfunction of the digital isolator and eventually the system. Therefore, the immunity against such common mode noise is important for a stable operation of the system. CMTI demonstrates the capability to handle the high slew-rate transients that occur between such GND ; the larger CMTI, the more noise-resistant and suitable it is for applications in which isolation is required.

3.3.4. Output ORing Circuit

This power supply is equipped with a ORing circuit in 12 V output, so that it can respond to requirements for N+1 redundant operation. Oring circuit consists of a Texas Instruments controller TPS2412 (IC8) (hereafter referred to as ORing controller) and on/off MOSFETs (Q15-Q24). If the output voltage of this power supply is higher than the output voltage of another power supply while the output of this power supply and other power supplies are connected in parallel, ORing controller turns on the on/off MOSFET and supplies current to the output. If the output voltage of this power supply is lower than the output voltage of other power supplies, ORing controller turns off the on/off MOSFET to prevent current from flowing back to this power supply from other power supplies. Refer to TPS2412 datasheet and related documentats for detailed designs of ORing circuit of this power supply. The type and quantity of MOSFET for on/off must be determined so that the power loss due to voltage-drops and on-resistors is within the tolerance of the system when the max-load (133 A) is applied. Ten TPHR6503PL1 are mounted in this power supply. Since the on-resistance of MOSFET rises at high temperatures, components must be selected in consideration of the environmental temperature supported by the system and the temperature rise of FET at the maximum load.

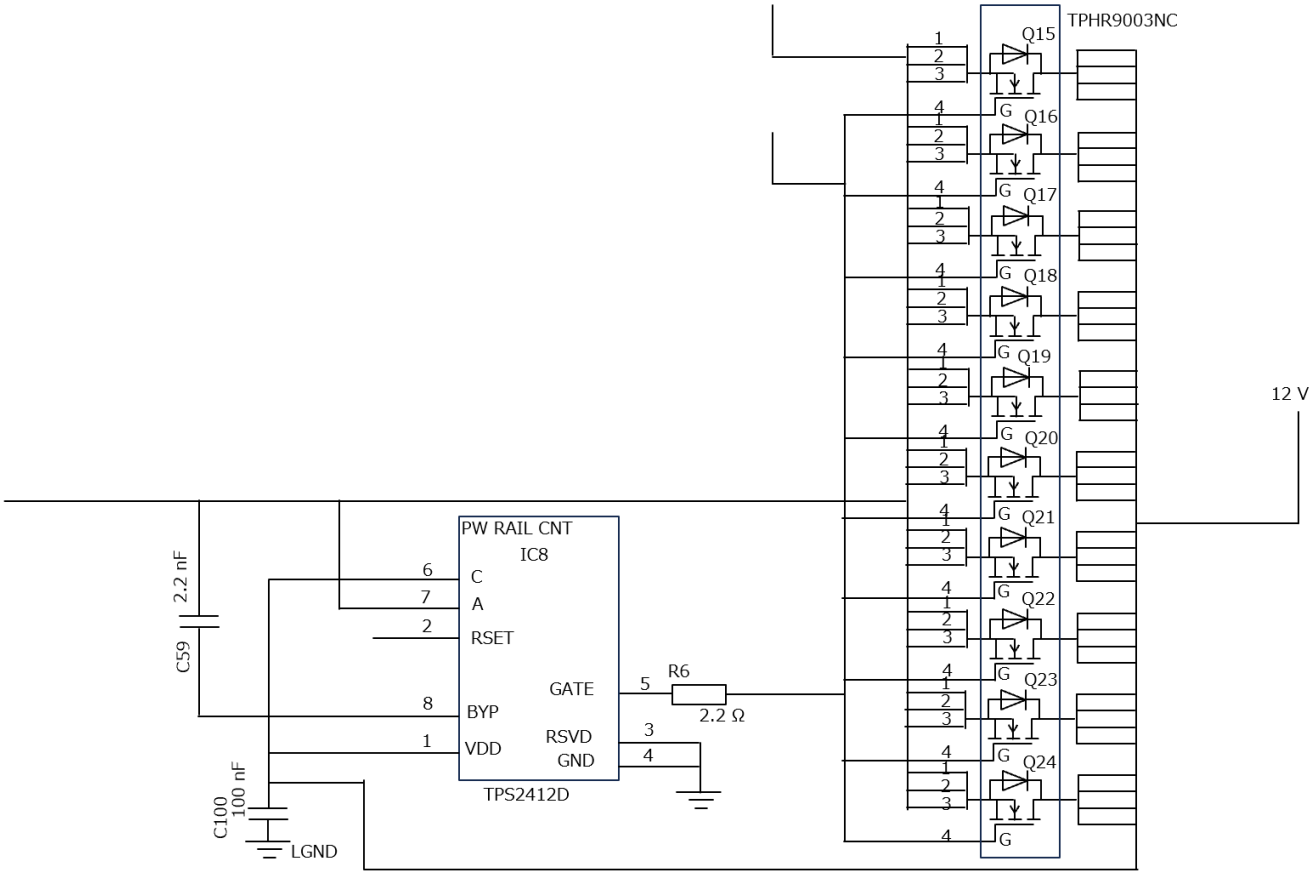


Fig.3.13 ORing Circuit

3.3.5. Auxiliary Power Supply

This upgraded power supply is equipped with an auxiliary power supply for supplying the necessary power to the controllers and MOSFET drive IC, etc., eliminating the need for external power input, which was required by the existing power supply, and therefore this operates only with AC input.

The auxiliary power supply employs a discontinuous current mode (DCM) flyback configuration with a Texas Instruments Controller UCC28910 (IC80) (hereafter referred to as the auxiliary power controller) to generate 12 V for the primary-side and 12 V for the secondary-side. Fig. 3.13 shows the auxiliary power supply circuit.

This section describes the transformer design for the auxiliary power supply circuit. Refer to UCC28910 datasheet and related documentation for more details about designing the circuit.

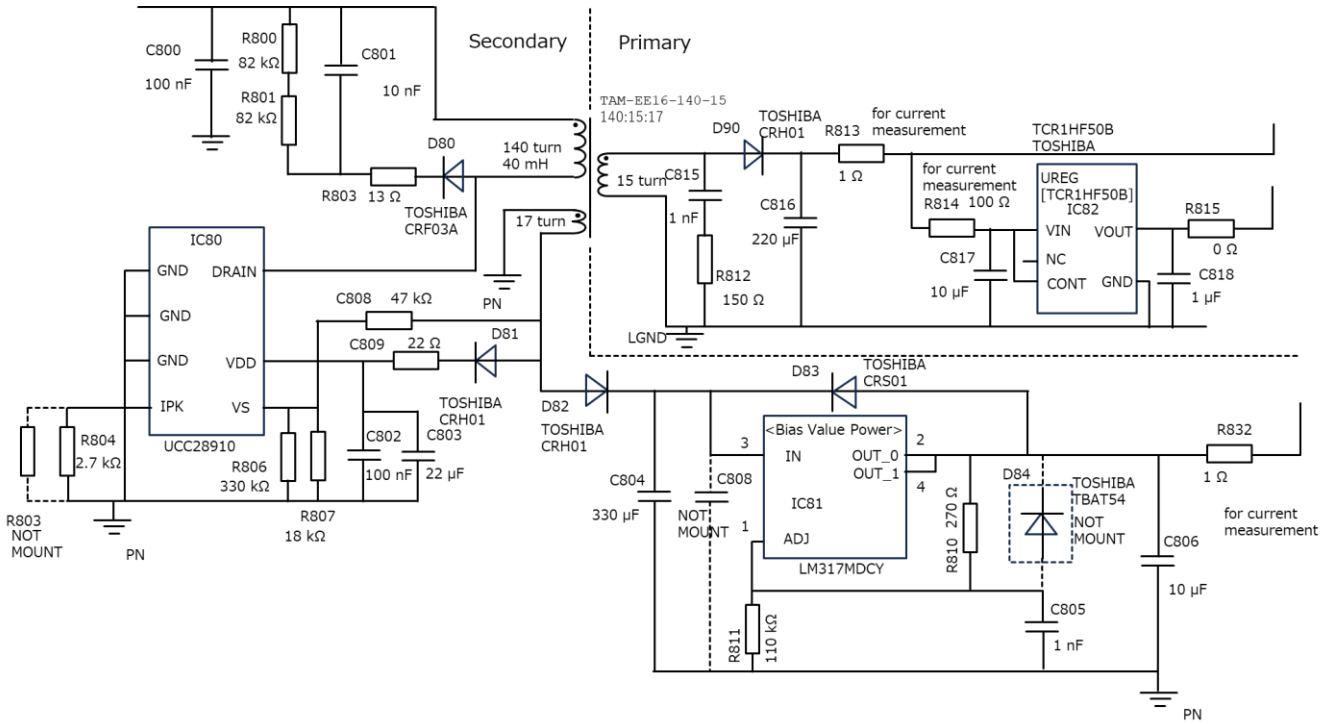


Fig. 3.13 Auxiliary Power Supply Circuit

Auxiliary Power Transformer Design

The maximum On Duty D_{max} of the flyback converter is calculated using the following equation with DCM Resonance Time t_R (assumed to be 1 / 500 kHz here) and the regulation gain K_{CC} of the CC mode, maximum oscillation frequency $f_{sw(max)}$ of the auxiliary power controller.

$$D_{max} = 1 - \left(\frac{t_R}{2} \times f_{sw(max)}\right) - K_{CC} = 1 - \left(\frac{1\mu s}{2} \times 115kHz\right) - 0.413 = 0.472$$

Based on the calculated maximum On Duty and minimum bulk-voltage $V_{BULK(min)}$ of the input capacitor, the winding ratio (N_{PS}) of the primary-side winding and secondary windings of the transformer is calculated as follows:

$$N_{PS} < \frac{D_{max} \times V_{Bulk(min)}}{K_{CC} \times \left(V_{out} + V_{F(D90)}\right)} = \frac{0.472 \times 110V}{0.413 \times (12V + 0.71V)} = 9.891$$

Assuming that the number of windings in the primary-side (N_P) is 140 turns, the number of windings in the secondary-side (N_S) can be calculated by the following equation.

$$N_S > \frac{N_P}{N_{PS}} = \frac{140}{9.891} = 14.15$$

Therefore, the number of turns Ns of the secondary winding is 15 turns in this power supply.
Next, using the minimum output voltage Vout(min) required for secondary-side control and the stop voltage $VDD_{OFF(max)}$ of the auxiliary power supply controller, calculate the winding number ratio N_{PA} of the primary winding and the auxiliary winding using the following equations.

$$N_{PA} < N_{PS} \times \frac{\left(V_{out(min)} + V_{F(D90)}\right)}{VDD_{OFF(max)} + V_{FAUX(D81)}} = \frac{140}{15} \times \frac{(6.15 + 0.71)}{7 + 0.71} = 8.30$$

Here, the minimum output voltage Vout(min) is calculated using the minimum operating voltage 6.15 V of PSFB controller, and the turns of the auxiliary winding (N_{AUX}) is calculated as follows.

$$N_{AUX} > \frac{N_P}{N_{PA}} = \frac{140}{8.30} = 16.86$$

Therefore, N_{AUX} number of windings of the auxiliary winding is set to 17 turns in this power supply.
The primary control voltage is generating a 12 V via LDO (IC81) from the output from auxiliary winding.

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