

**48 V Bus Compatible 1.2 V/100 A  
Double Step-Down DC-DC Converter**

**Design Guide**

**RD231-DGUIDE-01**

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**Toshiba Electronic Devices & Storage Corporation**

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## 1. Introduction

This design guide describes how to design the 48 V Bus Compatible 1.2 V/100 A Double Step-Down DC-DC Converter (hereafter referred to as this power supply). Refer to the reference guide for the specifications, operation check procedure, characteristics, etc. of this power supply.

In recent years, the amount of power consumed by data-centers has been increasing, and therefore 48 V power supply bus for server equipment is becoming popular in order to reduce power dissipation. This is a high-efficiency DC-DC converter that takes input power from 48 V bus lines and delivers 1.2 V, 100 A for powering CPU, GPU, ASIC and other devices on the board.

This power supply has two stages of step-down to achieve an efficient step-down from 50 V (Typ.) to 1.2 V, and the first-stage converts the voltage to 12 V. The power MOSFET [TPH1400ANH](#) is used as a high-side switching device in the first-stage, and the power MOSFET [TPH5R60APL](#) is used as a low-side switching device (synchronous rectification). This step-down circuit operates in two phases. The power MOSFET [TPH8R903NL](#) is used as a high-side switching device in the second-stage and the power MOSFET [TPHR9203PL1](#) is used as a low-side switching device (synchronous rectification). This step-down circuit operates in 5 phases. By using these Toshiba semiconductor devices, we have realized a highly efficient Double step-down DC-DC converter.

## 2. Main Components Used

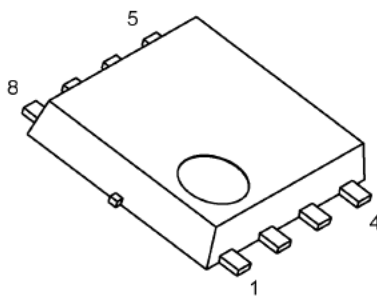
### 2.1. Power MOSFET TPH1400ANH

The power MOSFET [TPH1400ANH](#) is used as a high-side switching device on the first-stage. The main features of TPH1400ANH are as follows.

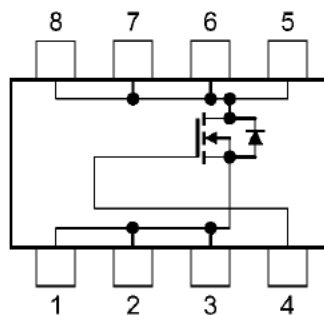
#### Features

- Small, thin package
- High-speed switching
- Small gate charge:  $Q_{sw} = 9.4 \text{ nC (Typ.)}$
- Low drain-source on-resistance:  $R_{DS(ON)} = 11.3 \text{ m}\Omega \text{ (Typ.) (} V_{GS} = 10 \text{ V)}$
- Low leakage current:  $I_{DSS} = 10 \text{ }\mu\text{A (Max.) (} V_{DS} = 100 \text{ V)}$
- Enhancement mode:  $V_{th} = 2.0 \text{ to } 4.0 \text{ V (} V_{DS} = 10 \text{ V, } I_D = 0.3 \text{ mA)}$

#### External Appearance and Internal Circuit Configuration Diagram



SOP Advance



1, 2, 3: Source  
4: Gate  
5, 6, 7, 8: Drain

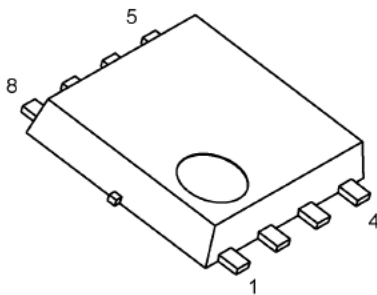
### 2.2. Power MOSFET TPH5R60APL

The power MOSFET [TPH5R60APL](#) is used as a low-side switching device on the first-stage. The main features of TPH5R60APL are as follows.

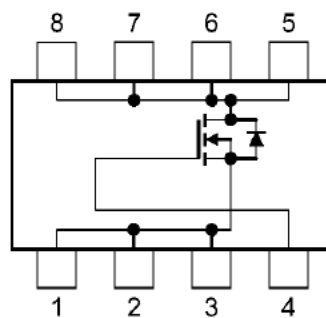
#### Features

- High-speed switching
- Small gate charge:  $Q_{SW} = 14 \text{ nC}$  (Typ.)
- Small output charge:  $Q_{OSS} = 46 \text{ nC}$  (Typ.)
- Low drain-source on-resistance:  $R_{DS(ON)} = 4.7 \text{ m}\Omega$  (Typ.) ( $V_{GS} = 10 \text{ V}$ )
- Low leakage current:  $I_{DSS} = 10 \text{ }\mu\text{A}$  (Max.) ( $V_{DS} = 100 \text{ V}$ )
- Enhancement mode:  $V_{th} = 1.5 \text{ to } 2.5 \text{ V}$  ( $V_{DS} = 10 \text{ V}$ ,  $I_D = 0.5 \text{ mA}$ )

#### External Appearance and Internal Circuit Configuration Diagram



SOP Advance



1, 2, 3: Source  
4: Gate  
5, 6, 7, 8: Drain

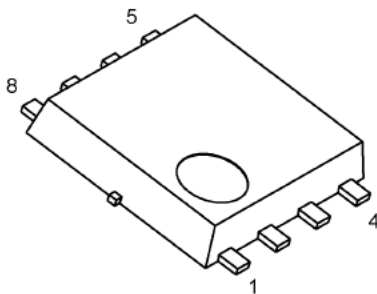
### 2.3. Power MOSFET TPH8R903NL

The power MOSFET [TPH8R903NL](#) is used as a high-side switching device on the second-stage. The main features of TPH8R903NL are as follows.

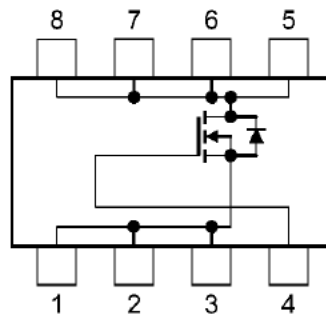
#### Features

- High-speed switching
- Small gate charge:  $Q_{SW} = 2.5 \text{ nC}$  (Typ.)
- Low drain-source on-resistance:  $R_{DS(ON)} = 10.2 \text{ m}\Omega$  (Typ.) ( $V_{GS} = 4.5 \text{ V}$ )
- Low leakage current:  $I_{DSS} = 10 \text{ }\mu\text{A}$  (Max.) ( $V_{DS} = 30 \text{ V}$ )
- Enhancement mode:  $V_{th} = 1.3 \text{ to } 2.3 \text{ V}$  ( $V_{DS} = 10 \text{ V}$ ,  $I_D = 0.1 \text{ mA}$ )

#### External Appearance and Internal Circuit Configuration Diagram



SOP Advance



1, 2, 3: Source  
4: Gate  
5, 6, 7, 8: Drain

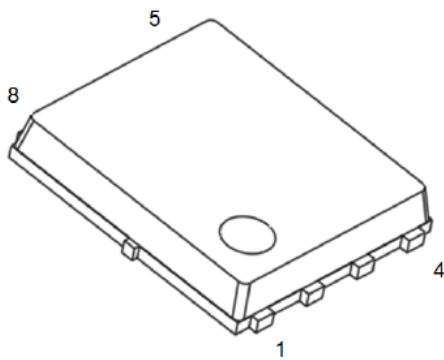
### 2.4. Power MOSFET TPHR9203PL1

The power MOSFET [TPHR9203PL1](#) is used as a low-side switching device on the second-stage. The main features of TPHR9203PL1 are as follows.

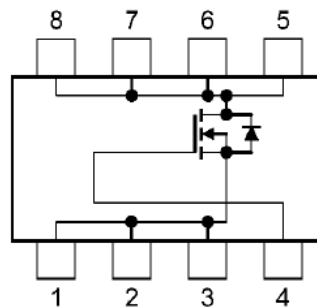
#### Features

- High-speed switchin
- Small gate charge:  $Q_{SW} = 19 \text{ nC}$  (Typ.)
- Small output charge:  $Q_{OSS} = 51 \text{ nC}$  (Typ.)
- Low drain-source on-resistance:  $R_{DS(ON)} = 0.61 \text{ m}\Omega$  (Typ.) ( $V_{GS} = 10 \text{ V}$ )
- Low leakage current:  $I_{DSS} = 10 \text{ }\mu\text{A}$  (Max.) ( $V_{DS} = 30 \text{ V}$ )
- Enhancement mode:  $V_{th} = 1.1 \text{ to } 2.1 \text{ V}$  ( $V_{DS} = 10 \text{ V}$ ,  $I_D = 0.5 \text{ mA}$ )

#### External Appearance and Internal Circuit Configuration Diagram



SOP Advance(N)



1, 2, 3: Source  
4: Gate  
5, 6, 7, 8: Drain



### 3. Step-Down DC-DC Converter

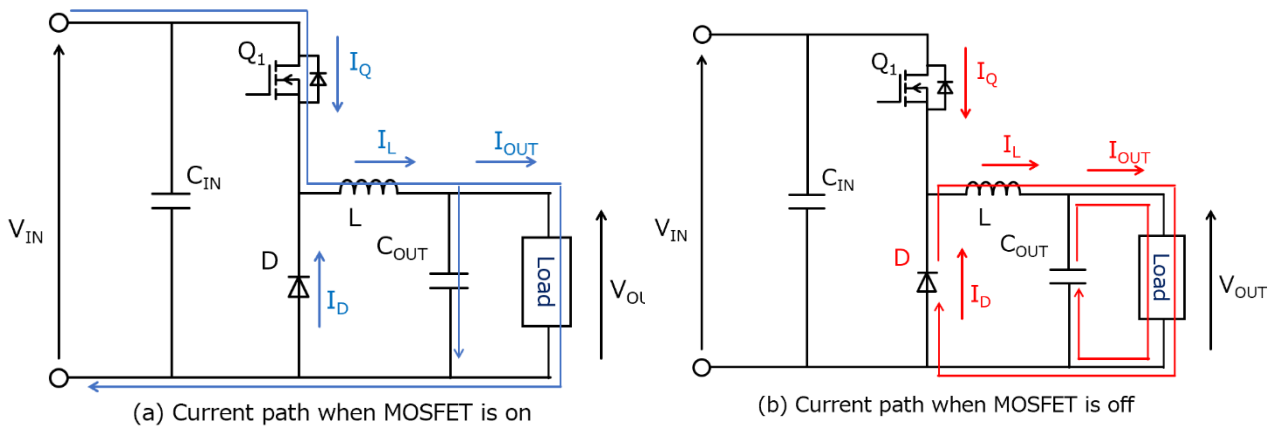
The step-down DC-DC converter converts the DC-input voltage to a lower DC voltage. Each electronic device, such as an IC, must have a voltage that matches the operating voltage.

#### 3.1. Step-Down DC-DC Converter Operation

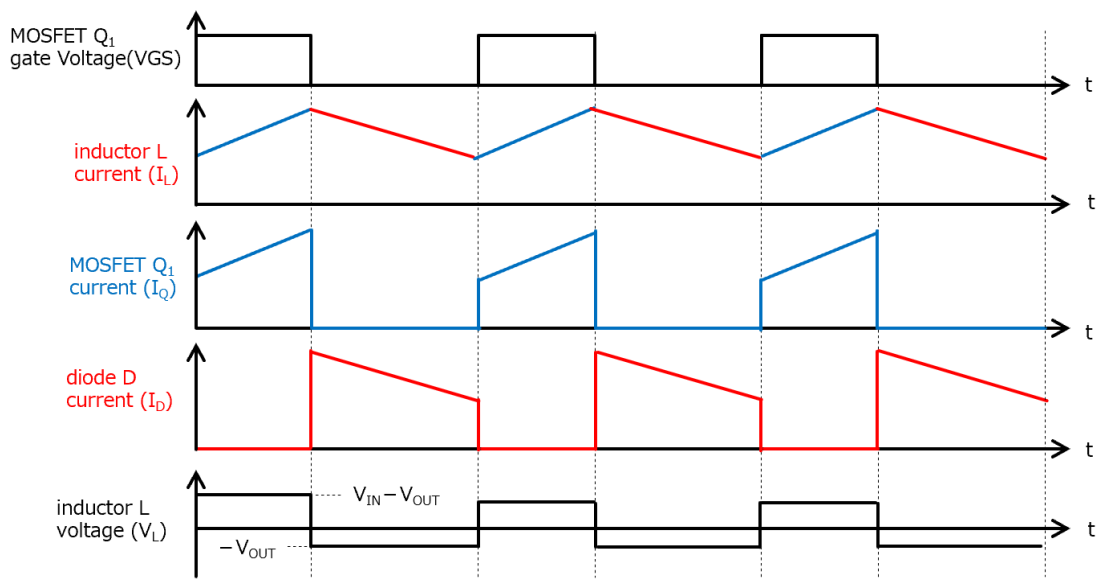
##### 3.1.1. Circuit Operation and Voltage/Current Waveforms

Fig. 3.1 shows the basic circuit and operation of the step-down DC-DC converter. Part (a) shows the current path when MOSFET  $Q_1$  is on. When  $Q_1$  is on, the current passes from the input  $V_{IN}$  through the inductor  $L$  to charge the output smoothing capacitor  $C_{OUT}$  and provide the output current  $I_{OUT}$ . At this time, energy is stored in  $L$ . Part (b) shows the current path when MOSFET  $Q_1$  is off. When  $Q_1$  is off, the diode  $D$  is on and stored energy in  $L$  is discharged to the output-side.

The waveforms of gate voltage of MOSFET  $Q_1$ , the current of inductor  $L$ , MOSFET  $Q_1$  and diode  $D$ , and the voltage across the inductor  $L$  are shown in Fig. 3.2. The relation between the input voltage and the output voltage is determined by the on duty of the MOSFET  $Q_1$ .



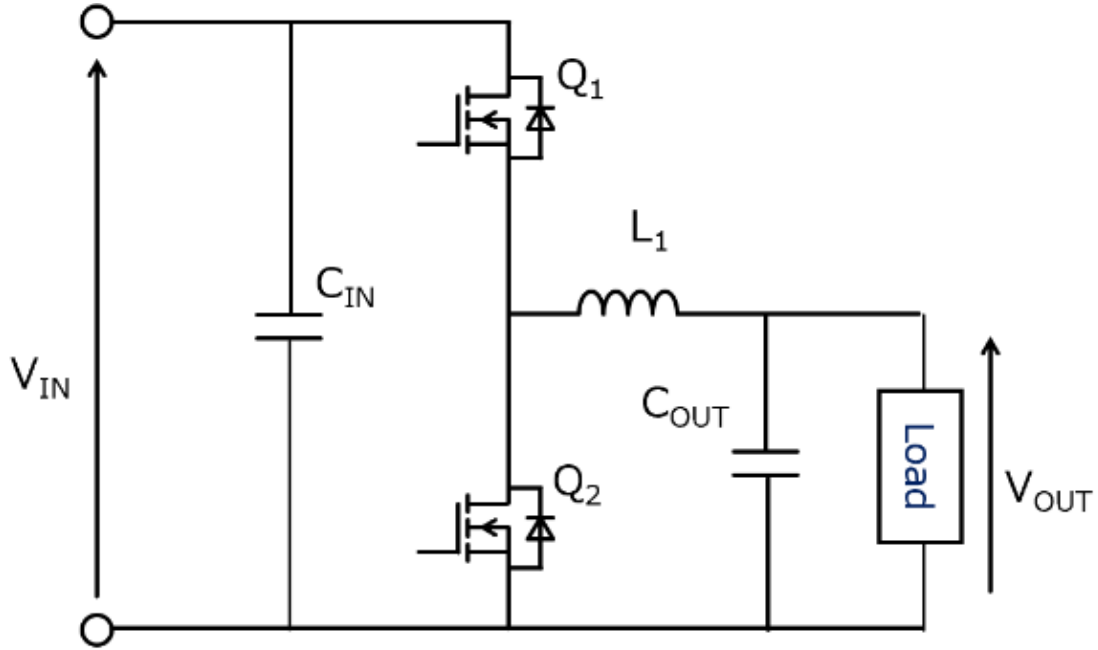
**Fig. 3.1 Basic Circuit and Operation of the Step-Down Converter**



**Fig. 3.2 Step-Down Converter Current and Voltage Waveforms**

**3.1.2. Synchronous Rectification Circuit**

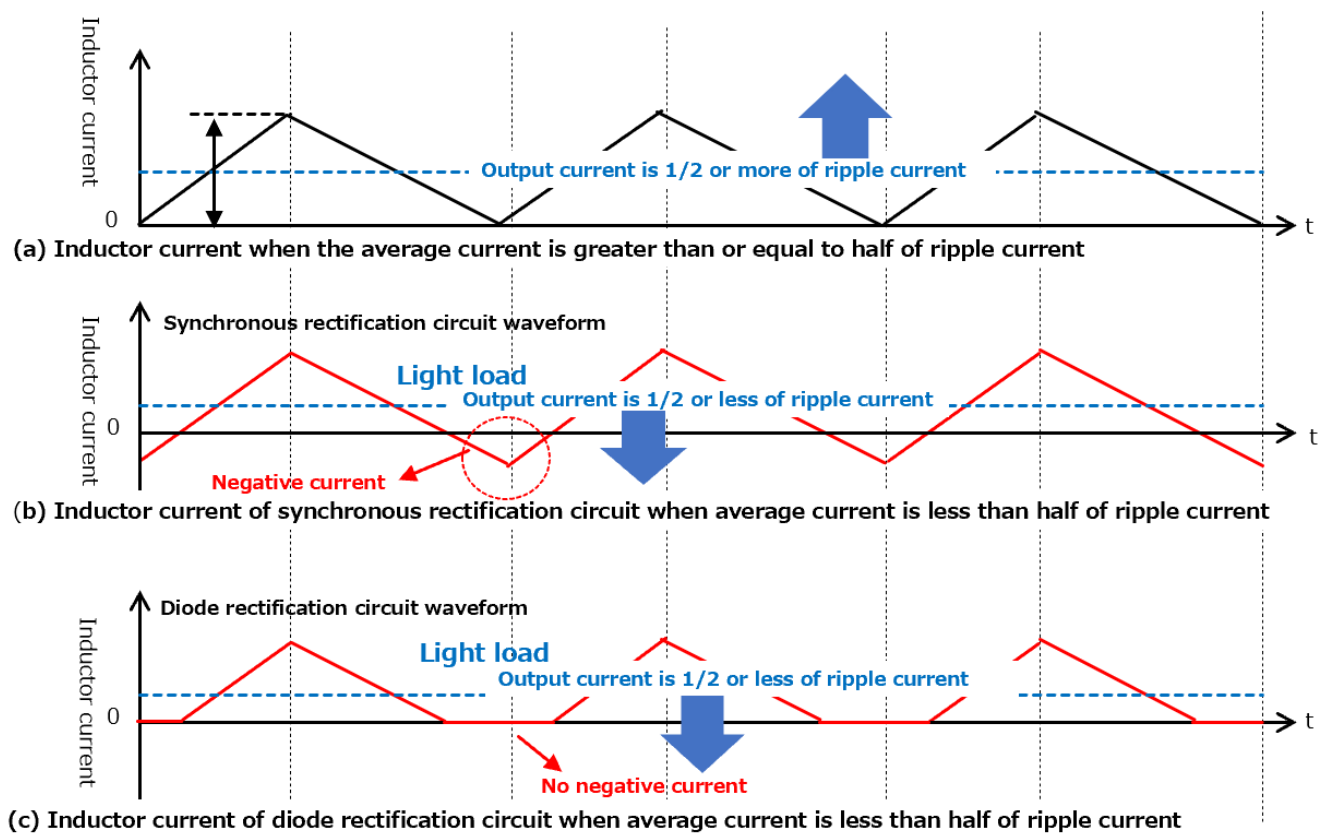
Fig. 3.3 shows a synchronous rectification method in which a MOSFET is used on the low-side instead of a diode-rectifier circuit in Fig. 3.1. Basic circuit operation is the same. In synchronous rectification,  $Q_2$  is turned on at the same time when  $Q_1$  is turned off. In synchronous rectification, current flows from the source to the drain of MOSFET  $Q_2$  instead of diode  $D$  in diode rectification. Changing the Diode  $D$  to MOSFET  $Q_2$  improves efficiency.



**Fig. 3.3 Step-Down Converter with Synchronous Rectification Circuit**

### 3.1.3. Comparison of Diode Rectification and Synchronous Rectification Under Light Load

As shown in Fig. 3.4 (a), when the load current is  $1/2$  or more of the inductor current ripple, the inductor current is equivalent to the synchronous rectification type and the diode rectification type, and the current is continuous mode. However, the magnitude of the load current is different when it is less than  $1/2$  of the ripple current. In the synchronous type, as shown in Fig. 3.4 (b), even if the inductor current becomes negative, the current continuously flows, because MOSFET  $Q_2$  is on. However, for diode-rectification, as shown in Fig. 3.4 (c), when the inductor current drops to zero, the current is blocked by the diode  $D$ . It is called the discontinuous current mode (DCM). discontinuous current.



**Fig. 3.4 Inductor Current Comparison Under Light Load**

**3.1.4. Improving Light Load Efficiency of Synchronous Rectification Circuit Using Reverse Current Prevention Function**

In a synchronous rectification circuit, the inductor current flows in reverse when the load current falls below half of the ripple current. This reverse current flows through the high-side MOSFET, causing conduction loss. This loss makes efficiency worse. To eliminate this loss, there is a DC-DC converter with a reverse current prevention function that detects the reverse current and turns off the low-side MOSFET.

**3.1.5. Output Voltage and Inductor**

The following relationship exists between the inductance of inductor L and, the voltage and current.

$$V = -L \frac{di}{dt}$$

Fig. 3.5 shows the inductor current wave form of DC-DC converter. In Fig. 3.3, the relation between MOSFET Q<sub>1</sub> on-period T<sub>ON</sub> and the voltage/current is expressed by the equation above as follows. The on-voltage of MOSFET Q<sub>1</sub> at this time is used as V<sub>Q1</sub>.

$$V_{IN} - V_{Q1} - V_{OUT} = -L \times \frac{I_{LMAX} - I_{LMIN}}{T_{ON}}$$

$$I_{LMAX} - I_{LMIN} = - \frac{(V_{IN} - V_{Q1} - V_{OUT}) \times T_{ON}}{L}$$

In Fig. 3.3, relation between the voltage and current of MOSFET Q<sub>1</sub> off-period T<sub>OFF</sub> (MOSFET Q<sub>2</sub> is on) in the circuit is expressed as follows. The on-voltage of MOSFET Q<sub>2</sub> at this time is used as V<sub>Q2</sub>.

$$V_{Q2} + V_{OUT} = -L \times \frac{I_{LMAX} - I_{LMIN}}{T_{OFF}}$$

$$I_{LMAX} - I_{LMIN} = - \frac{(V_{Q2} + V_{OUT}) \times T_{OFF}}{L}$$

From the equations above,

$$(V_{IN} - V_{Q1} - V_{OUT}) \times T_{ON} = (V_{Q2} + V_{OUT}) \times T_{OFF}$$

By the way, the on-duty D can be expressed as follows: T is MOSFET Q<sub>1</sub> on/off cycle.

$$D = \frac{T_{ON}}{T} = \frac{T_{ON}}{T_{ON} + T_{OFF}} = T_{ON} \times f_{SW} = 1 - (T_{OFF} \times f_{SW})$$

T<sub>ON</sub>, T<sub>OFF</sub> is as follows.

$$T_{ON} = \frac{D}{f_{SW}} \quad T_{OFF} = \frac{1 - D}{f_{SW}}$$

The equation above gives following equation.

$$D = \frac{V_{Q2} + V_{OUT}}{V_{IN} - V_{Q1} + V_{Q2}}$$

When the output voltage is high,  $V_{Q1}$  and  $V_{Q2}$  in the equation above have little effect and can be simplified as shown in following equation.

$$D = \frac{V_{OUT}}{V_{IN}}$$

The equation of  $T_{ON}$  and the equation of  $D$  give the following equation.

$$T_{ON} = \frac{D}{f_{SW}} = \frac{V_{Q2} + V_{OUT}}{(V_{IN} - V_{Q1} + V_{Q2}) \times f_{SW}}$$

From the equation above,

$$I_{LMAX} - I_{LMIN} = \frac{(V_{IN} - V_{Q1} - V_{OUT}) \times (V_{Q2} + V_{OUT})}{(V_{IN} - V_{Q1} - V_{Q2}) \times L \times f_{SW}}$$

Now, if  $\Delta I_L$  is  $I_{LMAX} - I_{LMIN}$ , the following equations are given.

$$\Delta I_L = \frac{(V_{IN} - V_{Q1} - V_{OUT}) \times (V_{Q2} + V_{OUT})}{(V_{IN} - V_{Q1} - V_{Q2}) \times L \times f_{SW}}$$

$$\Delta I_L = \frac{1}{f_{SW} \times L} \times V_{OUT} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

$$L = \frac{(V_{IN} - V_{Q1} - V_{OUT}) \times (V_{Q2} + V_{OUT})}{(V_{IN} - V_{Q1} - V_{Q2}) \times f_{SW} \times \Delta I_L}$$

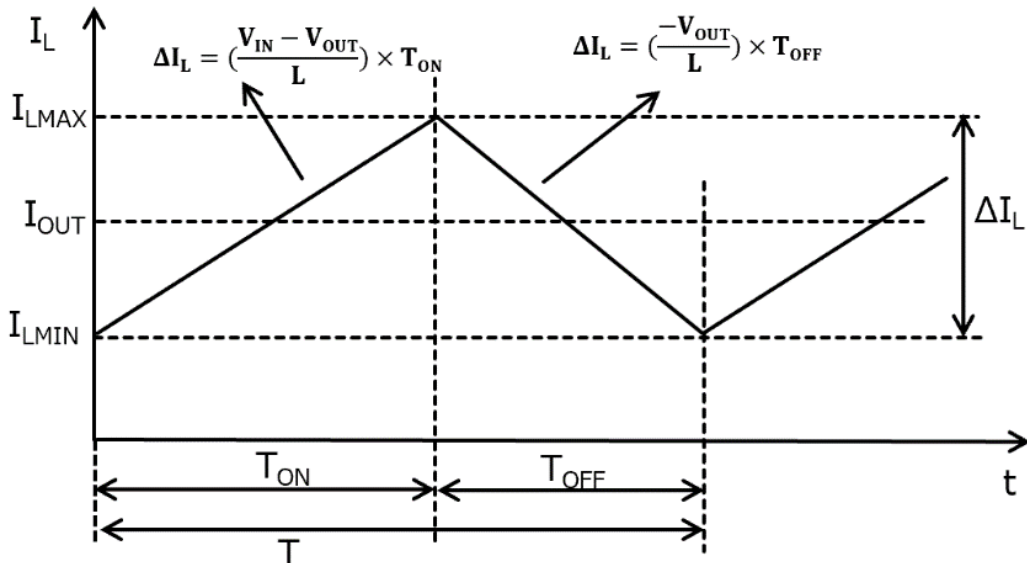
When the output voltage is high, the equation can be simplified as shown in following equation.

$$L = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN} \times f_{SW} \times \Delta I_L}$$

Replacing the inductor current change  $\Delta I_L$  into the output current and current ripple ratio  $r$  gives the following equation.

$$r = \frac{\Delta I_L}{I_{OUT}}$$

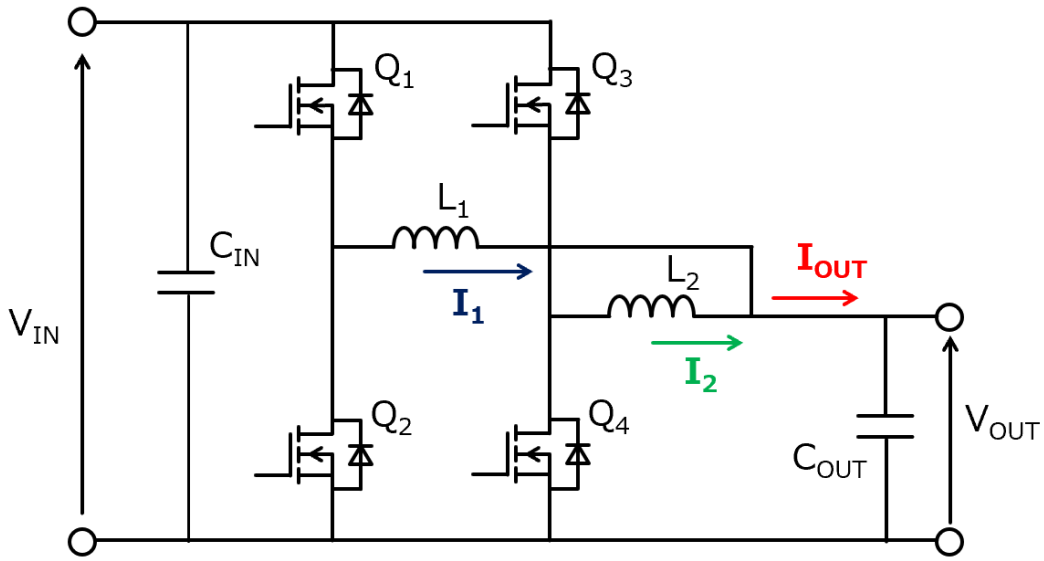
$$L = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN} \times f_{SW} \times r \times I_{OUT}}$$



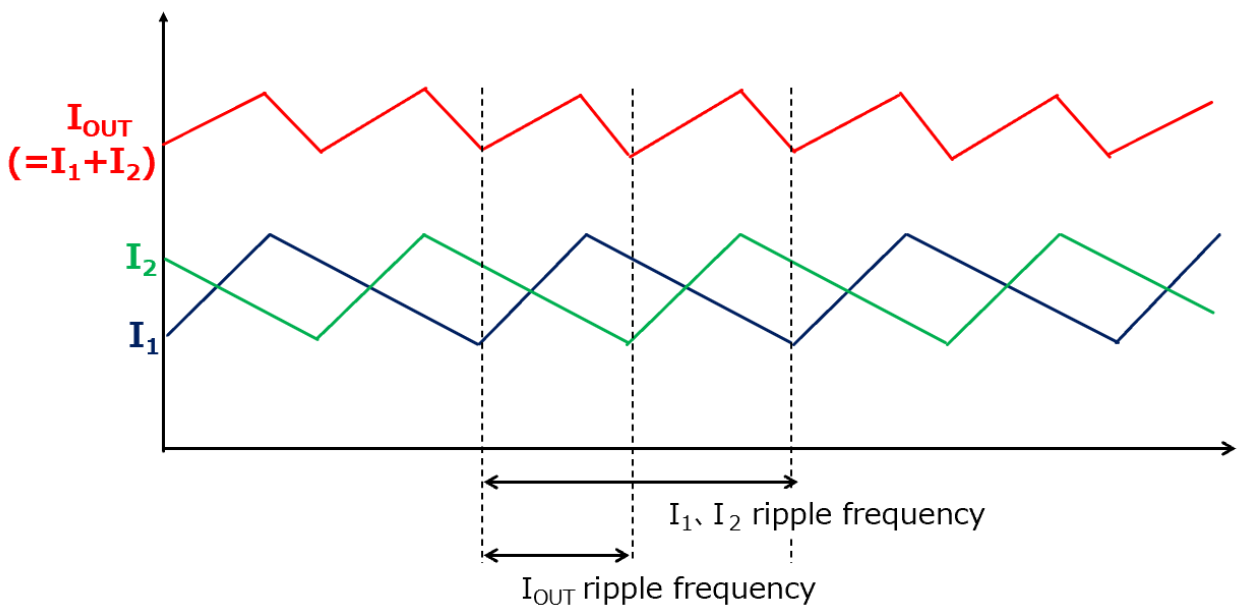
**Fig. 3.5 Inductor Current**

**3.1.6. Multi-Phase DC-DC Converter**

Multi-phase DC-DC converters are used to connect multiple converter circuits sharing some components, such as output capacitors, these are connected in parallel and operate with a staggered period. A single converter circuit in parallel is generally referred to as a phase. Fig. 3.6 shows an example of two-phase circuit. The operating frequency is the fundamental frequency multiplied by the number of phases, which is very high. This also reduces the output current ripple. Fig. 3.7 shows the ripple waveform of inductor currents  $I_1$  and  $I_2$  and the output current  $I_{OUT}$  of the circuit (two-phase DC-DC converter) shown in Fig. 3.6. Multi-phase DC-DC converters reduce the size of components and the capacitance of output capacitors. Also, the ripple of the output current is reduced to make the current more uniform.



**Fig. 3.6 Multiphase DC-DC Converter (Example of 2-Phase)**



**Fig. 3.7 Inductor and Output Current Waveforms**

### 3.1.7. Multi-Stage Step-Down DC-DC Converter

Some step-down DC-DC converter applications require a high-input voltage to be converted to a very low-output voltage for a low-voltage, high-current operation, such as LSI like CPU. When the voltage-difference between the input and output is large, the on-duty  $D$  of MOSFET  $Q_1$  becomes very small in the normal circuit shown in Fig. 3.3, as can be seen from the following relation. For example, when stepping down from the incoming 48 V to the outgoing 1.2 V, the on-duty is 2.5 %.

$$V_{OUT} = DV_{IN}$$

If the on-duty is low, MOSFET  $Q_1$  on-time will be very short if the switching frequency is high. This will result in poor controllability, for example, due to the difficulty of switching, although it will vary depending on the drive capability.

In addition, a large current must flow during  $Q_1$  on-time because the power-supplying inductor has a short time to store energy. When a large peak-to-average current flows, the switching loss of  $Q_1$  increases, causing a drop in efficiency.

A way to solve these problems is to provide the required voltage by multi-step operation. Taking the case of two stages as an example, the input voltage is once stepped down to the intermediate voltage in the first-stage, and then stepped down from the intermediate voltage to the final voltage in the second-stage. Fig. 3.8 shows an example. In this circuit, the voltage of 50 V is converted to 12 V in the circuit of the first-stage and the voltage of 12 V is converted to 1.2 V in the circuit of the second-stage.

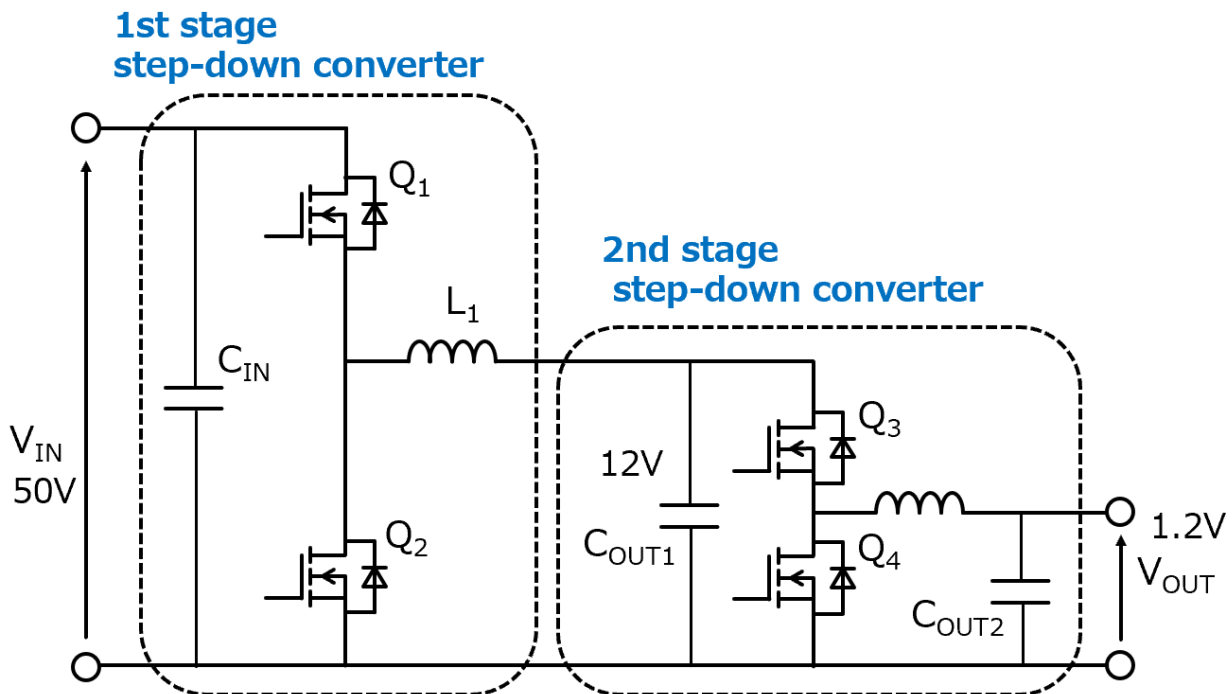


Fig. 3.8 Multi-Stage Step-Down DC-DC Converter (Example of 2 Stage Configuration)

## 4. Circuit Design of This Power Supply

This section describes the key points of the circuit design of this power supply. Refer to the data sheet and related documents of the controller IC used for detailed designs of each part.

### 4.1. Overview

#### 4.1.1. Specifications

This is a step-down DC-DC converter that provides an output of 1.2 V / 100 A to power the various loads on the board from 48 V power supply line of servers etc. Table 4.1 lists the main specifications of this power supply.

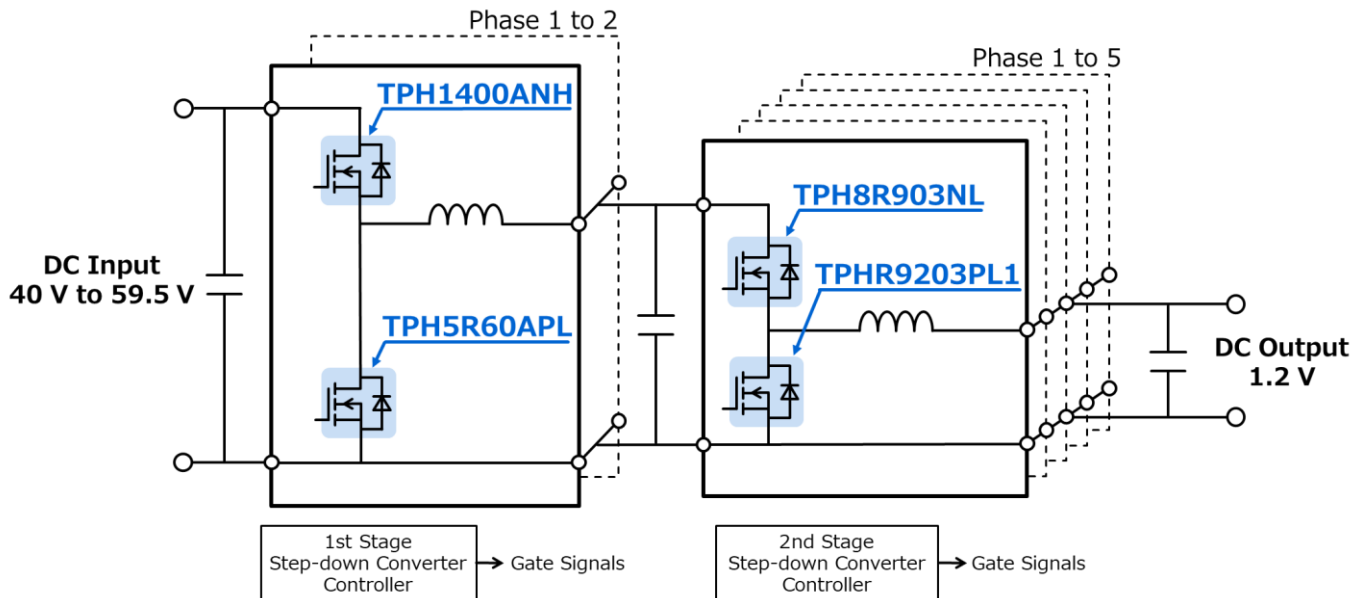
**Table 4.1 Main Specifications of This Power Supply**

Parameters	Conditions	Min.	Typ.	Max.	Unit
<b>External Specifications</b>					
Input Voltage		40	50	59.5	V
Output Voltage	Vout setting = 1.2 V	1.176	1.2	1.224	V
Output Voltage Variable Range	According to the on-board DIP setting	0.50		1.60	V
Output Current	Vout = 1.2 V			100	A
Output Ripple Voltage	Vout = 1.2 V			20	mV
Board Size	151 × 198 mm				
Board Configuration	FR-4, 6 layers, 1.6mm thick Copper foil thickness: Outer layer 35 μm, Inner layer 35 μm				
Cooling System	Convection cooling				
<b>Internal Specifications (First-Stage)</b>					
Output Voltage			12		V
Switching Frequency			100		kHz
Input Low Voltage Error Detection Voltage			35		V
Overheat Error Detection Temperature	IC1 junction temperature		180		°C
<b>Internal Specifications (Second-Stage)</b>					
Input Voltage			12		V
Switching Frequency			400		kHz
Input Low Voltage Error Detection Voltage			10		V



**4.1.2. Circuit Configuration**

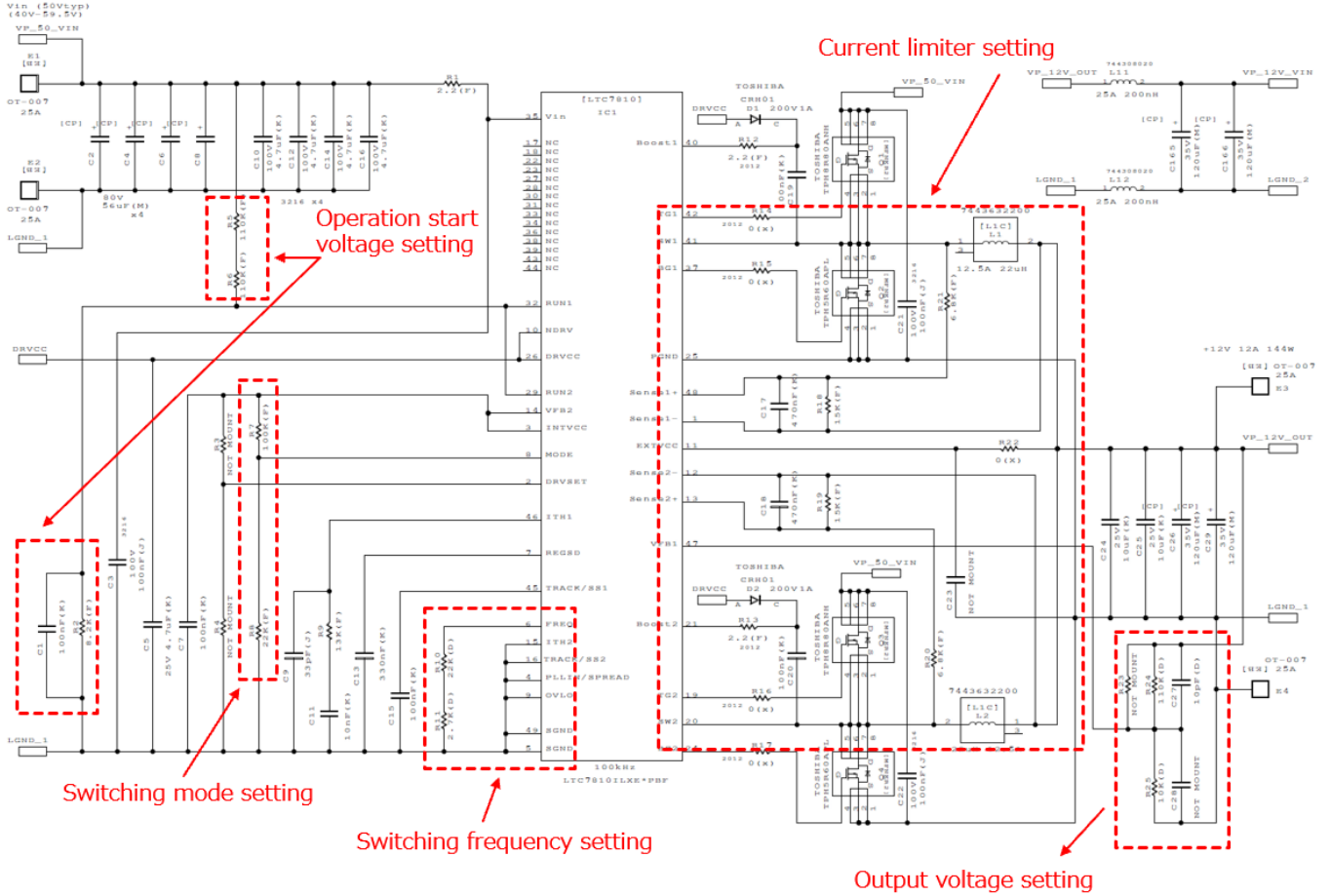
Fig. 4.1 shows a block diagram of this power supply. The step-down converter circuit consists of two stages, the first-stage consists of two phases, and the second-stage consists of five phases.



**Fig. 4.1 Block Diagram**

**4.2. First-Stage Step-Down DC-DC Converter**

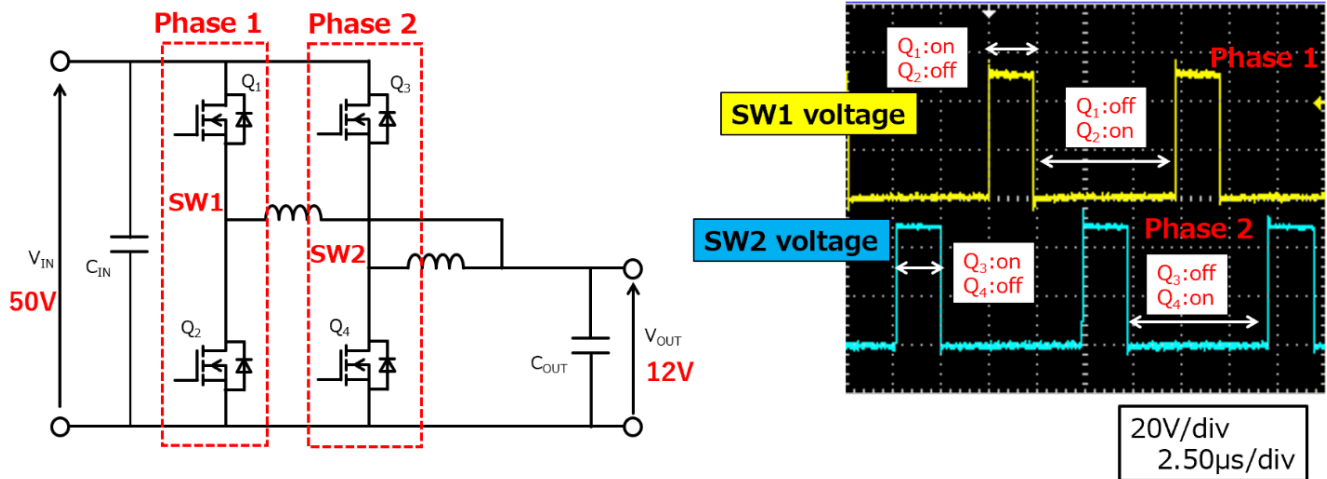
Fig. 4.2 shows the first-stage circuit. It is a synchronous step-down DC-DC converter with a two-phase configuration. The controller uses a LTC7810 made by Analog Devices (hereinafter referred to as the first-stage controller). The operation of each phase is shifted by 180 degrees.



**Fig. 4.2 First-Stage Step-Down DC-DC Converter Circuit**

**4.2.1. Circuit Operation**

The first step-down DC-DC converter has a two-phase DC-DC converter configuration. Fig. 4.3 shows the block diagram and the waveforms of the switching node voltage (SW1, SW2) for each phase. The output voltage is determined by the input voltage and the On duty of Q<sub>1</sub> and Q<sub>3</sub>. The frequency of operation in each phase is 100 kHz as can be seen from the wave form. Each phase operates with a phase difference of 180 degrees.

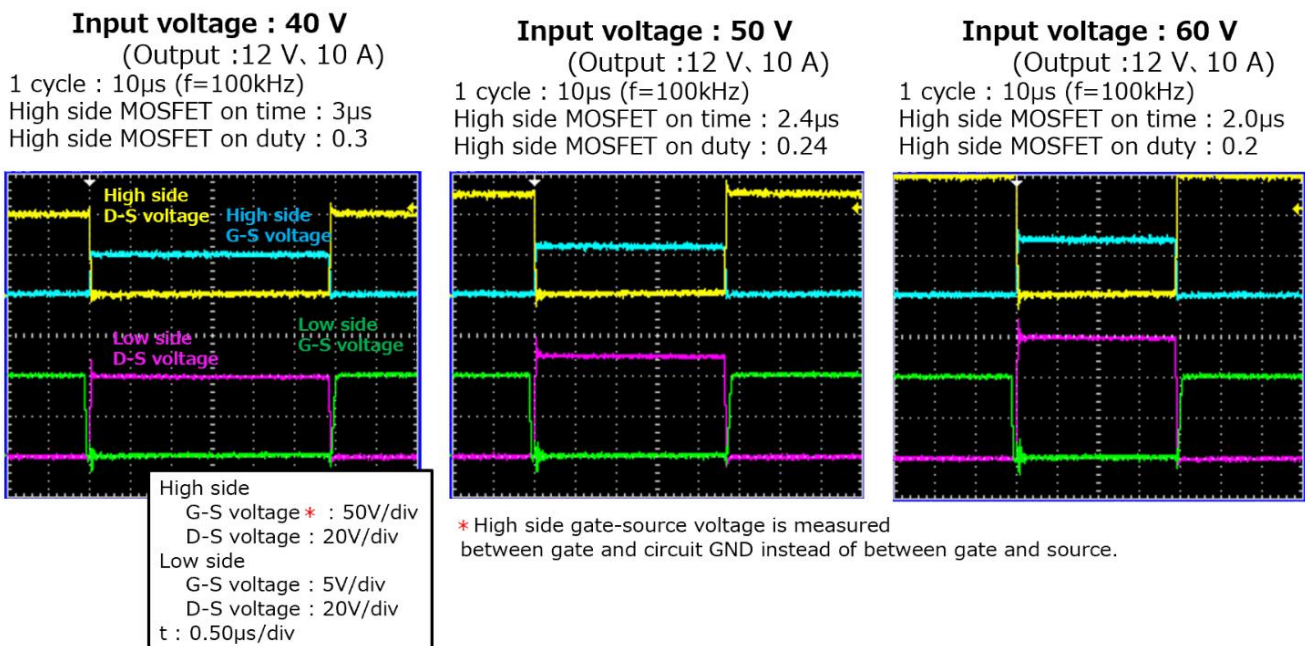


**Fig. 4.3 First-Stage Block Diagram and Switching Node Waveform**

The switching frequency of MOSFET is 100 kHz and one cycle is 10 µs to get the output-voltage of 12 V. When the input-voltage V<sub>IN</sub> fluctuates, the on-time of the high-side MOSFET is adjusted, and the on-duty D is changed to keep the output-voltage V<sub>OUT</sub> constant. The input and output voltages have the following relationship. Fig. 4.4 shows MOSFET switching waveform when the input-voltage V<sub>IN</sub> changes.

$$V_{OUT} = DV_{IN}$$

As the input voltage V<sub>IN</sub> increases, the on-time of the high-side MOSFET is shortened to keep the output V<sub>OUT</sub> constant.



**Fig. 4.4 MOSFET Switching Waveform of First-Stage Circuit**

### 4.2.2. Switching Frequency Setting

The switching frequency is set by the resistance of the external resistors (R10, R11) between FREQ (Pin 6) on the first-stage controller and GND shown in Fig. 4.5. The following equation calculates the switching frequency  $f_{LTC7810}$  from the relation between IC oscillator frequency and internal resistor.

$$f_{LTC7810}(kHz) = ((R10 + R11) - 13.5k) \times 9$$

With this power supply, the target value of the switching frequency is set as 100 kHz, and 22 kΩ is selected as the resistance value R10 and 2.7 kΩ is selected as the resistance value R11. The calculated value of this constant is 100.8 kHz.

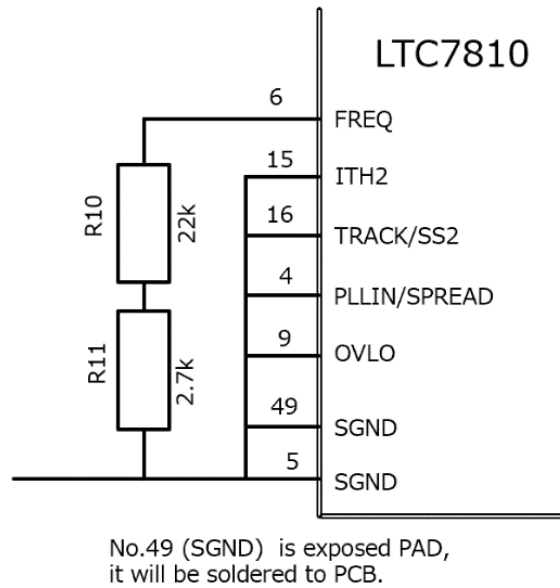


Fig. 4.5 Switching Frequency Setting Circuit

### 4.2.3. Operation Mode Setting

In the first-stage of this power supply, the switching operation at light load can be changed to the following three modes by the first-stage controller.

• **Forced Continuous Mode**

Switching pulses are output even when the inductor current is within the negative range, independent of the load current. Connect the INTVCC (pin 3) to the MODE (pin 8).

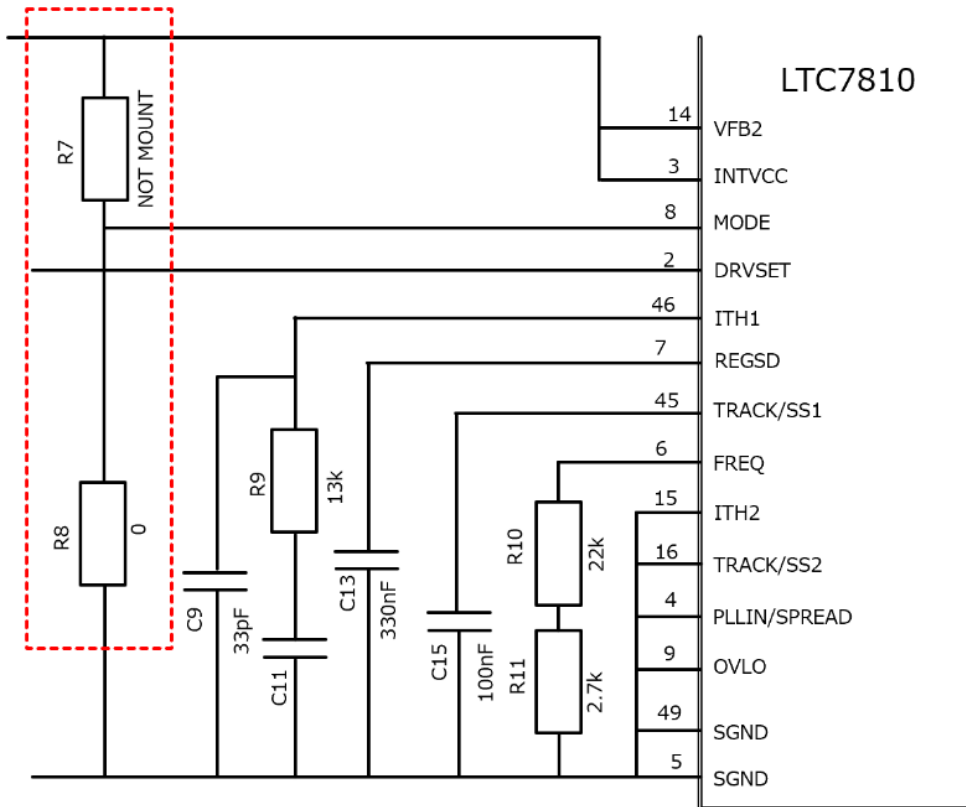
• **Pulse Skip Mode**

When the inductor current is excessive at light load, the low-side MOSFET turns off if the inductor current becomes negative. Connect a DC voltage to MODE terminal which is higher than 1.1 V, and lower than the INTVCC voltage -1.3 V.

• **Burst mode**

When the load is light, during the output voltage is kept by only the capacitance of the output capacitor with keeping the low-side MOSFET off, the high-side MOSFET is also kept off. Connect MODE terminal to GND or connect 0.5 V to 1.0 V voltage to it.

As shown in Fig. 4.6, this power supply is set to the burst mode. The level at which the mode switches from burst mode to continuous mode is approximately 25 % of the current limit value.



**Fig. 4.6 Operation Mode Setting Circuit**

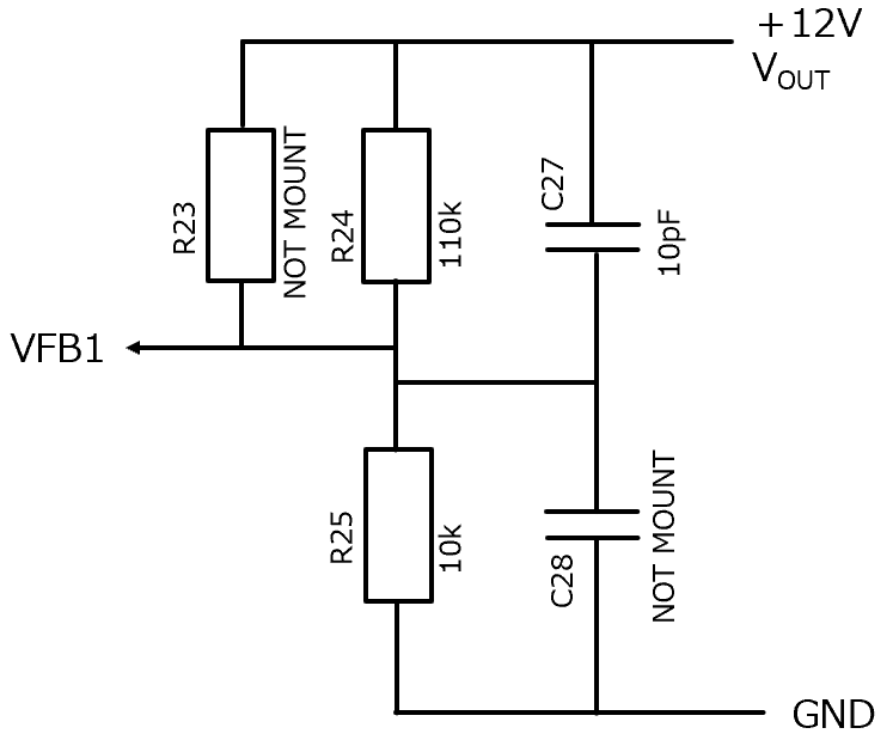
**4.2.4. Output Voltage Setting**

The output-voltage  $V_{OUT}$  of the first-stage is set by the external resistors (R24, R25) shown in Fig. 4.7.

Use the following equation to calculate the  $V_{OUT}$ :

$$V_{OUT} (V) = 1.0(V) \times \left(1.0 + \frac{R24}{R25}\right)$$

In this power supply the output-voltage is set to 12 V. As shown in Fig. 2.5, R24 is selected to be 110 k $\Omega$  and R25 to be 10 k $\Omega$ .



**Fig. 4.7 Output Voltage Setting**

**4.2.5. Current Limiter Circuit**

The first-stage controller has each phase current-sensing signals input terminals Sense1+ (pin48) /Sense1- (pin 1), Sense2+ (pin 13) /Sense2- (pin 12). By detecting the voltage across the inductor, the controller applies the current limit. Set the current limiter level  $I_{limit\_1phase}$  (per phase) with the inductor’s DCR, R18 (R19) located between the Sense1+ (Sense2+) terminal and Sense1- (Sense2-) terminal, and the resistor R21 (R20) from the switching node.

Let’s assume the second-stage efficiency  $\eta$  is 0.80, the maximum output of the first-stage is 144 W. Since the first-stage output is 12 V, the current becomes  $144\text{ W} \div 12\text{ V} = 12\text{ A}$ , and the current limiter for each phase ( $I_{limit\_1phase}$ ) is 8 A (Typ.) in the range of 120 % to 150 % (7.2 A to 9.0 A). Input-voltage  $V_{IN}$  (Typ.) is 50 V, the first-stage voltage  $V_{out(f)}$  is 12 V,  $f_{LTC7810}$  is 100 kHz, L is 22  $\mu\text{H}$ , and DCR is 11.72 m $\Omega$ . The detect voltage  $V_{sense}$  of the controller IC is 75 mV (Typ.).

$$R_{SENSE(EQUIV)} (\Omega) = DCR \times \frac{R18(R19)}{R21(R20) + R18(R19)}$$

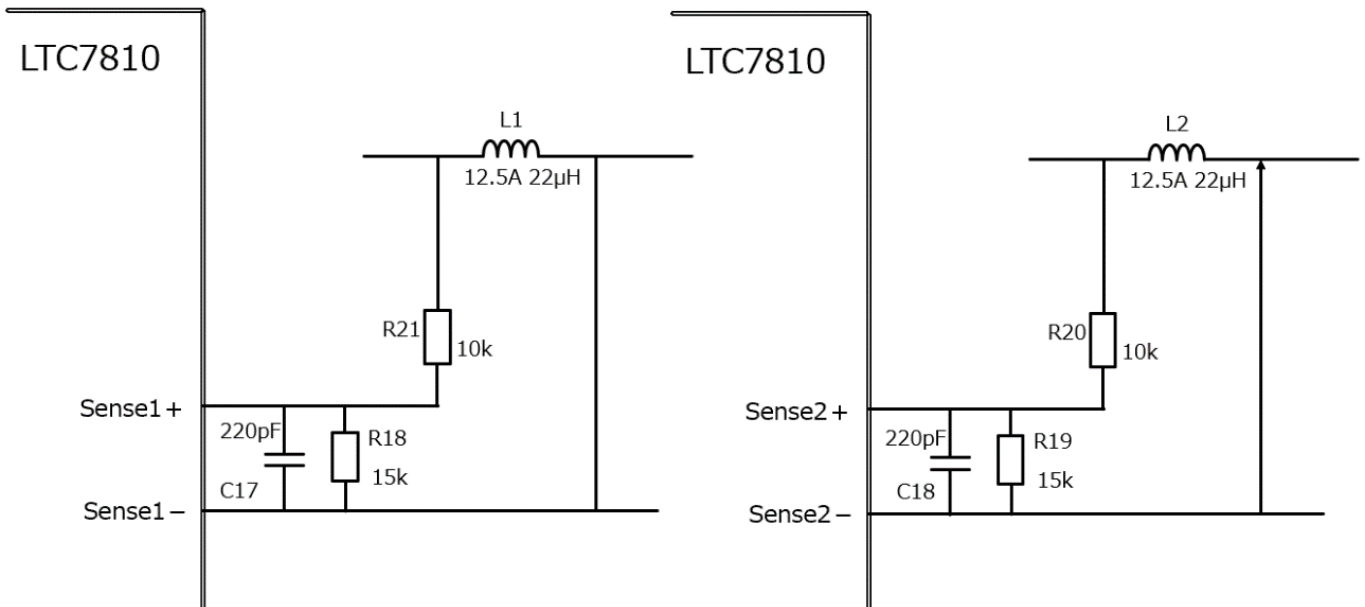
$$\Delta I_{L\_1phase} (A) = \frac{1}{f_{LTC7810} \times L} \times V_{OUT} \times \left(1 - \frac{V_{OUT}}{V_{IN\ typ.}}\right)$$

( $\Delta I_{L\_1phase}$  is the ripple current per 1 phase.)

$$I_{limit\_1phase} (A) = \frac{V_{SENSE}}{R_{SENSE(EQUIV)}} - \frac{\Delta I_{L\phi}}{2}$$

( $I_{limit\_1phase}$  is the current limiter level per 1 phase.)

The current limiter level corresponding to phase 1 is calculated as 8.61 A based on the above equation. Therefore, the total current limiter value for first-stage becomes 17.2 A. As shown in Fig. 4.8, 15 k $\Omega$  is selected for the resistance R18, R19 and 10 k $\Omega$  is selected for the resistance R21, R20.



**Fig. 4.8 Current Limiter Circuit**

**4.2.6. Output Capacitor Settings**

Set the capacitance  $C_{OUT}$  of the output capacitor so that the output ripple  $V_{ripple}$  of the multi-phase circuit is within the required range. The target is 1 % of the +12 V i.e. 120 mV. The ripple voltage is calculated by the generally used equation, which is shown below.

Here  $V_{OUT} = 12\text{ V}$ ,  $L = 22\ \mu\text{H}$ ,  $V_{IN\ typ.} = 50\text{ V}$ ,  $N = 2$ ,  $f_{LTC7810} = 100\text{ kHz}$ . Here,  $N$  in the ripple current calculation formula is the number of phases in the circuit, and the ripple current waveform of the entire multiphase circuit varies depending on the number of phases and the ratio of the input and output voltages (duty).

$$\Delta I_{L\_Nphase} (A) = \frac{1}{f_{LTC7810} \times L} \times V_{OUT} \times \left(1 - \frac{N \times V_{OUT}}{V_{IN\ typ.}}\right)$$

$$V_{ripple} (V) = \Delta I_{L\_Nphase} \times \left(ESR + \frac{1}{8 \times C_{OUT} \times f_{LTC7810}}\right)$$

For  $\Delta I_{L\_Nphase} (A) = 2.84\text{ A}$ ,  $ESR = 3.9\text{ m}\Omega (x2) + 18\text{ m}\Omega (x2) = 1.6\text{ m}\Omega$ ,  $C_{OUT} = 10\ \mu\text{F} \times 2 + 120\ \mu\text{F} \times 2 = 260\ \mu\text{F}$ ,  $f_{LTC7810} = 100\text{ kHz}$ . Consequently, ripple voltage=18.2 mV is calculated.

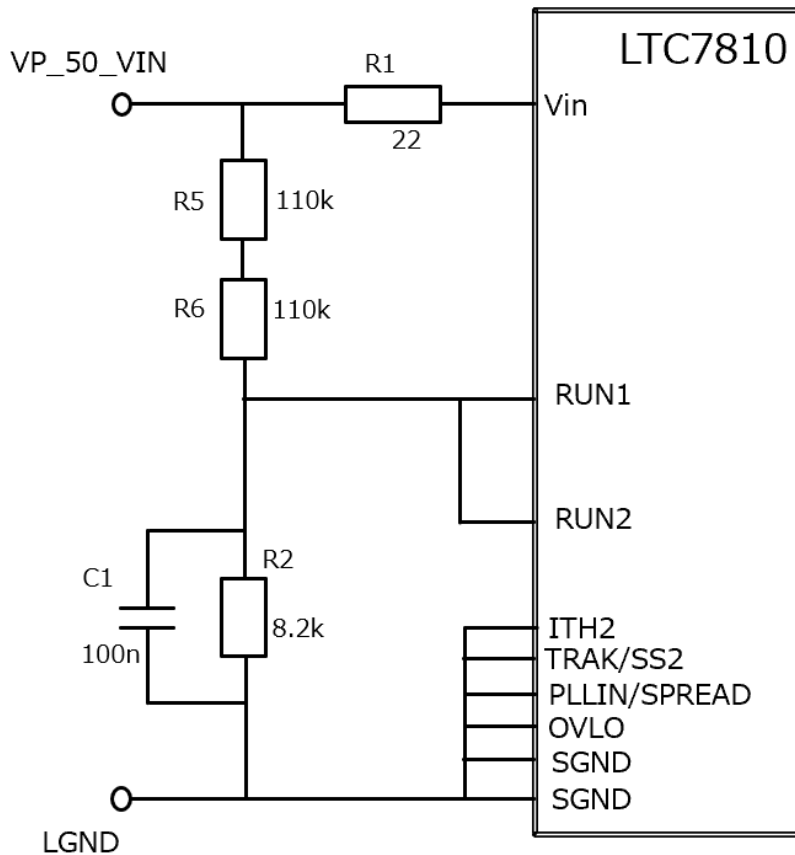


**4.2.7. Operation Start Voltage**

When the terminal voltage of RUN1 (pin 32) exceeds 1.22 V, the first-stage controller starts operation. Adjust R5, R6, and R2 so that RUN1 terminal voltage becomes 1.22 V, and set the operation-start-voltage  $V_{UV}$ . The operation-start-voltage  $V_{UV}$  is calculated by the following equation.

$$V_{UV}(V) = 1.22 (V) \times \left(1 + \frac{(R5 + R6)}{R2}\right)$$

With this power supply, the operation-start-voltage setting target value is set as 34 V, and therefore 110 kΩ is selected as the resistance value for R5 and R6, and 8.2 kΩ is selected as the resistance value for R2, as shown in Fig. 4.9. The calculated value of  $V_{UV}$  becomes 34.0 V.



**Fig. 4.9 Operation Start Voltage Setting**

**4.2.8. Overheat Protection**

The overheat protection function is built into the first-stage controller. It shuts down when the junction temperature of controller exceeds 180 °C and recovers when the junction temperature of controller returns to approximately 160 °C.

### 4.3. Second-Stage Step-Down DC-DC Converter

Fig. 4.10 shows the circuit of the second-stage. This stage is a 5-phase synchronous step-down DC-DC converter. Renesas controller ISL6336D (hereafter, the second-stage controller) is used to generate 1.2 V from the first-stage output of 12 V.

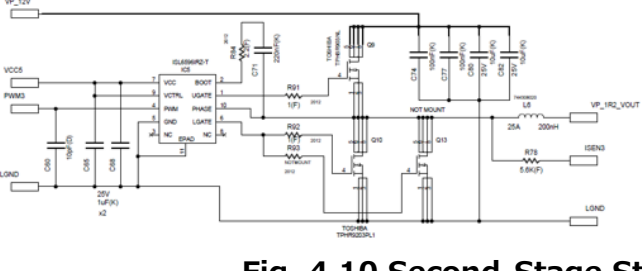
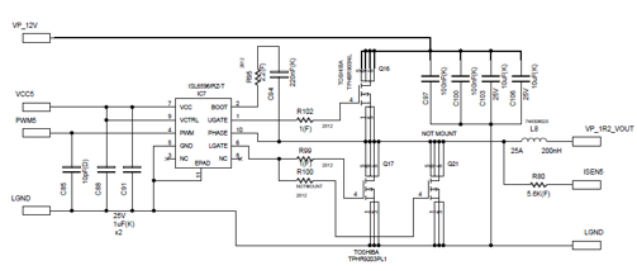
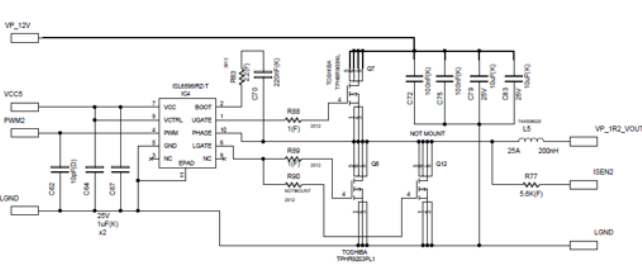
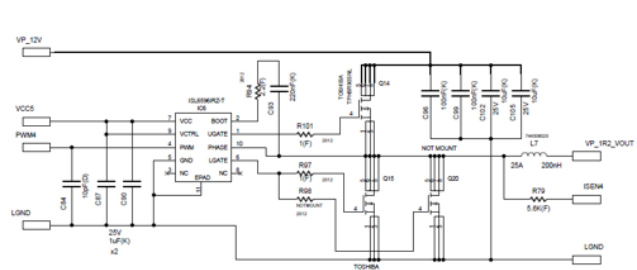
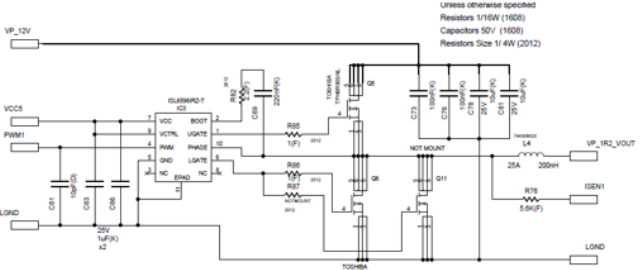
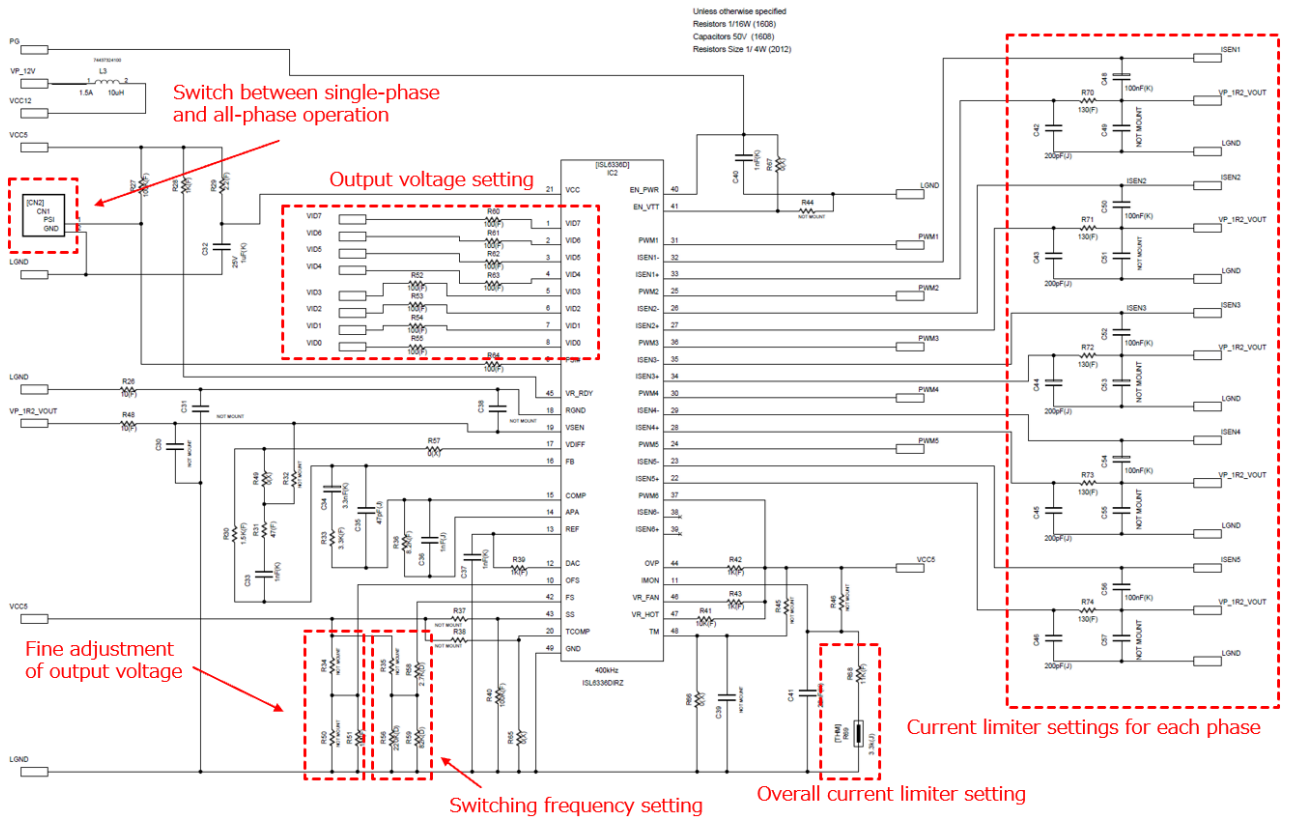


Fig. 4.10 Second-Stage Step-Down DC-DC Converter

4.3.1. Circuit Operation

The second-stage step-down DC-DC converter is a five-phase DC-DC converter. Fig. 4.11 shows the block diagram and the waveform of the switching node voltage for each phase. The circuit has 5-phase, but only 4-phase waveform is displayed for convenience. The frequency of each phase is operating at approximately 400 kHz as can be seen from the wave form. Each phase operates with the phase shift of 72 degrees.

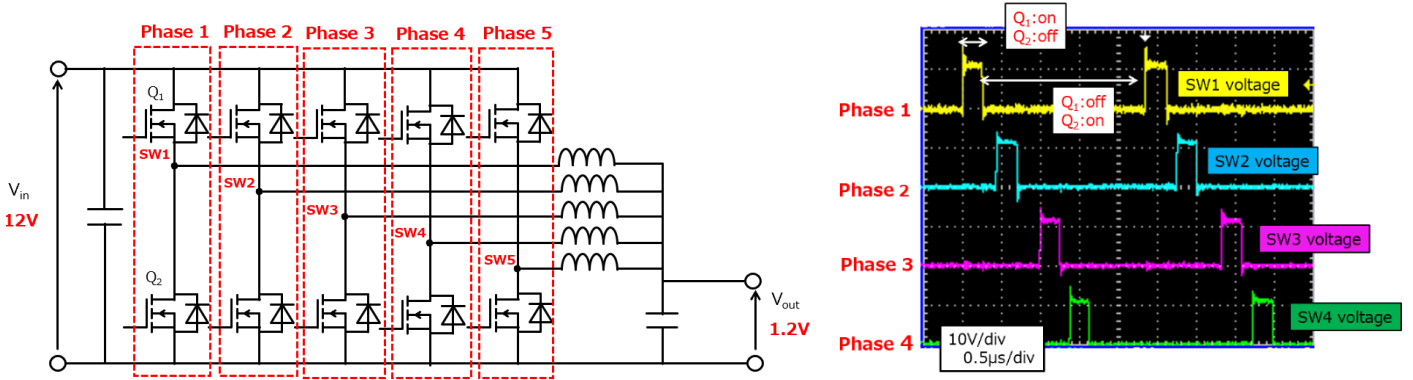


Fig. 4.11 Second-Stage Block Diagram and Switch Node Waveforms for Each Phase

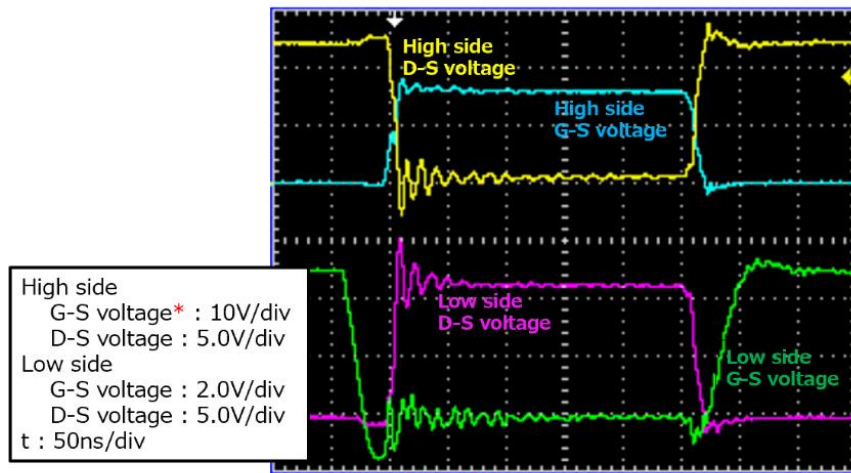
The output voltage is 1.2 V, the switching frequency of MOSFET is 400 kHz, and one cycle is 2.5 µs. The input and output voltage have the following relationship.

$$V_{OUT} = DV_{IN}$$

The on-duty of the high-side MOSFET must be 0.1 and the on-time of the high-side MOSFET must be 0.25 µs in order for the input voltage to be 12 V and the output voltage to be 1.2 V. Fig. 4.12 shows the high-side and low-side MOSFET gate-to-source voltage waveforms during the high-side MOSFET on-period.

**Input voltage : 12 V**  
 (Output voltage : 1.2 V)

1 cycle : 2.5µs (f=400kHz)  
 High side MOSFET on time : 0.25µs  
 High side MOSFET on duty : 0.1



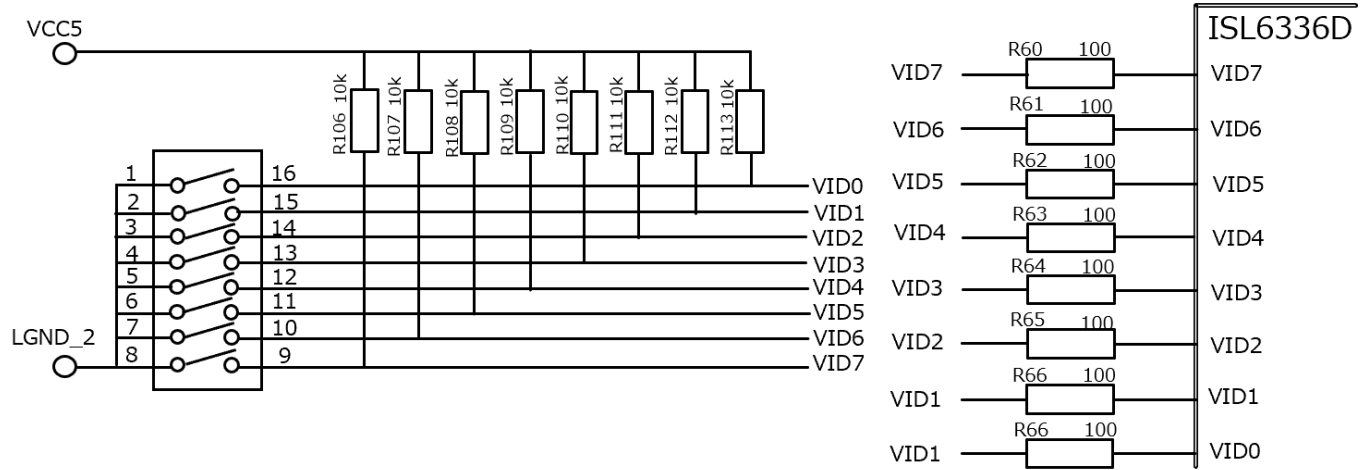
\* High side gate-source voltage is measured between gate and circuit GND instead of between gate and source.

Fig. 4.12 MOSFET Switching Waveforms of Second-Stage Circuit

**4.3.2. Output Voltage Setting**

Generates a reference voltage based on the status of VID0 to VID7 terminals (pin 8 to Pin 1) of the second-stage controller. Fig. 4.13 shows the voltage setting circuit. 0.5 V to 1.6 V can be set in 6.25 mV increments by a combination of high or low. All VID pins do not have an internal pull-up current source, so a R106 to R113 pull-up resistor is connected from VCC (5 V). The DIP-switch S1 on the board sets VID0 to VID7 parameters.

This power supply has 1.20000 V setting: VID0: Low, VID1: High, VID2 to 5: Low, VID6: High, VID7: Low.



**Fig. 4.13 Output Voltage Setting Circuit**

### 4.3.3. Switching Frequency Setting

The switching frequency ( $f_{ISL6336}$ ) is set by FS terminal (pin 42) of the second-stage controller and the resistance  $R_T$  (R56, R58, R59 connected to GND or  $V_{CC}$ ). For the combined resistance of  $R_T$  is:

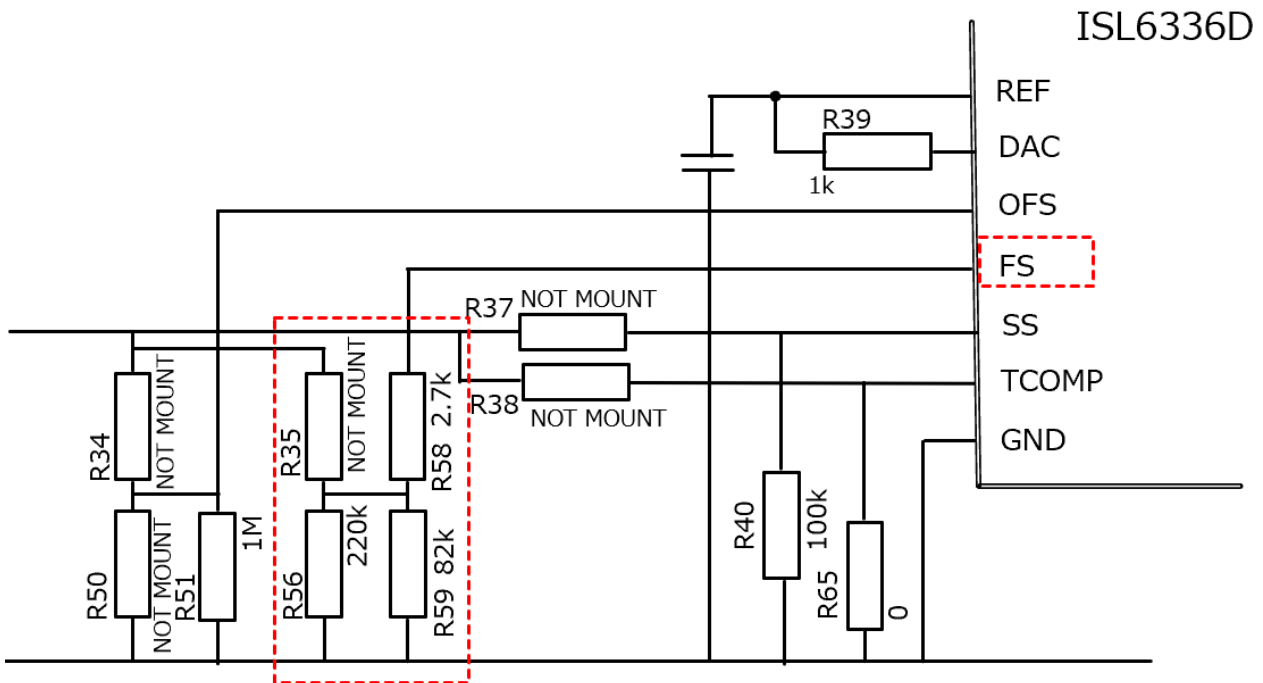
$$R_T(\Omega) = R58 + \frac{R56 \times R59}{R56 + R59}$$

Setting R58 to 2.7 k $\Omega$ , R56 to 220 k $\Omega$ , and R59 to 82 k $\Omega$ , makes  $R_T = 62.4$  k $\Omega$ .

$f_{ISL6336}$  is calculated by the following equation.

$$f_{ISL6336}(Hz) = \frac{2.5 \times 10^{10}}{R_T}$$

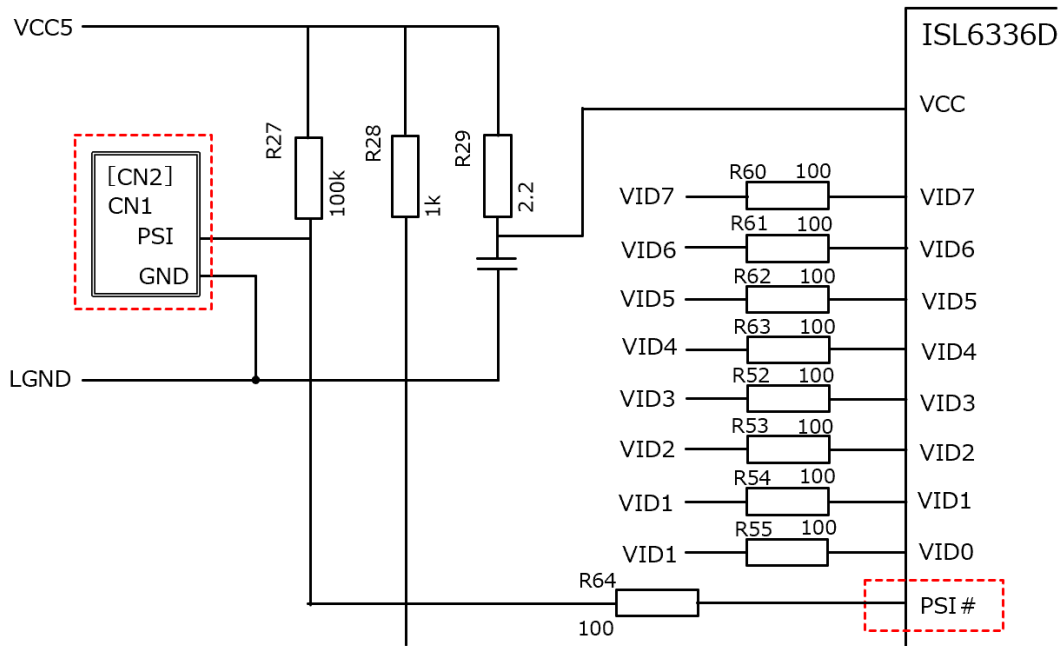
Setting  $R_T$  to 62.4 k $\Omega$  and makes ( $f_{ISL6336}$ ) to be 400.4 kHz.



**Fig. 4.14 Switching Frequency Setting Circuit**

**4.3.4. Switch Between Single-Phase Operation and Full-Phase Operation**

The second-stage circuit can be switched between single-phase operation and full-phase operation by input signal of PSI# (pin 9) terminal. Shorting both pins (PSI and GND) of the 2-pin connector CN1 mounted on the board results in single-phase operation. Single-phase operation only works on converter circuit connected to a PWM1 (pin 31) terminal. Leaving both pins of CN1 connector (PSI and GND) open will make the second-stage controller operates all connected 5-phase circuits.



**Fig. 4.15 Single-Phase or Full-phase Operation Switch Circuit**

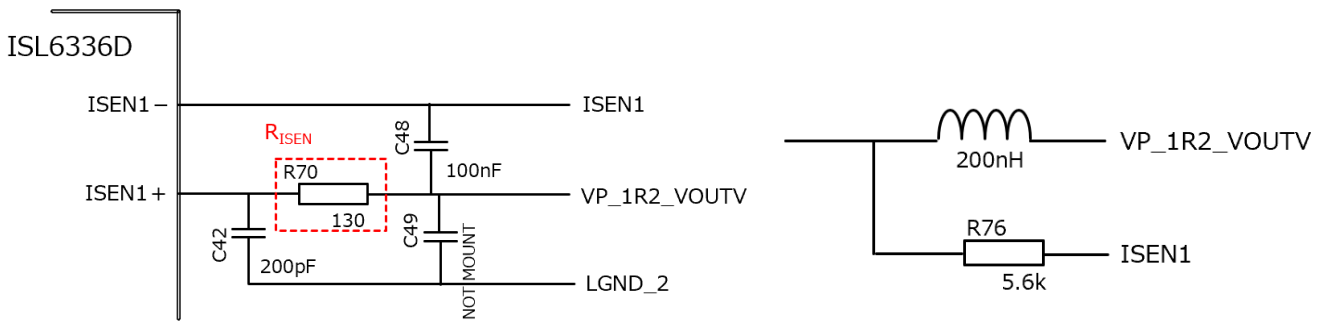
**4.3.5. Current Limiter of Each Phase**

Each phase of the second-stage controller has current-sensing signals input terminals ISEn+/ISEn- (n:1 to 6). By detecting the voltage across the inductor, the controller applies the current limit.

Let’s consider the phase 1 (PWM1) as the example. The limiter level  $I_{limit1\_1phase}$  of phase 1 is set using DCR of the inductor and resistance value of R70 which is connected between ISEN1+ (pin 33) and the output voltage, and the current sense level  $I_{SEN}$  of the controller i.e. 105  $\mu$ A. DCR is 0.37 m $\Omega$ .

$$I_{limit\_1phase} (A) = I_{SEN} \times R_{ISEN} \times \frac{1}{DCR}$$

From the equation above, the current limiter level corresponding to each phase is calculated to be 36.9 A. Since this specification has a maximum 100 A for 5 phases, it is equivalent to 20 A for each phase and the calculated value is around 185 %. However, considering the variation in DCR and the variation in the current balance, the value is selected.



**Fig. 4.16 Current Limiter Setting for Each Phase**

**4.3.6. Current Limiter for the Entire Output**

IMON terminal (Pin 11) of the second-stage controller allows the user to limit the total current of each phase. The current flowing out of IMON is equal to the mean current of the detected current  $I_{SEN}$ . The detected current is given by the following equation.

$$I_{SEN} = I_L \times \frac{DCR}{R_{ISEN}}$$

IMON terminal voltage  $V_{IMON}$  is proportional to the total resistance value of R68 and R69 and  $I_{SEN}$ .

$$V_{IMON} = (R68 + R69) \times I_{SEN}$$

Assigning  $I_{SEN}$  in the above equation yields the following equation:

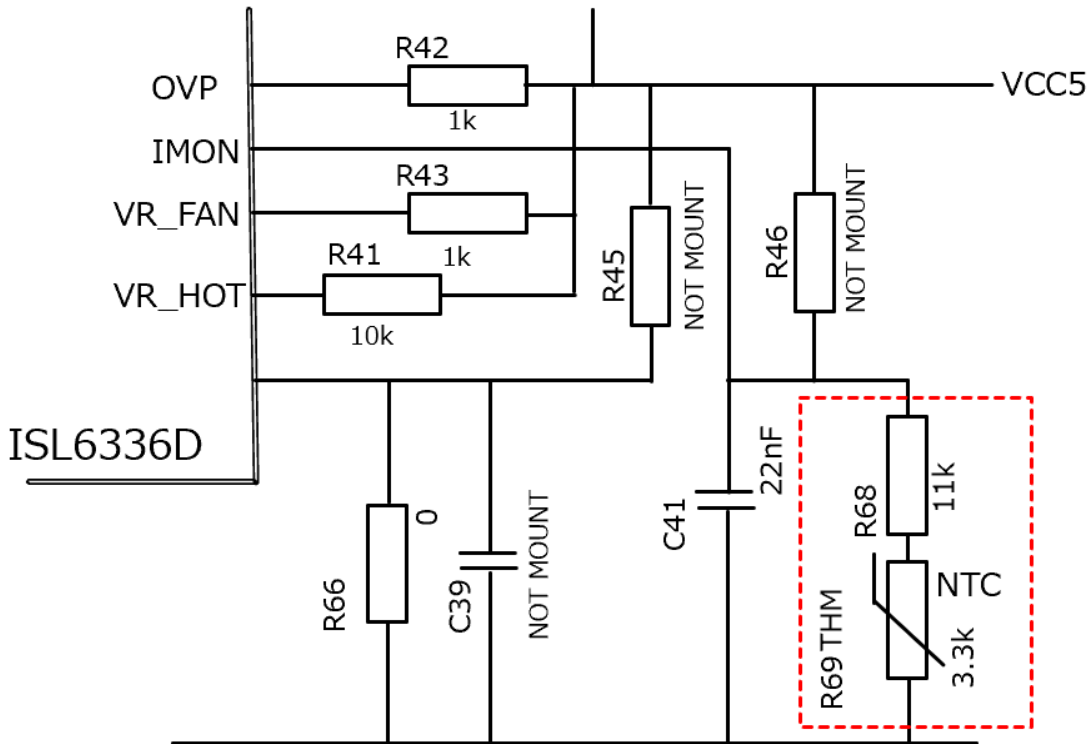
$$V_{IMON} = (R68 + R69) \times I_L \times \frac{DCR}{R_{ISEN}}$$

$$I_L = \frac{IMON \times R_{ISEN}}{(R68 + R69) \times DCR}$$

The current limiter level  $I_{limit}$  (A) of the entire  $I_L$  of N phases is set using DCR of the Inductor,  $R_{ISEN}$  (R70) in the first-stage, and the resistors (R68, R69) between IMON and GND. Controller detection voltage  $V_{IMON}$  is 1.11 V (Typ.). N is 5 for the number of phases. DCR is 0.37 mΩ.

$$I_{limit}(A) = \frac{IMON \times N \times R_{ISEN}}{(R68 + R69) \times DCR}$$

The total current limiter level is calculated as 135 A using the above equation, when 11 kΩ is selected for the resistor R68 and 3.3 kΩ is selected for R69 as shown in Fig. 4.17.



**Fig. 4.17 Overall Current Limiter Setting**



### 4.3.7. Output Capacitor Setting

Set the capacitance  $C_{out}$  of the output capacitor so that the output-voltage ripple  $V_{ripple}$  is within the required range. Required spec is less than 20 mV at + 1.2 V power. It is also assumed to operate in one phase when the load is light. Since the ripple voltage at one phase is larger than that at five phases, the ripple voltage at one phase is considered as follows.

The ripple current  $\Delta I_L$  is as follows when the phase number  $N$  is considered in the equation.

$$\Delta I_L = \frac{(V_{IN} - N \times V_{OUT}) \times V_{OUT}}{V_{IN} \times L \times f_{SW}}$$

Ripple voltage is calculated by multiplying ripple current by ESR using the following equation.

$$\Delta I_L = \frac{(V_{IN} - N \times V_{OUT}) \times V_{OUT}}{V_{IN} \times L \times f_{SW}}$$

ESR consist of 42 MLCC (Multi-Layer Ceramic Capacitor) of 3 m $\Omega$  and 5 conductive polymer aluminum electrolytic capacitors of 8 m $\Omega$  with a combined resistor of 1.3 m $\Omega$  and  $V_{in} = 12$  V,  $N = 1$  (1-phase operation),  $V_{out} = 1.2$  V,  $f_{ISL6336} = 400$  kHz,  $L = 200$  nH.

The resulting ripple-voltage is calculated to be 17.6 mV.

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