32-bit RISC Microcontroller

TXZ+ Family
TMPM4M Group(1)

Reference Manual
Product Information
(PINFO-M4M(1))

Revision 1.1

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Toshiba Electronic Devices & Storage Corporation

Contents

List of Figures

List of Tables

Preface

Related documents

Document name	IP Symbol
Input/Output Ports	PORT-M4M(1)
Exception	EXCEPT-M4M(1)
Clock Control and Operation Mode	CG-M4M(1)-E
DMA controller	DMAC-B
32-bit Timer Event Counter	T32A-C
Asynchronous Serial Communication Circuit	UART-C
Serial Peripheral Interface	TSPI-E
I^2C interface	I2C-B
I^2C interface Version A	EI2C-A
12-bit Analog to Digital Converter	ADC-I
CAN Controller	CAN-B
Operational Amplifier	OPAMP-B
Advanced Programmable Motor Control Circuit	A-PMD-A
Advanced Encoder Input Circuit (32bit)	A-ENC32-A
Advanced Vector Engine Plus	A-VE+-B
Clock Selective Watchdog Timer	SIWDT-A
Oscillation Frequency Detector	OFD-A
Debug Interface	DEBUG-A
Non Break Debug Interface	NBDIF-A
Digital Noise Filter Circuit	DNF-A
Trimming Circuit	TRM-B
Voltage Detection Circuit	LVD-D
CRC Calculation Circuit	CRC-A
RAM Parity	RAMP-B
Flash Memory	FLASH512UD32-B

Conventions

- Numeric formats follow the rules as shown below:
  Hexadecimal: 0xABC
  Decimal: 123 or 0d123 - Only when it needs to be explicitly shown that they are decimal numbers.
  Binary: 0b111 - It is possible to omit the "0b" when the number of bits can be distinctly understood from a sentence.
- "_N" is added to the end of signal names to indicate low active signals.
- It is called "assert" that a signal moves to its active level, "deassert" to its inactive level.
- When two or more signal names are referred, they are described like as [m:n].
  Example: S[3:0] shows four signal names S3, S2, S1 and S0 together.
- The characters surrounded by ***[ ]*** defines the register.
  Example: ***[ABCD]***
- "N" substitutes suffix number of two or more same kind of registers, fields, and bit names.
  Example: ***[XYZ1]***, ***[XYZ2]***, ***[XYZ3]*** → ***[XYZn]***
- "x" substitutes suffix number or character of units and channels in the register list.
- In case of unit, "x" means A, B, and C, ...
  Example: ***[ADACR0]***, ***[ADBCR0]***, ***[ADCCR0]*** → ***[ADxCR0]***
- In case of channel, "x" means 0, 1, and 2, ...
  Example: ***[T32A0RUNA]***, ***[T32A1RUNA]***, ***[T32A2RUNA]*** → ***[T32AxRUNA]***
- The bit range of a register is written like as [m: n].
  Example: Bit[3: 0] expresses the range of bit 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.
  Example: ***[ABCD]***<EFG> = 0x01 (hexadecimal), ***[XYZn]***<VW> = 1 (binary)
- Word and byte represent the following bit length.
  Byte: 8 bits
  Half word: 16 bits
  Word: 32 bits
  Double word: 64 bits
- Properties of each bit in a register are expressed as follows:
  R: Read only
  W: Write only
  R/W: Read and write are possible.
- Unless otherwise specified, register access supports only word access.
- The register defined as "Reserved" must not be rewritten. Moreover, do not use the read value.
- The value read from the bit having default value of "-" is unknown.
- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value, In the cases that default is "-", follow the definition of each register.
- Reserved bits of the write-only register should be written with their default value. In the cases that default is "-", follow the definition of each register.
- Do not use read-modified-write processing to the register of a definition which is different by writing and read out.

Terms and Abbreviations

Some of abbreviations used in this document are as follows:

ADC	Analog to Digital Converter
A-ENC32	Advanced Encoder input Circuit(32-bit)
A-PMD	Advanced Programmable Motor Control Circuit
A-VE+	Advanced Vector Engine Plus
CAN	Controller Area Network
CRC	Cyclic Redundancy Check
DMAC	Direct Memory Access Controller
DNF	Digital Noise Filter
EHOSC	External High-Speed Oscillator
EI2C	I^2C Interface Version A
IHOSC	Internal High-Speed Oscillator
INT	Interrupt
I2C	Inter-Integrated Circuit
LVD	Voltage Detection Circuit
NBDIF	Non Break Debug Interface
NMI	Non-Maskable Interrupt
OFD	Oscillation Frequency Detector
OPAMP	Operational Amplifier
RAMP	RAM Parity
SIWDT	Clock Selective Watchdog Timer
TRGSEL	Trigger Selection Circuit
TRM	Trimming Circuit
TSPI	Serial Peripheral Interface
T32A	32-bit Timer Event Counter
UART	Asynchronous Serial Communication Circuit

1. Overview

This chapter describes number of channels or units, information of pins and product-specific function information related to peripheral functions. Use this chapter in conjunction with Reference Manual for Peripheral Function.

2. Information of Peripheral Function

2.1. Register Base address

The following table shows the type of base address of each peripheral.

Table 2.1 Type of Register base address (1/2)

Peripheral function			Type of Base Address (✓: Applicable, -: N/A)			Base Address
			TYPE1	TYPE2	TYPE3	
CAN Controller	CAN	Unit A	✓	-	-	0x40005000
Voltage Detection Circuit	LVD	-	✓	-	-	0x4003EC00
RAM Parity	RAMP	ch 0	-	-	✓	0x40043000
		ch 1	-	✓	-	0x400A3000
CRC calculation circuit	CRC	-	-	-	✓	0x40043100
Digital Noise Filter Circuit	DNF	unit A	-	✓	-	0x400A0200
		unit B				0x400A0300
		unit C				0x400A0800
Clock Selective Watchdog Timer	SIWDT	ch 0	-	✓	-	0x400A0600
Non Break Debug Interface	NBDIF	-	-	✓	-	0x400A2000
Direct Memory Access Controller	DMAC	unit A	-	✓	-	0x400A4000
12-bit Analog to Digital Converter	ADC	unit A	-	✓	-	0x400BA000
		unit B				0x400BA400
		unit C				0x400BA800
Operational Amplifier	OPAMP	-	-	✓	-	0x400BD000
32-bit Timer Event Counter	T32A	ch 0	-	✓	-	0x400C1000
		ch 1				0x400C1400
		ch 2				0x400C1800
		ch 3				0x400C1C00
		ch 4				0x400C2000
		ch 5				0x400C2400
Serial Peripheral Interface	TSPI	ch 0	-	✓	-	0x400CA000
		ch 1				0x400CA400
Universal Asynchronous Receiver Transmitter Circuit	UART	ch 0	-	✓	-	0x400CE000
		ch 1				0x400CE400
		ch 2				0x400CE800
		ch 3				0x400CEC00
I^2C interface	I2C	ch 0	-	✓	-	0x400D1000
		ch 1				0x400D2000

Table 2.2 Type of Register base address (2/2)

Peripheral function			Type of Base Address (✓: Applicable, -: N/A)			Start Address
			TYPE1	TYPE2	TYPE3	
I^2C interface version A	EI2C	ch 0	-	✓	-	0x400D8000
		ch 1				0x400D9000
Trimming Circuit	TRM	-	-	✓	-	0x400E3100
Oscillation Frequency Detector	OFD	-	-	✓	-	0x400E4000
Advanced Programmable Motor Control Circuit	A-PMD	ch 0	-	✓	-	0x400E9000
		ch 1				0x400E9400
		ch 2				0x400E9800
Advanced Encoder Input Circuit (32-bit)	A-ENC32	ch 0	-	✓	-	0x400EA000
		ch 1				0x400EA400
		ch 2				0x400EA800
Advanced Vector Engine Plus	A-VE+	ch 0	-	✓	-	0x400EB000
Flash Memory	Flash	-	✓	-	-	0x5DFF0000

To develop each peripheral function, please refer to the above type of base address.

2.2. Trigger Selector (TRGSEL)

The trigger selector is the circuit which chooses the one trigger and outputs the trigger signal to the peripheral function from two or more triggers inputted from the peripheral function, the port, etc.

The trigger chosen from eight triggers by ***[TSEL0CRn]***<INSELm> is outputted to the peripheral function of a connection destination.

"Figure 2.1 Example of Trigger Selector Connection" is the example of the trigger signal which is input from port terminals (PA2, PA3, PA4) or timer register (A1, B1, C1) match trigger output of the 32-bit timer event counter (channel 5) and is connected to UART (channel 3) via the trigger selector. The setup of input trigger selection, edge detection condition selection, trigger output selection, and trigger output control is performed by ***[TSEL0CR6]***.

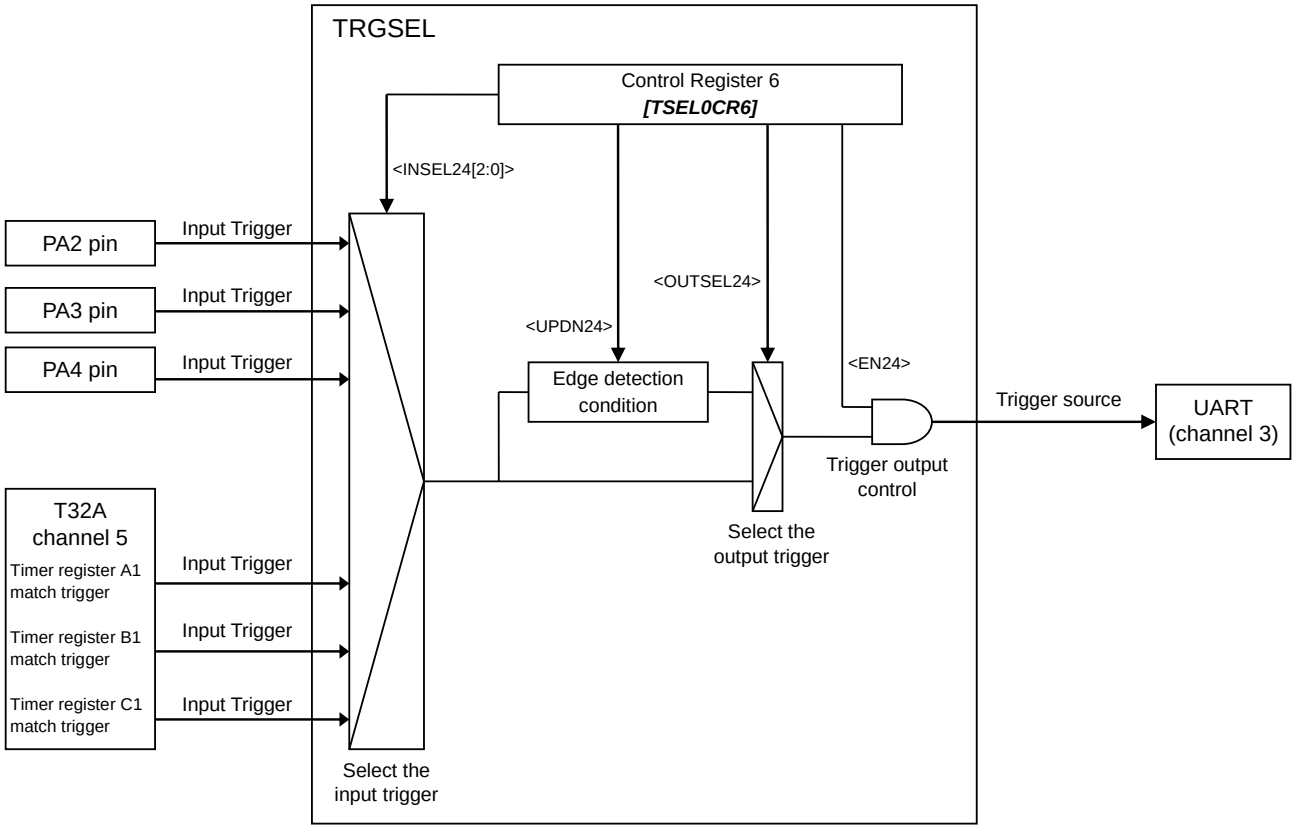

Figure 2.1 Example of Trigger Selector Connection

2.2.1. Trigger Selector List for the each Products

Trigger selector of TMPM4M Group(1) consist of 11 control registers(***[TSEL0CR0 to 10]***), and 43 triggers are controlled.

The following table shows "Trigger Selector List of each Product".

Table 2.3 Trigger Selector List for each Product (1/6)

Register		Trigger unit	Trigger Source	Product (✓: Available, -: N/A)		
	Bit Symbol			M4MN	M4MM	M4ML
[TSEL0CR0]	INSEL0	DMA ch16	ADC unit A general purpose trigger DMA request ADC unit A single conversion DMA request ADC unit A continuous conversion DMA request	✓	✓	✓
	INSEL1	DMA ch17	ADC unit B general purpose trigger DMA request ADC unit B single conversion DMA request ADC unit B continuous conversion DMA request	✓	✓	✓
	INSEL2	DMA ch18	ADC unit C general purpose trigger DMA request ADC unit C single conversion DMA request ADC unit C continuous conversion DMA request	✓	✓	✓
	INSEL3	DMA ch19	T32A ch0 DMA request at match A1 register T32A ch0 DMA request at match C1 register T32A ch1 DMA request at match A1 register T32A ch1 DMA request at match C1 register A-PMD ch0 PWM interrupt	✓	✓	✓
[TSEL0CR1]	INSEL4	DMA ch20	T32A ch2 DMA request at match A1 register T32A ch2 DMA request at match C1 register T32A ch3 DMA request at match A1 register T32A ch3 DMA request at match C1 register A-PMD ch1 PWM interrupt	✓	✓	✓
	INSEL5	DMA ch21	T32A ch4 DMA request at match A1 register T32A ch4 DMA request at match C1 register T32A ch5 DMA request at match A1 register T32A ch5 DMA request at match C1 register A-PMD ch2 PWM interrupt	✓	✓	✓
	INSEL6	DMA ch22	T32A ch0 DMA request at match B1 register T32A ch1 DMA request at match B1 register T32A ch2 DMA request at match B1 register T32A ch3 DMA request at match B1 register T32A ch4 DMA request at match B1 register T32A ch5 DMA request at match B1 register	✓	✓	✓
	INSEL7	DMA ch23	T32A ch0 DMA request at capture A0 register T32A ch0 DMA request at capture A1 register T32A ch1 DMA request at capture A0 register T32A ch1 DMA request at capture A1 register T32A ch0 DMA request at capture C0 register T32A ch0 DMA request at capture C1 register T32A ch1 DMA request at capture C0 register T32A ch1 DMA request at capture C1 register	✓	✓	✓

Table 2.4 Trigger Selector List for each Product (2/6)

Register		Trigger unit	Trigger Source	Product (✓: Available, -: N/A)		
	Bit Symbol			M4MN	M4MM	M4ML
[TSEL0CR2]	INSEL8	DMA ch24	T32A ch2 DMA request at capture A0 register T32A ch2 DMA request at capture A1 register T32A ch3 DMA request at capture A0 register T32A ch3 DMA request at capture A1 register T32A ch2 DMA request at capture C0 register T32A ch2 DMA request at capture C1 register T32A ch3 DMA request at capture C0 register T32A ch3 DMA request at capture C1 register	✓	✓	✓
	INSEL9	DMA ch25	T32A ch4 DMA request at capture A0 register T32A ch4 DMA request at capture A1 register T32A ch5 DMA request at capture A0 register T32A ch5 DMA request at capture A1 register T32A ch4 DMA request at capture C0 register T32A ch4 DMA request at capture C1 register T32A ch5 DMA request at capture C0 register T32A ch5 DMA request at capture C1 register	✓	✓	✓
	INSEL10	DMA ch26	T32A ch0 DMA request at capture B0 register T32A ch0 DMA request at capture B1 register T32A ch1 DMA request at capture B0 register T32A ch1 DMA request at capture B1 register T32A ch2 DMA request at capture B0 register T32A ch2 DMA request at capture B1 register	✓	✓	✓
	INSEL11	DMA ch27	T32A ch3 DMA request at capture B0 register T32A ch3 DMA request at capture B1 register T32A ch4 DMA request at capture B0 register T32A ch4 DMA request at capture B1 register T32A ch5 DMA request at capture B0 register T32A ch5 DMA request at capture B1 register	✓	✓	✓
[TSEL0CR3]	INSEL12	DMA ch28	DMAC ch0 transfer completion DMAC ch1 transfer completion DMAC ch8 transfer completion DMAC ch9 transfer completion DMAC ch16 transfer completion DMAC ch17 transfer completion DMAC ch22 transfer completion	✓	✓	✓
	INSEL13	DMA ch29	DMAC ch2 transfer completion DMAC ch3 transfer completion DMAC ch10 transfer completion DMAC ch11 transfer completion DMAC ch18 transfer completion DMAC ch19 transfer completion DMAC ch23 transfer completion	✓	✓	✓
			PA2 (TRGIN0)	✓	✓	✓
	INSEL14	DMA ch30	DMAC ch4 transfer completion DMAC ch5 transfer completion DMAC ch12 transfer completion DMAC ch13 transfer completion DMAC ch20 transfer completion DMAC ch24 transfer completion DMAC ch26 transfer completion	✓	✓	✓
			PA3 (TRGIN1)	✓	✓	✓
	INSEL15	DMA ch31	DMAC ch6 transfer completion DMAC ch7 transfer completion DMAC ch14 transfer completion DMAC ch15 transfer completion DMAC ch21 transfer completion DMAC ch25 transfer completion DMAC ch27 transfer completion	✓	✓	✓
			PA4 (TRGIN2)	✓	✓	✓

Table 2.5 Trigger Selector List for each Product (3/6)

Register		Trigger unit	Trigger Source	Product (✓: Available, -: N/A)		
	Bit Symbol			M4MN	M4MM	M4ML
[TSEL0CR4]	INSEL16	ADC unit A	PA2 (TRGIN0)	✓	✓	✓
			PA3 (TRGIN1)	✓	✓	✓
			PA4 (TRGIN2)	✓	✓	✓
			T32A ch1 Timer register A1 match trigger T32A ch1 Timer register B1 match trigger T32A ch1 Timer register C1 match trigger	✓	✓	✓
	INSEL17	ADC unit B	PA2 (TRGIN0)	✓	✓	✓
			PA3 (TRGIN1)	✓	✓	✓
			PA4 (TRGIN2)	✓	✓	✓
			T32A ch3 Timer register A1 match trigger T32A ch3 Timer register B1 match trigger T32A ch3 Timer register C1 match trigger	✓	✓	✓
	INSEL18	ADC unit C	PA2 (TRGIN0)	✓	✓	✓
			PA3 (TRGIN1)	✓	✓	✓
			PA4 (TRGIN2)	✓	✓	✓
			T32A ch5 Timer register A1 match trigger T32A ch5 Timer register B1 match trigger T32A ch5 Timer register C1 match trigger	✓	✓	✓
	INSEL19	TSPI ch0	PA2 (TRGIN0)	✓	✓	✓
			PA3 (TRGIN1)	✓	✓	✓
			PA4 (TRGIN2)	✓	✓	✓
			T32A ch5 Timer register A1 match trigger T32A ch5 Timer register B1 match trigger T32A ch5 Timer register C1 match trigger	✓	✓	✓
[TSEL0CR5]	INSEL20	TSPI ch1	PA2 (TRGIN0)	✓	✓	✓
			PA3 (TRGIN1)	✓	✓	✓
			PA4 (TRGIN2)	✓	✓	✓
			T32A ch5 Timer register A1 match trigger T32A ch5 Timer register B1 match trigger T32A ch5 Timer register C1 match trigger	✓	✓	✓
	INSEL21	UART ch0	PA2 (TRGIN0)	✓	✓	✓
			PA3 (TRGIN1)	✓	✓	✓
			PA4 (TRGIN2)	✓	✓	✓
			T32A ch5 Timer register A1 match trigger T32A ch5 Timer register B1 match trigger T32A ch5 Timer register C1 match trigger	✓	✓	✓
	INSEL22	UART ch1	PA2 (TRGIN0)	✓	✓	✓
			PA3 (TRGIN1)	✓	✓	✓
			PA4 (TRGIN2)	✓	✓	✓
			T32A ch5 Timer register A1 match trigger T32A ch5 Timer register B1 match trigger T32A ch5 Timer register C1 match trigger	✓	✓	✓
	INSEL23	UART ch2	PA2 (TRGIN0)	✓	✓	✓
			PA3 (TRGIN1)	✓	✓	✓
			PA4 (TRGIN2)	✓	✓	✓
			T32A ch5 Timer register A1 match trigger T32A ch5 Timer register B1 match trigger T32A ch5 Timer register C1 match trigger	✓	✓	✓

Table 2.6 Trigger Selector List for each Product (4/6)

Register		Trigger unit	Trigger Source	Product (✓: Available, -: N/A)		
	Bit Symbol			M4MN	M4MM	M4ML
[TSEL0CR6]	INSEL24	UART ch3	PA2 (TRGIN0)	✓	✓	-
			PA3 (TRGIN1)	✓	✓	-
			PA4 (TRGIN2)	✓	✓	-
			T32A ch5 Timer register A1 match trigger T32A ch5 Timer register B1 match trigger T32A ch5 Timer register C1 match trigger	✓	✓	-
	INSEL25	T32A ch0 Timer A	PA2 (TRGIN0)	✓	✓	✓
			PA3 (TRGIN1)	✓	✓	✓
			PA4 (TRGIN2)	✓	✓	✓
			UART ch0 transmission completion trigger UART ch0 reception completion trigger TSPI ch0 transmit completion trigger TSPI ch0 receive completion trigger	✓	✓	✓
			I2C ch0 interrupt EI2C ch0 status interrupt	✓	✓	✓
	INSEL26	T32A ch0 Timer B	T32A ch0 Timer register A0 match trigger T32A ch0 Timer register A1 match trigger T32A ch0 Timer A overflow trigger T32A ch0 Timer A underflow trigger	✓	✓	✓
	INSEL27	T32A ch0 Timer C	T32A ch5 Timer register C0 match trigger T32A ch5 Timer register C1 match trigger T32A ch5 Timer C overflow trigger T32A ch5 Timer C underflow trigger	✓	✓	✓
[TSEL0CR7]	INSEL28	T32A ch1 Timer A	PA2 (TRGIN0)	✓	✓	✓
			PA3 (TRGIN1)	✓	✓	✓
			PA4 (TRGIN2)	✓	✓	✓
			UART ch1 transmission completion trigger UART ch1 reception completion trigger TSPI ch1 transmit completion trigger TSPI ch1 receive completion trigger	✓	✓	✓
			A-ENC32 ch0 divided pulse signal (TIMPLS)	✓	✓	-
	INSEL29	T32A ch1 Timer B	T32A ch1 Timer register A0 match trigger T32A ch1 Timer register A1 match trigger T32A ch1 Timer A overflow trigger T32A ch1 Timer A underflow trigger	✓	✓	✓
	INSEL30	T32A ch1 Timer C	T32A ch0 Timer register C0 match trigger T32A ch0 Timer register C1 match trigger T32A ch0 Timer C overflow trigger T32A ch0 Timer C underflow trigger	✓	✓	✓
	INSEL31	T32A ch2 Timer A	PA2 (TRGIN0)	✓	✓	✓
			PA3 (TRGIN1)	✓	✓	✓
			PA4 (TRGIN2)	✓	✓	✓
			UART ch2 transmission completion trigger UART ch2 reception completion trigger	✓	✓	✓
			A-ENC32 ch1 divided pulse signal (TIMPLS)	✓	✓	-
			I2C ch1 interrupt EI2C ch1 status interrupt	✓	✓	✓

Table 2.7 Trigger Selector List for each Product (5/6)

Register		Trigger unit	Trigger Source	Product (✓: Available, -: N/A)		
	Bit Symbol			M4MN	M4MM	M4ML
[TSEL0CR8]	INSEL32	T32A ch2 Timer B	T32A ch2 Timer register A0 match trigger T32A ch2 Timer register A1 match trigger T32A ch2 Timer A overflow trigger T32A ch2 Timer A underflow trigger	✓	✓	✓
	INSEL33	T32A ch2 Timer C	T32A ch1 Timer register C0 match trigger T32A ch1 Timer register C1 match trigger T32A ch1 Timer C overflow trigger T32A ch1 Timer C underflow trigger	✓	✓	✓
	INSEL34	T32A ch3 Timer A	PA2 (TRGIN0)	✓	✓	✓
			PA3 (TRGIN1)	✓	✓	✓
			PA4 (TRGIN2)	✓	✓	✓
			UART ch3 transmission completion trigger UART ch3 reception completion trigger	✓	✓	-
			ADC unit C general purpose trigger interrupt ADC unit C single conversion interrupt ADC unit C continuous conversion interrupt	✓	✓	✓
	INSEL35	T32A ch3 Timer B	T32A ch3 Timer register A0 match trigger T32A ch3 Timer register A1 match trigger T32A ch3 overflow A trigger T32A ch3 underflow A trigger	✓	✓	✓
[TSEL0CR9]	INSEL36	T32A ch3 Timer C	T32A ch2 Timer register C0 match trigger T32A ch2 Timer register C1 match trigger T32A ch2 Timer C overflow trigger T32A ch2 Timer C underflow trigger	✓	✓	✓
	INSEL37	T32A ch4 Timer A	PA2 (TRGIN0)	✓	✓	✓
			PA3 (TRGIN1)	✓	✓	✓
			PA4 (TRGIN2)	✓	✓	✓
			ADC unit A general purpose trigger interrupt ADC unit A single conversion interrupt ADC unit A continuous conversion interrupt ADC unit A monitor function 0 Interrupt	✓	✓	✓
			A-ENC ch2 divided pulse signal (TIMPLS)	✓	✓	✓
	INSEL38	T32A ch4 Timer B	T32A ch4 Timer register A0 match trigger T32A ch4 Timer register A1 match trigger T32A ch4 Timer A overflow trigger T32A ch4 Timer A underflow trigger	✓	✓	✓
	INSEL39	T32A ch4 Timer C	T32A ch3 Timer register C0 match trigger T32A ch3 Timer register C1 match trigger T32A ch3 Timer C overflow trigger T32A ch3 Timer C underflow trigger	✓	✓	✓

Table 2.8 Trigger Selector List for each Product (6/6)

Register		Trigger unit	Trigger Source	Product (✓: Available, -: N/A)		
	Bit Symbol			M4MN	M4MM	M4ML
[TSEL0CR10]	INSEL40	T32A ch5 Timer A	PA2 (TRGIN0)	✓	✓	✓
			PA3 (TRGIN1)	✓	✓	✓
			PA4 (TRGIN2)	✓	✓	✓
			ADC unit B general purpose trigger interrupt ADC unit B single conversion interrupt ADC unit B continuous conversion interrupt ADC unit B monitor function 0 Interrupt ADC unit B monitor function 1 Interrupt	✓	✓	✓
	INSEL41	T32A ch5 Timer B	T32A ch5 Timer register A0 match trigger T32A ch5 Timer register A1 match trigger T32A ch5 Timer A overflow trigger T32A ch5 Timer A underflow trigger	✓	✓	✓
	INSEL42	T32A ch5 Timer C	T32A ch4 Timer register C0 match trigger T32A ch4 Timer register C1 match trigger T32A ch4 Timer C overflow trigger T32A ch4 Timer C underflow trigger	✓	✓	✓

2.2.2. Operation and setting

When using TRGSEL, please set an applicable clock enable bit to "1" (clock supply) in fsys supply stop register A (***[CGFSYSENA]***, ***[CGFSYSMENA]***), fsys supply stop register B (***[CGFSYSENB]***, ***[CGFSYSMENB]***), fsys supply stop register C (***[CGFSYSMENC]***), and fc supply stop register (***[CGFCEN]***).

An applicable register and the bit position vary according to a product. Therefore, the register may not exist with the product. Please refer to the reference manual "Clock Control and Operation Mode" the reference manual for the details.

Setting procedure of Trigger selector is as following.

(1) Selection of an input trigger (***[TSEL0CRn]***<INSELm>)

Selection of the input trigger used for the trigger source is performed.

Please set up selection of the input trigger by the input trigger selector bit (***[TSEL0CRn]***<INSELm>) of the control register. (n: register number, m: trigger number)

(2) Selection of edge detection conditions (***[TSEL0CRn]***<UPDNm>)

For the input trigger signal which needs edge detection, selection of rising edge or falling edge detection is performed.

Please set up selection of edge detection conditions in the selection bit (***[TSEL0CRn]***<UPDNm>) of a control register.

The following shows the trigger signal which needs edge detection.

- External trigger input (TRGIN0, TRGIN1, and TRGIN2)

(3) Selection of a trigger output (***[TSEL0CRn]***<OUTSELm>)

Selection of an output without or with edge detection is performed.

Please set up selection of a trigger output in the selection bit (***[TSEL0CRn]***<OUTSELm>) of a control register.

(4) Output enable (***[TSEL0CRn]***<ENm>)

The output (enable/disable) of the selected trigger signal is chosen.

Please set up selection of output (enable/disable) in the setting bit (***[TSEL0CRn]***<ENm>) of a control register. A trigger output will be enabled if ***[TSEL0CRn]***<ENm> is set to "1".

2.2.3. List of Registers

The table below shows control registers and their addresses.

Peripheral function		Channel/Unit	Base address
Trigger selector	TRGSEL	ch0	0x400A0400

Register name		Address(Base+)
Control Register 0	***[TSELxCR0]***	0x0000
Control Register 1	***[TSELxCR1]***	0x0004
Control Register 2	***[TSELxCR2]***	0x0008
Control Register 3	***[TSELxCR3]***	0x000C
Control Register 4	***[TSELxCR4]***	0x0010
Control Register 5	***[TSELxCR5]***	0x0014
Control Register 6	***[TSELxCR6]***	0x0018
Control Register 7	***[TSELxCR7]***	0x001C
Control Register 8	***[TSELxCR8]***	0x0020
Control Register 9	***[TSELxCR9]***	0x0024
Control Register 10	***[TSELxCR10]***	0x0028

2.2.4. Details of Registers

The following sections show the detail of registers. The symbol in the parenthesis in function column of each table expresses each function signal name.

2.2.4.1. *[TSELxCR0]* (Control Register 0)

Bit	Bit Symbol	After Reset	Type	Function
31	-	0	R	Read as "0"
30:28	INSEL3[2:0]	000	R/W	Select the input trigger (DMA ch19) 000: T32A ch0 DMA request at match A1 register (T32A00DMAREQCMPA1) 001: T32A ch0 DMA request at match C1 register (T32A00DMAREQCMPC1) 010: T32A ch1 DMA request at match A1 register (T32A01DMAREQCMPA1) 011: T32A ch1 DMA request at match C1 register (T32A01DMAREQCMPC1) 100: A-PMD ch0 PWM interrupt (INTPWM0) 101: Reserved 110: Reserved 111: Reserved
27	-	0	R	Read as "0"
26	UPDN3	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
25	OUTSEL3	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
24	EN3	0	R/W	Trigger output control 0: disable 1: enable
23	-	0	R	Read as "0"
22:20	INSEL2[2:0]	000	R/W	Select the input trigger (DMA ch18) 000: ADC unit C general purpose trigger DMA request (ADCTRG_DMAREQ) 001: ADC unit C single conversion DMA request (ADCSGL_DMAREQ) 010: ADC unit C continuous conversion DMA request (ADCCNT_DMAREQ) 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved
19	-	0	R	Read as "0"
18	UPDN2	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
17	OUTSEL2	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
16	EN2	0	R/W	Trigger output control 0: disable 1: enable
15	-	0	R	Read as "0"

Bit	Bit Symbol	After Reset	Type	Function
14:12	INSEL1[2:0]	000	R/W	Select the input trigger (DMA ch17) 000: ADC unit B general purpose trigger DMA request (ADBTRG_DMAREQ) 001: ADC unit B single conversion DMA request (ADBSGL_DMAREQ) 010: ADC unit B continuous conversion DMA request (ADBCNT_DMAREQ) 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved
11	-	0	R	Read as "0"
10	UPDN1	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
9	OUTSEL1	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
8	EN1	0	R/W	Trigger output control 0: disable 1: enable
7	-	0	R	Read as "0"
6:4	INSEL0[2:0]	000	R/W	Select the input trigger (DMA ch16) 000: ADC unit A general purpose trigger DMA request (ADATRG_DMAREQ) 001: ADC unit A single conversion DMA request (ADASGL_DMAREQ) 010: ADC unit A continuous conversion DMA request (ADACNT_DMAREQ) 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved
3	-	0	R	Read as "0"
2	UPDN0	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
1	OUTSEL0	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
0	EN0	0	R/W	Trigger output control 0: disable 1: enable

2.2.4.2. *[TSELxCR1]* (Control Register1)

Bit	Bit Symbol	After Reset	Type	Function
31	-	0	R	Read as "0"
30:28	INSEL7[2:0]	000	R/W	Select the input trigger (DMA ch23) 000: T32A ch0 DMA request capture A0 register (T32A00DMAREQCAPA0) 001: T32A ch0 DMA request capture A1 register (T32A00DMAREQCAPA1) 010: T32A ch1 DMA request capture A0 register (T32A01DMAREQCAPA0) 011: T32A ch1 DMA request capture A1 register (T32A01DMAREQCAPA1) 100: T32A ch0 DMA request capture C0 register (T32A00DMAREQCAPC0) 101: T32A ch0 DMA request capture C1 register (T32A00DMAREQCAPC1) 110: T32A ch1 DMA request capture C0 register (T32A01DMAREQCAPC0) 111: T32A ch1 DMA request capture C1 register (T32A01DMAREQCAPC1)
27	-	0	R	Read as "0"
26	UPDN7	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
25	OUTSEL7	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
24	EN7	0	R/W	Trigger output control 0: disable 1: enable
23	-	0	R	Read as "0"
22:20	INSEL6[2:0]	000	R/W	Select the input trigger (DMA ch22) 000: T32A ch0 DMA request at match B1 register (T32A00DMAREQCMPB1) 001: T32A ch1 DMA request at match B1 register (T32A01DMAREQCMPB1) 010: T32A ch2 DMA request at match B1 register (T32A02DMAREQCMPB1) 011: T32A ch3 DMA request at match B1 register (T32A03DMAREQCMPB1) 100: T32A ch4 DMA request at match B1 register (T32A04DMAREQCMPB1) 101: T32A ch5 DMA request at match B1 register (T32A05DMAREQCMPB1) 110: Reserved 111: Reserved
19	-	0	R	Read as "0"
18	UPDN6	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
17	OUTSEL6	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
16	EN6	0	R/W	Trigger output control 0: disable 1: enable
15	-	0	R	Read as "0"
14:12	INSEL5[2:0]	000	R/W	Select the input trigger (DMA ch21) 000: T32A ch4 DMA request at match A1 register (T32A04DMAREQCMPA1) 001: T32A ch4 DMA request at match C1 register (T32A04DMAREQCMPC1) 010: T32A ch5 DMA request at match A1 register (T32A05DMAREQCMPA1) 011: T32A ch5 DMA request at match C1 register (T32A05DMAREQCMPC1) 100: A-PMD ch2 PWM interrupt (INTPWM2) 101: Reserved 110: Reserved 111: Reserved

Bit	Bit Symbol	After Reset	Type	Function
11	-	0	R	Read as "0"
10	UPDN5	0	R/W	Edge detection 0: Rising edge detection 1: falling edge detection
9	OUTSEL5	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
8	EN5	0	R/W	Trigger output control 0: disable 1: enable
7	-	0	R	Read as "0"
6:4	INSEL4[2:0]	000	R/W	Select the input trigger (DMA ch20) 000: T32A ch2 DMA request at match A1 register (T32A02DMAREQCMPA1) 001: T32A ch2 DMA request at match C1 register (T32A02DMAREQCMPC1) 010: T32A ch3 DMA request at match A1 register (T32A03DMAREQCMPA1) 011: T32A ch3 DMA request at match C1 register (T32A03DMAREQCMPC1) 100: A-PMD ch1 PWM interrupt (INTPWM1) 101: Reserved 110: Reserved 111: Reserved
3	-	0	R	Read as "0"
2	UPDN4	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
1	OUTSEL4	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
0	EN4	0	R/W	Trigger output control 0: disable 1: enable

2.2.4.3. *[TSELxCR2]* (Control Register 2)

Bit	Bit Symbol	After Reset	Type	Function
31	-	0	R	Read as "0"
30:28	INSEL11[2:0]	000	R/W	Select the input trigger (DMA ch27) 000: T32A ch3 DMA request capture B0 register (T32A03DMAREQCAPB0) 001: T32A ch3 DMA request capture B1 register (T32A03DMAREQCAPB1) 010: T32A ch4 DMA request capture B0 register (T32A04DMAREQCAPB0) 011: T32A ch4 DMA request capture B1 register (T32A04DMAREQCAPB1) 100: T32A ch5 DMA request capture B0 register (T32A05DMAREQCAPB0) 101: T32A ch5 DMA request capture B1 register (T32A05DMAREQCAPB1) 110: Reserved 111: Reserved
27	-	0	R	Read as "0"
26	UPDN11	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
25	OUTSEL11	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
24	EN11	0	R/W	Trigger output control 0: disable 1: enable
23	-	0	R	Read as "0"
22:20	INSEL10[2:0]	000	R/W	Select the input trigger (DMA ch26) 000: T32A ch0 DMA request capture B0 register (T32A00DMAREQCAPB0) 001: T32A ch0 DMA request capture B1 register (T32A00DMAREQCAPB1) 010: T32A ch1 DMA request capture B0 register (T32A01DMAREQCAPB0) 011: T32A ch1 DMA request capture B1 register (T32A01DMAREQCAPB1) 100: T32A ch2 DMA request capture B0 register (T32A02DMAREQCAPB0) 101: T32A ch2 DMA request capture B1 register (T32A02DMAREQCAPB1) 110: Reserved 111: Reserved
19	-	0	R	Read as "0"
18	UPDN10	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
17	OUTSEL1	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
16	EN10	0	R/W	Trigger output control 0: disable 1: enable
15	-	0	R	Read as "0"
14:12	INSEL9[2:0]	000	R/W	Select the input trigger (DMA ch25) 000: T32A ch4 DMA request capture A0 register (T32A04DMAREQCAPA0) 001: T32A ch4 DMA request capture A1 register (T32A04DMAREQCAPA1) 010: T32A ch5 DMA request capture A0 register (T32A05DMAREQCAPA0) 011: T32A ch5 DMA request capture A1 register (T32A05DMAREQCAPA1) 100: T32A ch4 DMA request capture C0 register (T32A04DMAREQCAPC0) 101: T32A ch4 DMA request capture C1 register (T32A04DMAREQCAPC1) 110: T32A ch5 DMA request capture C0 register (T32A05DMAREQCAPC0) 111: T32A ch5 DMA request capture C1 register (T32A05DMAREQCAPC1)

Bit	Bit Symbol	After Reset	Type	Function
11	-	0	R	Read as "0"
10	UPDN9	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
9	OUTSEL9	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
8	EN9	0	R/W	Trigger output control 0: disable 1: enable
7	-	0	R	Read as "0"
6:4	INSEL8[2:0]	000	R/W	Select the input trigger (DMA ch24) 000: T32A ch2 DMA request capture A0 register (T32A02DMAREQCAPA0) 001: T32A ch2 DMA request capture A1 register (T32A02DMAREQCAPA1) 010: T32A ch3 DMA request capture A0 register (T32A03DMAREQCAPA0) 011: T32A ch3 DMA request capture A1 register (T32A03DMAREQCAPA1) 100: T32A ch2 DMA request capture C0 register (T32A02DMAREQCAPC0) 101: T32A ch2 DMA request capture C1 register (T32A02DMAREQCAPC1) 110: T32A ch3 DMA request capture C0 register (T32A03DMAREQCAPC0) 111: T32A ch3 DMA request capture C1 register (T32A03DMAREQCAPC1)
3	-	0	R	Read as "0"
2	UPDN8	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
1	OUTSEL8	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
0	EN8	0	R/W	Trigger output control 0: disable 1: enable

2.2.4.4. *[TSELxCR3]* (Control Register 3)

Bit	Bit Symbol	After Reset	Type	Function
31	-	0	R	Read as "0"
30:28	INSEL15[2:0]	000	R/W	Select the input trigger (DMA ch31) 000: DMAC ch6 transfer completion (INTDMAATC6) 001: DMAC ch7 transfer completion (INTDMAATC7) 010: DMAC ch14 transfer completion (INTDMAATC14) 011: DMAC ch15 transfer completion (INTDMAATC15) 100: DMAC ch21 transfer completion (INTDMAATC21) 101: DMAC ch25 transfer completion (INTDMAATC25) 110: DMAC ch27 transfer completion (INTDMAATC27) 111: PA4(TRGIN2)
27	-	0	R	Read as "0"
26	UPDN15	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
25	OUTSEL15	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
24	EN15	0	R/W	Trigger output control 0: disable 1: enable
23	-	0	R	Read as "0"
22:20	INSEL14[2:0]	000	R/W	Select the input trigger (DMA ch30) 000: DMAC ch4 transfer completion (INTDMAATC4) 001: DMAC ch5 transfer completion (INTDMAATC5) 010: DMAC ch12 transfer completion (INTDMAATC12) 011: DMAC ch13 transfer completion (INTDMAATC13) 100: DMAC ch20 transfer completion (INTDMAATC20) 101: DMAC ch24 transfer completion (INTDMAATC24) 110: DMAC ch26 transfer completion (INTDMAATC26) 111: PA3(TRGIN1)
19	-	0	R	Read as "0"
18	UPDN14	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
17	OUTSEL14	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
16	EN14	0	R/W	Trigger output control 0: disable 1: enable
15	-	0	R	Read as "0"
14:12	INSEL13[2:0]	000	R/W	Select the input trigger (DMA ch29) 000: DMAC ch2 transfer completion (INTDMAATC2) 001: DMAC ch3 transfer completion (INTDMAATC3) 010: DMAC ch10 transfer completion (INTDMAATC10) 011: DMAC ch11 transfer completion (INTDMAATC11) 100: DMAC ch18 transfer completion (INTDMAATC18) 101: DMAC ch19 transfer completion (INTDMAATC19) 110: DMAC ch23 transfer completion (INTDMAATC23) 111: PA2 (TRGIN0)

Bit	Bit Symbol	After Reset	Type	Function
11	-	0	R	Read as "0"
10	UPDN13	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
9	OUTSEL13	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
8	EN13	0	R/W	Trigger output control 0: disable 1: enable
7	-	0	R	Read as "0"
6:4	INSEL12[2:0]	000	R/W	Select the input trigger (DMA ch28) 000: DMAC ch0 transfer completion (INTDMAATC0) 001: DMAC ch1 transfer completion (INTDMAATC1) 010: DMAC ch8 transfer completion (INTDMAATC8) 011: DMAC ch9 transfer completion (INTDMAATC9) 100: DMAC ch16 transfer completion (INTDMAATC16) 101: DMAC ch17 transfer completion (INTDMAATC17) 110: DMAC ch22 transfer completion (INTDMAATC22) 111: Reserved
3	-	0	R	Read as "0"
2	UPDN12	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
1	OUTSEL12	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
0	EN12	0	R/W	Trigger output control 0: disable 1: enable

2.2.4.5. *[TSELxCR4]* (Control Register 4)

Bit	Bit Symbol	After Reset	Type	Function
31	-	0	R	Read as "0"
30:28	INSEL19[2:0]	000	R/W	Select the input trigger (TSPI ch0 trigger input) 000: PA2 (TRGIN0) 001: PA3 (TRGIN1) 010: PA4 (TRGIN2) 011: T32A ch5 Timer register A1 match trigger (T32A05TRGOUTCMPA1) 100: T32A ch5 Timer register B1 match trigger (T32A05TRGOUTCMPB1) 101: T32A ch5 Timer register C1 match trigger (T32A05TRGOUTCMPC1) 110: Reserved 111: Reserved
27	-	0	R	Read as "0"
26	UPDN19	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
25	OUTSEL19	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
24	EN19	0	R/W	Trigger output control 0: disable 1: enable
23	-	0	R	Read as "0"
22:20	INSEL18[2:0]	000	R/W	Select the input trigger (ADC unit C general purpose trigger) 000: PA2 (TRGIN0) 001: PA3 (TRGIN1) 010: PA4 (TRGIN2) 011: T32A ch5 Timer register A1 match trigger (T32A05TRGOUTCMPA1) 100: T32A ch5 Timer register B1 match trigger (T32A05TRGOUTCMPB1) 101: T32A ch5 Timer register C1 match trigger (T32A05TRGOUTCMPC1) 110: Reserved 111: Reserved
19	-	0	R	Read as "0"
18	UPDN18	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
17	OUTSEL18	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
16	EN18	0	R/W	Trigger output control 0: disable 1: enable
15	-	0	R	Read as "0"
14:12	INSEL17[2:0]	000	R/W	Select the input trigger (ADC unit B general purpose trigger) 000: PA2 (TRGIN0) 001: PA3 (TRGIN1) 010: PA4 (TRGIN2) 011: T32A ch3 Timer register A1 match trigger (T32A03TRGOUTCMPA1) 100: T32A ch3 Timer register B1 match trigger (T32A03TRGOUTCMPB1) 101: T32A ch3 Timer register C1 match trigger (T32A03TRGOUTCMPC1) 110: Reserved 111: Reserved

Bit	Bit Symbol	After Reset	Type	Function
11	-	0	R	Read as "0"
10	UPDN17	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
9	OUTSEL17	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
8	EN17	0	R/W	Trigger output control 0: disable 1: enable
7	-	0	R	Read as "0"
6:4	INSEL16[2:0]	000	R/W	Select the input trigger (ADC unit A general purpose trigger) 000: PA2 (TRGIN0) 001: PA3 (TRGIN1) 010: PA4 (TRGIN2) 011: T32A ch1 Timer register A1 match trigger (T32A01TRGOUTCMPA1) 100: T32A ch1 Timer register B1 match trigger (T32A01TRGOUTCMPB1) 101: T32A ch1 Timer register C1 match trigger (T32A01TRGOUTCMPC1) 110: Reserved 111: Reserved
3	-	0	R	Read as "0"
2	UPDN16	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
1	OUTSEL16	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
0	EN16	0	R/W	Trigger output control 0: disable 1: enable

2.2.4.6. *[TSELxCR5]* (Control Register 5)

Bit	Bit Symbol	After Reset	Type	Function
31	-	0	R	Read as "0"
30:28	INSEL23[2:0]	000	R/W	Select the input trigger (UART ch2 trigger input) 000: PA2 (TRGIN0) 001: PA3 (TRGIN1) 010: PA4 (TRGIN2) 011: T32A ch5 Timer register A1 match trigger (T32A05TRGOUTCMPA1) 100: T32A ch5 Timer register B1 match trigger (T32A05TRGOUTCMPB1) 101: T32A ch5 Timer register C1 match trigger (T32A05TRGOUTCMPC1) 110: Reserved 111: Reserved
27	-	0	R	Read as "0"
26	UPDN23	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
25	OUTSEL23	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
24	EN23	0	R/W	Trigger output control 0: disable 1: enable
23	-	0	R	Read as "0"
22:20	INSEL22[2:0]	000	R/W	Select the input trigger (UART ch1 trigger input) 000: PA2 (TRGIN0) 001: PA3 (TRGIN1) 010: PA4 (TRGIN2) 011: T32A ch5 Timer register A1 match trigger (T32A05TRGOUTCMPA1) 100: T32A ch5 Timer register B1 match trigger (T32A05TRGOUTCMPB1) 101: T32A ch5 Timer register C1 match trigger (T32A05TRGOUTCMPC1) 110: Reserved 111: Reserved
19	-	0	R	Read as "0"
18	UPDN22	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
17	OUTSEL22	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
16	EN22	0	R/W	Trigger output control 0: disable 1: enable
15	-	0	R	Read as "0"
14:12	INSEL21[2:0]	000	R/W	Select the input trigger (UART ch0 trigger input) 000: PA2 (TRGIN0) 001: PA3 (TRGIN1) 010: PA4 (TRGIN2) 011: T32A ch5 Timer register A1 match trigger (T32A05TRGOUTCMPA1) 100: T32A ch5 Timer register B1 match trigger (T32A05TRGOUTCMPB1) 101: T32A ch5 Timer register C1 match trigger (T32A05TRGOUTCMPC1) 110: Reserved 111: Reserved

Bit	Bit Symbol	After Reset	Type	Function
11	-	0	R	Read as "0"
10	UPDN21	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
9	OUTSEL21	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
8	EN21	0	R/W	Trigger output control 0: disable 1: enable
7	-	0	R	Read as "0"
6:4	INSEL20[2:0]	000	R/W	Select the input trigger (TSPI ch1 trigger input) 000: PA2 (TRGIN0) 001: PA3 (TRGIN1) 010: PA4 (TRGIN2) 011: T32A ch5 Timer register A1 match trigger (T32A05TRGOUTCMPA1) 100: T32A ch5 Timer register B1 match trigger (T32A05TRGOUTCMPB1) 101: T32A ch5 Timer register C1 match trigger (T32A05TRGOUTCMPC1) 110: Reserved 111: Reserved
3	-	0	R	Read as "0"
2	UPDN20	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
1	OUTSEL20	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
0	EN20	0	R/W	Trigger output control 0: disable 1: enable

2.2.4.7. *[TSELxCR6]* (Control Register 6)

Bit	Bit Symbol	After Reset	Type	Function
31	-	0	R	Read as "0"
30:28	INSEL27[2:0]	000	R/W	Select the input trigger (T32A ch0 Timer C internal trigger input) 000: T32A ch5 Timer register C0 match trigger (T32A05TRGOUTCMPC0) 001: T32A ch5 Timer register C1 match trigger (T32A05TRGOUTCMPC1) 010: T32A ch5 Timer C overflow trigger (T32A05TRGOUTOFC) 011: T32A ch5 Timer C underflow trigger (T32A05TRGOUTUFC) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
27	-	0	R	Read as "0"
26	UPDN27	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
25	OUTSEL27	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
24	EN27	0	R/W	Trigger output control 0: disable 1: enable
23	-	0	R	Read as "0"
22:20	INSEL26[2:0]	000	R/W	Select the input trigger (T32A ch0 Timer B internal trigger input) 000: T32A ch0 Timer register A0 match trigger (T32A00TRGOUTCMPA0) 001: T32A ch0 Timer register A1 match trigger (T32A00TRGOUTCMPA1) 010: T32A ch0 Timer A overflow trigger (T32A00TRGOUTOFA) 011: T32A ch0 Timer A underflow trigger (T32A00TRGOUTUFA) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
19	-	0	R	Read as "0"
18	UPDN26	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
17	OUTSEL26	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
16	EN26	0	R/W	Trigger output control 0: disable 1: enable
15	-	0	R	Read as "0"
14:12	INSEL25[2:0]	000	R/W	Select the input trigger (T32A ch0 Timer A internal trigger input) 000: PA2 (TRGIN0) 001: PA3 (TRGIN1) 010: PA4 (TRGIN2) 011: UART ch0 transmission completion trigger (UART0TXTRG) 100: UART ch0 reception completion trigger (UART0RXTRG) 101: TSPI ch0 transmit completion trigger (TSPI0TXEND) 110: TSPI ch0 receive completion trigger (TSPI0RXEND) 111: I2C ch0 interrupt (INTI2C0) / EI2C ch0 status interrupt (INTI2C0ST)

Bit	Bit Symbol	After Reset	Type	Function
11	-	0	R	Read as "0"
10	UPDN25	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
9	OUTSEL25	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
8	EN25	0	R/W	Trigger output control 0: disable 1: enable
7	-	0	R	Read as "0"
6:4	INSEL24[2:0]	000	R/W	Select the input trigger (UART ch3 trigger input) 000: PA2 (TRGIN0) 001: PA3 (TRGIN1) 010: PA4 (TRGIN2) 011: T32A ch5 Timer register A1 match trigger (T32A05TRGOUTCMPA1) 100: T32A ch5 Timer register B1 match trigger (T32A05TRGOUTCMPB1) 101: T32A ch5 Timer register C1 match trigger (T32A05TRGOUTCMPC1) 110: Reserved 111: Reserved
3	-	0	R	Read as "0"
2	UPDN24	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
1	OUTSEL24	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
0	EN24	0	R/W	Trigger output control 0: disable 1: enable

2.2.4.8. *[TSELxCR7]* (Control Register 7)

Bit	Bit Symbol	After Reset	Type	Function
31	-	0	R	Read as "0"
30:28	INSEL31[2:0]	000	R/W	Select the input trigger (T32A ch2 Timer A internal trigger input) 000: PA2 (TRGIN0) 001: PA3 (TRGIN1) 010: PA4 (TRGIN2) 011: UART ch2 transmission completion trigger (UART2TXTRG) 100: UART ch2 reception completion trigger (UART2RXTRG) 101: A-ENC32 ch1 divided pulse signal (ENC1TIMPLS) 110: I2C ch1 interrupt (INTI2C1) / EI2C ch0 status interrupt (INTI2C1ST) 111: Reserved
27	-	0	R	Read as "0"
26	UPDN31	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
25	OUTSEL31	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
24	EN31	0	R/W	Trigger output control 0: disable 1: enable
23	-	0	R	Read as "0"
22:20	INSEL30[2:0]	000	R/W	Select the input trigger (T32A ch1 Timer C internal trigger input) 000: T32A ch0 Timer register C0 match trigger (T32A00TRGOUTCMPC0) 001: T32A ch0 Timer register C1 match trigger (T32A00TRGOUTCMPC1) 010: T32A ch0 Timer C overflow trigger (T32A00TRGOUTOFC) 011: T32A ch0 Timer C underflow trigger (T32A00TRGOUTUFC) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
19	-	0	R	Read as "0"
18	UPDN30	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
17	OUTSEL30	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
16	EN30	0	R/W	Trigger output control 0: disable 1: enable
15	-	0	R	Read as "0"
14:12	INSEL29[2:0]	000	R/W	Select the input trigger (T32A ch1 Timer B internal trigger input) 000: T32A ch1 Timer register A0 match trigger (T32A01TRGOUTCMPA0) 001: T32A ch1 Timer register A1 match trigger (T32A01TRGOUTCMPA1) 010: T32A ch1 Timer A overflow trigger (T32A01TRGOUTOFA) 011: T32A ch1 Timer A underflow trigger (T32A01TRGOUTUFA) 100: Reserved 101: Reserved 110: Reserved 111: Reserved

Bit	Bit Symbol	After Reset	Type	Function
11	-	0	R	Read as "0"
10	UPDN29	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
9	OUTSEL29	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
8	EN29	0	R/W	Trigger output control 0: disable 1: enable
7	-	0	R	Read as "0"
6:4	INSEL28[2:0]	000	R/W	Select the input trigger (T32A ch1 Timer A internal trigger input) 000: PA2 (TRGIN0) 001: PA3 (TRGIN1) 010: PA4 (TRGIN2) 011: UART ch1 transmission completion trigger (UART1TXTRG) 100: UART ch1 reception completion trigger (UART1RXTRG) 101: TSPI ch1 transmit completion trigger (TSPI1TXEND) 110: TSPI ch1 receive completion trigger (TSPI1RXEND) 111: A-ENC32 ch0 divided pulse signal (ENC0TIMPLS)
3	-	0	R	Read as "0"
2	UPDN28	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
1	OUTSEL28	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
0	EN28	0	R/W	Trigger output control 0: disable 1: enable

2.2.4.9. *[TSELxCR8]* (Control Register 8)

Bit	Bit Symbol	After Reset	Type	Function
31	-	0	R	Read as "0"
30:28	INSEL35[2:0]	000	R/W	Select the input trigger (T32A ch3 Timer B internal trigger input) 000: T32A ch3 Timer register A0 match trigger (T32A03TRGOUTCMPA0) 001: T32A ch3 Timer register A1 match trigger (T32A03TRGOUTCMPA1) 010: T32A ch3 overflow A (T32A03TRGOUTOFA) 011: T32A ch3 underflow A (T32A03TRGOUTUFA) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
27	-	0	R	Read as "0"
26	UPDN35	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
25	OUTSEL35	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
24	EN35	0	R/W	Trigger output control 0: disable 1: enable
23	-	0	R	Read as "0"
22:20	INSEL34[2:0]	000	R/W	Select the input trigger (T32A ch3 Timer A internal trigger input) 000: PA2 (TRGIN0) 001: PA3 (TRGIN1) 010: PA4 (TRGIN2) 011: UART ch3 transmission completion trigger (UART3TXTRG) 100: UART ch3 reception completion trigger (UART3RXTRG) 101: ADC unit C general purpose trigger interrupt (INTADCTRG) 110: ADC unit C single conversion interrupt (INTADCSGL) 111: ADC unit C continuous conversion interrupt (INTADCCNT)
19	-	0	R	Read as "0"
18	UPDN34	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
17	OUTSEL34	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
16	EN34	0	R/W	Trigger output control 0: disable 1: enable
15	-	0	R	Read as "0"
14:12	INSEL33[2:0]	000	R/W	Select the input trigger (T32A ch2 Timer C internal trigger input) 000: T32A ch1 Timer register C0 match trigger (T32A01TRGOUTCMPC0) 001: T32A ch1 Timer register C1 match trigger (T32A01TRGOUTCMPC1) 010: T32A ch1 Timer C overflow trigger (T32A01TRGOUTOFC) 011: T32A ch1 Timer C underflow trigger (T32A01TRGOUTUFC) 100: Reserved 101: Reserved 110: Reserved 111: Reserved

Bit	Bit Symbol	After Reset	Type	Function
11	-	0	R	Read as "0"
10	UPDN33	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
9	OUTSEL33	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
8	EN33	0	R/W	Trigger output control 0: disable 1: enable
7	-	0	R	Read as "0"
6:4	INSEL32[2:0]	000	R/W	Select the input trigger (T32A ch2 Timer B internal trigger input) 000: T32A ch2 Timer register A0 match trigger (T32A02TRGOUTCMPA0) 001: T32A ch2 Timer register A1 match trigger (T32A02TRGOUTCMPA1) 010: T32A ch2 Timer A overflow trigger (T32A02TRGOUTOFA) 011: T32A ch2 Timer A underflow trigger (T32A02TRGOUTUFA) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
3	-	0	R	Read as "0"
2	UPDN32	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
1	OUTSEL32	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
0	EN32	0	R/W	Trigger output control 0: disable 1: enable

2.2.4.10. *[TSELxCR9]* (Control Register 9)

Bit	Bit Symbol	After Reset	Type	Function
31	-	0	R	Read as "0"
30:28	INSEL39[2:0]	000	R/W	Select the input trigger (T32A ch4 Timer C internal trigger input) 000: T32A ch3 Timer register C0 match trigger (T32A03TRGOUTCMPC0) 001: T32A ch3 Timer register C1 match trigger (T32A03TRGOUTCMPC1) 010: T32A ch3 Timer C overflow trigger (T32A03TRGOUTOFC) 011: T32A ch3 Timer C underflow trigger (T32A03TRGOUTUFC) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
27	-	0	R	Read as "0"
26	UPDN39	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
25	OUTSEL39	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
24	EN39	0	R/W	Trigger output control 0: disable 1: enable
23	-	0	R	Read as "0"
22:20	INSEL38[2:0]	000	R/W	Select the input trigger (T32A ch4 Timer B internal trigger input) 000: T32A ch4 Timer register A0 match trigger (T32A04TRGOUTCMPA0) 001: T32A ch4 Timer register A1 match trigger (T32A04TRGOUTCMPA1) 010: T32A ch4 Timer A overflow trigger (T32A04TRGOUTOFA) 011: T32A ch4 Timer A underflow trigger (T32A04TRGOUTUFA) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
19	-	0	R	Read as "0"
18	UPDN38	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
17	OUTSEL38	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
16	EN38	0	R/W	Trigger output control 0: disable 1: enable
15	-	0	R	Read as "0"
14:12	INSEL37[2:0]	000	R/W	Select the input trigger (T32A ch4 Timer A internal trigger input) 000: PA2 (TRGIN0) 001: PA3 (TRGIN1) 010: PA4 (TRGIN2) 011: ADC unit A general purpose trigger interrupt (INTADATRG) 100: ADC unit A single conversion interrupt (INTADASGL) 101: ADC unit A continuous conversion interrupt (INTADACNT) 110: ADC unit A monitor function 0 Interrupt (INTADACP0) 111: A-ENC32 ch2 divided pulse signal (ENC2TIMPLS)

Bit	Bit Symbol	After Reset	Type	Function
11	-	0	R	Read as "0"
10	UPDN37	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
9	OUTSEL37	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
8	EN37	0	R/W	Trigger output control 0: disable 1: enable
7	-	0	R	Read as "0"
6:4	INSEL36[2:0]	000	R/W	Select the input trigger (T32A ch3 Timer C internal trigger input) 000: T32A ch2 Timer register C0 match trigger (T32A02TRGOUTCMPC0) 001: T32A ch2 Timer register C1 match trigger (T32A02TRGOUTCMPC1) 010: T32A ch2 Timer C overflow trigger (T32A02TRGOUTOFC) 011: T32A ch2 Timer C underflow trigger (T32A02TRGOUTUFC) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
3	-	0	R	Read as "0"
2	UPDN36	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
1	OUTSEL36	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
0	EN36	0	R/W	Trigger output control 0: disable 1: enable

2.2.4.11. *[TSELxCR10]* (Control Register 10)

Bit	Bit Symbol	After Reset	Type	Function
31:23	-	0	R	Read as "0"
22:20	INSEL42[2:0]	000	R/W	Select the input trigger (T32A ch5 Timer C internal trigger input) 000: T32A ch4 Timer register C0 match trigger (T32A04TRGOUTCMPC0) 001: T32A ch4 Timer register C1 match trigger (T32A04TRGOUTCMPC1) 010: T32A ch4 Timer C overflow trigger (T32A04TRGOUTOFC) 011: T32A ch4 Timer C underflow trigger (T32A04TRGOUTUFC) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
19	-	0	R	Read as "0"
18	UPDN42	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
17	OUTSEL42	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
16	EN42	0	R/W	Trigger output control 0: disable 1: enable
15	-	0	R	Read as "0"
14:12	INSEL41[2:0]	000	R/W	Select the input trigger (T32A ch5 Timer B internal trigger input) 000: T32A ch5 Timer register A0 match trigger (T32A05TRGOUTCMPA0) 001: T32A ch5 Timer register A1 match trigger (T32A05TRGOUTCMPA1) 010: T32A ch5 Timer A overflow trigger (T32A05TRGOUTOFA) 011: T32A ch5 Timer A underflow trigger (T32A05TRGOUTUFA) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
11	-	0	R	Read as "0"
10	UPDN41	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
9	OUTSEL41	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
8	EN41	0	R/W	Trigger output control 0: disable 1: enable
7	-	0	R	Read as "0"
6:4	INSEL40[2:0]	000	R/W	Select the input trigger (T32A ch5 Timer A internal trigger input) 000: PA2 (TRGIN0) 001: PA3 (TRGIN1) 010: PA4 (TRGIN2) 011: ADC unit B general purpose trigger interrupt (INTADBTRG) 100: ADC unit B single conversion interrupt (INTADBSGL) 101: ADC unit B continuous conversion interrupt (INTADBCNT) 110: ADC unit B monitor function 0 Interrupt (INTADBCP0) 111: ADC unit B monitor function 1 Interrupt (INTADBCP1)

Bit	Bit Symbol	After Reset	Type	Function
3	-	0	R	Read as "0"
2	UPDN40	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
1	OUTSEL40	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
0	EN40	0	R/W	Trigger output control 0: disable 1: enable

2.3. Clock Selective Watchdog Timer (SIWDT)

2.3.1. Built-in channel

The following table shows the SIWDT built-in channel of each product.

Table 2.9 SIWDT built-in channel

Product	SIWDT channel (✓: Available, -: N/A)
	ch0
M4MN	✓
M4MM	✓
M4ML	✓

2.3.2. Count Clock

The Clock Selective Watchdog Timer can select the clock to count.
The following table shows the selectable clock.

Table 2.10 SIWDT count clock

Clock	Signal	Selection
System clock	fsysm	Selected by ***[SIWD0MOD]***<WDCLS>
Internal High speed oscillator1 clock	f_{IHOSC1}	
Internal High speed oscillator2 clock	f_{IHOSC2}	

2.3.3. Oscillation clock protection function

If the Internal High speed oscillator 2(f_{IHOSC2}) is selected, rewriting of the internal High speed oscillator 2 can be forbidden.

Table 2.11 SIWDT Oscillation clock protection function

Output control	Signal name	Remark
Protect signal of Internal High speed oscillator 2 control bit (***[CGOSCCR]***<IHOSC2EN>)	OSCPRO	Setting by ***[SIWD0OSCCR]***<OSCPRO>

2.4. Oscillation Frequency Detector (OFD)

2.4.1. Built-in list

The following table shows the built-in list for each product.

Table 2.12 OFD built-in list

Product	Built-in OFD (✓: Available, -: N/A)
M4MN	✓
M4MM	✓
M4ML	✓

2.4.2. Reference Clock

The oscillation frequency detection circuit operates considering the clock of the following tables as a reference clock.

Table 2.13 OFD reference clock

Reference clock	Signal name	Divide value
Internal High speed oscillator 2	f_{IHOSC2}	128

2.4.3. Clock for detection

The oscillation frequency detection circuit chooses the clock to monitor from the detection object clock of the following tables.

Table 2.14 OFD clock for detection

Clock for detection		Signal name
Input signal	External High speed oscillator clock	f_{EHOSC}
	Selected clock by the ***[CGOSCCR]***<OSCSEL> and ***[CGPLL0SEL]***<PLL0SEL> in CG(Clock control block)	fc

2.5. Debug interface

2.5.1. Debug interface List for each product

Table 2.15 Debug interface List

Debug function	Debug Pin	Port	Support Pin list (✓: Available, -: N/A)		
			M4MN	M4MM	M4ML
Serial wire	SWDIO	PF0	✓	✓	✓
	SWCLK	PF1	✓	✓	✓
	SWV	PF2	✓	-	-
JTAG	TMS	PF0	✓	-	-
	TCK	PF1	✓	-	-
	TDO	PF2	✓	-	-
	TDI	PF3	✓	-	-
	TRST_N	PF4	✓	-	-
ETM trace	TRACECLK	PF5	✓	-	-
	TRACEDATA0	PF6	✓	-	-
	TRACEDATA1	PF7	✓	-	-
	TRACEDATA2	PN0	✓	-	-
	TRACEDATA3	PN1	✓	-	-

2.5.2. Trace clock division ratio

Table 2.16 Trace clock division ratio

Source Clock	division ratio	Output
fsysh	1/4	TRACECLK

2.6. Non Break Debug Interface (NBDIF)

2.6.1. Correspondence table

The following table shows the NBDIF correspondence of each product.

Table 2.17 NBDIF correspondence table

Product	Function (✓: Available, -: N/A)
M4MN	✓
M4MM	-
M4ML	-

2.6.2. NBDIF list of each product

Table 2.18 NBDIF list

Debug pin (Signal name)		Port	Pin (✓: Available, -: N/A)		
			M4MN	M4MM	M4ML
NBDCLK	Input	PF5	✓	-	-
NBDDATA0	Input/Output	PF6	✓	-	-
NBDDATA1	Input/Output	PF7	✓	-	-
NBDDATA2	Input/Output	PN0	✓	-	-
NBDDATA3	Input/Output	PN1	✓	-	-
NBDSYNC	Input	PF4	✓	-	-

2.7. Flash Memory

2.7.1. Clock for the Programming/Erasing

As for flash memory, the clock of the following tables is used for programming/erasing of the code flash memory or the data flash memory.

Table 2.19 Clock for Programming/Erasing

Clock for Programming/Erasing
f_{IHOSC1}

Note: The oscillation control register is ***[CGOSCCR]***<IHOSC1EN>.

2.7.2. The code flash block configuration of each product

The code flash memory differs in the block configuration of the memory with the product, as shown in the following table.

Table 2.20 The code flash of each product

Area	Block name		M4MNFYA M4MMFYA M4MLFYA	M4MNFWA M4MMFWA M4MLFWA	Block Size (KB)
0	Block0	PG0	✓	✓	4
		PG1	✓	✓	4
		PG2	✓	✓	4
		PG3	✓	✓	4
		PG4	✓	✓	4
		PG5	✓	✓	4
		PG6	✓	✓	4
		PG7	✓	✓	4
	Block1		✓	✓	32
	Block2		✓	✓	32
	Block3		✓	✓	32
	Block4		✓	-	32
	Block5		✓	-	32
	Block6		✓	-	32
	Block7		✓	-	32

Note: ✓: Available, -: N/A

2.7.3. The data flash memory block configuration of each product

The data flash memory differs in the block configuration of the memory with the product, as shown in the following table.

Table 2.21 The data flash memory of each product

Area	Block name	M4MNFYA M4MMFYA M4MLFYA	M4MNFWA M4MMFWA M4MLFWA	Block Size (KB)
4	Block0	✓	✓	4
	Block1	✓	✓	4
	Block2	✓	✓	4
	Block3	✓	✓	4
	Block4	✓	✓	4
	Block5	✓	✓	4
	Block6	✓	✓	4
	Block7	✓	✓	4

Note: ✓: Available, -: N/A

2.7.4. Access control register setting

The settings of access control register ***[FCACCR]***<FDLC[2:0]> and <FCLC[2:0]> are as follows.

Table 2.22 Access Control register *[FCACCR]*<FCLC[2:0]> setting

Bit	Bit Symbol	After Reset	Function
10:8	<FDLC[2:0]>	100	Data flash memory read clock control 100: fsysh > 80MHz 011: fsysh ≤ 80MHz
2:0	<FCLC[2:0]>	100	Code flash memory read clock control 100: fsysh > 80MHz 011: fsysh ≤ 80MHz

2.7.5. Macro code at ID-Read

The macro code values for this product are as follows.

Table 2.23 Macro code at ID-Read

Code	ID[15:0]
Macro code (Code Flash)	0x0411
Macro code (Data flash)	0x0411

2.7.6. Single boot resource

The peripheral function of the following table is used in single boot.

Table 2.24 Single boot resource

Peripheral function	Channel	Function	Pin Name
BOOT	-	-	PG2 (BOOT_N)
UART	ch0	RXD	PC1 (UT0RXD)
		TXD	PC0 (UT0TXDA)
T32A	ch0	-	-

The range of the RAM address transmitted by the RAM loader command should use the following table.

Table 2.25 The address in which RAM transmission is possible

The address in which RAM transmission is possible
0x20000400 to 0x20003FFF

2.8. Direct Memory Access Controller (DMAC)

2.8.1. Built-in unit

The following table shows the built-in unit of each product.

Table 2.26 DMAC built-in unit

Product Name	DMAC unit (✓: Available, -: N/A)
	A
M4MN	✓
M4MM	✓
M4ML	✓

2.8.2. DMA transfer request list

The following tables show the DMA transfer request list.
As for the channel which has a register name in the trigger selector column of a table, choose the request by a trigger selector.
"-" in the table does not have an applicable function.

Table 2.27 DMA transfer request list (1/4)

ch	Single transfer request		Trigger selector	Burst transfer request	
		Signal name			Signal name
0	TSPI ch0 receive DMA request	TSPI0RX_DMA	-	TSPI ch0 receive DMA request	TSPI0RX_DMA
1	TSPI ch0 transmit DMA request	TSPI0TX_DMA	-	TSPI ch0 transmit DMA request	TSPI0TX_DMA
2	TSPI ch1 receive DMA request	TSPI1RX_DMA	-	TSPI ch1 receive DMA request	TSPI1RX_DMA
3	TSPI ch1 transmit DMA request	TSPI1TX_DMA	-	TSPI ch1 transmit DMA request	TSPI1TX_DMA
4	UART ch0 reception DMA request	UART0RX_DMAREQ	-	UART ch0 reception DMA request	UART0RX_DMAREQ
5	UART ch0 transmission DMA request	UART0TX_DMAREQ	-	UART ch0 transmission DMA request	UART0TX_DMAREQ
6	UART ch1 reception DMA request	UART1RX_DMAREQ	-	UART ch1 reception DMA request	UART1RX_DMAREQ
7	UART ch1 transmission DMA request	UART1TX_DMAREQ	-	UART ch1 transmission DMA request	UART1TX_DMAREQ
8	UART ch2 reception DMA request	UART2RX_DMAREQ	-	UART ch2 reception DMA request	UART2RX_DMAREQ
9	UART ch2 transmission DMA request	UART2TX_DMAREQ	-	UART ch2 transmission DMA request	UART2TX_DMAREQ
10	UART ch3 reception DMA request	UART3RX_DMAREQ	-	UART ch3 reception DMA request	UART3RX_DMAREQ
11	UART ch3 transmission DMA request	UART3TX_DMAREQ	-	UART ch3 transmission DMA request	UART3TX_DMAREQ
12	-	-	-	EI2C / I2C ch0 receiving DMA request	I2C0ARXDMAREQ/ I2C0RXDMAREQ
13	-	-	-	EI2C / I2C ch0 transmitting DMA request	I2C0ATXDMAREQ/ I2C0TXDMAREQ
14	-	-	-	EI2C / I2C ch1 receiving DMA request	I2C1ARXDMAREQ/ I2C1RXDMAREQ
15	-	-	-	EI2C / I2C ch1 transmitting DMA request	I2C1ATXDMAREQ/ I2C1TXDMAREQ

Table 2.28 DMA transfer request list (2/4)

ch	Single transfer request		Trigger selector	Burst transfer request	
		Signal name			Signal name
16	-	-	***[TSEL0CR0]*** <INSEL0>	AD unit A general purpose trigger DMA request	ADATRG_DMAREQ
				AD unit A single conversion DMA request	ADASLG_DMAREQ
				AD unit A continue conversion DMA request	ADACNT_DMAREQ
17	-	-	***[TSEL0CR0]*** <INSEL1>	AD unit B general purpose trigger DMA request	ADBTRG_DMAREQ
				AD unit B single conversion DMA request	ADBSLG_DMAREQ
				AD unit B continue conversion DMA request	ADBCNT_DMAREQ
18	-	-	***[TSEL0CR0]*** <INSEL2>	AD unit C general purpose trigger DMA request	ADCTRG_DMAREQ
				AD unit C single conversion DMA request	ADCSLG_DMAREQ
				AD unit C continue conversion DMA request	ADCCNT_DMAREQ
19	-	-	***[TSEL0CR0]*** <INSEL3>	T32A ch0 DMA request at match A1 register	T32A00DMAREQCMPA1
				T32A ch0 DMA request at match C1 register	T32A00DMAREQCMPC1
				T32A ch1 DMA request at match A1 register	T32A01DMAREQCMPA1
				T32A ch1 DMA request at match C1 register	T32A01DMAREQCMPC1
				A-PMD ch0 PWM interrupt	INTPWM0
20	-	-	***[TSEL0CR1]*** <INSEL4>	T32A ch2 DMA request at match A1 register	T32A02DMAREQCMPA1
				T32A ch2 DMA request at match C1 register	T32A02DMAREQCMPC1
				T32A ch3 DMA request at match A1 register	T32A03DMAREQCMPA1
				T32A ch3 DMA request at match C1 register	T32A03DMAREQCMPC1
				A-PMD ch1 PWM interrupt	INTPWM1
21	-	-	***[TSEL0CR1]*** <INSEL5>	T32A ch4 DMA request at match A1 register	T32A04DMAREQCMPA1
				T32A ch4 DMA request at match C1 register	T32A04DMAREQCMPC1
				T32A ch5 DMA request at match A1 register	T32A05DMAREQCMPA1
				T32A ch5 DMA request at match C1 register	T32A05DMAREQCMPC1
				A-PMD ch2 PWM interrupt	INTPWM2
22	-	-	***[TSEL0CR1]*** <INSEL6>	T32A ch0 DMA request at match B1 register	T32A00DMAREQCMPB1
				T32A ch1 DMA request at match B1 register	T32A01DMAREQCMPB1
				T32A ch2 DMA request at match B1 register	T32A02DMAREQCMPB1
				T32A ch3 DMA request at match B1 register	T32A03DMAREQCMPB1
				T32A ch4 DMA request at match B1 register	T32A04DMAREQCMPB1
				T32A ch5 DMA request at match B1 register	T32A05DMAREQCMPB1
23	-	-	***[TSEL0CR1]*** <INSEL7>	T32A ch0 DMA request at capture A0 register	T32A00DMAREQCAPA0
				T32A ch0 DMA request at capture A1 register	T32A00DMAREQCAPA1
				T32A ch1 DMA request at capture A0 register	T32A01DMAREQCAPA0
				T32A ch1 DMA request at capture A1 register	T32A01DMAREQCAPA1
				T32A ch0 DMA request at capture C0 register	T32A00DMAREQCAPC0
				T32A ch0 DMA request at capture C1 register	T32A00DMAREQCAPC1
				T32A ch1 DMA request at capture C0 register	T32A01DMAREQCAPC0
				T32A ch1 DMA request at capture C1 register	T32A01DMAREQCAPC1

Note: Each of ch16 to 31 is set by the trigger source of DMA request. For the detail of connection, refer to the "2.2.Trigger Selector (TRGSEL)".

Table 2.29 DMA transfer request list (3/4)

ch	Single transfer request		Trigger selector	Burst transfer request	
		Signal name			Signal name
24	-	-	***[TSEL0CR2]*** <INSEL8>	T32A ch2 DMA request at capture A0 register	T32A02DMAREQCAPA0
				T32A ch2 DMA request at capture A1 register	T32A02DMAREQCAPA1
				T32A ch3 DMA request at capture A0 register	T32A03DMAREQCAPA0
				T32A ch3 DMA request at capture A1 register	T32A03DMAREQCAPA1
				T32A ch2 DMA request at capture C0 register	T32A02DMAREQCAPC0
				T32A ch2 DMA request at capture C1 register	T32A02DMAREQCAPC1
				T32A ch3 DMA request at capture C0 register	T32A03DMAREQCAPC0
				T32A ch3 DMA request at capture C1 register	T32A03DMAREQCAPC1
25	-	-	***[TSEL0CR2]*** <INSEL9>	T32A ch4 DMA request at capture A0 register	T32A04DMAREQCAPA0
				T32A ch4 DMA request at capture A1 register	T32A04DMAREQCAPA1
				T32A ch5 DMA request at capture A0 register	T32A05DMAREQCAPA0
				T32A ch5 DMA request at capture A1 register	T32A05DMAREQCAPA1
				T32A ch4 DMA request at capture C0 register	T32A04DMAREQCAPC0
				T32A ch4 DMA request at capture C1 register	T32A04DMAREQCAPC1
				T32A ch5 DMA request at capture C0 register	T32A05DMAREQCAPC0
				T32A ch5 DMA request at capture C1 register	T32A05DMAREQCAPC1
26	-	-	***[TSEL0CR2]*** <INSEL10>	T32A ch0 DMA request at capture B0 register	T32A00DMAREQCAPB0
				T32A ch0 DMA request at capture B1 register	T32A00DMAREQCAPB1
				T32A ch1 DMA request at capture B0 register	T32A01DMAREQCAPB0
				T32A ch1 DMA request at capture B1 register	T32A01DMAREQCAPB1
				T32A ch2 DMA request at capture B0 register	T32A02DMAREQCAPB0
				T32A ch2 DMA request at capture B1 register	T32A02DMAREQCAPB1
27	-	-	***[TSEL0CR2]*** <INSEL11>	T32A ch3 DMA request at capture B0 register	T32A03DMAREQCAPB0
				T32A ch3 DMA request at capture B1 register	T32A03DMAREQCAPB1
				T32A ch4 DMA request at capture B0 register	T32A04DMAREQCAPB0
				T32A ch4 DMA request at capture B1 register	T32A04DMAREQCAPB1
				T32A ch5 DMA request at capture B0 register	T32A05DMAREQCAPB0
				T32A ch5 DMA request at capture B1 register	T32A05DMAREQCAPB1

Note: Each of ch16 to 31 is set by the trigger source of DMA request. For the detail of connection, refer to the "2.2.Trigger Selector (TRGSEL)".

Table 2.30 DMA transfer request list (4/4)

ch.	Single transfer request		Trigger selector	Burst transfer request	
		Signal name			Signal name
28	-	-	***[TSEL0CR3]*** <INSEL12>	DMAC ch0 transfer completion	INTDMAATC0
				DMAC ch1 transfer completion	INTDMAATC1
				DMAC ch8 transfer completion	INTDMAATC8
				DMAC ch9 transfer completion	INTDMAATC9
				DMAC ch16 transfer completion	INTDMAATC16
				DMAC ch17 transfer completion	INTDMAATC17
				DMAC ch22 transfer completion	INTDMAATC22
29	-	-	***[TSEL0CR3]*** <INSEL13>	DMAC ch2 transfer completion	INTDMAATC2
				DMAC ch3 transfer completion	INTDMAATC3
				DMAC ch10 transfer completion	INTDMAATC10
				DMAC ch11 transfer completion	INTDMAATC11
				DMAC ch18 transfer completion	INTDMAATC18
				DMAC ch19 transfer completion	INTDMAATC19
				DMAC ch23 transfer completion	INTDMAATC23
				PA2(TRGIN0)	TRGIN0
30	-	-	***[TSEL0CR3]*** <INSEL14>	DMAC ch4 transfer completion	INTDMAATC4
				DMAC ch5 transfer completion	INTDMAATC5
				DMAC ch12 transfer completion	INTDMAATC12
				DMAC ch13 transfer completion	INTDMAATC13
				DMAC ch20 transfer completion	INTDMAATC20
				DMAC ch24 transfer completion	INTDMAATC24
				DMAC ch26 transfer completion	INTDMAATC26
				PA3(TRGIN1)	TRGIN1
31	-	-	***[TSEL0CR3]*** <INSEL15>	DMAC ch6 transfer completion	INTDMAATC6
				DMAC ch7 transfer completion	INTDMAATC7
				DMAC ch14 transfer completion	INTDMAATC14
				DMAC ch15 transfer completion	INTDMAATC15
				DMAC ch21 transfer completion	INTDMAATC21
				DMAC ch25 transfer completion	INTDMAATC25
				DMAC ch27 transfer completion	INTDMAATC27
				PA4(TRGIN2)	TRGIN2

Note: Each of ch16 to 31 is set by the trigger source of DMA request. For the detail of connection, refer to the "2.2.Trigger Selector (TRGSEL)".

2.9. Advanced Programmable Motor Control Circuit (A-PMD)

2.9.1. Built-in channel

The following table shows the A-PMD built-in channel of each product.

Table 2.31 A-PMD built-in channel

Product	A-PMD channel (✓: Available, -: N/A)		
	ch0	ch1	ch2
M4MN	✓	✓	✓
M4MM	✓(Note)	✓(Note)	✓(Note)
M4ML	✓(Note)	✓(Note)	✓(Note)

Note: There is no OVVx pin in M4MM and M4ML.

2.9.2. System clock

The A-PMD operates with the clock in the following table as the system clock.

Table 2.32 A-PMD system clock

clock	Signal name
System clock	fsysm

2.9.3. Function Pin and Port

The function pins are assigned to the ports of the following table.

Table 2.33 A-PMD function pin

Channel	Function pin		Port	Product table (✓: Available, -: N/A)		
				M4MN	M4MM	M4ML
ch0	UO0	Output	PB0	✓	✓	✓
	VO0	Output	PB2	✓	✓	✓
	WO0	Output	PB4	✓	✓	✓
	XO0	Output	PB1	✓	✓	✓
	YO0	Output	PB3	✓	✓	✓
	ZO0	Output	PB5	✓	✓	✓
	EMG0	Input	PB6	✓	✓	✓
	OVV0	Input	PB7	✓	-	-
	PMD0DBG	Output	PB7	✓	-	-
			PC2	✓	✓	✓
ch1	UO1	Output	PE0	✓	✓	✓
	VO1	Output	PE2	✓	✓	✓
	WO1	Output	PE4	✓	✓	✓
	XO1	Output	PE1	✓	✓	✓
	YO1	Output	PE3	✓	✓	✓
	ZO1	Output	PE5	✓	✓	✓
	EMG1	Input	PE6	✓	✓	✓
	OVV1	Input	PE7	✓	-	-
	PMD1DBG	Output	PC3	✓	✓	✓
			PE7	✓	-	-
ch2	UO2	Output	PU0	✓	✓	✓
	VO2	Output	PU2	✓	✓	✓
	WO2	Output	PU4	✓	✓	✓
	XO2	Output	PU1	✓	✓	✓
	YO2	Output	PU3	✓	✓	✓
	ZO2	Output	PU5	✓	✓	✓
	EMG2	Input	PU6	✓	✓	✓
	OVV2	Input	PU7	✓	-	-
	PMD2DBG	Output	PA2	✓	✓	✓
			PU7	✓	-	-

2.9.4. DMA request

The following table shows the DMA request in the A-PMD.

Table 2.34 A-PMD DMA request

Channel	Request	Signal name	Trigger selector	DMA request channel		
					Single transfer	Burst transfer
ch0	PWM interrupt	INTPWM0	***[TSEL0CR0]*** <INSEL3>	19	-	✓
ch1	PWM interrupt	INTPWM1	***[TSEL0CR1]*** <INSEL4>	20	-	✓
ch2	PWM interrupt	INTPWM2	***[TSEL0CR1]*** <INSEL5>	21	-	✓

Note: ✓: Available, -: N/A

2.9.5. Internal signal connection specification

2.9.5.1. Other connection

In the A-PMD, there is a signal connected with the peripheral function inside in addition to this as shown in the following table.

Table 2.35 A-PMD inside connection list: Input

Channel	Function input		Input source	
		Signal name		Signal name
ch0	ADC conversion signal	ADABUSY	ADC unit A	ADABUSY
	ADC monitor function 0 (OVV detection)	ADACMP0L_N		ADACP0L_N
	ADC monitor function 1 (OVV detection)	ADACMP1L_N		ADACP1L_N
	ADC conversion completion interrupt A	INTADAPDA		INTADAPDA
	ADC conversion completion interrupt B	INTADAPDB		INTADAPDB
	ADC conversion completion interrupt C	INTADAPDC	-	-
	ADC conversion completion interrupt D	INTADAPDD		
	ADC conversion priority interrupt	INTADAPFLG		
	Commutation trigger (A-ENC position detect synchronous)	INTENC00	A-ENC32 ch0	INTENC00
	Commutation trigger (General purpose timer synchronous)	PMD0TMR	T32A ch0 Timer A	T32A00TRGOUTCMPA0
	Commutation trigger (A-ENC MCMP completion synchronous)	ENC0CTRGO	A-ENC32 ch0	ENC0CTRGO
	VE U-phase PWM duty	VE0CMPU	A-VE+ ch0	VE0CMPU
	VE V-phase PWM duty	VE0CMPV		VE0CMPV
	VE W-phase PWM duty	VE0CMPW		VE0CMPW
	VE Trigger comparison 0	VE0TRGCMP0		VE0TRGCMP0
	VE Trigger comparison 1	VE0TRGCMP1		VE0TRGCMP1
	VE Trigger output selection	VE0TRGSEL		VE0TRGSEL
	VE Conduction control/Output control	VE0OUTCR		VE0OUTCR
	VE EMG release	VE0EMGRS		VE0EMGRS
	VE Task transition signal	VE0TASKP		VE0DBGO
	VE interrupt	INTVCN0		INTVCN0
ch1	ADC conversion signal	ADBBUSY	ADC unit B	ADBBUSY
	ADC monitor function 0 (OVV detection)	ADBCMP0L_N		ADBCP0L_N
	ADC monitor function1 (OVV detection)	ADBCMP1L_N		ADBCP1L_N
	ADC conversion completion interrupt A	INTADBPDA		INTADBPDA
	ADC conversion completion interrupt B	INTADBPDB		INTADBPDB
	ADC conversion completion interrupt C	INTADBPDC	-	-
	ADC conversion completion interrupt D	INTADBPDD		
	ADC conversion priority interrupt	INTADBPFLG		
	Commutation trigger (A-ENC position detect synchronous)	INTENC10	A-ENC32 ch1	INTENC10
	Commutation trigger (General purpose timer synchronous)	PMD1TMR	T32A ch1 Timer A	T32A01TRGOUTCMPA0
	Commutation trigger (A-ENC MCMP completion synchronous)	ENC1CTRGO	A-ENC32 ch1	ENC1CTRGO
ch2	ADC conversion signal	ADCBUSY	ADC unit C	ADCBUSY
	ADC monitor function 0 (OVV detection)	ADCCMP0L_N		ADCCP0L_N
	ADC monitor function1 (OVV detection)	ADCCMP1L_N		ADCCP1L_N
	ADC conversion completion interrupt A	INTADCPDA		INTADCPDA

Channel	Function input		Input source	
		Signal name		Signal name
	ADC conversion completion interrupt B	INTADCPDB		INTADCPDB
	ADC conversion completion interrupt C	INTADCPDC	-	-
	ADC conversion completion interrupt D	INTADCPDD		
	ADC conversion priority interrupt	INTADCPFLG		
	Commutation trigger (A-ENC position detect synchronous)	INTENC20	A-ENC32 ch2	INTENC20
	Commutation trigger (General purpose timer synchronous)	PMD2TMR	T32A ch2 Timer A	T32A02TRGOUTCMPA0
	Commutation trigger (A-ENC MCMP completion synchronous)	ENC2CTRGO	A-ENC32 ch2	ENC2CTRGO

Note: VE is not connected to ch1 and ch2.

Table 2.36 A-PMD inside connection list: Output

Channel	Function output		Output destination	
		Signal name		Signal name
ch0	ADC synchronous trigger output 0	PMD0TRG0	ADC unit A	PMDTRG0
			ADC unit B	PMDTRG0
			ADC unit C	PMDTRG0
	ADC synchronous trigger output 1	PMD0TRG1	ADC unit A	PMDTRG1
			ADC unit B	PMDTRG1
			ADC unit C	PMDTRG1
	ADC synchronous trigger output 2	PMD0TRG2	ADC unit A	PMDTRG2
			ADC unit B	PMDTRG2
			ADC unit C	PMDTRG2
	ADC synchronous trigger output 3	PMD0TRG3	ADC unit A	PMDTRG3
			ADC unit B	PMDTRG3
			ADC unit C	PMDTRG3
	ADC synchronous trigger output 4	PMD0TRG4	ADC unit A	PMDTRG4
			ADC unit B	PMDTRG4
			ADC unit C	PMDTRG4
	ADC synchronous trigger output 5	PMD0TRG5	ADC unit A	PMDTRG5
			ADC unit B	PMDTRG5
			ADC unit C	PMDTRG5
	PWM signal for the encoder input	PMD0PWMON	A-ENC32 ch0	ENC0PWMON
	PWM interrupt	INTPWM0	A-VE+ ch0	INTPWM0
ch1	ADC synchronous trigger output 0	PMD1TRG0	ADC unit A	PMDTRG6
			ADC unit B	PMDTRG6
	ADC synchronous trigger output 1	PMD1TRG1	ADC unit A	PMDTRG7
			ADC unit B	PMDTRG7
	ADC synchronous trigger output 2	PMD1TRG2	ADC unit A	PMDTRG8
			ADC unit B	PMDTRG8
	ADC synchronous trigger output 3	PMD1TRG3	ADC unit A	PMDTRG9
			ADC unit B	PMDTRG9
	ADC synchronous trigger output 4	PMD1TRG4	ADC unit A	PMDTRG10
			ADC unit B	PMDTRG10
	ADC synchronous trigger output 5	PMD1TRG5	ADC unit A	PMDTRG11
			ADC unit B	PMDTRG11
	PWM signal for the encoder input	PMD1PWMON	A-ENC32 ch1	ENC1PWMON
ch2	ADC synchronous trigger output 0	PMD2TRG0	ADC unit C	PMDTRG6
	ADC synchronous trigger output 1	PMD2TRG1	ADC unit C	PMDTRG7
	ADC synchronous trigger output 2	PMD2TRG2	ADC unit C	PMDTRG8
	ADC synchronous trigger output 3	PMD2TRG3	ADC unit C	PMDTRG9
	ADC synchronous trigger output 4	PMD2TRG4	ADC unit C	PMDTRG10
	ADC synchronous trigger output 5	PMD2TRG5	ADC unit C	PMDTRG11
	PWM signal for the encoder input	PMD2PWMON	A-ENC32 ch2	ENC2PWMON

2.9.5.2. Inter-channel synchronous control connection

The PMD is synchronously connected between the channels as shown in the table below.

Table 2.37 PMD Inter-channel synchronous control connection

Master			Slave		
Channel	**Function(output)**	**Signal name**	**Channel**	**Function(input)**	**Signal name**
ch0	Synchronization output for PWM enable	PMD0SYNCMDENO	ch1	Synchronization input for PWM enable	PMD1SYNCMDENI
			ch2	Synchronization input for PWM enable	PMD2SYNCMDENI
	Synchronization output for EMG protection	PMD0SYNCEMGO	ch1	Synchronization input for EMG protection	PMD1SYNCEMGI
			ch2	Synchronization input for EMG protection	PMD2SYNCEMGI
	Synchronization output for OVV protection	PMD0SYNCOVVO	ch1	Synchronization input for OVV protection	PMD1SYNCOVVI
			ch2	Synchronization input for OVV protection	PMD2SYNCOVVI

2.10. Advanced Encoder Input Circuit(32-bit) (A-ENC32)

2.10.1. Built-in channel

The following table shows the A-ENC built-in channel of each product.

Table 2.38 A-ENC32 built-in channel

Product	A-ENC32 channel (✓: Available, -: N/A)		
	ch0	ch1	ch2
M4MN	✓	✓	✓
M4MM	✓	✓(Note)	✓
M4ML	-	-	✓

Note: There is no ENC1Z terminal.

2.10.2. Function Pin and Port

The function pins are assigned to the ports of the following table.

Table 2.39 A-ENC32 function pin

Channel	Function		Port	Product table (✓: Available, -: N/A)		
				M4MN	M4MM	M4ML
ch0	ENC0A	Input	PN0	✓	✓	-
	ENC0B	Input	PN1	✓	✓	-
	ENC0Z	Input	PN2	✓	✓	-
ch1	ENC1A	Input	PF3	✓	✓	-
	ENC1B	Input	PF4	✓	✓	-
	ENC1Z	Input	PF5	✓	-	-
ch2	ENC2A	Input	PD3	✓	-	-
			PU3	✓	✓	✓
	ENC2B	Input	PD4	✓	-	-
			PU5	✓	✓	✓
	ENC2Z	Input	PD5	✓	-	-
			PU6	✓	✓	✓

2.10.3. Internal signal connection specification

2.10.3.1. T32A/A-PMD Connection

In the A-ENC32, there is a signal connected with the peripheral function inside in addition to this as shown in the following table.

"-" in the table does not have an applicable function.

Table 2.40 A-ENC32 Internal connection specification: Input

Channel	Function Input		Input signal		
		Signal name	Peripheral function		Signal Name
ch0	General purpose timer output signal	ENC0PSGI	T32A ch0	T32A timer A output	T32A00OUTA
	PWM signal for sampling	ENC0PWMON	A-PMD ch0	A-PMD PWM signal	PMD0PWMON
ch1	General purpose timer output signal	ENC1PSGI	T32A ch1	T32A timer A output	T32A01OUTA
	PWM signal for sampling	ENC1PWMON	A-PMD ch1	A-PMD PWM signal	PMD1PWMON
ch2	General purpose timer output signal	ENC2PSGI	T32A ch2	T32A timer A output	T32A02OUTA
	PWM signal for sampling	ENC2PWMON	A-PMD ch2	A-PMD PWM signal	PMD2PWMON

Table 2.41 A-ENC32 Internal connection specification: Output

Channel	Function output		Trigger selector	Output destination		
		Signal name		Peripheral function		Signal name
ch0	Divided pulse	ENC0TIMPLS	***[TSEL0CR7]*** <INSEL28>	T32A ch1	T32A timer A Capture trigger input	T32A01TRGINAPCK
	Commutation trigger output for PMD	ENC0CTRGO	-	A-PMD ch0	PMD commutation trigger(Electrical angle synchronous)	ENC0CTRGO
	Encoder input interrupt 0	INTENC00	-		PMD commutation trigger(ENC position detection synchronous)	INTENC00
ch1	Divided pulse	ENC1TIMPLS	***[TSEL0CR7]*** <INSEL31>	T32A ch2	T32A timer A Capture trigger input	T32A02TRGINAPCK
	Commutation trigger output for PMD	ENC1CTRGO	-	A-PMD ch1	PMD commutation trigger(Electrical angle synchronous)	ENC1CTRGO
	Encoder input interrupt 0	INTENC10	-		PMD commutation trigger(ENC position detection synchronous)	INTENC10
ch2	Divided pulse	ENC2TIMPLS	***[TSEL0CR9]*** <INSEL37>	T32A ch4	T32A timer A Capture trigger input	T32A04TRGINAPCK
	Commutation trigger output for PMD	ENC2CTRGO	-	A-PMD ch2	PMD commutation trigger(Electrical angle synchronous)	ENC2CTRGO
	Encoder input interrupt 0	INTENC20	-		PMD commutation trigger(ENC position detection synchronous)	INTENC20

2.11. Advanced Vector Engine Plus (A-VE+)

2.11.1. Built-in channel

The following table shows the A-VE+ built-in channel of each product.

Table 2.42 A-VE+ built-in channel

Product	A-VE+ channel (✓: Available, -: N/A)
	ch0
M4MN	✓
M4MM	✓
M4ML	✓

2.11.2. Internal signal connection specification

2.11.2.1. Other connection

In the A-VE+, there is a signal connected with the peripheral function inside in addition to this as shown in the following table.

Table 2.43 A-VE+ Internal connection specification: Input

Channel	Input function		Input source	
		Signal name		Signal name
ch0	ADC conversion completion interrupt A	INTADAPDA	ADC unit A	INTADAPDA
	ADC conversion completion interrupt B	INTADAPDB		INTADAPDB
	AD conversion result 0 (Current 1 data)	ADAREG0		ADAREG0
	AD conversion result 1 (Current 2 data)	ADAREG1		ADAREG1
	AD conversion result 2 (Current 3 data)	ADAREG2		ADAREG2
	AD conversion result 3 (DC voltage data)	ADAREG3		ADAREG3
	PWM interrupt	INTPWM0	A-PMD ch0	INTPWM0

Table 2.44 A-VE+ Internal connection specification: Output

Channel	Output function		Output destination	
		Signal name		Signal name
ch0t	U-phase PWM duty	VE0CMPU	A-PMD ch0	VE0CMPU
	V-phase PWM duty	VE0CMPV		VE0CMPV
	W-phase PWM duty	VE0CMPW		VE0CMPW
	Trigger compare 0	VE0TRGCMP0		VE0TRGCMP0
	Trigger compare 1	VE0TRGCMP1		VE0TRGCMP1
	Synchronous trigger output selection	VE0TRGSEL		VE0TRGSEL
	Conduction control / output control	VE0OUTCR		VE0OUTCR
	EMG release	VE0EMGRS		VE0EMGRS
	Task transition signal	VE0DBGO		VE0TASKP
	Schedule end interrupt	INTVCN0		INTVCN0

2.12. 12-bit Analog to Digital Converter (ADC)

2.12.1. Built-in unit

The following table shows the ADC built-in unit of each product.
The operating voltage of the TMPM4M Group(1) ADC is 4.5 to 5.5V.

Table 2.45 ADC built-in unit

Product	ADC unit (✓: Available, -: N/A)		
	A	B	C
M4MN	✓	✓	✓
M4MM	✓	✓	✓
M4ML	✓	✓	✓

2.12.2. Corresponding registers

The following table shows the correspondence registers for each unit of TMPM4M Group(1).

Table 2.46 ADC Corresponding registers for each unit

Unit	General Purpose Start-up Factor Program Register	Conversion Result Storage Register
A	*[ADATSET0] to [ADATSET23]*	*[ADAREG0] to [ADAREG23]*
B	*[ADBTSET0 to [ADBTSET15]*	*[ADBREG0] to [ADBREG15]*
C	*[ADCTSET0] to [ADCTSET15]*	*[ADCREG0] to [ADCREG15]*

2.12.3. Function Pin and Port

The function pins are assigned to the ports of the following table.
There is also a channel which does not have function pins depending on a product.

Table 2.47 ADC function pin and port

Unit		Function pin	Port	Product table (✓: Available, -: N/A)		
	Signal input			M4MN	M4MM	M4ML
A	AINA00 to AINA04	-	-	-	-	-
	AINA05	AINA05	PM2	✓	-	-
	AINA06	AINA06	PM1	✓	-	-
	AINA07	AINA07	PM0	✓	-	-
	AINA08	AINA08	PL7	✓	✓	✓
	AINA09	AINA09	PL6	✓	✓	✓
	AINA10 to AINA12	-	-	-	-	-
	AINA13	AINA13	PL5	✓	✓	✓
	AINA14	AINA14	PL3	✓	✓	✓
	AINA15	AINA15	PL1	✓	✓	✓
	AINA16	AINA16(Note2)	PL0	✓	✓	✓
		AMPA AOUT	-	✓	✓	✓
	AINA17	AINA17(Note2)	PL2	✓	✓	✓
		AMPB AOUT	-	✓	✓	✓
	AINA18	AINA18(Note2)	PL4	✓	✓	✓
		AMPC AOUT	-	✓	✓	✓
	AINA19	VREFHA	-	✓	✓	✓
	AINA20	VREFLA	-	✓	✓	✓
	AINA21	Reference power(Note3)	-	✓	✓	✓
	AINA22, AINA23	-	-	-	-	-
B	AINB00	AINB00	PK0	✓	✓	✓
	AINB01	AINB01	PK1	✓	✓	✓
	AINB02	AINB02	PK2	✓	✓	✓
	AINB03	AINB03	PK3	✓	✓	-
	AINB04	AINB04	PK4	✓	✓	-
	AINB05 to AINB07	-	-	-	-	-
	AINB08	AINA17(Note2)	PL2	✓	✓	✓
		AMPB AOUT	-	✓	✓	✓
	AINB09	VREFHB	-	✓	✓	✓
	AINB10	VREFLB	-	✓	✓	✓
	AINB11	Reference power(Note3)	-	✓	✓	✓
	AINB12 to AINB23	-	-	-	-	-
C	AINC00	AINC00	PJ0	✓	✓	✓
	AINC01	AINC01	PJ1	✓	✓	✓
	AINC02	AINC02	PJ2	✓	✓	✓
	AINC03	AINC03	PJ3	✓	✓	-

Unit		Function pin	Port	Product table (✓: Available, -: N/A)		
	Signal input			M4MN	M4MM	M4ML
	AINC04	AINC04	PJ4	✓	-	-
	AINC05	AINC05	PJ5	✓	-	-
	AINC06, AINC07	-	-	-	-	-
	AINC08	AINA18(Note2)	PL4	✓	✓	✓
		AMPC AOUT	-	✓	✓	✓
	AINC09	VREFHC	-	✓	✓	✓
	AINC10	VREFLC	-	✓	✓	✓
	AINC11	Reference power(Note3)	-	✓	✓	✓
	AINC12 to AINC23	-	-	-	-	-

Note1: AINA19/AINA20/AINA21 of unit A, AINB09/AINB10/AINB11 of unit B, and AINC09/AINC10/AINC11 of unit C are connected to internal signal of MCU for self-check function.

Note2: When OPAMP is not used.

Note3: For the reference power supply, refer to the electrical characteristics of "TMPM4M Group(1) Datasheet".

2.12.4. Analog reference pins

The analog reference pin of ADC is common to units A/B/C. The following table shows the pin assignment of the analog reference pin of each ADC unit.

Table 2.48 Analog reference pin assignment

Unit	Pin name	M4MNxxDFG	M4MNxxFG	M4MMxxDFG M4MMxxFG	M4MLxxUG M4MLxxFG
A	VREFHA/VREFLA	37/34	34/31	29/26	24/21
B	VREFHB/VREFLB				
C	VREFHC/VREFLC				

2.12.5. Conversion clock for ADC

The ADC uses the clock of the following table as a conversion clock.

Table 2.49 Conversion clock for ADC

Clock
ADCLK

2.12.6. Usage conditions and register settings

Table 2.50 and Table 2.51 show the corresponding usage conditions for TMPM4M Group(1).
For Conversion Clock Setting Register (***[ADxCLK]***), Mode Setting Register 1 (***[ADxMOD1]***), and Mode Setting Register 2 (***[ADxMOD2]***), set them to the values in the tables below.

Table 2.50 ADC Usage conditions and register settings (1)

Conversion time [μs]	AVDD5 [V]	Clock		Setting value of register			
		ADCLK [MHz]	SCLK [MHz]	*[ADxCLK]* <VADCLK[2:0]>	*[ADxCLK]* <EXAZ0[3:0]> <EXAZ1[3:0]>	*[ADxMOD1]*	*[ADxMOD2]*
0.96	4.5 to 5.5	160	40	000	0001	0x00306122	0x00000000
0.91	4.5 to 5.5	120	30	000	0000	0x00308012	0x00000000
1.09	4.5 to 5.5	160	20	001	0000	0x00104011	0x00000000
1.09	4.5 to 5.5	80	20	000	0000	0x00104011	0x00000000

When sampling the output of the built-in OP-AMP with 2 units of ADC simultaneously, set the registers to the values in the table below.

Table 2.51 ADC Usage conditions and register settings (2)

Conversion time [μs]	AVDD5 [V]	Clock		Setting value of register			
		ADCLK [MHz]	SCLK [MHz]	*[ADxCLK]* <VADCLK[2:0]>	*[ADxCLK]* <EXAZ0[3:0]> <EXAZ1[3:0]>	*[ADxMOD1]*	*[ADxMOD2]*
1.21	4.5 to 5.5	160	40	000	0011	0x00306122	0x00000000
1.11	4.5 to 5.5	120	30	000	0001	0x00308012	0x00000000
1.29	4.5 to 5.5	160	20	001	0001	0x00104011	0x00000000
1.29	4.5 to 5.5	80	20	000	0001	0x00104011	0x00000000

2.12.7. DMA request

The following table shows the DMA request in the ADC.

Table 2.52 ADC DMA request

Unit	Request	Signal name	Trigger selector	DMA request channel		
					Single transfer	Burst transfer
A	General purpose trigger DMA request	ADATRG_DMAREQ	*[TSEL0CR0]* <INSEL0>	16	-	✓
	Single conversion DMA request	ADASGL_DMAREQ			-	✓
	Continuous conversion DMA request	ADACNT_DMAREQ			-	✓
B	General purpose trigger DMA request	ADBTRG_DMAREQ	*[TSEL0CR0]* <INSEL1>	17	-	✓
	Single conversion DMA request	ADBSGL_DMAREQ			-	✓
	Continuous conversion DMA request	ADBCNT_DMAREQ			-	✓
C	General purpose trigger DMA request	ADCTRG_DMAREQ	*[TSEL0CR0]* <INSEL2>	18	-	✓
	Single conversion DMA request	ADCSGL_DMAREQ			-	✓
	Continuous conversion DMA request	ADCCNT_DMAREQ			-	✓

Note: ✓: Available, -: N/A

2.12.8. Internal signal connection specification

2.12.8.1. Startup trigger

The 12-bit ADC has an AD conversion function with the Trigger signal.

As for the input trigger signal which has the register in the trigger selector column of the following table, choose the input trigger by the register.

"-" in the table does not have an applicable function.

Table 2.53 ADC Startup trigger: Input

Unit	Function input		Trigger selector	Input source	
		Signal name			Signal name
A	PMD0 PMD trigger 0	PMDTRG0	-	A-PMD ch0	PMD0TRG0
	PMD0 PMD trigger 1	PMDTRG1	-		PMD0TRG1
	PMD0 PMD trigger 2	PMDTRG2	-		PMD0TRG2
	PMD0 PMD trigger 3	PMDTRG3	-		PMD0TRG3
	PMD0 PMD trigger 4	PMDTRG4	-		PMD0TRG4
	PMD0 PMD trigger 5	PMDTRG5	-		PMD0TRG5
	PMD1 PMD trigger 0	PMDTRG6		A-PMD ch1	PMD1TRG0
	PMD1 PMD trigger 1	PMDTRG7	-		PMD1TRG1
	PMD1 PMD trigger 2	PMDTRG8	-		PMD1TRG2
	PMD1 PMD trigger 3	PMDTRG9	-		PMD1TRG3
	PMD1 PMD trigger 4	PMDTRG10	-		PMD1TRG4
	PMD1 PMD trigger 5	PMDTRG11	-		PMD1TRG5
	General purpose trigger	ADATRGIN	***[TSEL0CR4]*** <INSEL16>	PA2(TRGIN0)	TRGIN0
				PA3(TRGIN1)	TRGIN1
				PA4(TRGIN2)	TRGIN2
				T32A ch1	T32A01TRGOUTCMPA1
					T32A01TRGOUTCMPB1
					T32A01TRGOUTCMPC1
B	PMD0 PMD trigger 0	PMDTRG0	-	A-PMD ch0	PMD0TRG0
	PMD0 PMD trigger 1	PMDTRG1	-		PMD0TRG1
	PMD0 PMD trigger 2	PMDTRG2	-		PMD0TRG2
	PMD0 PMD trigger 3	PMDTRG3	-		PMD0TRG3
	PMD0 PMD trigger 4	PMDTRG4	-		PMD0TRG4
	PMD0 PMD trigger 5	PMDTRG5	-		PMD0TRG5
	PMD1 PMD trigger 0	PMDTRG6		A-PMD ch1	PMD1TRG0
	PMD1 PMD trigger 1	PMDTRG7	-		PMD1TRG1
	PMD1 PMD trigger 2	PMDTRG8	-		PMD1TRG2
	PMD1 PMD trigger 3	PMDTRG9	-		PMD1TRG3
	PMD1 PMD trigger 4	PMDTRG10	-		PMD1TRG4
	PMD1 PMD trigger 5	PMDTRG11	-		PMD1TRG5
	General purpose trigger	ADBTRGIN	***[TSEL0CR4]*** <INSEL17>	PA2(TRGIN0)	TRGIN0
				PA3(TRGIN1)	TRGIN1
				PA4(TRGIN2)	TRGIN2
				T32A ch3	T32A03TRGOUTCMPA1
					T32A03TRGOUTCMPB1
					T32A03TRGOUTCMPC1

Unit	Function input		Trigger selector	Input source	
		Signal name			Signal name
C	PMD0 PMD trigger 0	PMDTRG0	-	A-PMD ch0	PMD0TRG0
	PMD0 PMD trigger 1	PMDTRG1	-		PMD0TRG1
	PMD0 PMD trigger 2	PMDTRG2	-		PMD0TRG2
	PMD0 PMD trigger 3	PMDTRG3	-		PMD0TRG3
	PMD0 PMD trigger 4	PMDTRG4	-		PMD0TRG4
	PMD0 PMD trigger 5	PMDTRG5	-		PMD0TRG5
	PMD2 PMD trigger 0	PMDTRG6		A-PMD ch2	PMD2TRG0
	PMD2 PMD trigger 1	PMDTRG7	-		PMD2TRG1
	PMD2 PMD trigger 2	PMDTRG8	-		PMD2TRG2
	PMD2 PMD trigger 3	PMDTRG9	-		PMD2TRG3
	PMD2 PMD trigger 4	PMDTRG10	-		PMD2TRG4
	PMD2 PMD trigger 5	PMDTRG11	-		PMD2TRG5
	General purpose trigger	ADCTRGIN	***[TSEL0CR4]*** <INSEL18>	PA2(TRGIN0)	TRGIN0
				PA3(TRGIN1)	TRGIN1
				PA4(TRGIN2)	TRGIN2
				T32A ch5	T32A05TRGOUTCMPA1
					T32A05TRGOUTCMPB1
					T32A05TRGOUTCMPC1

Note: The trigger source is selected by the trigger selector: ***[TSEL0CR4]***<INSEL16><INSEL17><INSEL18> . For the detail of connection, refer to the "2.2.Trigger Selector (TRGSEL)".

2.12.8.2. Other connection

In the ADC, there is a signal connected with the peripheral function inside in addition to this as shown in the following table.

"-" in the table does not have an applicable function.

Table 2.54 ADC inside connection: Output

Unit	Function output		Trigger selector	Output destination	
		Signal name			Signal name
A	General purpose trigger interrupt	INTADATRG	***[TSEL0CR9]*** <INSEL37>	T32A ch4 Timer A	T32A04TRGINAPCK
	Single conversion interrupt	INTADASGL			
	Continuous conversion interrupt	INTADACNT			
	Monitor function 0 interrupt	INTADACP0			
	Monitor function 0 output for PMD protect function	ADACP0L_N	-	A-PMD ch0	ADACMP0L_N
	Monitor function 1 output for PMD protect function	ADACP1L_N	-		ADACMP1L_N
	PMD trigger interrupt A	INTADAPDA	-	A-PMD ch0	INTADAPDA
				A-VE+ ch0	INTADAPDA
	PMD trigger interrupt B	INTADAPDB	-	A-PMD ch0	INTADAPDB
				A-VE+ ch0	INTADAPDB
	AD conversion flag	ADABUSY	-	A-PMD ch0	ADABUSY
	Conversion result storage register	ADAREG0	-	A-VE+ ch0	ADAREG0
		ADAREG1	-		ADAREG1
		ADAREG2	-		ADAREG2
		ADAREG3	-		ADAREG3
B	General purpose trigger interrupt	INTADBTRG	***[TSEL0CR10]*** <INSEL40>	T32A ch5 Timer A	T32A05TRGINAPCK
	Single conversion interrupt	INTADBSGL			
	Continuous conversion interrupt	INTADBCNT			
	Monitor function 0 interrupt	INTADBCP0			
	Monitor function 1 interrupt	INTADBCP1			
	Monitor function 0 output for PMD protect function	ADBCP0L_N	-	A-PMD ch1	ADBCMP0L_N
	Monitor function 1 output for PMD protect function	ADBCP1L_N	-		ADBCMP1L_N
	PMD trigger interrupt A	INTADBPDA	-		INTADBPDA
	PMD trigger interrupt B	INTADBPDB	-		INTADBPDB
	AD conversion flag	ADBBUSY	-		ADBBUSY
C	General purpose trigger interrupt	INTADCTRG	***[TSEL0CR8]*** <INSEL34>	T32A ch3 Timer A	T32A03TRGINAPCK
	Single conversion interrupt	INTADCSGL			
	Continuous conversion interrupt	INTADCCNT			
	Monitor function 0 output for PMD protect function	ADCCP0L_N	-	A-PMD ch2	ADCCMP0L_N
	Monitor function 1 output for PMD protect function	ADCCP1L_N	-		ADCCMP1L_N
	PMD trigger interrupt A	INTADCPDA	-		INTADCPDA
	PMD trigger interrupt B	INTADCPDB	-		INTADCPDB
	AD conversion flag	ADCBUSY	-		ADCBUSY

Note: VE is not connected to unit B and unit C.

2.13. Operational Amplifier (OPAMP)

2.13.1. Built-in unit

The following table shows the OPAMP built-in unit of each product.

Table 2.55 OPAMP built-in unit

Product	OPAMP unit (✓: Available, -: N/A)		
	A	B	C
M4MN	✓	✓	✓
M4MM	✓	✓	✓
M4ML	✓	✓	✓

2.13.2. Function pin and port

The function pins are assigned to the ports of the following table.
There is also a channel which does not have function pins depending on a product.

Table 2.56 OPAMP function pin and port

OPAMP	Signal input	Function pin	Port	Product table (✓: Available, -: N/A)		
				M4MN	M4MM	M4ML
AMPA	AINAP	AINA16	PL0	✓	✓	✓
	AINAM	AINA15	PL1	✓	✓	✓
AMPB	AINBP	AINA17	PL2	✓	✓	✓
	AINBM	AINA14	PL3	✓	✓	✓
AMPC	AINCP	AINA18	PL4	✓	✓	✓
	AINCM	AINA13	PL5	✓	✓	✓

2.13.3. ADC connection

The connection between ADC and OPAMP is as follows.

Table 2.57 OPAMP output connection

OPAMP	Output pin	ADC input pin	Products (✓: Available, -: N/A)		
			M4MN	M4MM	M4ML
AMPA	AMPOUTA	AINA16	✓	✓	✓
AMPB	AMPOUTB	AINA17 / AINB08	✓	✓	✓
AMPC	AMPOUTC	AINA18 / AINC08	✓	✓	✓

2.14. 32-bit Timer Event Counter (T32A)

2.14.1. Built-in channel

The following table shows the T32A built-in channel of each product.

Table 2.58 T32A built-in channel

Product	T32A channel (✓: Available, -: N/A)					
	ch0	ch1	ch2	ch3	ch4	ch5
M4MN	✓	✓	✓	✓	✓	✓
M4MM	✓	✓	✓	✓	✓	✓
M4ML	✓	✓	✓	✓	✓	✓

2.14.2. Function pin and port

The function pins are assigned to the ports of the following tables.
Please do not use simultaneously the same function currently assigned to two or more pins.
There is also a channel which does not have function pins depending on a product.

Table 2.59 T32A function pin and port (1/3)

Channel	Function pin		Port	Ports for products (✓: Available, -: N/A)		
				M4MN	M4MM	M4ML
ch0	T32A00INA0	Input	PA2	✓	✓	✓
	T32A00OUTA	Output	PA3	✓	✓	✓
	T32A00INB0	Input	PA0	✓	✓	-
	T32A00INB1	Input	PA1	✓	✓	-
	T32A00OUTB	Output	PA4	✓	✓	✓
	T32A00INC0	Input	PA2	✓	✓	✓
	T32A00OUTC	Output	PA3	✓	✓	✓
ch1	T32A01INA0	Input	PF3	✓	✓	-
	T32A01INA1	Input	PF5	✓	-	-
	T32A01OUTA	Output	PF4	✓	✓	-
	T32A01INB0	Input	PF6	✓	✓	-
	T32A01INB1	Input	PF7	✓	✓	-
	T32A01OUTB	Output	PV0	✓	-	-
	T32A01INC0	Input	PF3	✓	✓	-
	T32A01INC1	Input	PF5	✓	-	-
	T32A01OUTC	Output	PF4	✓	✓	-

Table 2.60 T32A function pin and port (2/3)

Channel	Function pin		Port	Ports for products (✓: Available, -: N/A)		
				M4MN	M4MM	M4ML
ch2	T32A02INA0	Input	PC0	✓	✓	✓
			PU1	✓	✓	✓
	T32A02INA1	Input	PC6	✓	-	-
			PU5	✓	✓	✓
	T32A02OUTA	Output	PC1	✓	✓	✓
			PU2	✓	✓	✓
	T32A02INB0	Input	PC7	✓	-	-
			PU3	✓	✓	✓
	T32A02INB1	Input	PD0	✓	-	-
			PU0	✓	✓	✓
	T32A02OUTB	Output	PD1	✓	-	-
			PU4	✓	✓	✓
	T32A02INC0	Input	PC0	✓	✓	✓
			PU1	✓	✓	✓
	T32A02INC1	Input	PC6	✓	-	-
			PU4	✓	✓	✓
	T32A02OUTC	Output	PC1	✓	✓	✓
			PU2	✓	✓	✓
ch3	T32A03INA0	Input	PD2	✓	-	-
			PE1	✓	✓	✓
	T32A03INA1	Input	PD3	✓	-	-
			PE3	✓	✓	✓
	T32A03OUTA	Output	PC2	✓	✓	✓
			PE2	✓	✓	✓
	T32A03INB0	Input	PD4	✓	-	-
			PE4	✓	✓	✓
	T32A03INB1	Input	PD5	✓	-	-
			PE5	✓	✓	✓
	T32A03OUTB	Output	PC3	✓	✓	✓
			PE6	✓	✓	✓
	T32A03INC0	Input	PD2	✓	-	-
			PE1	✓	✓	✓
	T32A03INC1	Input	PD3	✓	-	-
			PE3	✓	✓	✓
	T32A03OUTC	Output	PC2	✓	✓	✓
			PE2	✓	✓	✓

Table 2.61 T32A function pin and port (3/3)

Channel	Function pin		Port	Ports for products (✓: Available, -: N/A)		
				M4MN	M4MM	M4ML
ch4	T32A04INA0	Input	PG0	✓	✓	-
	T32A04INA1	Input	PG1	✓	✓	-
	T32A04OUTA	Output	PG2	✓	✓	✓
	T32A04INB0	Input	PG4	✓	✓	✓
	T32A04INB1	Input	PG5	✓	✓	✓
	T32A04OUTB	Output	PG3	✓	✓	✓
	T32A04INC0	Input	PG0	✓	✓	-
	T32A04INC1	Input	PG1	✓	✓	-
	T32A04OUTC	Output	PG2	✓	✓	✓
ch5	T32A05INA0	Input	PF0	✓	✓	✓
			PN0	✓	✓	-
	T32A05INA1	Input	PF2	✓	-	-
			PN2	✓	✓	-
	T32A05OUTA	Output	PF1	✓	✓	✓
			PN1	✓	✓	-
	T32A05INC0	Input	PF0	✓	✓	✓
			PN0	✓	✓	-
	T32A05INC1	Input	PF2	✓	-	-
			PN2	✓	✓	-
	T32A05OUTC	Output	PF1	✓	✓	✓
			PN1	✓	✓	-

2.14.3. Clock for prescaler

The T32A uses the clock of the following table as a prescaler clock.

Table 2.62 T32A clock for prescaler

Clock
ΦT0m

2.14.4. Internal signal connection specification

2.14.4.1. Capture trigger signal connection

In the T32A, capture trigger signals are connected to signals of the following table.
As for the input trigger signal which has the register in the trigger selector column of the following tables, choose the input trigger by the register.

Table 2.63 Capture trigger connection (1/3)

channel			Trigger source		
	Timer	Input signal name of capture trigger	Trigger selector	Input trigger signal	Signal name
ch0	Timer A	T32A00TRGINAPHCK (Other timer output)	-	-	-
		T32A00TRGINAPCK (Internal trigger input)	***[TSEL0CR6]*** <INSEL25>	PA2(TRGIN0)	TRGIN0
				PA3(TRGIN1)	TRGIN1
				PA4(TRGIN2)	TRGIN2
				UART ch0 transmission completion trigger	UART0TXTRG
				UART ch0 reception completion trigger	UART0RXTRG
				TSPI ch0 transmit completion trigger	TSPI0TXEND
				TSPI ch0 receive completion trigger	TSPI0RXEND
				EI2C ch0 status interrupt / I2C ch0 interrupt	INTI2C0ST / INTI2C0
	Timer B	T32A00TRGINBPHCK (Other timer output)	-	T32A ch0 Timer A output	T32A00OUTA
		T32A00TRGINBPCK (Internal trigger input)	***[TSEL0CR6]*** <INSEL26>	T32A ch0 Timer register A0 match trigger	T32A00TRGOUTCMPA0
				T32A ch0 Timer register A1 match trigger	T32A00TRGOUTCMPA1
				T32A ch0 Timer A overflow trigger	T32A00TRGOUTOFA
				T32A ch0 Timer A underflow trigger	T32A00TRGOUTUFA
	Timer C	T32A00TRGINCPHCK (Other timer output)	-	-	-
		T32A00TRGINCPCK (Internal trigger input)	***[TSEL0CR6]*** <INSEL27>	T32A ch5 Timer register C0 match trigger	T32A05TRGOUTCMPC0
				T32A ch5 Timer register C1 match trigger	T32A05TRGOUTCMPC1
				T32A ch5 Timer C overflow trigger	T32A05TRGOUTOFC
				T32A ch5 Timer C underflow trigger	T32A05TRGOUTUFC
ch1	Timer A	T32A01TRGINAPHCK (Other timer output)	-	-	-
		T32A01TRGINAPCK (Internal trigger input)	***[TSEL0CR7]*** <INSEL28>	PA2(TRGIN0)	TRGIN0
				PA3(TRGIN1)	TRGIN1
				PA4(TRGIN2)	TRGIN2
				UART ch1 transmission completion trigger	UART1TXTRG
				UART ch1 reception completion trigger	UART1RXTRG
				TSPI ch1 transmit completion trigger	TSPI1TXEND
				TSPI ch1 receive completion trigger	TSPI1RXEND
				A-ENC32 ch0 divided pulse signal	ENC0TIMPLS
	Timer B	T32A01TRGINBPHCK (Other timer output)	-	T32A ch1 Timer A output	T32A01OUTA
		T32A01TRGINBPCK (Internal trigger input)	***[TSEL0CR7]*** <INSEL29>	T32A ch1 Timer register A0 match trigger	T32A01TRGOUTCMPA0
				T32A ch1 Timer register A1 match trigger	T32A01TRGOUTCMPA1
				T32A ch1 Timer A overflow trigger	T32A01TRGOUTOFA
				T32A ch1 Timer A underflow trigger	T32A01TRGOUTUFA
	Timer C	T32A01TRGINCPHCK (Other timer output)	-	-	-
		T32A01TRGINCPCK (Internal trigger input)	***[TSEL0CR7]*** <INSEL30>	T32A ch0 Timer register C0 match trigger	T32A00TRGOUTCMPC0
				T32A ch0 Timer register C1 match trigger	T32A00TRGOUTCMPC1
				T32A ch0 Timer C overflow trigger	T32A00TRGOUTOFC
				T32A ch0 Timer C underflow trigger	T32A00TRGOUTUFC

Note: The trigger source for the internal trigger is selected by the trigger selector: ***[TSEL0CRn]***<INSELm>.
For the detail of connection, refer to the "2.2.Trigger Selector (TRGSEL)".

Table 2.64 Capture trigger connection (2/3)

channel			Trigger source		
	Timer	Input signal name of capture trigger	Trigger selector	Input trigger signal	Signal name
ch2	Timer A	T32A02TRGINAPHCK (Other timer output)	-	-	-
		T32A02TRGINAPCK (Internal trigger input)	***[TSEL0CR7]*** <INSEL31>	PA2(TRGIN0)	TRGIN0
				PA3(TRGIN1)	TRGIN1
				PA4(TRGIN2)	TRGIN2
				UART ch2 transmission completion trigger	UART2TXTRG
				UART ch2 reception completion trigger	UART2RXTRG
				A-ENC32 ch1 divided pulse signal	ENC1TIMPLS
				EI2C ch1 status interrupt / I2C ch1 interrupt	INTI2C1ST / INTI2C1
	Timer B	T32A02TRGINBPHCK (Other timer output)	-	T32A ch2 Timer A output	T32A02OUTA
		T32A02TRGINBPCK (Internal trigger input)	***[TSEL0CR8]*** <INSEL32>	T32A ch2 Timer register A0 match trigger	T32A02TRGOUTCMPA0
				T32A ch2 Timer register A1 match trigger	T32A02TRGOUTCMPA1
				T32A ch2 Timer A overflow trigger	T32A02TRGOUTOFA
				T32A ch2 Timer A underflow trigger	T32A02TRGOUTUFA
	Timer C	T32A02TRGINCPHCK (Other timer output)	-	-	-
		T32A02TRGINCPCK (Internal trigger input)	***[TSEL0CR8]*** <INSEL33>	T32A ch1 Timer register C0 match trigger	T32A01TRGOUTCMPC0
				T32A ch1 Timer register C1 match trigger	T32A01TRGOUTCMPC1
				T32A ch1 Timer C overflow trigger	T32A01TRGOUTOFC
				T32A ch1 Timer C underflow trigger	T32A01TRGOUTUFC
ch3	Timer A	T32A03TRGINAPHCK (Other timer output)	-	-	-
		T32A03TRGINAPCK (Internal trigger input)	***[TSEL0CR8]*** <INSEL34>	PA2(TRGIN0)	TRGIN0
				PA3(TRGIN1)	TRGIN1
				PA4(TRGIN2)	TRGIN2
				UART ch3 transmission completion trigger	UART3TXTRG
				UART ch3 reception completion trigger	UART3RXTRG
				ADC unit C general purpose trigger interrupt	INTADCTRG
				ADC unit C single conversion interrupt	INTADCSGL
				ADC unit C continuous conversion interrupt	INTADCCNT
	Timer B	T32A03TRGINBPHCK (Other timer output)	-	T32A ch3 Timer A output	T32A03OUTA
		T32A03TRGINBPCK (Internal trigger input)	***[TSEL0CR8]*** <INSEL35>	T32A ch3 Timer register A0 match trigger	T32A03TRGOUTCMPA0
				T32A ch3 Timer register A1 match trigger	T32A03TRGOUTCMPA1
				T32A ch3 Timer A overflow trigger	T32A03TRGOUTOFA
				T32A ch3 Timer A underflow trigger	T32A03TRGOUTUFA
	Timer C	T32A03TRGINCPHCK (Other timer output)	-	-	-
		T32A03TRGINCPCK (Internal trigger input)	***[TSEL0CR9]*** <INSEL36>	T32A ch2 Timer register C0 match trigger	T32A02TRGOUTCMPC0
				T32A ch2 Timer register C1 match trigger	T32A02TRGOUTCMPC1
				T32A ch2 Timer C overflow trigger	T32A02TRGOUTOFC
				T32A ch2 Timer C underflow trigger	T32A02TRGOUTUFC

Note: The trigger source for the internal trigger is selected by the trigger selector: ***[TSEL0CRn]***<INSELm>.
For the detail of connection, refer to the "2.2.Trigger Selector (TRGSEL)".

Table 2.65 T32A Capture trigger connection (3/3)

channel			Trigger source		
	Timer	Input signal name of capture trigger	Trigger selector	Input trigger signal	Signal name
ch4	Timer A	T32A04TRGINAPHCK (Other timer output)	-	-	-
		T32A04TRGINAPCK (Internal trigger input)	***[TSEL0CR9]*** <INSEL37>	PA2(TRGIN0)	TRGIN0
				PA3(TRGIN1)	TRGIN1
				PA4(TRGIN2)	TRGIN2
				ADC unit A general purpose trigger interrupt	INTADATRG
				ADC unit A single conversion interrupt	INTADASGL
				ADC unit A continuous conversion interrupt	INTADACNT
				ADC unit A monitor function 0 interrupt	INTADACP0
				A-ENC32 ch2 divided pulse signal	ENC2TIMPLS
	Timer B	T32A04TRGINBPHCK (Other timer output)	-	T32A ch4 Timer A output	T32A04OUTA
		T32A04TRGINBPCK (Internal trigger input)	***[TSEL0CR9]*** <INSEL38>	T32A ch4 Timer register A0 match trigger	T32A04TRGOUTCMPA0
				T32A ch4 Timer register A1 match trigger	T32A04TRGOUTCMPA1
				T32A ch4 Timer A overflow trigger	T32A04TRGOUTOFA
				T32A ch4 Timer A underflow trigger	T32A04TRGOUTUFA
	Timer C	T32A04TRGINCPHCK (Other timer output)	-	-	-
		T32A04TRGINCPCK (Internal trigger input)	***[TSEL0CR9]*** <INSEL39>	T32A ch3 Timer register C0 match trigger	T32A03TRGOUTCMPC0
				T32A ch3 Timer register C1 match trigger	T32A03TRGOUTCMPC1
				T32A ch3 Timer C overflow trigger	T32A03TRGOUTOFC
				T32A ch3 Timer C underflow trigger	T32A03TRGOUTUFC
ch5	Timer A	T32A05TRGINAPHCK (Other timer output)	-	-	-
		T32A05TRGINAPCK (Internal trigger input)	***[TSEL0CR10]*** <INSEL40>	PA2(TRGIN0)	TRGIN0
				PA3(TRGIN1)	TRGIN1
				PA4(TRGIN2)	TRGIN2
				ADC unit B general purpose trigger interrupt	INTADBTRG
				ADC unit B single conversion interrupt	INTADBSGL
				ADC unit B continuous conversion interrupt	INTADBCNT
				ADC unit B monitor function 0 interrupt	INTADBCP0
				ADC unit B monitor function 1 interrupt	INTADBCP1
	Timer B	T32A05TRGINBPHCK (Other timer output)	-	T32A ch5 Timer A output	T32A05OUTA
		T32A05TRGINBPCK (Internal trigger input)	***[TSEL0CR10]*** <INSEL41>	T32A ch5 Timer register A0 match trigger	T32A05TRGOUTCMPA0
				T32A ch5 Timer register A1 match trigger	T32A05TRGOUTCMPA1
				T32A ch5 Timer A overflow trigger	T32A05TRGOUTOFA
				T32A ch5 Timer A underflow trigger	T32A05TRGOUTUFA
	Timer C	T32A05TRGINCPHCK (Other timer output)	-	-	-
		T32A05TRGINCPCK (Internal trigger input)	***[TSEL0CR10]*** <INSEL42>	T32A ch4 Timer register C0 match trigger	T32A04TRGOUTCMPC0
				T32A ch4 Timer register C1 match trigger	T32A04TRGOUTCMPC1
				T32A ch4 Timer C overflow trigger	T32A04TRGOUTOFC
				T32A ch4 Timer C underflow trigger	T32A04TRGOUTUFC

Note: The trigger source for the internal trigger is selected by the trigger selector: ***[TSEL0CRn]***<INSELm>.
For the detail of connection, refer to the "2.2.Trigger Selector (TRGSEL)".

2.14.4.2. Other connection

Table 2.66 T32A trigger output connection list (1/3)

Channel		Function output		Trigger selector	Output destination	
	Timer		Signal name			Signal name
ch0	Timer A	Timer A output	T32A00OUTA	-	T32A ch0 Timer B	T32A00TRGINBPHCK
				-	A-ENC32 ch0	ENC0PSGI
		Timer register A0 match trigger	T32A00TRGOUTCMPA0	-	A-PMD ch0	PMD0TMR
		Timer register A1 match trigger	T32A00TRGOUTCMPA1	***[TSEL0CR6]*** <INSEL26>	T32A ch0 Timer B	T32A00TRGINBPCK
		Timer A overflow trigger	T32A00TRGOUTOFA			
		Timer A underflow trigger	T32A00TRGOUTUFA			
	Timer B	Timer B output	T32A00OUTB	-	-	-
		Timer B overflow trigger	T32A00TRGOUTOFB	-	-	-
		Timer B underflow trigger	T32A00TRGOUTUFB	-	-	-
		Timer register B0 match trigger	T32A00TRGOUTCMPB0	-	-	-
		Timer register B1 match trigger	T32A00TRGOUTCMPB1	-	-	-
	Timer C	Timer C output	T32A00OUTC	-	-	-
		Timer C overflow trigger	T32A00TRGOUTOFC	***[TSEL0CR7]*** <INSEL30>	T32A ch1 Timer C	T32A01TRGINCPCK
		Timer C underflow trigger	T32A00TRGOUTUFC			
		Timer register C0 match trigger	T32A00TRGOUTCMPC0			
		Timer register C1 match trigger	T32A00TRGOUTCMPC1			
ch1	Timer A	Timer A output	T32A01OUTA	-	T32A ch1 Timer B	T32A01TRGINBPHCK
				-	A-ENC32 ch1	ENC1PSGI
		Timer register A0 match trigger	T32A01TRGOUTCMPA0	-	A-PMD ch1	PMD1TMR
				[TSEL0CR7] <INSEL29>	T32A ch1 Timer B	T32A01TRGINBPCK
		Timer register A1 match trigger	T32A01TRGOUTCMPA1	***[TSEL0CR4]*** <INSEL16>	ADC unit A	ADATRGIN
		Timer A overflow trigger	T32A01TRGOUTOFA	***[TSEL0CR7]*** <INSEL29>	T32A ch1 Timer B	T32A01TRGINBPCK
		Timer A underflow trigger	T32A01TRGOUTUFA			
	Timer B	Timer B output	T32A01OUTB	-	-	-
		Timer B overflow trigger	T32A01TRGOUTOFB	-	-	-
		Timer B underflow trigger	T32A01TRGOUTUFB	-	-	-
		Timer register B0 match trigger	T32A01TRGOUTCMPB0	-	-	-
		Timer register B1 match trigger	T32A01TRGOUTCMPB1	***[TSEL0CR4]*** <INSEL16>	ADC unit A	ADATRGIN
	Timer C	Timer C output	T32A01OUTC	-	-	-
		Timer C overflow trigger	T32A01TRGOUTOFC	***[TSEL0CR8]*** <INSEL33>	T32A ch2 Timer C	T32A02TRGINCPCK
		Timer C underflow trigger	T32A01TRGOUTUFC			
		Timer register C0 match trigger	T32A01TRGOUTCMPC0			
		Timer register C1 match trigger	T32A01TRGOUTCMPC1	***[TSEL0CR4]*** <INSEL16>	ADC unit A	ADATRGIN

Note: The trigger source for the internal trigger is selected by the trigger selector: ***[TSEL0CRn]***<INSELm>.
For the detail of connection, refer to the "2.2.Trigger Selector (TRGSEL)".

Table 2.67 T32A trigger output connection list (2/3)

Channel	Timer	Function output	Signal name	Trigger selector	Output destination	Signal name
ch2	Timer A	Timer A output	T32A02OUTA	-	T32A ch2 Timer B	T32A02TRGINBPHCK
				-	A-ENC32 ch2	ENC2PSGI
		Timer register A0 match trigger	T32A02TRGOUTCMPA0	-	A-PMD ch2	PMD2TMR
		Timer register A1 match trigger	T32A02TRGOUTCMPA1	***[TSEL0CR8]*** <INSEL32>	T32A ch2 Timer B	T32A02TRGINBPCK
		Timer A overflow trigger	T32A02TRGOUTOFA			
		Timer A underflow trigger	T32A02TRGOUTUFA			
	Timer B	Timer B output	T32A02OUTB	-	-	-
		Timer B overflow trigger	T32A02TRGOUTOFB	-	-	-
		Timer B underflow trigger	T32A02TRGOUTUFB	-	-	-
		Timer register B0 match trigger	T32A02TRGOUTCMPB0	-	-	-
		Timer register B1 match trigger	T32A02TRGOUTCMPB1	-	-	-
	Timer C	Timer C output	T32A02OUTC	-	-	-
		Timer C overflow trigger	T32A02TRGOUTOFC	***[TSEL0CR9]*** <INSEL36>	T32A ch3 Timer C	T32A03TRGINCPCK
		Timer C underflow trigger	T32A02TRGOUTUFC			
		Timer register C0 match trigger	T32A02TRGOUTCMPC0			
		Timer register C1 match trigger	T32A02TRGOUTCMPC1			
ch3	Timer A	Timer A output	T32A03OUTA	-	T32A ch3 Timer B	T32A03TRGINBPHCK
		Timer A overflow trigger	T32A03TRGOUTOFA	***[TSEL0CR8]*** <INSEL35>	T32A ch3 Timer B	T32A03TRGINBPCK
		Timer A underflow trigger	T32A03TRGOUTUFA			
		Timer register A0 match trigger	T32A03TRGOUTCMPA0			
		Timer register A1 match trigger	T32A03TRGOUTCMPA1	***[TSEL0CR4]*** <INSEL17>	ADC unit B	ADBTRGIN
	Timer B	Timer B output	T32A03OUTB	-	-	-
		Timer B overflow trigger	T32A03TRGOUTOFB	-	-	-
		Timer B underflow trigger	T32A03TRGOUTUFB	-	-	-
		Timer register B0 match trigger	T32A03TRGOUTCMPB0	-	-	-
		Timer register B1 match trigger	T32A03TRGOUTCMPB1	***[TSEL0CR4]*** <INSEL17>	ADC unit B	ADBTRGIN
	Timer C	Timer C output	T32A03OUTC	-	-	-
		Timer C overflow trigger	T32A03TRGOUTOFC	***[TSEL0CR9]*** <INSEL39>	T32A ch4 Timer C	T32A04TRGINCPCK
		Timer C underflow trigger	T32A03TRGOUTUFC			
		Timer register C0 match trigger	T32A03TRGOUTCMPC0			
		Timer register C1 match trigger	T32A03TRGOUTCMPC1	***[TSEL0CR4]*** <INSEL17>	ADC unit B	ADBTRGIN
ch4	Timer A	Timer A output	T32A04OUTA	-	T32A ch4 Timer B	T32A04TRGINBPHCK
		Timer A overflow trigger	T32A04TRGOUTOFA	***[TSEL0CR9]*** <INSEL38>	T32A ch4 Timer B	T32A04TRGINBPCK
		Timer A underflow trigger	T32A04TRGOUTUFA			
		Timer register A0 match trigger	T32A04TRGOUTCMPA0			
		Timer register A1 match trigger	T32A04TRGOUTCMPA1			
	Timer B	Timer B output	T32A04OUTB	-	-	-
		Timer B overflow trigger	T32A04TRGOUTOFB	-	-	-
		Timer B underflow trigger	T32A04TRGOUTUFB	-	-	-
		Timer register B0 match trigger	T32A04TRGOUTCMPB0	-	-	-
		Timer register B1 match trigger	T32A04TRGOUTCMPB1	-	-	-
	Timer C	Timer C output	T32A04OUTC	-	-	-
		Timer C overflow trigger	T32A04TRGOUTOFC	***[TSEL0CR10]*** <INSEL42>	T32A ch5 Timer C	T32A05TRGINCPCK
		Timer C underflow trigger	T32A04TRGOUTUFC			
		Timer register C0 match trigger	T32A04TRGOUTCMPC0			
		Timer register C1 match trigger	T32A04TRGOUTCMPC1			

Note: The trigger source for the internal trigger is selected by the trigger selector: ***[TSEL0CRn]***<INSELm>.
For the detail of connection, refer to the "2.2.Trigger Selector (TRGSEL)".

Table 2.68 T32A trigger output connection list (3/3)

Channel	Timer	Function output	Signal name	Trigger selector	Output destination	Signal name
ch5	Timer A	Timer A output	T32A05OUTA	-	T32A ch5 Timer B	T32A05TRGINBPHCK
		Timer A overflow trigger	T32A05TRGOUTOFA	***[TSEL0CR10]*** <INSEL41>	T32A ch5 Timer B	T32A05TRGINBPCK
		Timer A underflow trigger	T32A05TRGOUTUFA			
		Timer register A0 match trigger	T32A05TRGOUTCMPA0			
		Timer register A1 match trigger	T32A05TRGOUTCMPA1	***[TSEL0CR4]*** <INSEL18>	ADC unit C	ADCTRGIN
				[TSEL0CR4] <INSEL19>	TSPI ch0	TSPI0TRG
				[TSEL0CR5] <INSEL20>	TSPI ch1	TSPI1TRG
				[TSEL0CR5] <INSEL21>	UART ch0	UART0TRGIN
				[TSEL0CR5] <INSEL22>	UART ch1	UART1TRGIN
				[TSEL0CR5] <INSEL23>	UART ch2	UART2TRGIN
				[TSEL0CR6] <INSEL24>	UART ch3	UART3TRGIN
	Timer B	Timer B output	T32A05OUTB	-	-	-
		Timer B overflow trigger	T32A05TRGOUTOFB	-	-	-
		Timer B underflow trigger	T32A05TRGOUTUFB	-	-	-
		Timer register B0 match trigger	T32A05TRGOUTCMPB0	-	-	-
		Timer register B1 match trigger	T32A05TRGOUTCMPB1	***[TSEL0CR4]*** <INSEL18>	ADC unit C	ADCTRGIN
				[TSEL0CR4] <INSEL19>	TSPI ch0	TSPI0TRG
				[TSEL0CR5] <INSEL20>	TSPI ch1	TSPI1TRG
				[TSEL0CR5] <INSEL21>	UART ch0	UART0TRGIN
				[TSEL0CR5] <INSEL22>	UART ch1	UART1TRGIN
				[TSEL0CR5] <INSEL23>	UART ch2	UART2TRGIN
				[TSEL0CR6] <INSEL24>	UART ch3	UART3TRGIN
	Timer C	Timer C output	T32A05OUTC	-	-	-
		Timer C overflow trigger	T32A05TRGOUTOFC	***[TSEL0CR6]*** <INSEL27>	T32A ch0 Timer C	T32A00TRGINCPCK
		Timer C underflow trigger	T32A05TRGOUTUFC			
		Timer register C0 match trigger	T32A05TRGOUTCMPC0			
		Timer register C1 match trigger	T32A05TRGOUTCMPC1	***[TSEL0CR4]*** <INSEL18>	ADC unit C	ADCTRGIN
				[TSEL0CR4] <INSEL19>	TSPI ch0	TSPI0TRG
				[TSEL0CR5] <INSEL20>	TSPI ch1	TSPI1TRG
				[TSEL0CR5] <INSEL21>	UART ch0	UART0TRGIN
				[TSEL0CR5] <INSEL22>	UART ch1	UART1TRGIN
				[TSEL0CR5] <INSEL23>	UART ch2	UART2TRGIN
				[TSEL0CR6] <INSEL24>	UART ch3	UART3TRGIN

Note: The trigger source for the internal trigger is selected by the trigger selector: ***[TSEL0CRn]***<INSELm>. For the detail of connection, refer to the "2.2.Trigger Selector (TRGSEL)".

2.14.4.3. Synchronous control connection

In the T32A, as shown in the following table, synchronous connection of the timer is carried out within the same channel.

Table 2.69 Synchronous control connection specifications

Channel	Timer	Master		Timer	Slave	
		Function(output)	Signal name		Function(input)	Signal name
ch0	Timer A	Synchronous start output A	T32A00SYNCSTARTOUTA	Timer B	Synchronous start B	T32A00SYNCSTARTB
		Synchronous stop output A	T32A00SYNCSTOPOUTA		Synchronous stop B	T32A00SYNCSTOPB
		Synchronous Reload output A	T32A00SYNCRELOADOUTA		Synchronous Reload B	T32A00SYNCRELOADB
ch1	Timer A	Synchronous start output A	T32A01SYNCSTARTOUTA	Timer B	Synchronous start B	T32A01SYNCSTARTB
		Synchronous stop output A	T32A01SYNCSTOPOUTA		Synchronous stop B	T32A01SYNCSTOPB
		Synchronous Reload output A	T32A01SYNCRELOADOUTA		Synchronous Reload B	T32A01SYNCRELOADB
ch2	Timer A	Synchronous start output A	T32A02SYNCSTARTOUTA	Timer B	Synchronous start B	T32A02SYNCSTARTB
		Synchronous stop output A	T32A02SYNCSTOPOUTA		Synchronous stop B	T32A02SYNCSTOPB
		Synchronous Reload output A	T32A02SYNCRELOADOUTA		Synchronous Reload B	T32A02SYNCRELOADB
ch3	Timer A	Synchronous start output A	T32A03SYNCSTARTOUTA	Timer B	Synchronous start B	T32A03SYNCSTARTB
		Synchronous stop output A	T32A03SYNCSTOPOUTA		Synchronous stop B	T32A03SYNCSTOPB
		Synchronous Reload output A	T32A03SYNCRELOADOUTA		Synchronous Reload B	T32A03SYNCRELOADB
ch4	Timer A	Synchronous start output A	T32A04SYNCSTARTOUTA	Timer B	Synchronous start B	T32A04SYNCSTARTB
		Synchronous stop output A	T32A04SYNCSTOPOUTA		Synchronous stop B	T32A04SYNCSTOPB
		Synchronous Reload output A	T32A04SYNCRELOADOUTA		Synchronous Reload B	T32A04SYNCRELOADB
ch5	Timer A	Synchronous start output A	T32A05SYNCSTARTOUTA	Timer B	Synchronous start B	T32A05SYNCSTARTB
		Synchronous stop output A	T32A05SYNCSTOPOUTA		Synchronous stop B	T32A05SYNCSTOPB
		Synchronous Reload output A	T32A05SYNCRELOADOUTA		Synchronous Reload B	T32A05SYNCRELOADB

2.14.5. Pulse Counter List for each product

In the T32A, as shown in the following tables, correspondence of a pulse counter changes with products.

Table 2.70 T32A Pulse counter list for each product

Channel	Support Mode (-: Not available)		
	M4MN	M4MM	M4ML
ch0	1-phase pulse count		
ch1	2-phase pulse count 1-phase pulse count	1-phase pulse count	-
ch2	2-phase pulse count 1-phase pulse count		
ch3	2-phase pulse count 1-phase pulse count		
ch4	2-phase pulse count 1-phase pulse count		-
ch5	2-phase pulse count 1-phase pulse count		1-phase pulse count

2.14.6. DMA request

The T32A has the DMA request shown in the following tables.
When there is mention of the register name in the trigger selector column of the table, please select a request to use with a trigger selector.

Table 2.71 T32A DMA request (1/2)

Channel	Request	Signal name	Trigger selector	DMA request channel		
					Single transfer	Burst transfer
ch0	DMA request at match A1 register	T32A00DMAREQCMPA1	***[TSEL0CR0]*** <INSEL3>	19	-	✓
	DMA request at match C1 register	T32A00DMAREQCMPC1				
	DMA request at match B1 register	T32A00DMAREQCMPB1	***[TSEL0CR1]*** <INSEL6>	22	-	✓
	DMA request at capture A0 register	T32A00DMAREQCAPA0	***[TSEL0CR1]*** <INSEL7>	23	-	✓
	DMA request at capture A1 register	T32A00DMAREQCAPA1				
	DMA request at capture C0 register	T32A00DMAREQCAPC0				
	DMA request at capture C1 register	T32A00DMAREQCAPC1				
	DMA request at capture B0 register	T32A00DMAREQCAPB0	***[TSEL0CR2]*** <INSEL10>	26	-	✓
	DMA request at capture B1 register	T32A00DMAREQCAPB1				
ch1	DMA request at match A1 register	T32A01DMAREQCMPA1	***[TSEL0CR0]*** <INSEL3>	19	-	✓
	DMA request at match C1 register	T32A01DMAREQCMPC1				
	DMA request at match B1 register	T32A01DMAREQCMPB1	***[TSEL0CR1]*** <INSEL6>	22	-	✓
	DMA request at capture A0 register	T32A01DMAREQCAPA0	***[TSEL0CR1]*** <INSEL7>	23	-	✓
	DMA request at capture A1 register	T32A01DMAREQCAPA1				
	DMA request at capture C0 register	T32A01DMAREQCAPC0				
	DMA request at capture C1 register	T32A01DMAREQCAPC1				
	DMA request at capture B0 register	T32A01DMAREQCAPB0	***[TSEL0CR2]*** <INSEL10>	26	-	✓
	DMA request at capture B1 register	T32A01DMAREQCAPB1				
ch2	DMA request at match A1 register	T32A02DMAREQCMPA1	***[TSEL0CR1]*** <INSEL4>	20	-	✓
	DMA request at match C1 register	T32A02DMAREQCMPC1				
	DMA request at match B1 register	T32A02DMAREQCMPB1	***[TSEL0CR1]*** <INSEL6>	22	-	✓
	DMA request at capture A0 register	T32A02DMAREQCAPA0	***[TSEL0CR2]*** <INSEL8>	24	-	✓
	DMA request at capture A1 register	T32A02DMAREQCAPA1				
	DMA request at capture C0 register	T32A02DMAREQCAPC0				
	DMA request at capture C1 register	T32A02DMAREQCAPC1				
	DMA request at capture B0 register	T32A02DMAREQCAPB0	***[TSEL0CR2]*** <INSEL10>	26	-	✓
	DMA request at capture B1 register	T32A02DMAREQCAPB1				

Note: ✓: Available, -: N/A

Table 2.72 T32A DMA request (2/2)

Channel	Request	Signal name	Trigger selector	DMA request channel		
					Single transfer	Burst transfer
ch3	DMA request at match A1 register	T32A03DMAREQCMPA1	***[TSEL0CR1]*** <INSEL4>	20	-	✓
	DMA request at match C1 register	T32A03DMAREQCMPC1				
	DMA request at match B1 register	T32A03DMAREQCMPB1	***[TSEL0CR1]*** <INSEL6>	22	-	✓
	DMA request at capture A0 register	T32A03DMAREQCAPA0	***[TSEL0CR2]*** <INSEL8>	24	-	✓
	DMA request at capture A1 register	T32A03DMAREQCAPA1				
	DMA request at capture C0 register	T32A03DMAREQCAPC0				
	DMA request at capture C1 register	T32A03DMAREQCAPC1				
	DMA request at capture B0 register	T32A03DMAREQCAPB0	***[TSEL0CR2]*** <INSEL11>	27	-	✓
	DMA request at capture B1 register	T32A03DMAREQCAPB1				
ch4	DMA request at match A1 register	T32A04DMAREQCMPA1	***[TSEL0CR1]*** <INSEL5>	21	-	✓
	DMA request at match C1 register	T32A04DMAREQCMPC1				
	DMA request at match B1 register	T32A04DMAREQCMPB1	***[TSEL0CR1]*** <INSEL6>	22	-	✓
	DMA request at capture A0 register	T32A04DMAREQCAPA0	***[TSEL0CR2]*** <INSEL9>	25	-	✓
	DMA request at capture A1 register	T32A04DMAREQCAPA1				
	DMA request at capture C0 register	T32A04DMAREQCAPC0				
	DMA request at capture C1 register	T32A04DMAREQCAPC1				
	DMA request at capture B0 register	T32A04DMAREQCAPB0	***[TSEL0CR2]*** <INSEL11>	27	-	✓
	DMA request at capture B1 register	T32A04DMAREQCAPB1				
ch5	DMA request at match A1 register	T32A05DMAREQCMPA1	***[TSEL0CR1]*** <INSEL5>	21	-	✓
	DMA request at match C1 register	T32A05DMAREQCMPC1				
	DMA request at match B1 register	T32A05DMAREQCMPB1	***[TSEL0CR1]*** <INSEL6>	22	-	✓
	DMA request at capture A0 register	T32A05DMAREQCAPA0	***[TSEL0CR2]*** <INSEL9>	25	-	✓
	DMA request at capture A1 register	T32A05DMAREQCAPA1				
	DMA request at capture C0 register	T32A05DMAREQCAPC0				
	DMA request at capture C1 register	T32A05DMAREQCAPC1				
	DMA request at capture B0 register	T32A05DMAREQCAPB0	***[TSEL0CR2]*** <INSEL11>	27	-	✓
	DMA request at capture B1 register	T32A05DMAREQCAPB1				

Note: ✓: Available, -: N/A

2.14.7. Unsupported interrupt

Every count interrupt (INTT32AxEVRYC) does not correspond in the TMPM4M Group(1).

2.15. Universal Asynchronous Receiver Transmitter Circuit (UART)

2.15.1. Built-in channel

The following table shows the UART built-in channel of each product.
In TMPM4M Group(1), Maximum Communication speed of UART is 5.0 Mbps.

Table 2.73 UART built-in channel

Product	UART channel (✓: Available, -: N/A)			
	ch0	ch1	ch2	ch3
M4MN	✓	✓	✓	✓
M4MM	✓	✓	✓	✓
M4ML	✓	✓	✓	-

2.15.2. Function Pin and Port

The function pins are assigned to the ports of the following table.
Please do not use simultaneously the same function currently assigned to two or more pins.
There is also a channel which does not have function pins depending on a product.

Table 2.74 UART function pin and port

Channel	Function Pin		Port	Product table (✓: Available, -: N/A)		
				M4MN	M4MM	M4ML
ch0	UT0TXDA	Output	PC0	✓	✓	✓
			PC1	✓	✓	✓
			PN0	✓	✓	-
			PN1	✓	✓	-
	UT0RXD	Input	PC0	✓	✓	✓
			PC1	✓	✓	✓
			PN0	✓	✓	-
			PN1	✓	✓	-
	UT0CTS	Output	PD2	✓	-	-
			PN2	✓	✓	-
	UT0RTS	Input	PD3	✓	-	-
			PV1	✓	-	-
ch1	UT1TXDA	Output	PC4	✓	✓	-
			PC5	✓	✓	-
			PU5	✓	✓	✓
			PU6	✓	✓	✓
	UT1RXD	Input	PC4	✓	✓	-
			PC5	✓	✓	-
			PU5	✓	✓	✓
			PU6	✓	✓	✓
	UT1CTS	Output	PU4	✓	✓	✓
	UT1RTS	Input	PU3	✓	✓	✓
ch2	UT2TXDA	Output	PF0	✓	✓	✓
			PF1	✓	✓	✓
			PU0	✓	✓	✓
			PU1	✓	✓	✓
	UT2RXD	Input	PF0	✓	✓	✓
			PF1	✓	✓	✓
			PU0	✓	✓	✓
			PU1	✓	✓	✓
ch3	UT3TXDA	Output	PF3	✓	✓	-
			PF4	✓	✓	-
			PF6	✓	✓	-
			PF7	✓	✓	-
	UT3RXD	Input	PF3	✓	✓	-
			PF4	✓	✓	-
			PF6	✓	✓	-
			PF7	✓	✓	-

2.15.3. Half Clock mode support

Half clock mode of the UART corresponds to 1-pin mode only.

2.15.4. Clock for Prescaler

The UART uses the clock of the following table as a prescaler clock.

Table 2.75 UART Clock for prescaler

Clock
ΦT0m

2.15.5. DMA request

The following table shows the DMA request in the UART.

Table 2.76 UART DMA request

Channel	Request	Signal Name	DMA request channel		
				Single transfer	Burst transfer
ch0	Reception DMA request	UART0RX_DMAREQ	4	✓	✓
	Transmission DMA request	UART0TX_DMAREQ	5	✓	✓
ch1	Reception DMA request	UART1RX_DMAREQ	6	✓	✓
	Transmission DMA request	UART1TX_DMAREQ	7	✓	✓
ch2	Reception DMA request	UART2RX_DMAREQ	8	✓	✓
	Transfer DMA request	UART2TX_DMAREQ	9	✓	✓
ch3	Reception DMA request	UART3RX_DMAREQ	10	✓	✓
	Transmission DMA request	UART3TX_DMAREQ	11	✓	✓

Note: ✓: Available, -: N/A

2.15.6. Internal signal connection specification

2.15.6.1. Trigger transfer signal connection

Transfer function of the UART has a trigger signal control.
A trigger control signal is selected with the trigger source and use it as the following table.

Table 2.77 UART trigger transfer signal connection: Input

Channel	Function input		Trigger selector	Trigger source	
		Signal name		Input trigger signal	Signal name
ch0	Trigger transmission signal input	UART0TRGIN	***[TSEL0CR5]*** <INSEL21>	PA2(TRGIN0)	TRGIN0
				PA3(TRGIN1)	TRGIN1
				PA4(TRGIN2)	TRGIN2
				T32A ch5 timer register A1match trigger	T32A05TRGOUTCMPA1
				T32A ch5 timer register B1match trigger	T32A05TRGOUTCMPB1
				T32A ch5 timer register C1 match trigger	T32A05TRGOUTCMPC1
ch1	Trigger transmission signal input	UART1TRGIN	***[TSEL0CR5]*** <INSEL22>	PA2(TRGIN0)	TRGIN0
				PA3(TRGIN1)	TRGIN1
				PA4(TRGIN2)	TRGIN2
				T32A ch5 timer register A1 match trigger	T32A05TRGOUTCMPA1
				T32A ch5 timer register B1 match trigger	T32A05TRGOUTCMPB1
				T32A ch5 timer register C1 match trigger	T32A05TRGOUTCMPC1
ch2	Trigger transmission signal input	UART2TRGIN	***[TSEL0CR5]*** <INSEL23>	PA2(TRGIN0)	TRGIN0
				PA3(TRGIN1)	TRGIN1
				PA4(TRGIN2)	TRGIN2
				T32A ch5 timer register A1 match trigger	T32A05TRGOUTCMPA1
				T32A ch5 timer register B1 match trigger	T32A05TRGOUTCMPB1
				T32A ch5 timer register C1 match trigger	T32A05TRGOUTCMPC1
ch3	Trigger transmission signal input	UART3TRGIN	***[TSEL0CR6]*** <INSEL24>	PA2(TRGIN0)	TRGIN0
				PA3(TRGIN1)	TRGIN1
				PA4(TRGIN2)	TRGIN2
				T32A ch5 timer register A1 match trigger	T32A05TRGOUTCMPA1
				T32A ch5 timer register B1 match trigger	T32A05TRGOUTCMPB1
				T32A ch5 timer register C1 match trigger	T32A05TRGOUTCMPC1

Note: The trigger source for the trigger signal is selected by the trigger selector: ***[TSEL0CRn]***<INSELm> .
For the detail of connection, refer to the "2.2.Trigger Selector (TRGSEL)".

2.15.6.2. T32A connection

In the UART, there is a signal connected with the peripheral function inside in addition to this as shown in the following table.

Table 2.78 UART inside connection list: Output

Channel	Function output		Trigger selector	Output destination	
		Signal name			Signal name
ch0	Transmission completion trigger	UART0TXTRG	***[TSEL0CR6]*** <INSEL25>	T32A ch0 Timer A	T32A00TRGINAPCK
	Reception completion trigger	UART0RXTRG			
ch1	Transmission completion trigger	UART1TXTRG	***[TSEL0CR7]*** <INSEL28>	T32A ch1 Timer A	T32A01TRGINAPCK
	Reception completion trigger	UART1RXTRG			
ch2	Transmission completion trigger	UART2TXTRG	***[TSEL0CR7]*** <INSEL31>	T32A ch2 Timer A	T32A02TRGINAPCK
	Reception completion trigger	UART2RXTRG			
ch3	Transmission completion trigger	UART3TXTRG	***[TSEL0CR8]*** <INSEL34>	T32A ch3 Timer A	T32A03TRGINAPCK
	Reception completion trigger	UART3RXTRG			

2.16. I²C interface (I2C)

2.16.1. Built-in channel

The following table shows the I²C interface built-in channel of each product.
In the TMPM4M Group(1), the I²C interface supports Standard mode and Fast mode.

Table 2.79 I2C built-in channel

Product	Channel (✓: Available, -: N/A)	
	ch0	ch1
M4MN	✓	✓
M4MM	✓	✓
M4ML	✓	✓

2.16.2. Function Pin and Port

The function pins are assigned to the ports of the following table.

Table 2.80 I2C function pin and port

Channel	Function pin		Port	Product table (✓: Available, -: N/A)		
				M4MN	M4MM	M4ML
ch0	I2C0SCL	I/O	PC1	✓	✓	✓
	I2C0SDA	I/O	PC0	✓	✓	✓
ch1	I2C1SCL	I/O	PD4	✓	-	-
			PU1	✓	✓	✓
	I2C1SDA	I/O	PD3	✓	-	-
			PU0	✓	✓	✓

2.16.3. Clock for Prescaler

The I²C interface uses the clock of the following table as a prescaler clock.

Table 2.81 I2C clock for prescaler

Clock
fsysm

2.16.4. Wakeup function

TMPM4M Group(1) products do not support I^2C interface wakeup function.

2.16.5. DMA request

The following table shows the DMA request in the I^2C interface.

Table 2.82 I2C DMA request

Channel	Request	Signal name	DMA request channel		
				Single transfer	Burst transfer
ch0	Receiving DMA request	I2C0RXDMAREQ	12	-	✓
	Transmitting DMA request	I2C0TXDMAREQ	13	-	✓
ch1	Receiving DMA request	I2C1RXDMAREQ	14	-	✓
	Transmitting DMA request	I2C1TXDMAREQ	15	-	✓

Note: ✓: Available, -: N/A

2.17. I²C interface Version A (EI2C)

2.17.1. Built-in channel

The following table shows the I²C interface version A built-in channel of each product.
In the TMPM4M Group(1), the I²C interface version A supports Standard mode, Fast mode, and Fast mode plus.

Table 2.83 EI2C built-in channel

Product	Channel (✓: Available, -: N/A)	
	ch0	ch1
M4MN	✓	✓
M4MM	✓	✓
M4ML	✓	✓

2.17.2. Function Pin and Port

The function pins are assigned to the ports of the following table.

Table 2.84 EI2C function pin and port

Channel	Function pin		Port	Product table (✓: Available, -: N/A)		
				M4MN	M4MM	M4ML
ch0	EI2C0SCL	I/O	PC1	✓	✓	✓
	EI2C0SDA	I/O	PC0	✓	✓	✓
ch1	EI2C1SCL	I/O	PD4	✓	-	-
			PU1	✓	✓	✓
	EI2C1SDA	I/O	PD3	✓	-	-
			PU0	✓	✓	✓

2.17.3. Clock for Prescaler

The I²C interface version A uses the clock of the following table as a prescaler clock.

Table 2.85 EI2C clock for prescaler

Clock
fsysm

2.17.4. Wakeup function

TMPM4M Group(1) products do not support I^2C interface Version A wakeup function.

2.17.5. DMA request

The following table shows the DMA request in the I^2C interface version A.

Table 2.86 EI2C DMA request

Channel	Request	Signal name	DMA request channel		
				Single transfer	Burst transfer
ch0	Receiving DMA request	I2C0ARXDMAREQ	12	-	✓
	Transmitting DMA request	I2C0ATXDMAREQ	13	-	✓
ch1	Receiving DMA request	I2C1ARXDMAREQ	14	-	✓
	Transmitting DMA request	I2C1ATXDMAREQ	15	-	✓

Note: ✓: Available, -: N/A

2.18. Serial Peripheral Interface (TSPI)

2.18.1. Built-in channel

The following table shows the TSPI built-in channel of each product.
In TMPM4M Group(1), Maximum Communication speed of TSPI is 10Mbps.

Table 2.87 TSPI built-in channel

Product	TSPI channel (✓: Available, -: N/A)	
	ch0	ch1
M4MN	✓	✓
M4MM	✓	✓
M4ML	✓	✓

2.18.2. Function Pin and Port

The function pins are assigned to the ports of the following table.
Please do not use simultaneously the same function currently assigned to two or more pins.
There is also a channel which does not have function pins depending on a product.

Table 2.88 TSPI function pin and port

Channel	Function pin		Port	Product table (✓: Available, -: N/A)		
				M4MN	M4MM	M4ML
ch0	TSPI0SCK	I/O	PA4	✓	✓	✓
			PC5	✓	✓	-
	TSPI0TXD	Output	PA3	✓	✓	✓
			PC4	✓	✓	-
	TSPI0RXD	Input	PA2	✓	✓	✓
			PC3	✓	✓	✓
	TSPI0CSIN	Input	PA0	✓	✓	-
			PC7	✓	-	-
	TSPI0CS0	Output	PC2	✓	✓	✓
	TSPI0CS1	Output	PA1	✓	✓	-
			PC6	✓	-	-
ch1	TSPI1SCK	I/O	PG6	✓	✓	✓
	TSPI1TXD	Output	PG5	✓	✓	✓
	TSPI1RXD	Input	PG4	✓	✓	✓
			PV1	✓	-	-
	TSPI1CSIN	Input	PG3	✓	✓	✓
			PV0	✓	-	-
	TSPI1CS0	Output	PG2	✓	✓	✓
	TSPI1CS1	Output	PG1	✓	✓	-

Note: In TMPM4M Group(1), there is no TSPIxCS2 pin and TSPIxCS3 pin.

2.18.3. Transfer mode of each product

The TSPI transfer modes of each product vary as shown in following table.

Table 2.89 TSPI mode list

Channel	Support Mode		
	M4MN	M4MM	M4ML
ch0	SPI mode SIO mode		SPI mode (Note) SIO mode
ch1	SPI mode SIO mode		

Note: There is no TSPI0CS1 output terminal and TSPI0CSIN input terminal.

2.18.4. *[TSPIxCR2]*<RXDLY[2:0]> set value

TMPM4M Group(1) products setting value of TSPI control register 2 ([TSPIxCR2]<RXDLY[2:0]>) is as follows.

Table 2.90 *[TSPIxCR2]*<RXDLY[2:0]> set Value

Bit	Bit Symbol	After Reset	Function
18:16	<RXDLY[2:0]>	001	000: fsysm ≤ 40MHz 001: fsysm > 40MHz

2.18.5. Clock for Prescaler

The TSPI uses the clock of the following table as a prescaler clock.

Table 2.91 TSPI clock for prescaler

Clock
ΦT0m

2.18.6. DMA request

The following table shows the DMA request in the TSPI.

Table 2.92 TSPI DMA request

Channel	Request	Signal name	DMA request channel		
				Single transfer	Burst transfer
ch0	Receive DMA request	TSPI0RX_DMA	0	✓	✓
	Transmit DMA request	TSPI0TX_DMA	1	✓	✓
ch1	Receive DMA request	TSPI1RX_DMA	2	✓	✓
	Transmit DMA request	TSPI1TX_DMA	3	✓	✓

Note: ✓: Available, -: N/A

2.18.7. Internal signal connection specification

2.18.7.1. Trigger Transfer signal connection

Transfer start function of the TSPI has a trigger signal control.
A trigger control signal is selected with the trigger source and use it as the following table.

Table 2.93 TSPI trigger transfer: Input

Channel	Function input		Trigger selector	Trigger source	
		Signal name		Input trigger signal	Signal name
ch0	Trigger input for start communication	TSPI0TRG	***[TSEL0CR4]*** <INSEL19>	PA2(TRGIN0)	TRGIN0
				PA3(TRGIN1)	TRGIN1
				PA4(TRGIN2)	TRGIN2
				T32A ch5 timer register A1 match trigger	T32A05TRGOUTCMPA1
				T32A ch5 timer register B1 match trigger	T32A05TRGOUTCMPB1
				T32A ch5 timer register C1 match trigger	T32A05TRGOUTCMPC1
ch1	Trigger input for start communication	TSPI1TRG	***[TSEL0CR5]*** <INSEL20>	PA2(TRGIN0)	TRGIN0
				PA3(TRGIN1)	TRGIN1
				PA4(TRGIN2)	TRGIN2
				T32A ch5 timer register A1 match trigger	T32A05TRGOUTCMPA1
				T32A ch5 timer register B1 match trigger	T32A05TRGOUTCMPB1
				T32A ch5 timer register C1 match trigger	T32A05TRGOUTCMPC1

Note: The trigger source for the trigger signal is selected by the trigger selector: ***[TSEL0CR4]***<INSEL19>, ***[TSEL0CR5]***<INSEL20>. For the detail of connection, refer to the "2.2.Trigger Selector (TRGSEL)".

2.18.7.2. T32A connection

In the TSPI, there is a signal connected with the peripheral function inside in addition to this as shown in the following table.

Table 2.94 TSPI inside connection: Output

Channel	Function output		Trigger selector	Output destination	
		Signal name			Signal name
ch0	Transmit completion	TSPI0TXEND	***[TSEL0CR6]*** <INSEL25>	T32A ch0 Timer A	T32A00TRGINAPCK
	Receive completion	TSPI0RXEND			
ch1	Transmit completion	TSPI1TXEND	***[TSEL0CR7]*** <INSEL28>	T32A ch1 Timer A	T32A01TRGINAPCK
	Receive completion	TSPI1RXEND			

2.19. CAN controller (CAN)

2.19.1. Built-in list

Built-in unit per product is shown in the following table.

Table 2.95 CAN built-in unit

Product	CAN unit (✓: Available, -: N/A)
	Unit A
M4MN	✓
M4MM	✓
M4ML	✓

2.19.2. System clock

The CAN operates with the clock in the following table as the system clock.

Table 2.96 CAN system clock

clock	Signal name
System clock	fsysm

2.19.3. Function Pin and Port

The function pins are assigned to the ports of the following table.
Please use exclusively the same functional pin currently assigned to plurality.

Table 2.97 CAN function pin and port

Unit	Function pin		Port	Product table (✓: Available, -: N/A)		
				M4MN	M4MM	M4ML
A	CANARX	Input	PA4/PE1	✓ / ✓	✓ / ✓	✓ / ✓
	CANATX	Output	PA3/PE0	✓ / ✓	✓ / ✓	✓ / ✓

2.20. Digital Noise Filter (DNF)

2.20.1. Built-in unit

The following table shows the DNF built-in unit of each product.

Table 2.98 DNF built-in unit

Product	DNF unit (✓: Available, -: N/A)		
	A	B	C
M4MN	✓	✓	✓
M4MM	✓	✓	✓
M4ML	✓	✓	✓

2.20.2. External Interrupt list for the each product

The DNF corresponds to the following external interrupt pins.

Table 2.99 External interrupt and DNF

External interrupt pin (Signal name)	Port	Unit	Setting register name	DNF (✓: Available, -: N/A)		
				M4MN	M4MM	M4ML
INT00	PA2	A	***[DNFAENCR]***<NFEN0>	✓	✓	✓
INT01a	PA4		***[DNFAENCR]***<NFEN1>	✓	✓	✓
INT01b	PA3		***[DNFAENCR]***<NFEN2>	✓	✓	✓
INT02a	PC1		***[DNFAENCR***]<NFEN3>	✓	✓	✓
INT02b	PC6		***[DNFAENCR]***<NFEN4>	✓	-	-
INT03a	PC3		***[DNFAENCR]***<NFEN5>	✓	✓	✓
INT03b	PD2		***[DNFAENCR]***<NFEN6>	✓	-	-
INT04a	PE3		***[DNFAENCR]***<NFEN7>	✓	✓	✓
INT04b	PE1		***[DNFAENCR]***<NFEN8>	✓	✓	✓
INT05a	PE5		***[DNFAENCR]***<NFEN9>	✓	✓	✓
INT11b						
INT05b	PE6		***[DNFAENCR]***<NFEN10>	✓	✓	✓
INT06a	PF1		***[DNFAENCR***]<NFEN11>	✓	✓	✓
INT06b	PF2		***[DNFAENCR]***<NFEN12>	✓	-	-
INT07a	PU1		***[DNFAENCR]***<NFEN13>	✓	✓	✓
INT07b	PU2		***[DNFAENCR]***<NFEN14>	✓	✓	✓
INT08a	PU3		***[DNFAENCR]***<NFEN15>	✓	✓	✓
INT08b	PU4	B	***[DNFBENCR]***<NFEN0>	✓	✓	✓
INT09	PU6		***[DNFBENCR]***<NFEN1>	✓	✓	✓
INT10	PC2		***[DNFBENCR]***<NFEN2>	✓	✓	✓
INT11a	PE4		***[DNFBENCR***]<NFEN3>	✓	✓	✓
INT12	PU0		***[DNFBENCR]***<NFEN4>	✓	✓	✓
INT13	PU5		***[DNFBENCR]***<NFEN5>	✓	✓	✓
INT14a	PF4		***[DNFBENCR]***<NFEN6>	✓	✓	-
INT14b	PF5		***[DNFBENCR]***<NFEN7>	✓	-	-
INT15	PA1		***[DNFBENCR]***<NFEN8>	✓	✓	-
INT16a	PN1		***[DNFBENCR]***<NFEN9>	✓	✓	-
INT16b	PN2		***[DNFBENCR]***<NFEN10>	✓	✓	-
INT17a	PD1		***[DNFBENCR***]<NFEN11>	✓	-	-
INT17b	PD0		***[DNFBENCR]***<NFEN12>	✓	-	-
INT18a	PD5		***[DNFBENCR]***<NFEN13>	✓	-	-
INT18b	PD4		***[DNFBENCR]***<NFEN14>	✓	-	-
INT21	PG3	C	***[DNFCENCR***]<NFEN3>	✓	✓	✓

2.20.3. Sampling source clock

The clock shown in the following table is used as a sauce clock for a sampling in DNF.

Table 2.100 DNF sampling source clock

Clock
fc

2.21. Voltage Detection Circuit (LVD)

2.21.1. Built-in list

The following table shows the built-in list for each product.

Table 2.101 LVD built-in list

Product	Built-in list LVD (✓: Available, -: N/A)
M4MN	✓
M4MM	✓
M4ML	✓

2.21.2. Detection power supply

A voltage detecting circuit monitors the power supply of the following tables

Table 2.102 LVD detection power supply

Detection power supply	Power supply name
Digital power source	DVDD5A/DVDD5B

2.22. CRC calculation circuit (CRC)

2.22.1. Built-in list

The following table shows the built-in list for each product.

Table 2.103 CRC built-in list

Product	Built-in list CRC (✓: Available, -: N/A)
M4MN	✓
M4MM	✓
M4ML	✓

2.23. RAM Parity (RAMP)

2.23.1. Built-in channel

The built-in channel for each product is shown in the following table.

Table 2.104 RAMP built-in channel

Product	RAMP channel (✓: Available, -: N/A)	
	ch0	ch1
M4MN	✓	✓
M4MM	✓	✓
M4ML	✓	✓

2.23.2. Error detection block area

The following table shows the detection RAM block area of each product.

Table 2.105 RAM area and address of RAMP

Channel	Register name	RAM area address	Products (✓: Available, -: N/A)		
			M4MN	M4MM	M4ML
ch0	***[RPAR0ST]***<RPARFG0>	0x20000000 to 0x20001FFF	✓	✓	✓
	[RPAR0ST]<RPARFG1>	0x20002000 to 0x20003FFF	✓	✓	✓
ch1	***[RPAR1ST]***<RPARFG0>	0x20004000 to 0x20005FFF	✓	✓	✓

2.24. Trimming Circuit (TRM)

2.24.1. Built-in list

The following table shows the built-in list for each product.

Table 2.106 TRM built-in list

Product	Built-in TRM (✓: Available, -: N/A)
M4MN	✓
M4MM	✓
M4ML	✓

2.24.2. Target oscillator

The target oscillator of the trimming circuit is the oscillator shown in the following table.

Table 2.107 TRM trimming target oscillator

Target oscillator	Oscillator
Internal High speed oscillator 1	IHOSC1

3. Revision History

Table 3.1 Revision History

Revision	Date	Description
1.0	2021-01-28	- First release
1.1	2023-12-20	- 2.9.2. System clock The section is added. - 2.19.2. System clock The section is added.

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