

TLP5814H

1. Applications

- Photovoltaic (PV) inverters
- Industrial Inverters
- SiC-MOSFET Gate Drivers
- IGBT Gate Drivers

2. General

The TLP5814H is a highly integrated gate driver photocoupler housed in a 8-pin SO8L package with a long creepage and clearance of 8 mm.

This gate driver photocoupler provides a maximum peak output current of +6.8 / -4.8 A with rail to rail output, and this enables stable operation and better switching performance in system. The built-in active Miller clamp function contributes to avoid a self-turn-on phenomenon of Power devices, making TLP5814H suitable for driving SiC-MOSFETs and IGBTs.

The TLP5814H consists of an infrared LED and an integrated high-gain, high-speed photodetector.

An internal faraday shield provides a guaranteed common-mode transient immunity of ± 70 kV/ μ s (min).

3. Features

- (1) Output peak current: +6.8 A / -4.8 A (max)
- (2) Peak Miller clamp sinking current: 6.8 A (max)
- (3) Operating temperature: -40 to 125 °C
- (4) Supply current: 5 mA (max)
- (5) Supply voltage: 13 to 23 V
- (6) Threshold input current: 3 mA (max)
- (7) Propagation delay time: 150 ns (max)
- (8) Common-mode transient immunity: ± 70 kV/ μ s (min)
- (9) Isolation voltage: 5000 Vrms (min)
- (10) Safety standards

UL-recognized: UL 1577, File No.E67349

cUL-recognized: CSA Component Acceptance Service No.5A File No.E67349

VDE-approved: EN IEC 60747-5-5, EN IEC 62368-1 (**Note 1**)

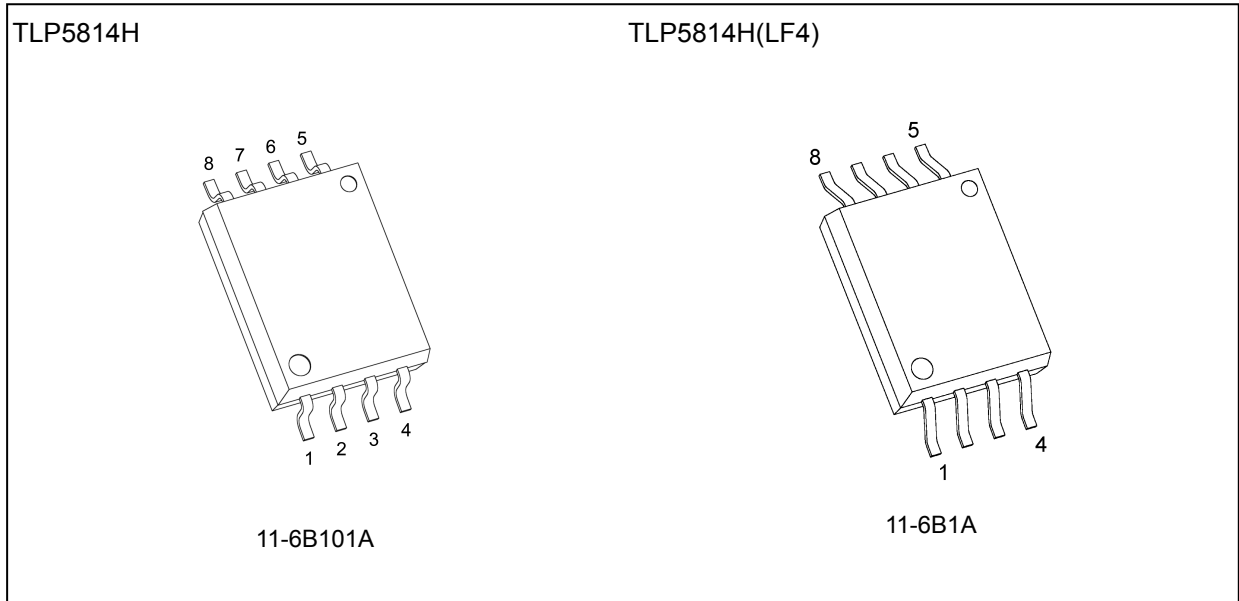
CQC-approved: GB4943.1 Japan Factory

Note 1: When a VDE approved type is needed, please designate the **Option (D4)**.

Start of commercial production

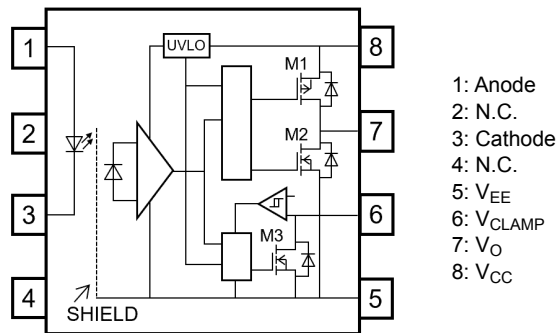
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4. Packaging (Note)

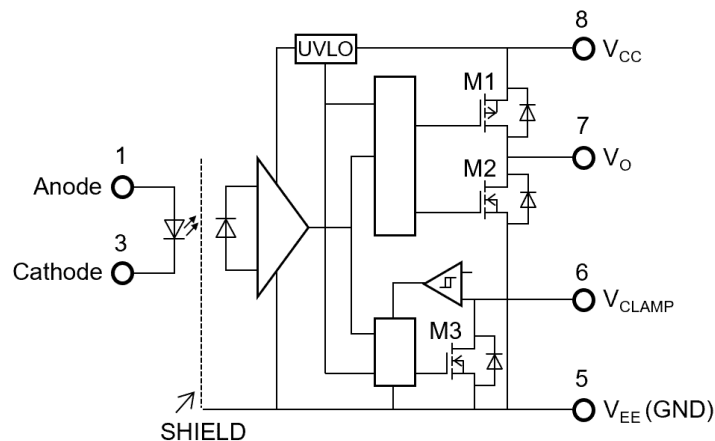


Note: Lead forming option: (LF4)

5. Pin Assignment



6. Internal Circuit (Note)



Note: A 1- μ F bypass capacitor must be connected between pin 8 and pin 5.

7. Principle of Operation

7.1. Truth Table

Input	LED	V_{CLAMP}	M1	M2	M3	Output
H	ON	$> V_{ICLAMP}$	ON	OFF	OFF	H
L	OFF	$> V_{ICLAMP}$	OFF	ON	OFF	L
L	OFF	$< V_{ICLAMP}$	OFF	ON	ON	L

7.2. Mechanical Parameters

Characteristics	Dimensions	Unit
Height	2.3 (max)	mm
Creepage distances	8.0 (min)	
Clearance distances	8.0 (min)	
Internal isolation thickness	0.4 (min)	

8. Absolute Maximum Ratings (Note) (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$)

	Characteristics	Symbol	Note	Rating	Unit
LED	Input forward current	I_F		25	mA
	Input forward current derating ($T_a \geq 100\text{ }^\circ\text{C}$)	$\Delta I_F/\Delta T_a$		-0.4	mA/ $^\circ\text{C}$
	Peak transient input forward current	I_{FPT}	(Note 1)	1	A
	Peak transient input forward current derating ($T_a \geq 100\text{ }^\circ\text{C}$)	$\Delta I_{FPT}/\Delta T_a$		-25	mA/ $^\circ\text{C}$
	Input reverse voltage	V_R		5	V
	Input power dissipation	P_D	(Note 3)	40	mW
	Input power dissipation derating ($T_a \geq 100\text{ }^\circ\text{C}$)	$\Delta P_D/\Delta T_a$	(Note 3)	-0.8	mW/ $^\circ\text{C}$
Detector	Peak high-level output current ($T_a = -40\text{ to }125\text{ }^\circ\text{C}$)	I_{OPH}	(Note 2)	-4.8	A
	Peak low-level output current ($T_a = -40\text{ to }125\text{ }^\circ\text{C}$)	I_{OPL}	(Note 2)	+6.8	A
	Peak clamp sinking current ($T_a = -40\text{ to }125\text{ }^\circ\text{C}$)	I_{CLAMP}	(Note 2)	+6.8	A
	Miller clamp pin voltage	V_{CLAMP}		V_{EE} to V_{CC}	V
Detector	Output voltage	V_O		V_{EE} to V_{CC}	V
	Supply voltage	$V_{CC}-V_{EE}$		-0.5 to 25	V
	Output power dissipation	P_O	(Note 3)	810	mW
	Output power dissipation derating ($T_a \geq 100\text{ }^\circ\text{C}$)	$\Delta P_O/\Delta T_a$	(Note 3)	-10.4	mW/ $^\circ\text{C}$
Common	Operating temperature	T_{opr}		-40 to 125	$^\circ\text{C}$
	Storage temperature	T_{stg}		-55 to 150	
	Lead soldering temperature (10 s)	T_{sol}	(Note 4)	260	
	Isolation voltage AC, 60 s, R.H. $\leq 60\%$	BV_S	(Note 5)	5000	Vrms

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

Note 1: Pulse width $\leq 1\text{ }\mu\text{s}$, 300 pps

Note 2: Pulse width $\leq 10\text{ }\mu\text{s}$, single pulse

Note 3: Mounting on the substrate made in accordance with JEDEC JESD51-7.

Note 4: For the effective lead soldering area.

Note 5: This device is considered as a two-terminal device: All pins on the LED side are shorted together, and all pins on the Output IC side are shorted together.

9. Recommended Operating Conditions (Note)

Characteristics	Symbol	Note	Min	Typ.	Max	Unit
Input on-state current	$I_{F(ON)}$	(Note 1)	4.5	—	10	mA
Input off-state voltage	$V_{F(OFF)}$		0	—	0.8	V
Supply voltage	V_{CC}	(Note 1)	13	—	23	V
Peak high-level output current (L/H)	I_{OLH}	(Note 2)	—	—	-2	A
Peak low-level output current (H/L)	I_{OHL}	(Note 2)	+2	—	—	A

Note: The recommended operating conditions are given as a design guide necessary to obtain the intended performance of the device. Each parameter is an independent value. When creating a system design using this device, the electrical characteristics specified in this data sheet should also be considered.

Note: A ceramic capacitor (1 μ F) should be connected between pin 8 (V_{CC}) and pin 5 (GND) to stabilize the operation of a high-gain linear amplifier. Otherwise, this photocoupler may not switch properly. The bypass capacitor should be placed within 1 cm of each pin.

Note 1: The rise and fall times of the input on-current should be less than 500 μ s, and the rise and fall slopes of V_{CC} and V_{EE} should be less than 1 V/ μ s.

Note 2: Load capacitor ($C \leq 10$ nF), $V_{CC} - V_{EE} = 23$ V, $T_a \leq 125$ °C, $f \leq (50)$ kHz, Duty = 50 %, JEDEC compliant substrate (JESD51-7)

10. Electrical Characteristics (Note) (Unless otherwise specified, $T_a = -40$ to 125 °C)

Characteristics	Symbol	Note	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Input forward voltage	V_F		—	$I_F = 10$ mA, $T_a = 25$ °C	1.43	—	1.7	V
Input forward voltage temperature coefficient	$\Delta V_F / \Delta T_a$		—	$I_F = 10$ mA	—	-0.14	—	mV/°C
Input reverse current	I_R		—	$V_R = 5$ V, $T_a = 25$ °C	—	—	10	μ A
Input capacitance	C_t		—	$V = 0$ V, $f = 1$ MHz, $T_a = 25$ °C	—	38	—	pF
Peak high-level output current	I_{OPH}	(Note 1)	Fig. 13.1.1	$I_F = 4.5$ mA $V_{8-7} = 3.5$ V $V_{CC} - V_{EE} = 23$ V	—	-3.5	-1.7	A
Peak low-level output current	I_{OPL}		Fig. 13.1.2	$I_F = 0$ mA $V_{7-5} = 3.5$ V $V_{CC} - V_{EE} = 23$ V	+2.0	+4.6	—	
Peak high-level output current (L/H)	I_{OLH}		—	$I_F = 0 \rightarrow 4.5$ mA $V_{CC} - V_{EE} = 15$ V $C_g = 3$ nF	—	-1.4	-0.7	
			—	$I_F = 0 \rightarrow 4.5$ mA $V_{CC} - V_{EE} = 23$ V $C_g = 10$ nF	—	-3.5	-2.0	
Peak low-level output current (H/L)	I_{OHL}		—	$I_F = 4.5 \rightarrow 0$ mA $V_{CC} - V_{EE} = 15$ V $C_g = 3$ nF	+0.7	+1.3	—	
			—	$I_F = 4.5 \rightarrow 0$ mA $V_{CC} - V_{EE} = 23$ V $C_g = 10$ nF	+2.0	+3.6	—	
Clamp pin low level sinking current	I_{CLAMP}		Fig. 13.1.5	$I_F = 0$ mA $V_{6-5} = 2.5$ V $V_{CC} - V_{EE} = 23$ V	+2.6	+3.6	—	
Clamp pin threshold voltage	V_{ICLAMP}		—	$I_F = 4.5 \rightarrow 0$ mA $V_{CC} - V_{EE} = 23$ V	2.0	2.5	3.0	V
ON-state resistance	$R_{ON\ CLAMP}$		—	$I_{CLAMP} = 2.0$ A	—	1.23	1.5	Ω
High-level output voltage	V_{OH}		Fig. 13.1.3	$I_F = 4.5$ mA, $I_O = -100$ mA $V_{CC} - V_{EE} = 23$ V	22.7	—	—	V
Low-level output voltage	V_{OL}		Fig. 13.1.4	$V_F = 0.8$ V, $I_O = 100$ mA $V_{CC} - V_{EE} = 23$ V	—	—	0.2	
High-level supply current	I_{CCH}		Fig. 13.1.6	$I_F = 4.5$ mA, $V_{CC} - V_{EE} = 23$ V, $V_O = \text{Open}$	—	3.0	5.0	mA
Low-level supply current	I_{CCL}		Fig. 13.1.7	$I_F = 0$ mA, $V_{CC} - V_{EE} = 23$ V, $V_O = \text{Open}$	—	2.8	5.0	
Threshold input current (L/H)	I_{FLH}		—	$V_{CC} - V_{EE} = 15$ V, $V_O > 1$ V	—	0.8	3.0	
Threshold input voltage (H/L)	V_{FHL}		—	$V_{CC} - V_{EE} = 15$ V, $V_O < 1$ V	0.8	—	—	V
UVLO threshold voltage	V_{UVLO+}		—	$I_F = 4.5$ mA, $V_{CC} = 0 \rightarrow 23$ V $V_O > 1$ V	11.7	12.5	13.2	
	V_{UVLO-}		—	$I_F = 4.5$ mA, $V_{CC} = 23 \rightarrow 0$ V $V_O < 1$ V	10.2	11.0	11.7	
UVLO hysteresis	$UVLO_{HYS}$		—	$V_{UVLO+} - V_{UVLO-}$	—	1.5	—	

Note: All typical values are at $T_a = 25$ °C.

Note 1: Application time ≤ 10 μ s, single pulse.

11. Isolation Characteristics (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$)

Characteristics	Symbol	Note	Test Condition	Min	Typ.	Max	Unit
Total capacitance (input to output)	C_S	(Note 1)	$V_S = 0\text{ V}$, $f = 1\text{ MHz}$	—	1.0	—	pF
Isolation resistance	R_S	(Note 1)	$V_S = 500\text{ V}$, R.H. $\leq 60\%$	10^{12}	10^{14}	—	Ω
Isolation voltage	BV_S	(Note 1)	AC, 60 s	5000	—	—	Vrms

Note 1: This device is considered as a two-terminal device: All pins on the LED side are shorted together, and all pins on the Output IC side are shorted together.

12. Switching Characteristics (Note) (Unless otherwise specified, $T_a = -40\text{ to }125\text{ }^\circ\text{C}$)

Characteristics	Symbol	Note	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Propagation delay time (L/H)	t_{pLH}	(Note 1)	Fig. 13.1.8	$I_F = 0 \rightarrow 4.5\text{ mA}$, $V_{CC} = 15\text{ V}$, $R_g = 10\ \Omega$, $C_g = 3\text{ nF}$	—	70	150	ns
				$I_F = 0 \rightarrow 4.5\text{ mA}$, $V_{CC} = 23\text{ V}$, $R_g = 10\ \Omega$, $C_g = 10\text{ nF}$	—	71	150	
Propagation delay time (H/L)	t_{pHL}	(Note 1)	Fig. 13.1.8	$I_F = 4.5 \rightarrow 0\text{ mA}$, $V_{CC} = 15\text{ V}$, $R_g = 10\ \Omega$, $C_g = 3\text{ nF}$	—	78	130	ns
				$I_F = 4.5 \rightarrow 0\text{ mA}$, $V_{CC} = 23\text{ V}$, $R_g = 10\ \Omega$, $C_g = 10\text{ nF}$	—	79	130	
Rise time	t_r	(Note 1)	Fig. 13.1.8	$I_F = 0 \rightarrow 4.5\text{ mA}$, $V_{CC} = 15\text{ V}$, $R_g = 10\ \Omega$, $C_g = 3\text{ nF}$	—	5.1	—	ns
				$I_F = 0 \rightarrow 4.5\text{ mA}$, $V_{CC} = 23\text{ V}$, $R_g = 10\ \Omega$, $C_g = 10\text{ nF}$	—	6.8	—	
Fall time	t_f	(Note 1)	Fig. 13.1.8	$I_F = 4.5 \rightarrow 0\text{ mA}$, $V_{CC} = 15\text{ V}$, $R_g = 10\ \Omega$, $C_g = 3\text{ nF}$	—	3.2	—	ns
				$I_F = 4.5 \rightarrow 0\text{ mA}$, $V_{CC} = 23\text{ V}$, $R_g = 10\ \Omega$, $C_g = 10\text{ nF}$	—	3.9	—	
Pulse width distortion	$ t_{pHL} - t_{pLH} $	(Note 1)	Fig. 13.1.8	$I_F = 0 \leftrightarrow 4.5\text{ mA}$, $V_{CC} = 15\text{ V}$, $R_g = 10\ \Omega$, $C_g = 3\text{ nF}$	—	8	40	ns
				$I_F = 0 \leftrightarrow 4.5\text{ mA}$, $V_{CC} = 23\text{ V}$, $R_g = 10\ \Omega$, $C_g = 10\text{ nF}$	—	8	40	
Propagation delay skew (device to device)	t_{psk}	(Note 1), (Note 2)	Fig. 13.1.9	$I_F = 0 \leftrightarrow 4.5\text{ mA}$, $V_{CC} = 15\text{ V}$, $R_g = 10\ \Omega$, $C_g = 3\text{ nF}$	-80	—	80	ns
				$I_F = 0 \leftrightarrow 4.5\text{ mA}$, $V_{CC} = 23\text{ V}$, $R_g = 10\ \Omega$, $C_g = 10\text{ nF}$	-80	—	80	
High-level common-mode transient immunity	CM_H	(Note 3)	Fig. 13.1.9	$V_{CM} = 1500\text{ V}_{p-p}$, $I_F = 4.5\text{ mA}$, $V_{CC} - V_{EE} = 23\text{ V}$, $T_a = 25\text{ }^\circ\text{C}$, $V_{O(min)} = 19\text{ V}$	± 70	—	—	kV/ μs
Low-level common-mode transient immunity	CM_L	(Note 4)	Fig. 13.1.9	$V_{CM} = 1500\text{ V}_{p-p}$, $I_F = 0\text{ mA}$, $V_{CC} - V_{EE} = 23\text{ V}$, $T_a = 25\text{ }^\circ\text{C}$, $V_{O(max)} = 1\text{ V}$	± 70	—	—	kV/ μs

Note: All typical values are at $T_a = 25\text{ }^\circ\text{C}$.

Note 1: Input signal duty = 50 %, $t_r = t_f = 5\text{ ns}$ or less

Note 2: The propagation delay skew, t_{psk} , is equal to the magnitude of the worst-case difference in t_{pHL} and/or t_{pLH} that will be seen between units at the same given conditions (supply voltage, input current, temperature, etc).

Note 3: CM_H is the maximum rate of rise of the common mode voltage that can be sustained with the output voltage in the logic high state ($V_O > 19\text{ V}$).

Note 4: CM_L is the maximum rate of fall of the common mode voltage that can be sustained with the output voltage in the logic low state ($V_O < 1\text{ V}$).

13. Test Circuits and Characteristics Curves

13.1. Test Circuits

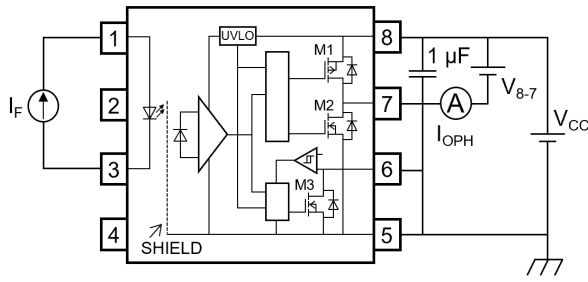


Fig. 13.1.1 I_{OPH} Test Circuit

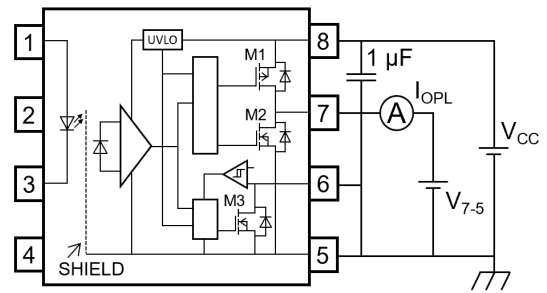


Fig. 13.1.2 I_{OPL} Test Circuit

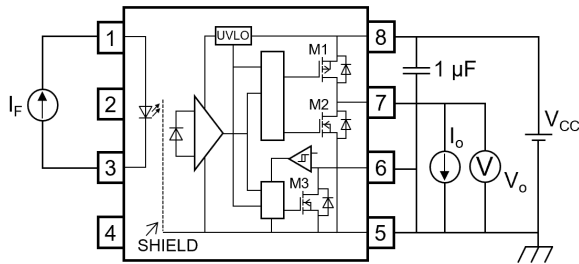


Fig. 13.1.3 V_{OH} Test Circuit

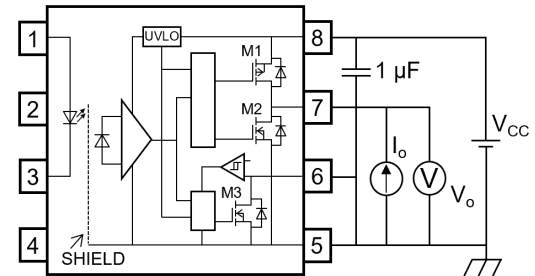


Fig. 13.1.4 V_{OL} Test Circuit

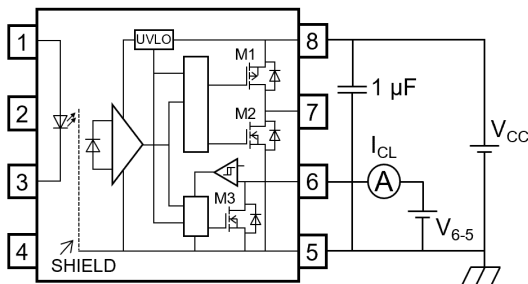


Fig. 13.1.5 I_{CLAMP} Test Circuit

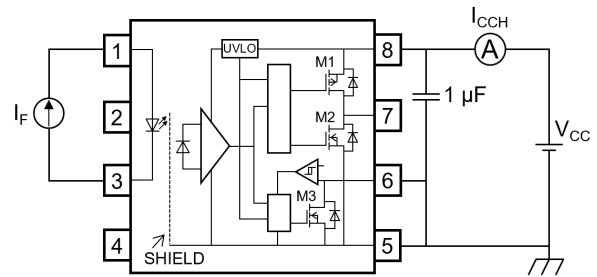


Fig. 13.1.6 I_{CCH} Test Circuit

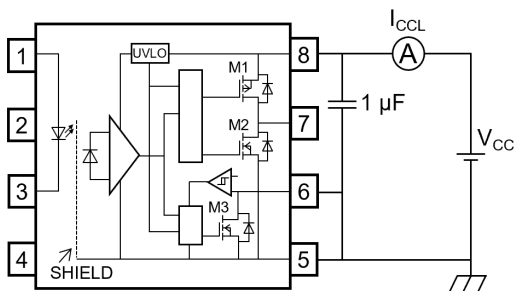
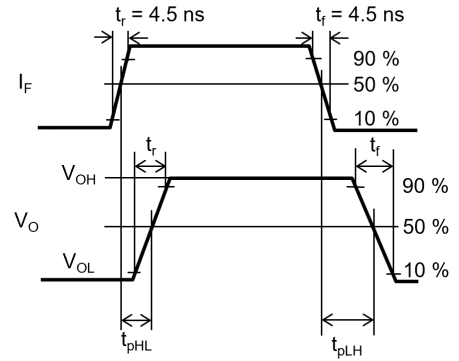
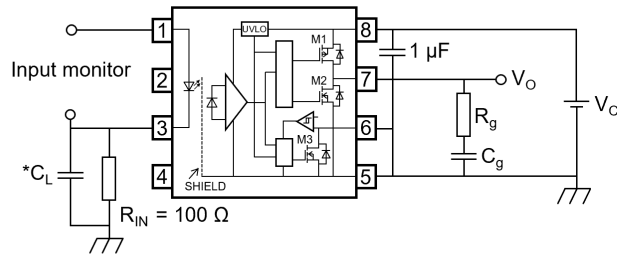


Fig. 13.1.7 I_{CCL} Test Circuit

$I_F = 4.5 \text{ mA}$ (P.G.)
 ($f = 10 \text{ kHz}$, duty = 50 %)



* C_L is less than 15 pF which includes probe and stay wiring capacitance.
 P.G.: Pulse generator

Fig. 13.1.8 Switching Time Test Circuit and Waveform

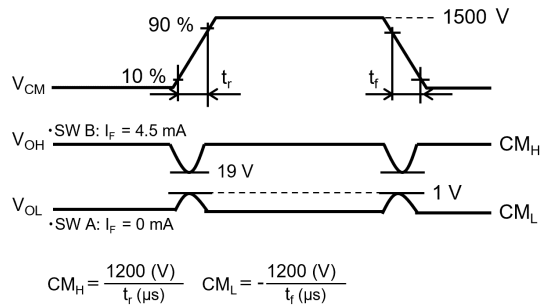
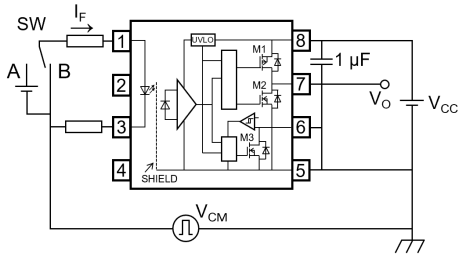


Fig. 13.1.9 Common-Mode Transient Immunity Test Circuit and Waveform

13.2. Characteristics Curves (Note)

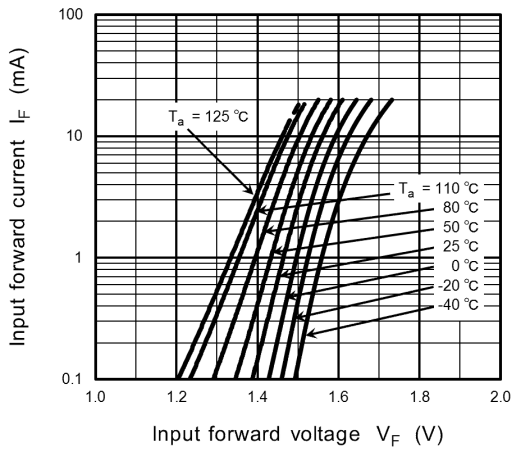


Fig. 13.2.1 $I_F - V_F$

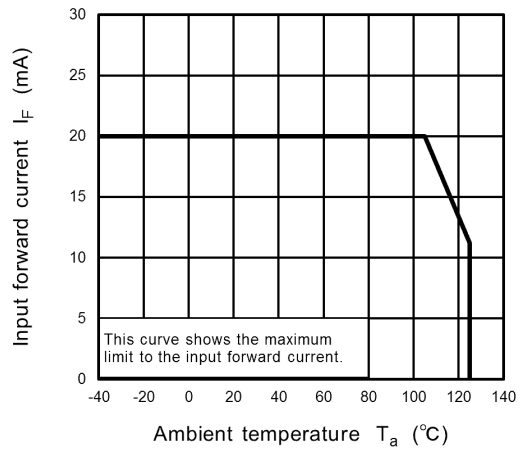


Fig. 13.2.2 $I_F - T_a$

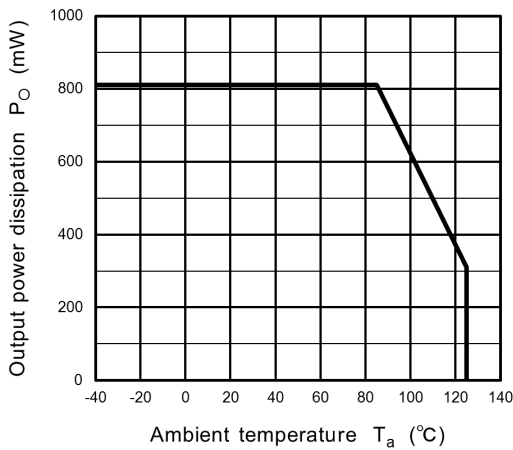


Fig. 13.2.3 $P_O - T_a$

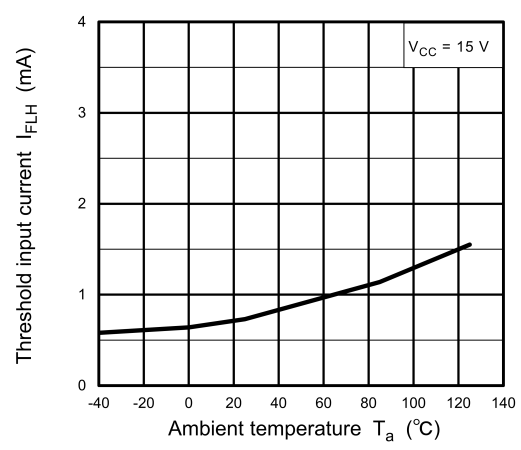


Fig. 13.2.4 $I_{FLH} - T_a$

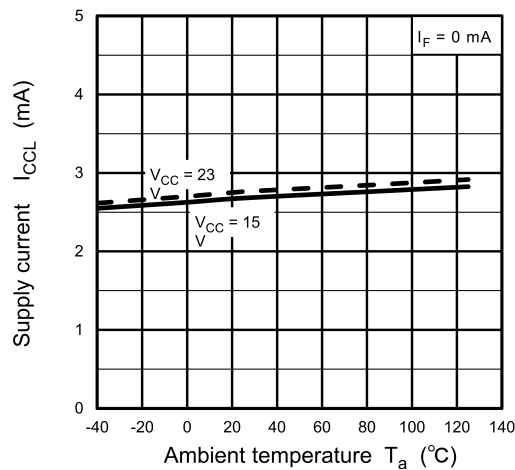


Fig. 13.2.5 $I_{CCL} - T_a$

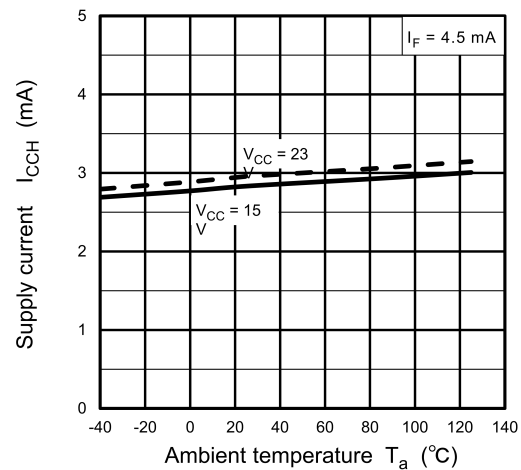


Fig. 13.2.6 $I_{CCH} - T_a$

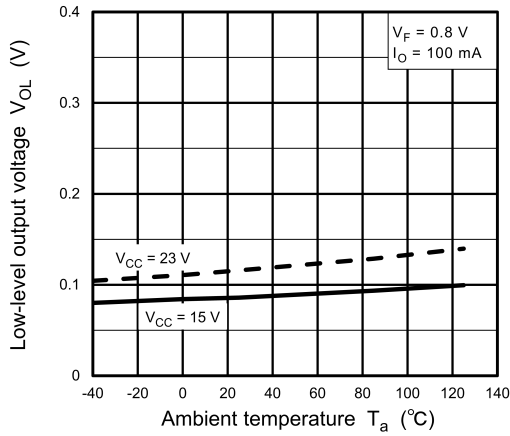


Fig. 13.2.7 $V_{OL} - T_a$

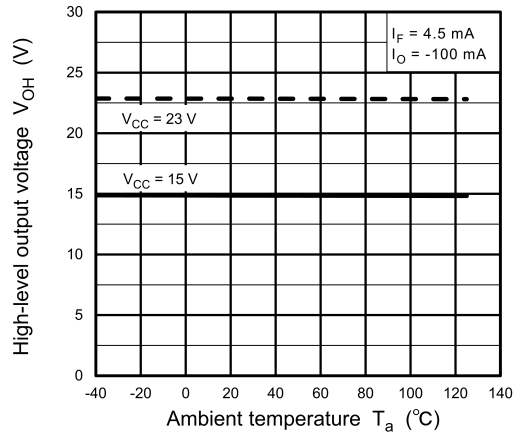


Fig. 13.2.8 $V_{OH} - T_a$

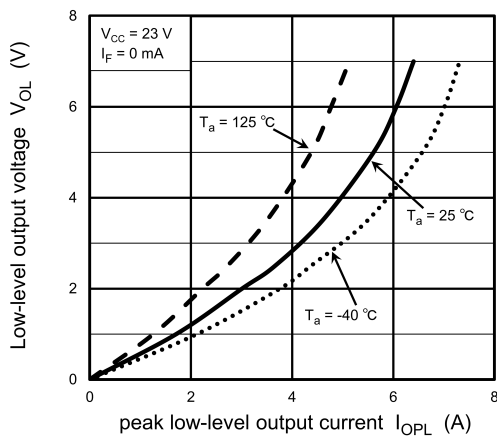


Fig. 13.2.9 $V_{OL} - I_{OPL}$

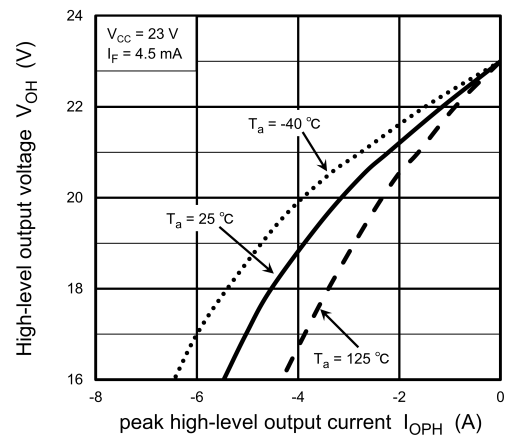


Fig. 13.2.10 $(V_{OH} - V_{CC}) - I_{OPH}$

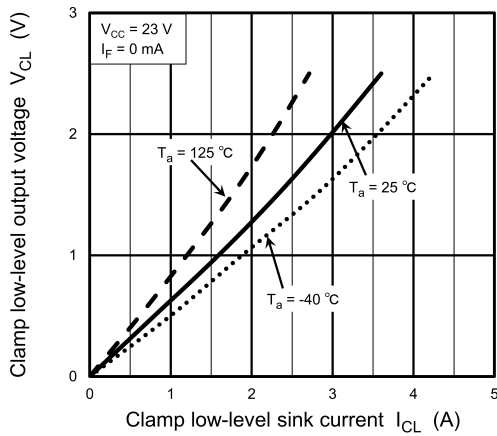


Fig. 13.2.11 $V_{CLAMP} - I_{CLAMP}$

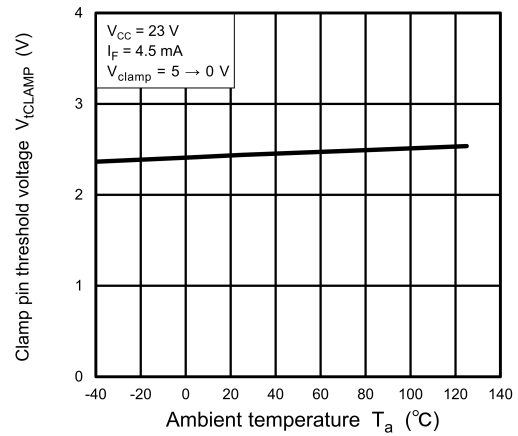


Fig. 13.2.12 $V_{tCLAMP} - T_a$

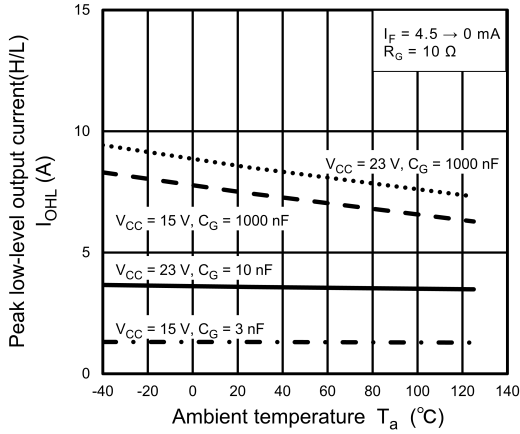


Fig. 13.2.13 $I_{OHL} - T_a$

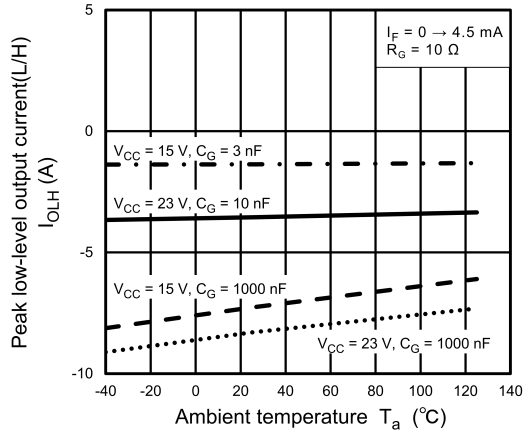


Fig. 13.2.14 $I_{OLH} - T_a$

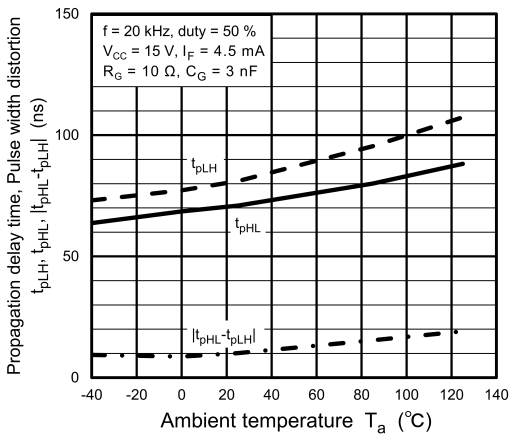


Fig. 13.2.15 $t_{pHL}, t_{pLH}, |t_{pHL} - t_{pLH}| - T_a$

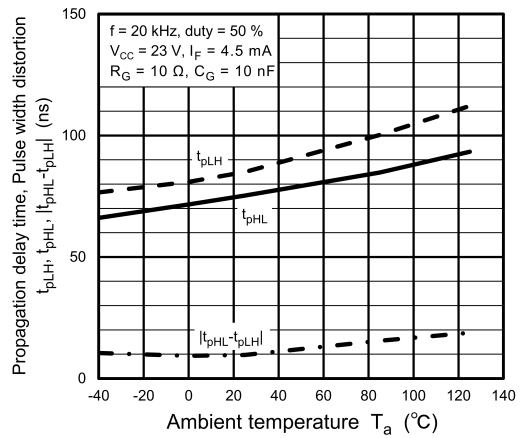


Fig. 13.2.16 $t_{pHL}, t_{pLH}, |t_{pHL} - t_{pLH}| - T_a$

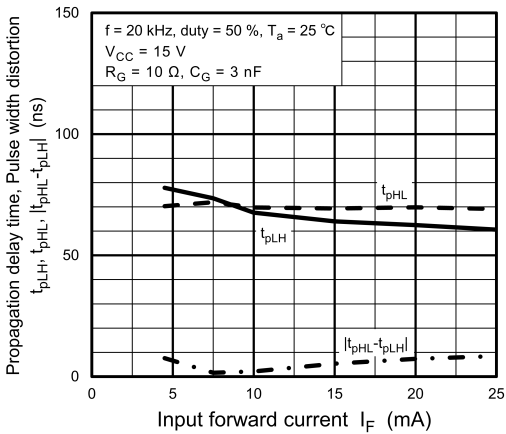


Fig. 13.2.17 $t_{pHL}, t_{pLH}, |t_{pHL} - t_{pLH}| - I_F$

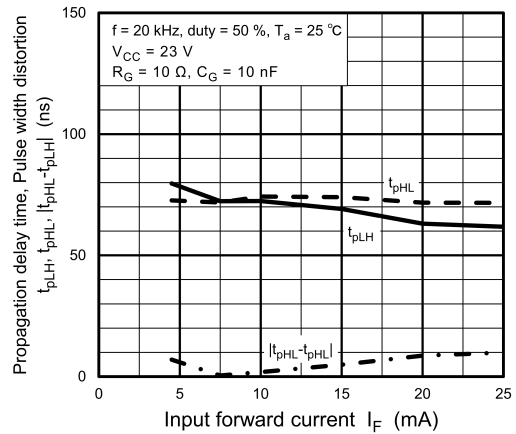


Fig. 13.2.18 $t_{pHL}, t_{pLH}, |t_{pHL} - t_{pLH}| - I_F$

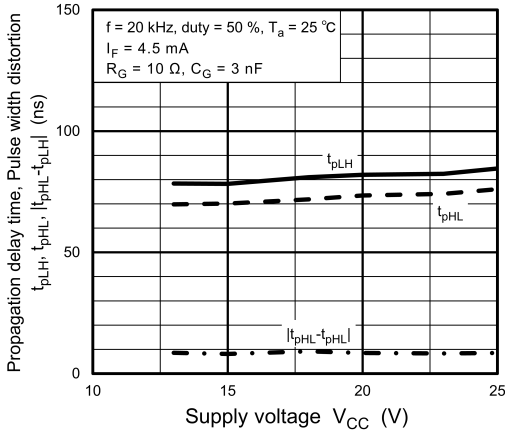


Fig. 13.2.19 t_{pHL} , t_{pLH} , $|t_{pHL} - t_{pLH}| - V_{CC}$

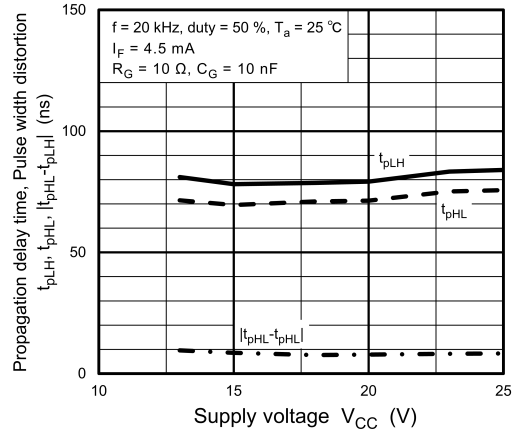


Fig. 13.2.20 t_{pHL} , t_{pLH} , $|t_{pHL} - t_{pLH}| - V_{CC}$

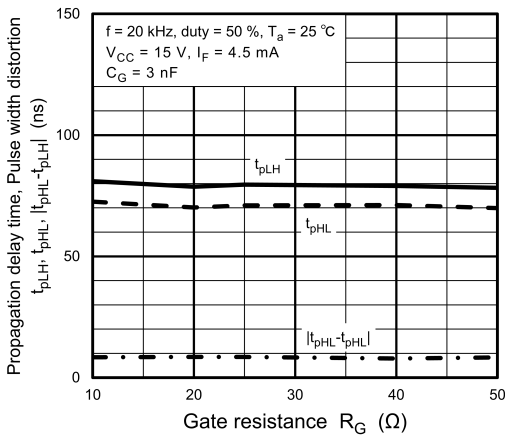


Fig. 13.2.21 t_{pHL} , t_{pLH} , $|t_{pHL} - t_{pLH}| - R_G$

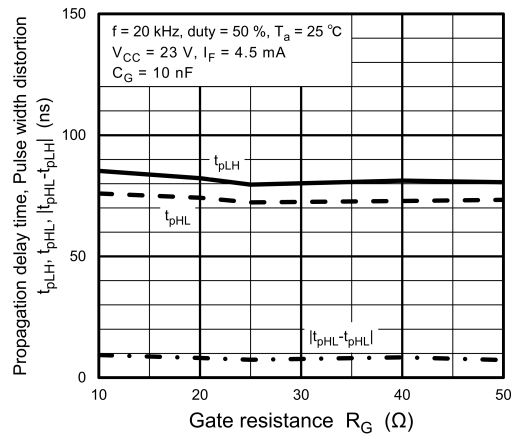


Fig. 13.2.22 t_{pHL} , t_{pLH} , $|t_{pHL} - t_{pLH}| - R_G$

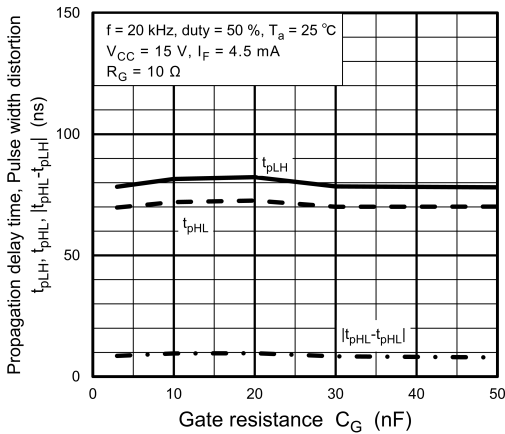


Fig. 13.2.23 t_{pHL} , t_{pLH} , $|t_{pHL} - t_{pLH}| - C_G$

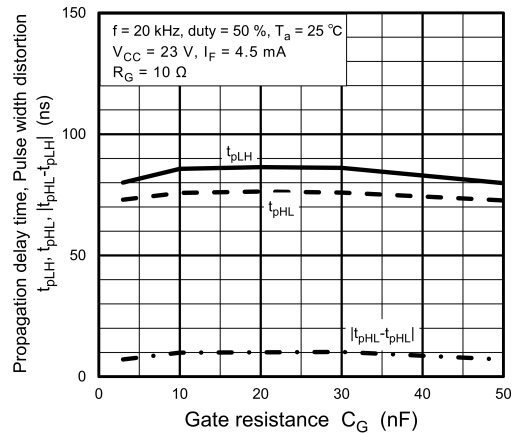


Fig. 13.2.24 t_{pHL} , t_{pLH} , $|t_{pHL} - t_{pLH}| - C_G$

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

14. Soldering and Storage

14.1. Precautions for Soldering

The soldering temperature should be controlled as closely as possible to the conditions shown below, irrespective of whether a soldering iron or a reflow soldering method is used.

- When using soldering reflow.

The soldering temperature profile is based on the package surface temperature.

(See the figure shown below, which is based on the package surface temperature.)

Reflow soldering must be performed once or twice.

The mounting should be completed with the interval from the first to the last mountings being 2 weeks.

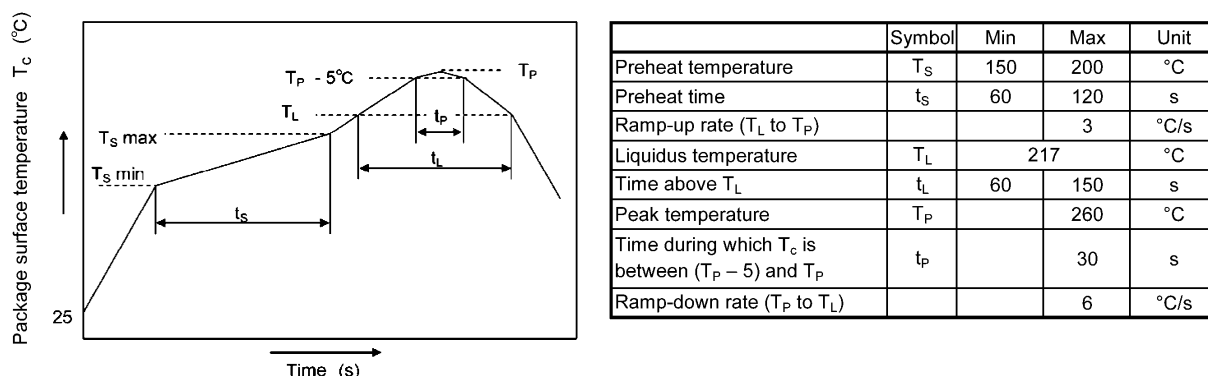


Fig. 14.1.1 An Example of a Temperature Profile When Lead(Pb)-Free Solder Is Used

- When using soldering flow
 - Preheat the device at a temperature of 150 °C (package surface temperature) for 60 to 120 seconds.
 - Mounting condition of 260 °C within 10 seconds is recommended.
 - Flow soldering must be performed once.
- When using soldering flow (Applicable to both eutectic solder and Lead(Pb)-Free solder)
 - Preheat the device at a temperature of 150 °C (package surface temperature) for 60 to 120 seconds.
 - Mounting condition of 260 °C within 10 seconds is recommended.
 - Flow soldering must be performed once.
- When using soldering iron
 - Complete soldering within 10 seconds for lead temperature not exceeding 260 °C or within 3 seconds not exceeding 350 °C
 - Heating by soldering iron must be done only once per lead.

14.2. Precautions for General Storage

- Avoid storage locations where devices may be exposed to moisture or direct sunlight.
- Follow the precautions printed on the packing label of the device for transportation and storage.
- Keep the storage location temperature and humidity within a range of 5 °C to 35 °C and 45 % to 75 %, respectively.
- Do not store the products in locations with poisonous gases (especially corrosive gases) or in dusty conditions.
- Store the products in locations with minimal temperature fluctuations. Rapid temperature changes during storage can cause condensation, resulting in lead oxidation or corrosion, which will deteriorate the solderability of the leads.
- When restoring devices after removal from their packing, use anti-static containers.
- Do not allow loads to be applied directly to devices while they are in storage.
- If devices have been stored for more than two years under normal storage conditions, it is recommended that you check the leads for ease of soldering prior to use.

15. Land Pattern Dimensions (for reference only)

Unit: mm

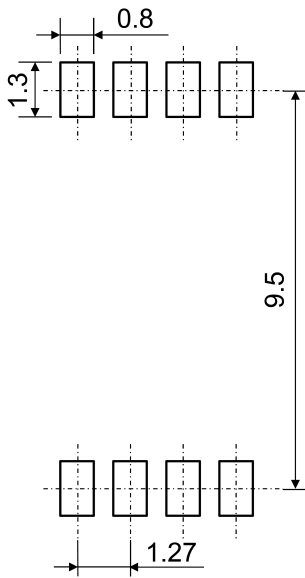


Fig. 15.1 Lead forming option (standard)

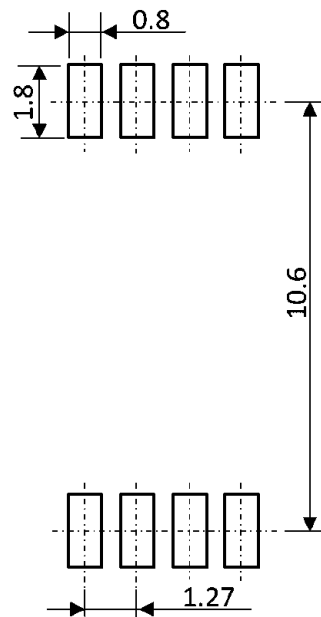
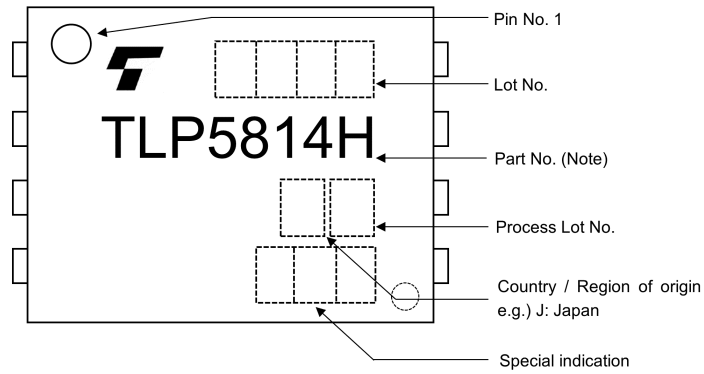


Fig. 15.2 Lead forming option (LF4)

16. Marking



17. EN IEC 60747-5-5 Option (D4) Specification

- Part number: TLP5814H (Note 1)
- The following part naming conventions are used for the devices that have been qualified according to option (D4) of EN IEC 60747.

Example: TLP5814H(D4-TP,E)

D4: EN IEC 60747 option

TP: Tape type

E: [[G]]/RoHS COMPATIBLE (Note 2)

Note 1: Use TOSHIBA standard type number for safety standard application.

e.g., TLP5814H(D4-TP,E → TLP5814H

Note 2: Please contact your Toshiba sales representative for details on environmental information such as the product's RoHS compatibility.

RoHS is the Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment.

Description	Symbol	Rating	Unit
Application classification for rated mains voltage ≤ 600 Vrms for rated mains voltage ≤ 1000 Vrms		I-IV I-III	—
Climatic classification		40 / 125 / 21	—
Pollution degree		2	—
Maximum operating insulation voltage	V _{ORM}	1500	V _{peak}
Input to output test voltage, Method A V _{pr} = 1.6 × V _{ORM} , type and sample test t _p = 10 s, partial discharge < 5 pC	V _{pr}	2400	V _{peak}
Input to output test voltage, Method B V _{pr} = 1.875 × V _{ORM} , 100 % production test t _p = 1 s, partial discharge < 5 pC	V _{pr}	2813	V _{peak}
Highest permissible overvoltage (transient overvoltage, t _{pr} = 60 s)	V _{TR}	8000	V _{peak}
Safety limiting values (max. permissible ratings in case of fault, also refer to thermal derating curve) current (input current I _F , P _{SO} = 0) power (output or total power dissipation) temperature	I _{si} P _{so} T _s	300 810 150	mA mW °C
Insulation resistance	V _{IO} = 500 V, T _a = 25 °C V _{IO} = 500 V, T _a = 100 °C V _{IO} = 500 V, T _a = T _s	R _{si}	$\geq 10^{12}$ $\geq 10^{11}$ $\geq 10^9$ Ω

Fig. 17.1 EN IEC 60747 Insulation Characteristics

Table Insulation Related Specifications (Note)

Insulation Related Parameters	Symbol	TLP5814H
Minimum creepage distance	Cr	8.0 mm
Minimum clearance	Cl	8.0 mm
Minimum insulation thickness	ti	0.4 mm
Comparative tracking index	CTI	500

Note: This photocoupler is suitable for **safe electrical isolation** only within the safety limit data. Maintenance of the safety data shall be ensured by means of protective circuits.



Fig. 17.2 Marking on Packing for EN IEC 60747

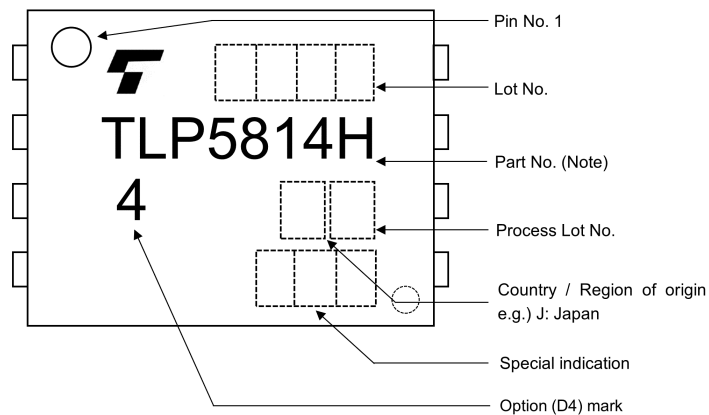


Fig. 17.3 Marking Example (Note)

Note: The above marking is applied to the photocouplers that have been qualified according to option (V4) of EN IEC 60747.

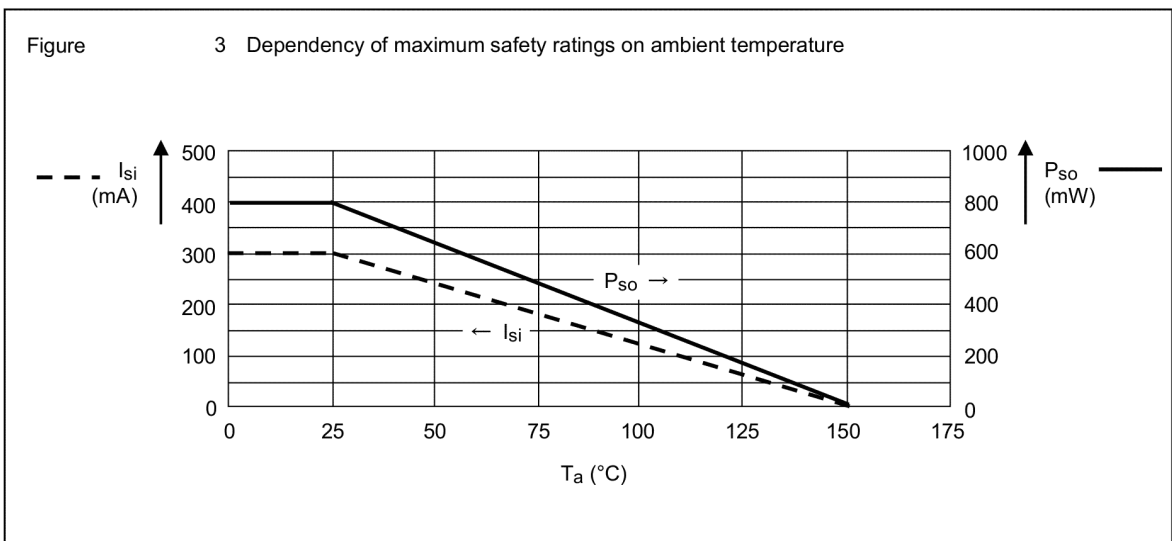
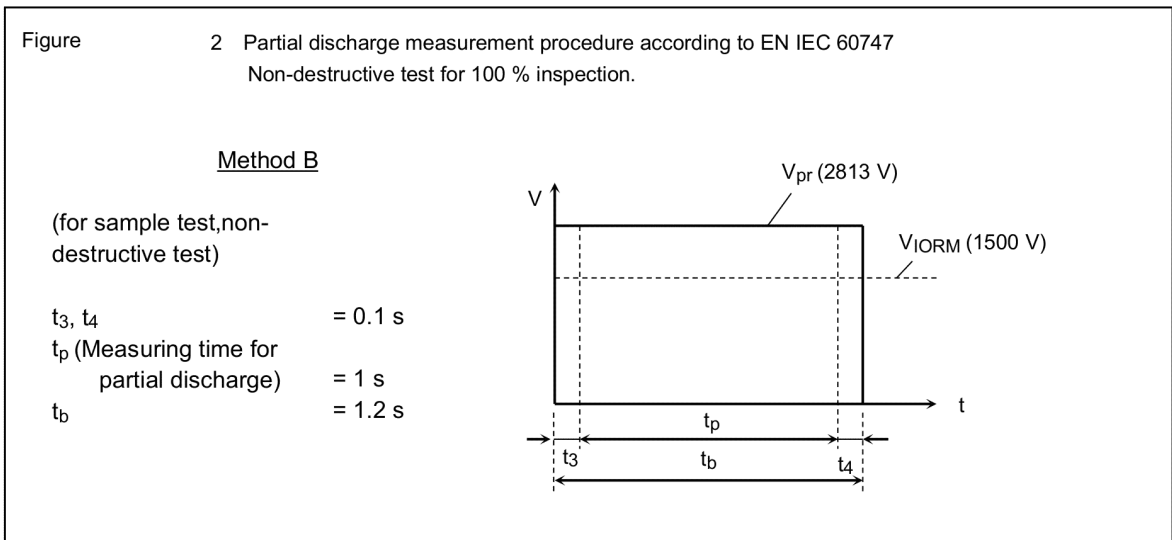
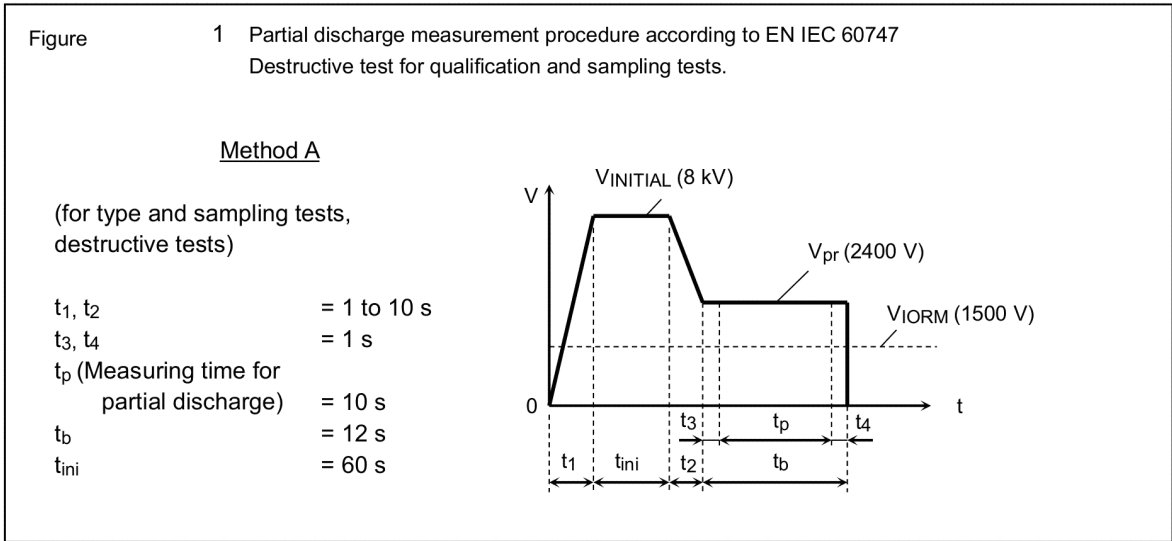


Fig. 17.4 Measurement Procedure

18. Ordering Information

When placing an order, please specify the part number, tape type and quantity as shown in the following example.

Example) TLP5814H(TP,E 1500 pcs

Part number: TLP5814H

Tape type: TP

[[G]]/RoHS COMPATIBLE: E (Note 1)

Quantity (must be a multiple of 1500): 1500 pcs

Note 1: Please contact your Toshiba sales representative for details on environmental information such as the product's RoHS compatibility.

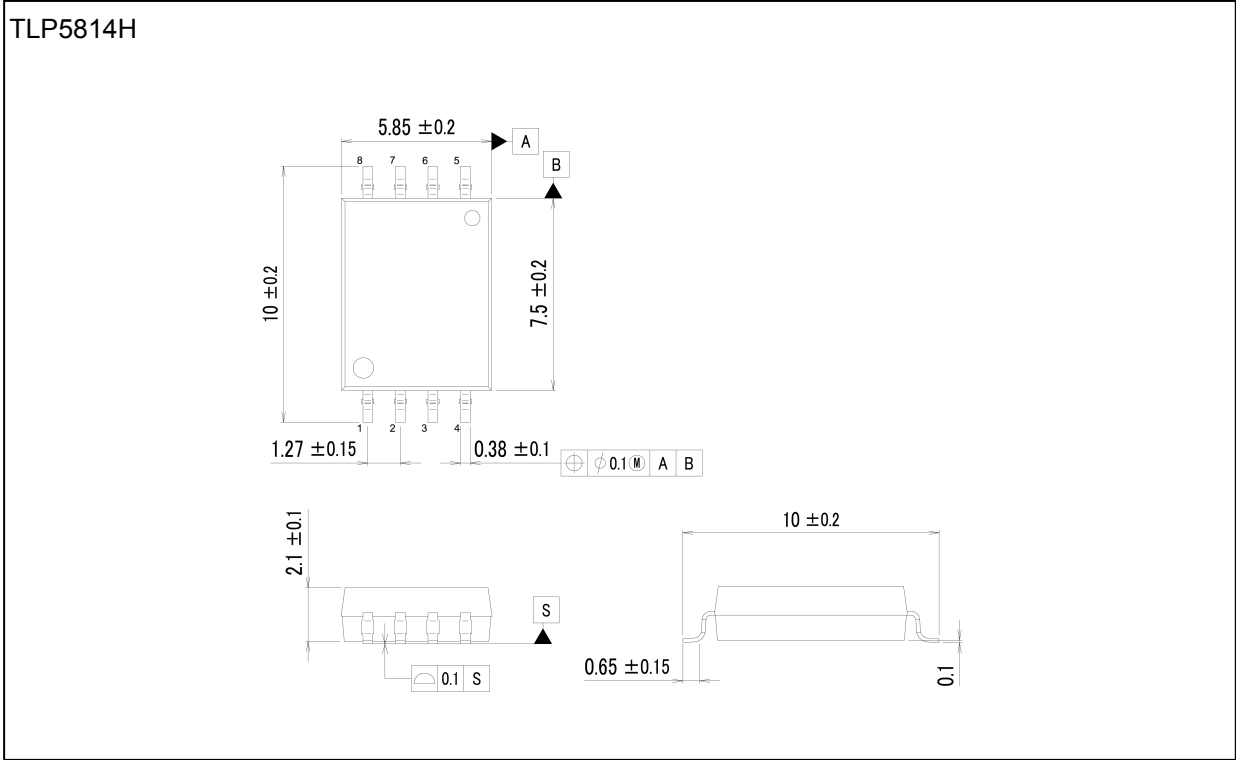
RoHS is the Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment.

19. Ordering Information (Example of Item Name)

Item Name	Packaging	VDE Option	Packing (MOQ)
TLP5814H(E			Magazine (75 pcs)
TLP5814H(TP,E			Tape and reel (1500 pcs)
TLP5814H(D4,E		EN IEC 60747-5-5	Magazine (75 pcs)
TLP5814H(D4-TP,E		EN IEC 60747-5-5	Tape and reel (1500 pcs)
TLP5814H(LF4,E	LF4, Wide forming		Magazine (75 pcs)
TLP5814H(TP4,E	LF4, Wide forming		Tape and reel (1500 pcs)
TLP5814H(D4-LF4,E	LF4, Wide forming	EN IEC 60747-5-5	Magazine (75 pcs)
TLP5814H(D4-TP4,E	LF4, Wide forming	EN IEC 60747-5-5	Tape and reel (1500 pcs)

Package Dimensions

Unit: mm

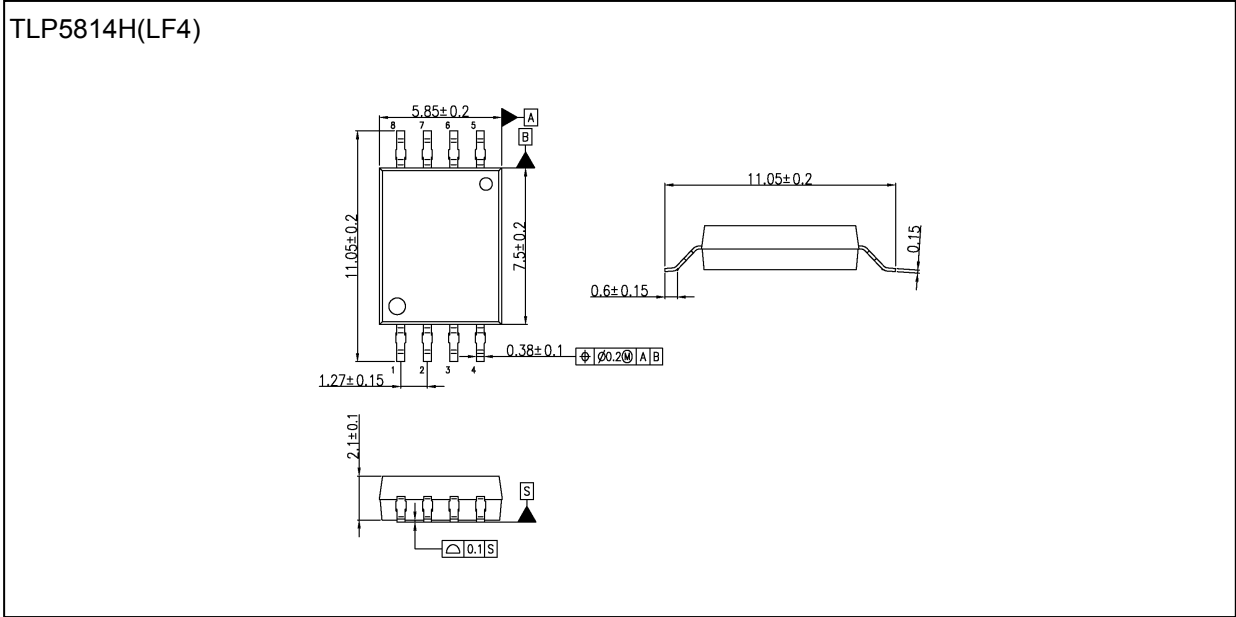


Weight: 0.203 g (typ.)

Package Name(s)
TOSHIBA: 11-6B101A

Package Dimensions

Unit: mm



Weight: 0.205 g (typ.)

Package Name(s)
TOSHIBA: 11-6B1A

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