32-bit RISC Microcontroller
Reference Manual

Trimming Circuit
(TRM-B)

Revision 1.4

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Toshiba Electronic Devices & Storage Corporation

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Preface

Related Document

Document name
Clock Control and Operation Mode
32-bit Timer Event Counter

Conventions

- Numeric formats follow the rules as shown below:
  Hexadecimal: 0xABC
  Decimal: 123 or 0d123 - Only when it needs to be explicitly shown that they are decimal numbers.
  Binary: 0b111 - It is possible to omit the "0b" when the number of bits can be distinctly understood from a sentence.
- "_N" is added to the end of signal names to indicate low active signals.
- It is called "assert" that a signal moves to its active level, "deassert" to its inactive level.
- When two or more signal names are referred, they are described like as [m:n].
  Example: S[3:0] shows four signal names S3, S2, S1 and S0 together.
- The characters surrounded by ***[ ]*** defines the register.
  Example: ***[ABCD]***
- "N" substitutes suffix number of two or more same kind of registers, fields, and bit names.
  Example: ***[XYZ1]***, ***[XYZ2]***, ***[XYZ3]*** → ***[XYZn]***
- "x" substitutes suffix number or character of units and channels in the register list.
- In case of unit, "x" means A, B, and C, ...
  Example: ***[ADACR0]***, ***[ADBCR0]***, ***[ADCCR0]*** → ***[ADxCR0]***
- In case of channel, "x" means 0, 1, and 2, ...
  Example: ***[T32A0RUNA]***, ***[T32A1RUNA]***, ***[T32A2RUNA]*** → ***[T32AxRUNA]***
- The bit range of a register is written like as [m: n].
  Example: Bit[3: 0] expresses the range of bit 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.
  Example: ***[ABCD]***<EFG> = 0x01 (hexadecimal), ***[XYZn]***<VW> = 1 (binary)
- Word and byte represent the following bit length.
  Byte: 8 bits
  Half word: 16 bits
  Word: 32 bits
  Double word: 64 bits
- Properties of each bit in a register are expressed as follows:
  R: Read only
  W: Write only
  R/W: Read and write are possible.
- Unless otherwise specified, register access supports only word access.
- The register defined as "Reserved" must not be rewritten. Moreover, do not use the read value.
- The value read from the bit having default value of "-" is unknown.
- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value, In the cases that default is "-", follow the definition of each register.
- Reserved bits of the write-only register should be written with their default value. In the cases that default is "-", follow the definition of each register.
- Do not use read-modified-write processing to the register of a definition which is different by writing and read out.

Terms and Abbreviations

Some of abbreviations used in this document are as follows:

CG	Clock Control and Operation Mode
TRM	Trimming Circuit

1. Outlines

The trimming circuit (TRM) can adjust the internal oscillator frequency.
The lists of functions are as follows.

Function classification	Function	Operation
Frequency adjustment of the internal oscillator	Target oscillator	Internal high-speed oscillator 1 (IHOSC1)
	Adjustment range	Trimming -9.07 to +9.00 % (Average 0.07 % step)
	Monitor function	The reading of the initial trimming value is possible. The reading of the valid trimming value is possible.
Protection	Protection function	Incorrect writing is prevented.

2. Configuration

The configuration of the trimming circuit is shown as follows.

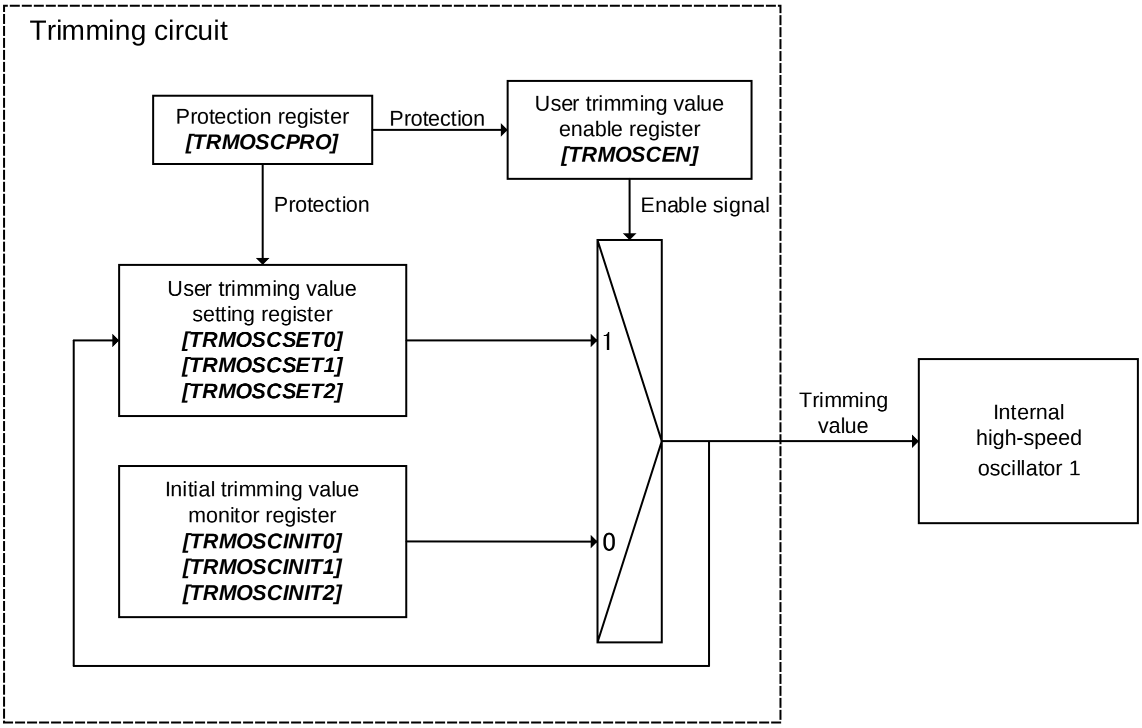

Figure 2.1 Trimming Circuit Configuration

3. Function and Operation

The internal high-speed oscillator 1(IHOSC1) frequency for the system clocks can be adjusted by the trimming circuit (TRM). The initial trimming level monitor register (***[TRMOSCINIT]***) can confirm the value that a factory trimmed before shipment.

When you use TRM, please set an applicable clock enable bit to "1" (clock supply) in fsys supply stop register A(***[CGFSYSENA]***, ***[CGFSYSMENA]***), fsys supply stop register B(***[CGFSYSENB]***, ***[CGFSYSMENB]***), fsys supply stop register C(***[CGFSYSMENC]***), and fc supply stop registers (***[CGFCEN]***).

The corresponding registers and the bit locations depend on a product. Some products do not have all registers. For the details, refer to reference manual "Clock Control and Operation Mode".

3.1. Adjustment

As for ***[TRMOSCSET0]***, ***[TRMOSCSET1]***, ***[TRMOSCSET2]***(user trimming value setting register 0, 1, 2) and ***[TRMOSCEN]*** (user trimming value enabling register), the protection is carried out after reset. And the writing is forbidden. In order to write in, please write "0xC1" in ***[TRMOSCPRO]***<PROTECT> (protection register), and remove the protection.

Also, initialization is required when using the trimming circuit.

Initialization procedure:

(1)	***[TRMOSCPRO]***<PROTECT[7:0]> = 0xC1	;	Protect function release.
(2)	***[TRMOSCSET0]*** ← ***[TRMOSINIT0]***	;	Read the initial value of ***[TRMOSCINIT0]*** and write it to ***[TRMOSCSET0].***
(3)	***[TRMOSCSET1]*** ← ***[TRMOSINIT1]***	;	Read the initial value of ***[TRMOSCINIT1]*** and write it to ***[TRMOSCSET1].***
(4)	***[TRMOSCSET2]*** ← ***[TRMOSINIT2]***	;	Read the initial value of ***[TRMOSCINIT2]*** and write it to ***[TRMOSCSET2].***
(5)	***[TRMOSCPRO]***<PROTECT[7:0]> = 0x00	;	Protect set.

To adjust the frequency, set ***[TRMOSCSET0]*** to the trimming value.

When ***[TRMOSCEN]***<TRIMEN> is set to "1", the trimming value is updated in a user trimming value from an initial trimming value.

Oscillating frequency is varied by change of temperature or power supply voltage, the stress from the outside, etc. Therefore, please perform trimming before operation in which the accuracy of frequency is needed, or regularly.

3.2. Adjustment Range

About the adjustment range, the trimming is available for the adjustment of 256 steps. Please perform the setup by ***[TRMOSCSET0]***<TRIMSET0[7:0]>.

Please refer to "Table 3.1 Adjustment range of the trimming (Sampled value)" for the range of adjustment.

Table 3.1 Adjustment Range of Trimming (Sampled Value)

Trimming			
+ Value		- Value	
<TRIMSET0[7:0]>	Frequency change (typ.)	<TRIMSET0[7:0]>	Frequency change(typ.)
01111111	9.00 %	11111111	-0.07 %
01111110	8.93 %	11111110	-0.14 %
01111101	8.86 %	11111101	-0.21 %
01111100	8.79 %	11111100	-0.28 %
01111011	8.72 %	11111011	-0.35 %
01111010	8.65 %	11111010	-0.43 %
01111001	8.57 %	11111001	-0.50 %
⋮	⋮	⋮	⋮
01100011	7.02 %	11100011	-2.06 %
01100010	6.94 %	11100010	-2.13 %
01100001	6.87 %	11100001	-2.20 %
01100000	6.80 %	11100000	-2.27 %
⋮	⋮	⋮	⋮
01001010	5.24 %	11001010	-3.83 %
01001001	5.17 %	11001001	-3.90 %
01001000	5.10 %	11001000	-3.97 %
01000111	5.03 %	11000111	-4.04 %
⋮	⋮	⋮	⋮
00110010	3.54 %	10110010	-5.53 %
00110001	3.47 %	10110001	-5.60 %
00110000	3.40 %	10110000	-5.67 %
00101111	3.33 %	10101111	-5.74 %
⋮	⋮	⋮	⋮
00011001	1.77 %	10011001	-7.30 %
00011000	1.70 %	10011000	-7.37 %
00010111	1.63 %	10010111	-7.44 %
00010110	1.56 %	10010110	-7.51 %
⋮	⋮	⋮	⋮
00000110	0.43 %	10000110	-8.65 %
00000101	0.35 %	10000101	-8.72 %
00000100	0.28 %	10000100	-8.79 %
00000011	0.21 %	10000011	-8.86 %
00000010	0.14 %	10000010	-8.93 %
00000001	0.07 %	10000001	-9.00 %
00000000	0.00 %	10000000	-9.07 %

4. Registers

The trimming registers for the internal high-speed oscillator 1 (IHOSC1) are described below.

4.1. List of Registers

The trimming control registers and their addresses for the internal high-speed oscillator 1 (IHOSC1) are shown as follows:

Peripheral function		Channel/unit	Base address		
			TYPE 1	TYPE 2	TYPE3
Trimming circuit	TRM	-	0x400F3200	0x400E3100	0x40083100

Note: The channel/unit and base address type are different by products. Please refer to reference manual "Product Information" for the details.

Register name		Base address (Base+)
Protection Register	***[TRMOSCPRO]***	0x0000
User Trimming Value Enable Register	***[TRMOSCEN]***	0x0004
Initial Trimming Value Monitor Register 0	***[TRMOSCINIT0]***	0x0010
Initial Trimming Value Monitor Register 1	***[TRMOSCINIT1]***	0x0014
Initial Trimming Value Monitor Register 2	***[TRMOSCINIT2]***	0x0018
User Trimming Value Setting Register 0	***[TRMOSCSET0]***	0x0020
User Trimming Value Setting Register 1	***[TRMOSCSET1]***	0x0024
User Trimming Value Setting Register 2	***[TRMOSCSET2]***	0x0028

4.2. Register Description

4.2.1. *[TRMOSCPRO]* (Protection Register)

Bit	Bit symbol	After reset	Type	Function
31:8	-	0	R	Read as "0"
7:0	PROTECT[7:0]	0x00	R/W	Protect control 0xC1: Protect function release. Other than 0xC1: Protect set

4.2.2. *[TRMOSCEN]* (User Trimming Value Enable Register)

Bit	Bit symbol	After reset	Type	Function
31:1	-	0	R	Read as "0"
0	TRIMEN	0	R/W	User trimming value enable control 0: Disabled (Use initial trimming value) 1: Enabled (Use user trimming value)

Note: When the first setting <TRIME> to "1" after releasing reset, set the value read from ***[TRMOSCINIT0]*** to ***[TRMOSCINIT2]*** is set into ***[TRMOSCSET0]*** to ***[TRMOSCSET2]***.

4.2.3. *[TRMOSCINIT0]* (Initial Trimming Value Monitor Register 0)

Bit	Bit symbol	After reset	Type	Function
31:9	-	0	R	Read as "0"
8:1	TRIMINIT0[7:0]	Undefined	R	Initial trimming value. The trimming value at the time of shipment is read.
0	-	Undefined	R	Read as "undefined value"

Note: When using the user trimming value, read this register value as the initial setting and write it to ***[TRMOSCSET0]***.

4.2.4. *[TRMOSCINIT1]* (Initial Trimming Value Monitor Register 1)

Bit	Bit symbol	After reset	Type	Function
31:0	TRIMINIT1[31:0]	Undefined	R	Trimming initial setting value

Note: When using the user trimming value, read this register value as the initial setting and write it to ***[TRMOSCSET1]***.

4.2.5. *[TRMOSCINIT2]* (Initial Trimming Value Monitor Register 2)

Bit	Bit symbol	After reset	Type	Function
31:0	TRIMINIT2[31:0]	Undefined	R	Trimming initial setting value

Note: When using the user trimming value, read this register value as the initial setting and write it to ***[TRMOSCSET2]***.

4.2.6. *[TRMOSCSET0]* (User Trimming Value Setting Register 0)

Bit	Bit symbol	After reset	Type	Function
31:9	-	0	R	Read as "0"
8:1	TRIMSET0[7:0]	Undefined	R	- When ***[TRMOSCEN]***<TRIMEN>=0: The initial trimming value of ***[TRMOSCINIT0]***<TRIMINIT0[7:0]> is read. - When ***[TRMOSCEN]***<TRIMEN>=1: The user trimming value is read.
			W	Set the user trimming value.
0	-	Undefined	R	- When ***[TRMOSCEN]***<TRIMEN>=0: The value of Bit 0 of ***[TRMOSCINIT0]*** is read. - When ***[TRMOSCEN]***<TRIMEN>=1: The written value is read.
			W	Write as "0"

4.2.7. *[TRMOSCSET1]* (User Trimming Value Setting Register 1)

Bit	Bit symbol	After reset	Type	Function
31:0	TRIMSET1[31:0]	Undefined	R	- When ***[TRMOSCEN]***<TRIMEN>=0: The initial trimming value of ***[TRMOSCINIT1]*** is read. - When ***[TRMOSCEN]***<TRIMEN>=1: The written value is read.
			W	Trimming initial setting value Write the initial value of ***[TRMOSCINIT1]***.

4.2.8. *[TRMOSCSET2]* (User Trimming Value Setting Register 2)

Bit	Bit symbol	After reset	Type	Function
31:0	TRIMSET2[31:0]	Undefined	R	- When ***[TRMOSCEN]***<TRIMEN>=0: The initial trimming value of ***[TRMOSCINIT2]*** is read. - When ***[TRMOSCEN]***<TRIMEN>=1: The written value is read.
			W	Trimming initial setting value Write the initial value of ***[TRMOSCINIT2]***.

5. Usage Example

5.1. Internal Oscillation Frequency Trimming Using 32-bit Timer Event Counter (T32A)

A pulse width measurement function of the T32A can be used to measure frequencies of the internal high-speed oscillator 1.

For more information about the T32A, please refer to reference manual "32-bit Timer Event Counter" .

5.1.1. Input of Reference Clock to T32AxINAx Pin

Set the prescaler output (ΦT0) as the count clock of the T32A. And the internal high-speed oscillator 1 is selected.

The reference clock is input to the T32AxINAx pin. Using the pulse width measurement function, the up-counter value is captured on the rising edge of the reference clock.

The trimming value is calculated with the difference between the frequency of the captured reference clock and the frequency of the input reference clock.

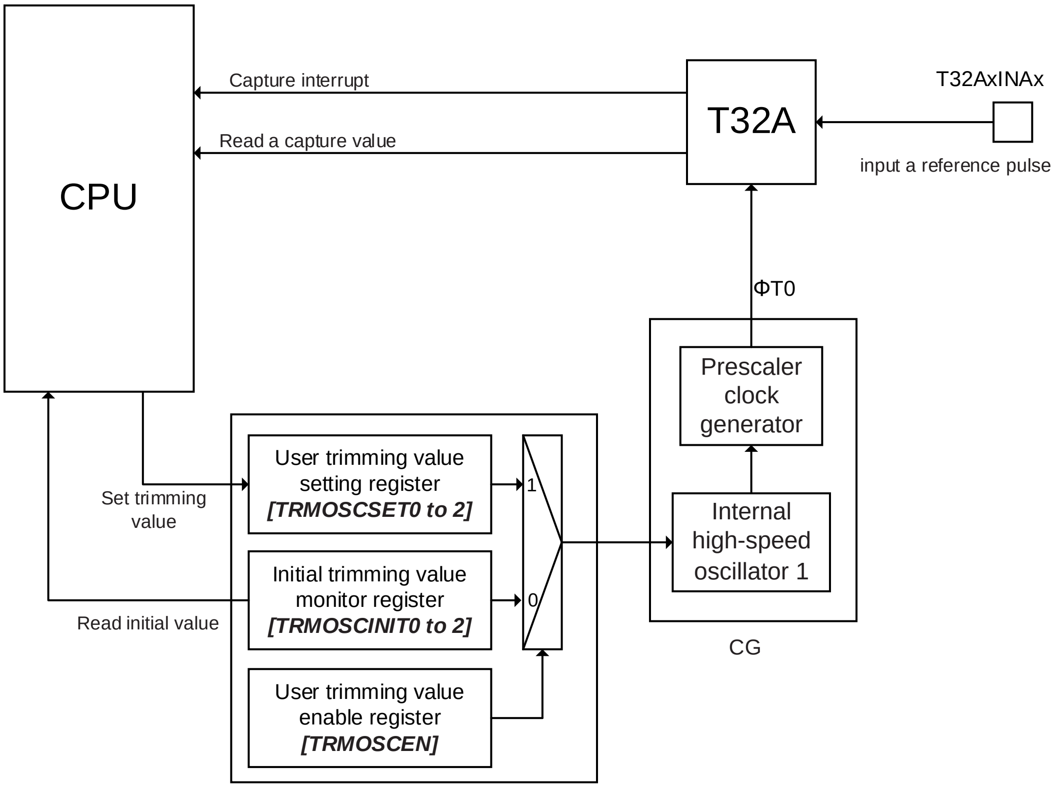

Figure 5.1 Example: Input of Reference Clock to T32AxINAx Pin

A trimming level calculation and a setting example:

<Conditions>

- Reference clock frequency: 10Hz (Input clock to the T32AxINAx pin)
- Prescaler value: 1/16 (ΦT0 fc = Internal high-speed oscillator 1 frequency)
- Prescaler division value in T32A: 1/1 (Capture trigger clock)
- Input to the T32AxINAx pin: Capture setting (CAPA0:Rising edge is selected)

(1) In the case of pulse width calculated value = 0xEBC1 (= 60353), it is at the one cycle of the reference signal.:
The frequency of the internal high-speed oscillator 1 is calculated as follows.

$$\text{Internal high-speed oscillator 1 frequency} = \frac{1}{(\,1 / \text{Reference clock frequency}\,) / (\,\text{Pulse width calculated value}\,) / (\,1 / \text{Prescaler value}\,)}$$

$$= \frac{1}{(\,1/10\ \text{Hz}\,)\ /\ (\,60353\,)\ /\ (\,1 / (1/16)\,)}$$

$$= 9.656\text{MHz}$$

(2) The difference from the target frequency (10MHz) of the internal high-speed oscillator 1 is calculated..

- Frequency deviation (%) = 1 - ((Pre-adjustment frequency) / (Reference clock frequency))
  = 1 - (9.656MHz / 10MHz)
  = 0.0344 = 3.44%

(3) The trimming values are selected in Table 3.1. The trimming value should be close to the calculated frequency deviation (%) of 3.44%. Those values should be set to the user trimming value setting register (***[TRMOSCSET0]***).

- Trimming value: 3.47 % <TRIMSET0[7:0]> = 00110001

(4) The user trimming level is output to internal high-speed oscillator 1 by setting "1" to the ***[TRMOSCEN]***<TRIMEN> after having set a trimming value.

(5) When the frequency error is calculated again and the target frequency range is not satisfied, repeat the above operation until the target frequency range is reached. However, perform it while ***[TRMOSCEN]*** <TRIMEN> remains "1".

Note1: To calculate the frequency error, set ***[TRMOSCEN]*** <TRIMEN> to "1", or set ***[TRMOSCSET0]*** to the trimming value when ***[TRMOSCEN]***<TRIMEN> is "1". Wait for the oscillation stabilization time (163.4 µs or more), and then use the captured value. For the oscillation stabilization time, refer to reference manual "Clock Control and Operation Mode" .

Note2: When adjusting the trimming of the internal high-speed oscillator 1, do not select "PLL output" as the clock for fsys.

Please write the data other than "0xC1" in protection control register ***[TRMOSCPRO]***<PROTECT> to enable the protection function after the end of trimming.

5.1.2. Input of fs on ch4 in Timer A

As for the following explanation, fs is connected to the internal trigger input of the T32A ch4 timer A, and the timer A output is connected to the internal trigger input of the timer B, for example.

The fs is chosen as the internal trigger input of the timer A of T32A ch4, and the count clock of the timer A is set to the internal trigger (fs). By matching the count value(n) of the timer register A1 with the counter, invert the timer output A to create the reference signal (= fs / 2n). The output of ch4 of timer A is connected to ch4 of timer B. Set the count clock of timer B of T32A ch4 to the prescaler output and, as ΦT0, chooses the internal high-speed oscillator 1. In addition, enable the pulse width measurement function of timer B and capture the value of the up counter in rising edge of the standard signal from timer A.

The trimming value is calculated with the difference between the frequency of the captured reference clock and the frequency of the input reference clock.

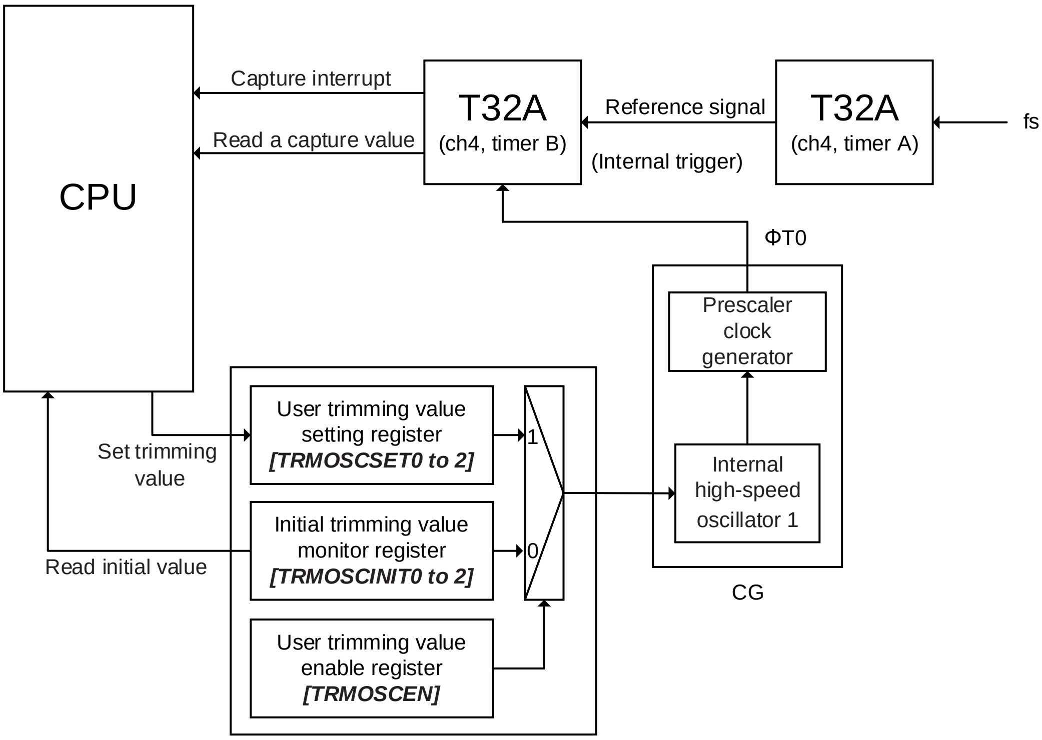

Figure 5.2 Example: Input of fs on ch4 in Timer A

6. Precaution for Usage

- The addresses to which no registers are assigned should not be accessed.

7. Revision History

Table 7.1 Revision History

Revision	Date	Description
1.0	2020-10-01	- First release
1.1	2021-01-29	- Added "Note 1" and "Note 2" to section 5.1.1.
1.2	2021-02-18	- Corrected table in section 1. - Added "Note" to section 4.2.2. - Corrected "Note" in section 4.2.3 to 4.2.5.
1.3	2021-03-29	- Corrected "Note 1" in section 5.1.1.
1.4	2024-05-10	- Appearance updated

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