eFuse Application Circuit (with Enhanced Overcurrent Protection)

Reference Guide

RD241B-RGUIDE-01

Toshiba Electronic Devices & Storage Corporation

Table of Contents

1. Introduction

This reference guide document describes the specifications and operation procedure of the eFuse Application Circuit (with Enhanced Overcurrent Protection).

In recent years, various protective functions have become important in various consumer devices such as notebook PCs, game machines, storage devices, servers, etc. This document describes the Protection Circuit (hereafter referred to as "this design"), which is ideal for these applications, it is built using the eFuse IC (electronic fuse) and the Thermoflagger™ IC.

eFuse IC (electronic fuse) operates when excessive current flows and has a fast current interruption function compared to the conventional fuse. In addition, it can be used repeatedly because it doesn’t get destroyed by a single event of overcurrent. Various other protection functions, such as overvoltage protection, are also built in.

This Design consists of a module board and a base board.

The module board consists of an eFuse IC (TCKE905ANA) with overcurrent protection, a Thermoflagger™ IC (TCTH021BE) and a PTC thermistor (PTC11). In this design, Thermoflagger™ is used to monitor the current of the eFuse IC, and when it detects overcurrent, it cuts off the output of the eFuse IC. It also cuts off the output of the eFuse IC when the PTC thermistor (PTC11) heats up and its resistance rises, causing the output of voltage divided circuit (built using the PTC thermistor (PTC11) and a 4.7kΩ resistor (R11)) to drop.

The base board is used for evaluating the module board. It is equipped with the N-ch power MOSFETs TPHR8504PL1, the MOSFET gate driver ICs TCK402G, the transistors with bias resistors for signal-control, the one-gate logic ICs TC7PZ17FU, and the CMOS logic ICs 74HC123D.

The base board is also used in the reference design of the Power Multiplexer Circuit.

2. Specifications and Appearance

2.1. Specifications

Table 2.1 and Table 2.2 show the main specifications of the module board and the base board.

Table 2.1 Module Board Specifications

Board Name	Input Voltage	Rated Output Current
eFuse Application Circuit (with Enhanced Overcurrent Protection)	Min. 2.7V Typ. 5V Max. 6V	1.4A (Typ.), up to 4A with appropriate resistor setting

Table 2.2 Base Board Specifications

Input/Output	Description
Input	VINA input (VINA 2.7V to 6V) VINB input (not used) Drive power supply (VDD 5V to 12V)
Output	Output load A to D (LOAD-A to LOAD-D, each Load can have both resistive load and capacitive load, Max current is 4A for the module board of this design) FLAG output (H-level (approximately 5V) is output when VINA is input)

2.2. Block Diagrams

2.2.1. Module Board Block Diagram

Fig. 2.1 shows the block diagram of the module board (eFuse Application Circuit (with Enhanced Overcurrent Protection)).

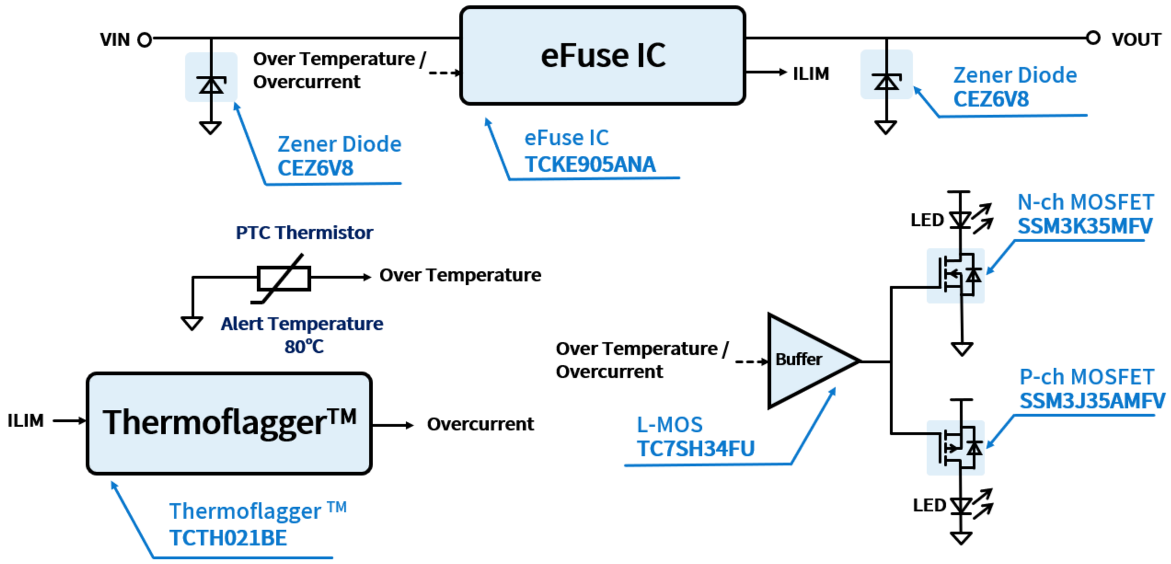


Fig. 2.1 Module Board Block Diagram

2.2.2. Base Board Block Diagram

Fig. 2.2 shows the block diagram of the base board.

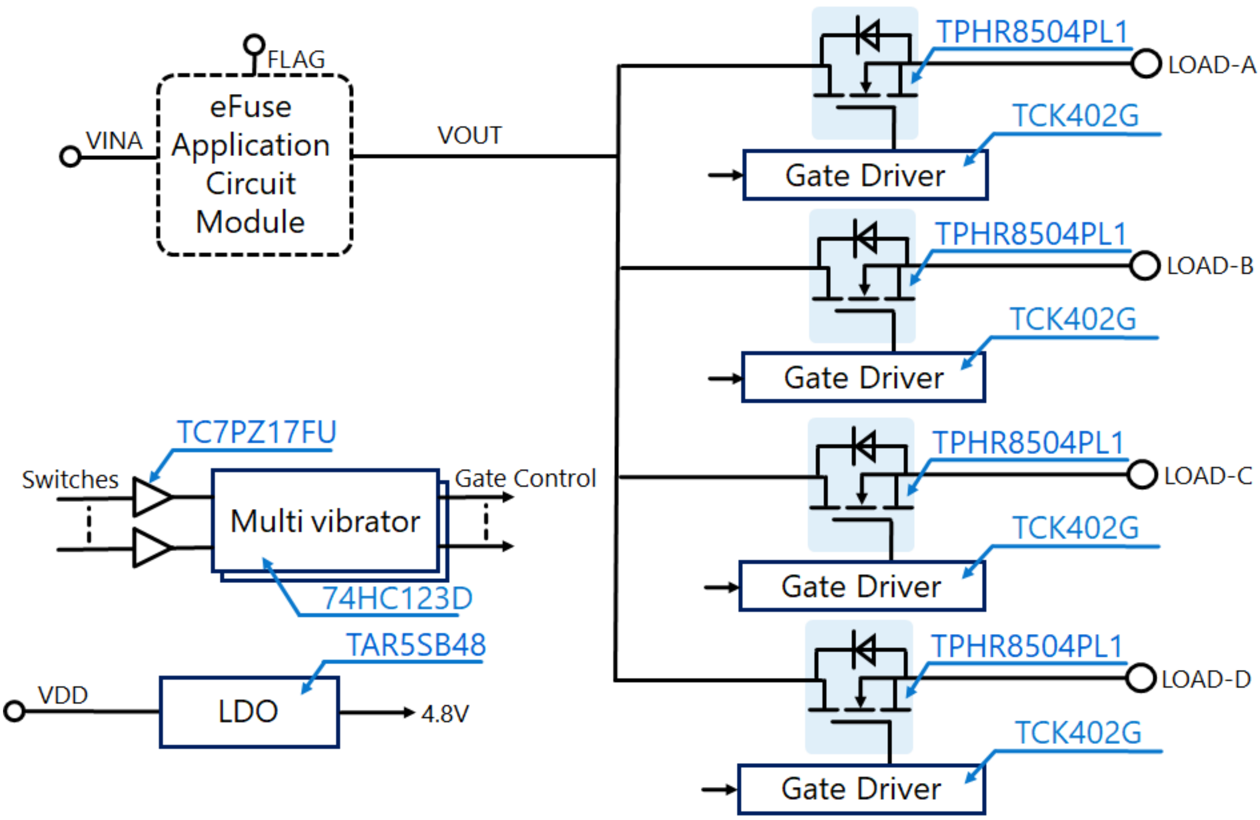


Fig. 2.2 Base Board Block Diagram

2.3. Appearance and Component Layout

The appearance and the component layout of the module board and the base board are shown below.

2.3.1. Module Board

Fig. 2.3 shows the appearance and Fig. 2.4 and 2.5 show the component layout of the module board.

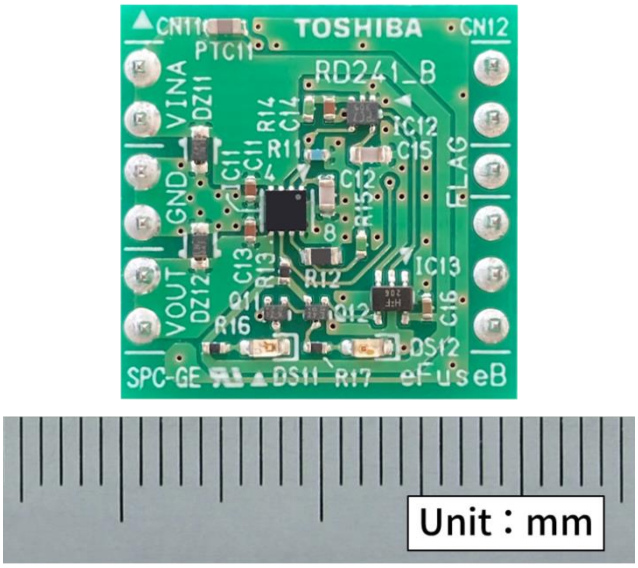


Fig. 2.3 Module Board (Top View)

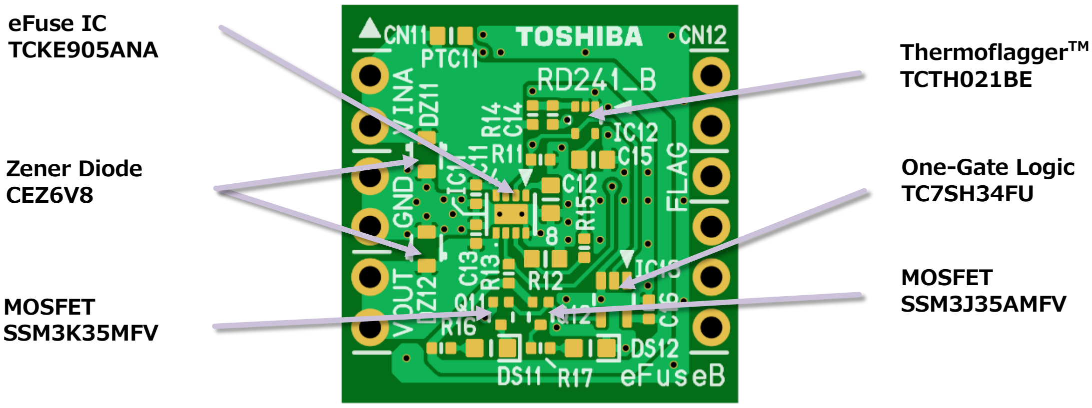


Fig. 2.4 Module Board Component Layout (Top View)

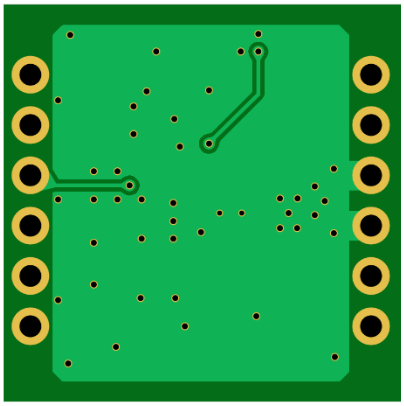


Fig. 2.5 Module Board Component Layout (Bottom View)

2.3.2. Base Board

Fig. 2.6 shows the appearance and Fig. 2.7 shows the component layout of the base board.

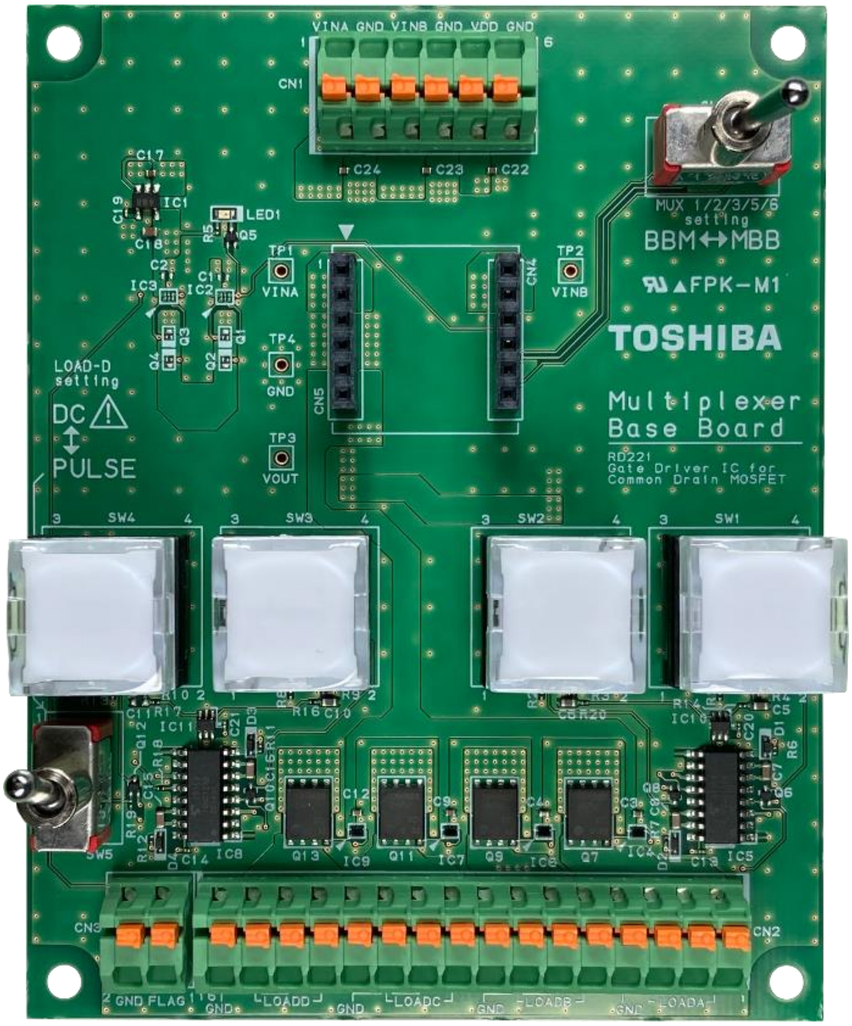


Fig. 2.6 Base Board (Top View)

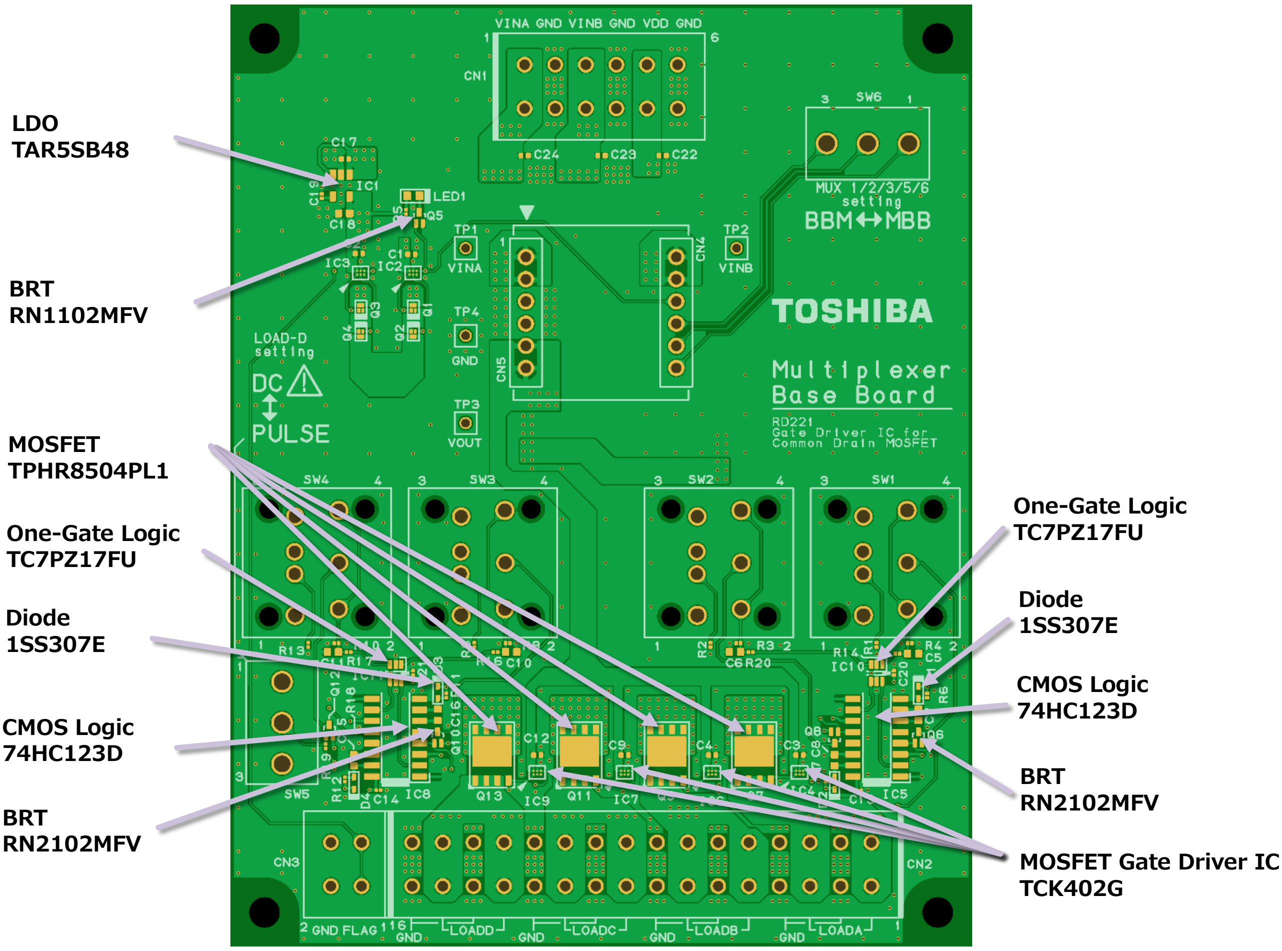


Fig. 2.7 Base Board Component Layout (Top View)

3. Schematic, Bill of Materials, and PCB Pattern

3.1. Schematic

Refer to the following files:

Module board RD241-SCHEMATIC2-xx.pdf
Base board RD221-SCHEMATIC7-xx.pdf
(xx is the revision number.)

3.2. Bill of Materials

Refer to the following files:

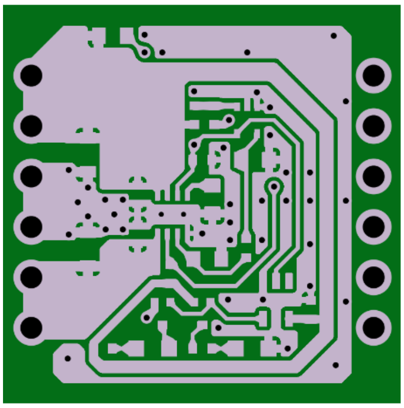
Module board RD241B-BOM1-xx.pdf
Base board RD221-BOM7-xx.pdf
(xx is the revision number.)

3.3. PCB Pattern

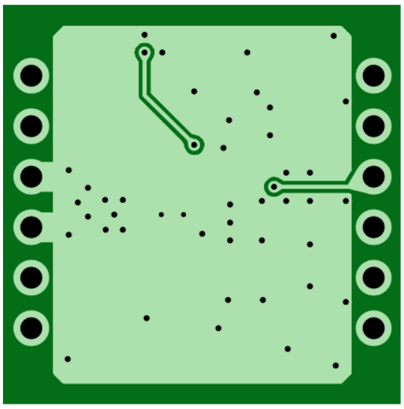
Fig. 3.1 shows the PCB pattern diagram of the module board, and Fig. 3.2 shows the pattern diagram of the base board.

For more details, refer to the following files:

Module board RD241-LAYER2-xx.pdf
Base board RD221-LAYER7-xx.pdf
(xx is the revision number.)

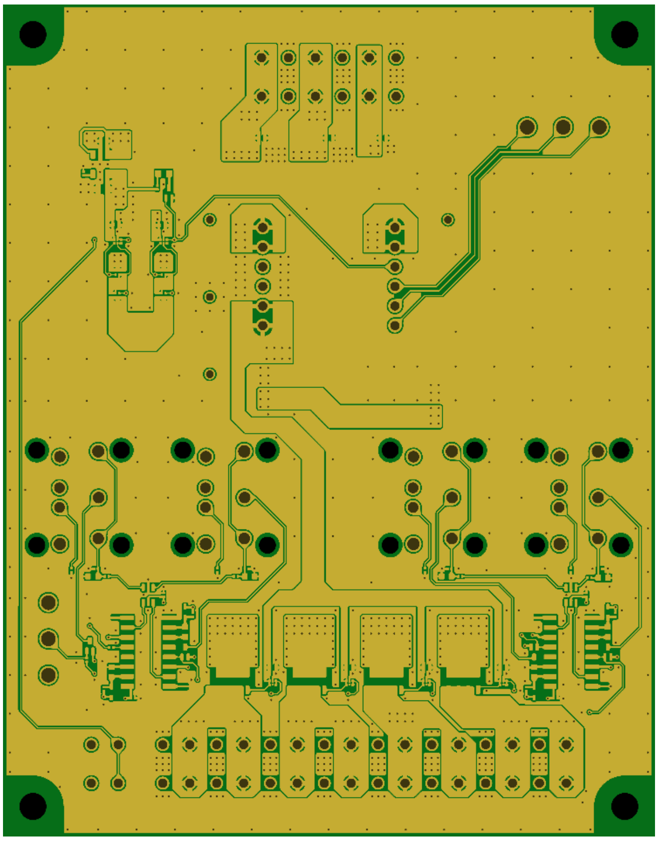


<Layer 1 Top>

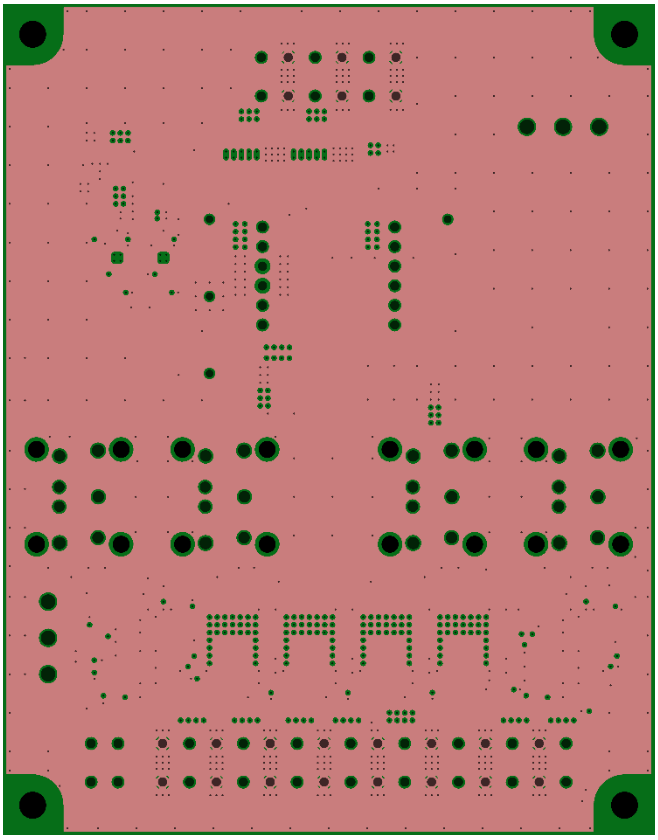


<Layer 2 Bottom>

Fig. 3.1 Module Board PCB Pattern Diagram (Top View)

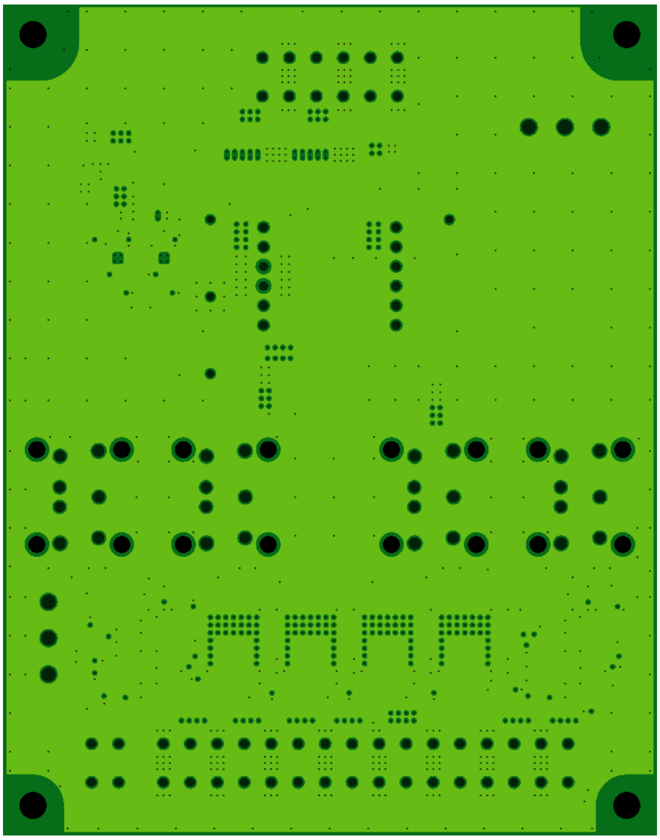


<LAYER1 Top>

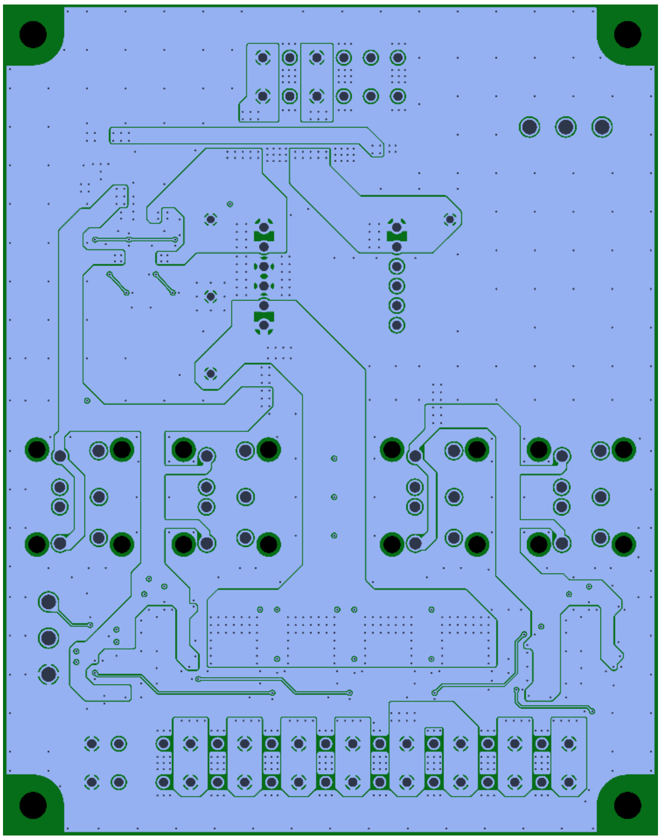


<LAYER2>

Fig. 3.2 (a) Base Board PCB Pattern Diagram (Top View)



<LAYER3>



<LAYER4 Bottom>

Fig. 3.2 (b) Base Board PCB Pattern Diagram (Top View)

4. Operation

4.1. Operation Procedure

The standard procedure to start up this design is as follows:

1. Connect the module board to the module board connector (CN4, CN5) on the base board as shown in Fig. 4.2.
2. At CN1 terminal block of the baseboard, first apply VDD power supply (5 V), and then apply VINA power supply (5 V).
3. To stop the operation, first turn off VINA power supply, and then turn off VDD power supply.
   *Be careful not to get burned from the overheated load resistance.

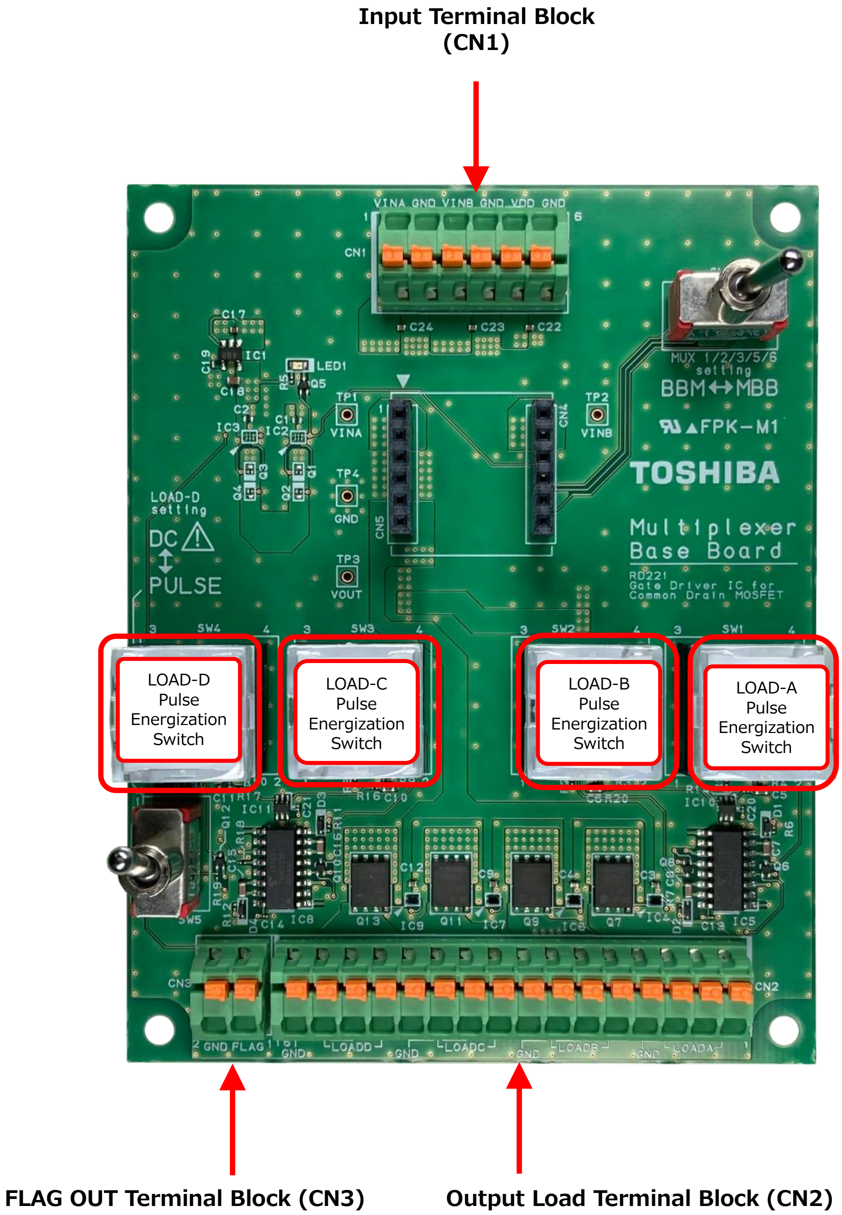


Fig. 4.1 Connectors and Switches on the Base Board

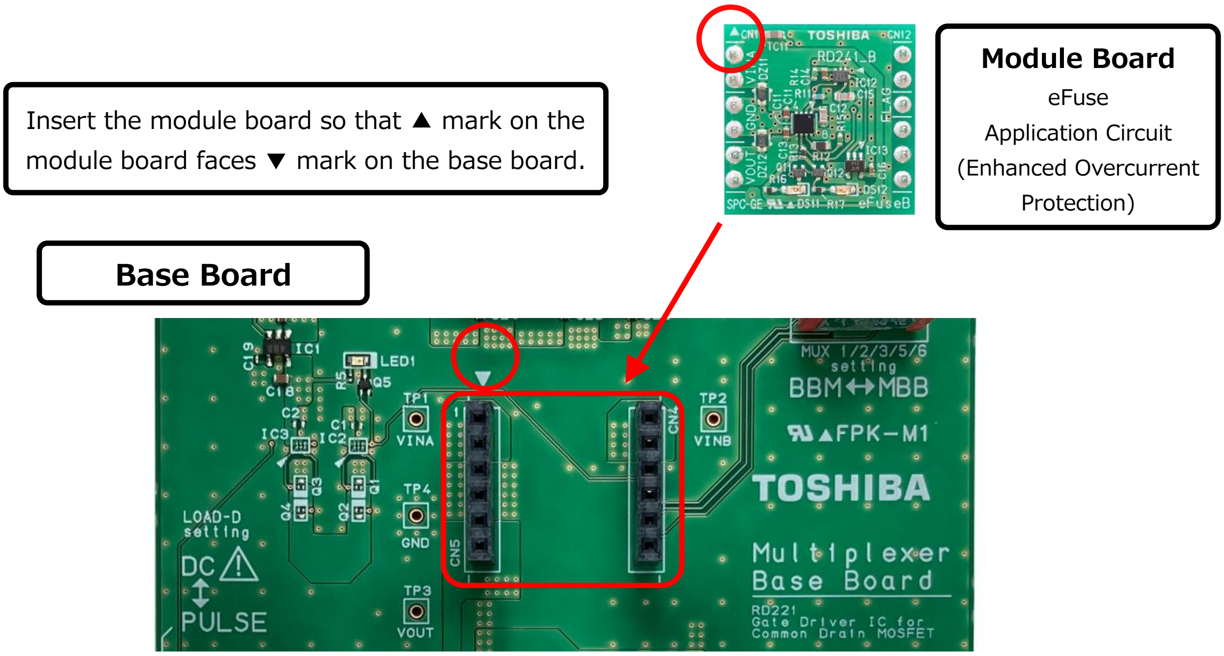


Fig. 4.2 Connection Between Base Board and Module Board

4.2. Base Board External Connector Specifications

The external connector specifications of the base board are as follows.

Table 4.1 Input Terminal Block (CN1) Specifications

Terminal No.	Input Terminal Name	Description	Voltage Range	Current Rating
1	VINA	eFuse Application Circuit (with Enhanced Overcurrent Protection) VINA input terminal	Max. 6 V	Max. 4 A*
2	GND	(GND of the above terminal)		
3	VINB	(not used)	-	-
4	GND	(not used)		
5	VDD	Power supply terminal for driving the base board	5 to 12 V	-
6	GND	(GND of the above terminal)		

* Individual component specifications allow a current flow greater than this value. However, the current on this board should not exceed this value because of the heat dissipation limitation.

Table 4.2 Output Load Terminal Block (CN2) Specifications

Terminal No.	Output Load Name	Description
1	LOAD-A	For resistive load connection
2		(GND of the above terminal)
3		For capacitive load connection
4		(GND of the above terminal)
5	LOAD-B	For resistive load connection
6		(GND of the above terminal)
7		For capacitive load connection
8		(GND of the above terminal)
9	LOAD-C	For resistive load connection
10		(GND of the above terminal)
11		For capacitive load connection
12		(GND of the above terminal)
13	LOAD-D	For resistive load connection
14		(GND of the above terminal)
15		For capacitive load connection
16		(GND of the above terminal)

Table. 4.3 FLAG Out Terminal Block (CN3) Specifications

Terminal No.	Output Terminal Name	Description
1	FLAG	FLAG output H-level (approximately 3.3 V) when VINA is input
2	GND	(GND of the above terminal)

4.3. Module Board Operation Summary

4.4. Overcurrent Detection

During overcurrent protection operation TCKE905ANA reduces the output current by lowering the output voltage. At this time, the power consumption of this device corresponds to the voltage difference (between its input and output) and the output current of this device. Therefore, TCKE905ANA (IC11) may generate heat temporarily and the overheat detection function may operate. Therefore, in this design, following actions are taken to avoid this.

TCTH021BE (IC12) is used for overcurrent detection. ILIM terminal of TCKE905ANA (IC11) outputs a current (approximately 1/3448) proportional to the output current of VOUT terminal. In this design the output current of more than 1.4 A is considered overcurrent. Therefore, when the output current is approximately 1.4 A, the voltage at PTCO terminal of TCTH021BE (IC12) exceeds its detection voltage (0.5 V (Typ.)), and PTCGOOD terminal becomes Low level. And in this situation EN/UVLO terminal of TCKE905ANA (IC11) connected to PTCGOOD terminal becomes Low level, VOUT is cut off, and TC7SH34FU (IC13) output becomes Low level. This causes SSM3K35MFV (Q11) to turn off, SSM3J35AMFV (Q12) to turn on, blue LED (DS11) to turn off, and the red LED (DS12) to turn on.

4.5. Over Temperature Detection

A voltage obtained by dividing the supply voltage by a PTC thermistor (PTC11) and a 4.7 kΩ resistor (R11) is applied to EN/UVLO terminal of TCKE905ANA (IC11). When PTC thermistor (PTC11) heats up, its resistance rises, the voltage of EN/UVLO terminal falls, and the output of TC7SH34FU (IC13) becomes Low level. This causes SSM3K35MFV (Q11) to turn off, SSM3J35AMFV (Q12) to turn on, blue LED (DS11) to turn off, and red LED (DS12) to turn on. In addition, TCKE905ANA (IC11) output current is cut off.

4.6. VOUT Cut Off of TCKE905ANA

The over temperature detection signal and the overcurrent detection signal are connected in a wired OR configuration and are also connected to the EN/UVLO terminal of TCKE905ANA (IC11) and to the input terminal of TC7SH34FU (IC13). For this reason, this design cuts off VOUT of TCKE905ANA when over temperature is detected or when overcurrent is detected. In this situation, the blue LED (DS11) is turned off and the red LED (DS12) is turned on.

5. Precautions

・Be careful of the electric shock as the applied voltage is high.
・Be careful not to get burned from the heat generated at the load.

Terms of Use

This terms of use is made between Toshiba Electronic Devices and Storage Corporation ("We") and Customer who downloads or uses this Reference Design. Customer shall comply with this terms of use. This Reference Design means all documents and data in order to design electronics applications on which our semiconductor device is embedded.

Section 1. Restrictions on usage

1. This Reference Design is provided solely as reference data for designing electronics applications. Customer shall not use this Reference Design for any other purpose, including without limitation, verification of reliability.
2. Customer shall not use this Reference Design for sale, lease or other transfer.
3. Customer shall not use this Reference Design for evaluation in high or low temperature, high humidity, or high electromagnetic environments.
4. This Reference Design shall not be used for or incorporated into any product or system whose manufacture, use, or sale is prohibited under any applicable laws or regulations.

Section 2. Limitations

1. We reserve the right to make changes to this Reference Design without notice.
2. This Reference Design should be treated as a reference only. WE ARE NOT RESPONSIBLE FOR ANY INCORRECT OR INCOMPLETE DATA AND INFORMATION.
3. Semiconductor devices can malfunction or fail. When designing electronics applications by referring to this Reference Design, Customer is responsible for complying with safety standards and for providing adequate designs and safeguards for their hardware, software and systems which minimize risk and avoid situations in which a malfunction or failure of semiconductor devices could cause loss of human life, bodily injury or damage to property, including data loss or corruption. Customer must also refer to and comply with the latest versions of all relevant our information, including without limitation, specifications, data sheets and application notes for semiconductor devices, as well as the precautions and conditions set forth in the "Semiconductor Reliability Handbook".
4. Designing electronics applications by referring to this Reference Design, Customer must evaluate the whole system sufficiently. Customer is solely responsible for applying this Reference Design to Customer's own product design or applications. WE ASSUME NO LIABILITY FOR CUSTOMER'S PRODUCT DESIGN OR APPLICATIONS.
5. WE SHALL NOT BE RESPONSIBLE FOR ANY INFRINGEMENT OF PATENTS OR ANY OTHER INTELLECTUAL PROPERTY RIGHTS OF THIRD PARTIES THAT MAY RESULT FROM THE USE OF THIS REFERENCE DESIGN. NO LICENSE TO ANY INTELLECTUAL PROPERTY RIGHT IS GRANTED BY THIS TERMS OF USE, WHETHER EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE.
6. THIS REFERENCE DESIGN IS PROVIDED "AS IS". WE (a) ASSUME NO LIABILITY WHATSOEVER, INCLUDING WITHOUT LIMITATION, INDIRECT, CONSEQUENTIAL, SPECIAL, OR INCIDENTAL DAMAGES OR LOSS, INCLUDING WITHOUT LIMITATION, LOSS OF PROFITS, LOSS OF OPPORTUNITIES, BUSINESS INTERRUPTION AND LOSS OF DATA, AND (b) DISCLAIM ANY AND ALL EXPRESS OR IMPLIED WARRANTIES AND CONDITIONS RELATED TO THIS REFERENCE DESIGN, INCLUDING WITHOUT LIMITATION, WARRANTIES OR CONDITIONS OF FUNCTION AND WORKING, WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, ACCURACY OF INFORMATION, OR NONINFRINGEMENT.

Section 3. Terms and Termination

It is assumed that Customer agrees to any and all this terms of use if Customer downloads or uses this Reference Design. We may, at its sole and exclusive discretion, change, alter, modify, add, and/or remove any part of this terms of use at any time without any prior notice. We may terminate this terms of use at any time and without any cause. Upon termination of this terms of use, Customer shall eliminate this Reference Design. Furthermore, upon our request, Customer shall submit to us a written confirmation to prove elimination of this Reference Design.

Section 4. Export Control

Customer shall not use or otherwise make available this Reference Design for any military purposes, including without limitation, for the design, development, use, stockpiling or manufacturing of nuclear, chemical, or biological weapons or missile technology products (mass destruction weapons). This Reference Design may be controlled under the applicable export laws and regulations including, without limitation, the Japanese Foreign Exchange and Foreign Trade Act and the U.S. Export Administration Regulations. Export and re-export of this Reference Design is strictly prohibited except in compliance with all applicable export laws and regulations.

Section 5. Governing Laws

This terms of use shall be governed and construed by laws of Japan, without reference to conflict of law principle.

Section 6. Jurisdiction

Unless otherwise specified, Tokyo District Court in Tokyo, Japan shall be exclusively the court of first jurisdiction for all disputes under this terms of use.