

eFuse Application Circuit (with Enhanced Overcurrent Protection)

Design guide

RD241B-DGUIDE-01

Toshiba Electronic Devices & Storage Corporation



Table of Contents

1.	Introduction	3
2.	Main Components Used	4
2.1.	eFuse IC TCKE905ANA	4
2.2.	Thermoflagger [™] TCTH021BE	5
2.3.	MOSFET	6
2.4.	L-MOS Logic IC	6
2.5.	Zener Diode	6
3.	Specifications and Block Diagram	7
3.1.	Specifications	7
3.2.	Block Diagrams	8
3.2.1	L. Module Board Block Diagram	8
3.2.2	2. Base Board Block Diagram	9
4.	Circuit Design1	0
4.1.	Module Board1	0
4.1.1	L. Over Temperature Detection1	1
4.1.2	2. Overcurrent Detection1	1
4.1.3	3. Setting the Slew Rate1	2
4.2.	Base Board 1	3
4.2.1	L. All Circuits on the Base Board1	3
4.2.2	2. Output Load Energizing Method1	5
5.	PCB Designs1	6
5.1.	Module Board 1	6
5.2.	Base Board 1	7
5.3.	Design Considerations 1	8



1. Introduction

This design guide document describes the design methodology of the eFuse Application Circuit (with Enhanced Overcurrent Protection).

In recent years, various protective functions have become important in various consumer devices such as notebook PCs, game machines, storage devices, servers, etc. This document describes the Protection Circuit (hereafter referred to as "this design"), which is ideal for these applications, it is built using the eFuse IC (electronic fuse) and the Thermoflagger™ IC.

eFuse IC (electronic fuse) operates when excessive current flows and has a fast current interruption function compared to the conventional fuse. In addition, it can be used repeatedly because it doesn't get destroyed by a single event of overcurrent. Various other protection functions, such as overvoltage protection, are also built in.

This Design consists of a module board and a base board.

The module board consists of an eFuse IC (TCKE905ANA) with overcurrent protection, a Thermoflagger™ IC (TCTH021BE) and a PTC thermistor (PTC11). In this design, Thermoflagger™ is used to monitor the current of the eFuse IC, and when it detects overcurrent, it cuts off the output of the eFuse IC. It also cuts off the output of the eFuse IC when the PTC thermistor (PTC11) heats up and its resistance rises, causing the output of voltage divided circuit (built using the PTC thermistor (PTC11) and a $4.7k\Omega$ resistor (R11)) to drop.

The base board is used for evaluating the module board. It is equipped with the N-ch power MOSFETs TPHR8504PL1, the MOSFET gate driver ICs TCK402G, the transistors with bias resistors for signal-control, the one-gate logic ICs TC7PZ17FU, and the CMOS logic ICs 74HC123D.

The base board is also used in the reference design of the Power Multiplexer Circuit.



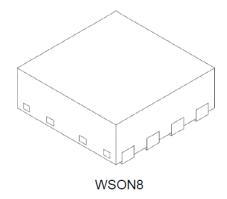
2. Main Components Used

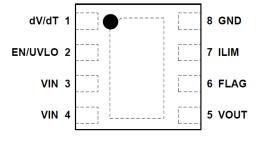
2.1. eFuse IC TCKE905ANA

The main features of TCKE905ANA are as follows. Please click here for more information.

- High input voltage: $V_{IN} = 25.0V$ (Max.)
- Low on-resistance: $R_{ON} = 34m\Omega$ (Typ.)
- Adjustable overcurrent limit: 0.5A to 4.0A
- Overvoltage clamp: TCKE905ANA: V_{OVC} = 5.7V (Typ.)
- Adjustable slew rate control by external capacitance for inrush current reduction
- Adjustable under voltage lockout by external resistor
- Thermal shutdown
- Small package
 WSON8 (2.0mm x 2.0mm (Typ.), t: 0.8mm (Max.))
- IEC62368-1 certification scheduled

Appearance and Terminal Layout







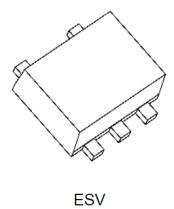
2.2. Thermoflagger[™] TCTH021BE

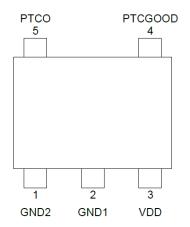
In this design it is used to monitor ILIM terminal of eFuse IC (TCKE905ANA). Please <u>click here</u> for more information.

The main features of TCTH021BE are as follows.

- PTCO output current: $I_{PTCO} = 10\mu A$ (Typ.)
- High PTCO output current accuracy: $\pm 8\%$ ($V_{DD} = 3.3V, 25^{\circ}C$)
- Low Current Consumption: $I_{DD} = 11.3 \mu A$ (Typ.)
- FLAG signal output (PTCGOOD): Open-drain type
- Standard package: ESV (SOT-553) (1.6mm x 1.6mm x 0.55mm)

Appearance and Terminal Layout







2.3. MOSFET

This design uses the following MOSFETs. Click the part number for details.

Product Number	Application	Package	V_{DSS}	V_{GSS}	R _{DS(ON)} (Max.)
SSM3K35MFV	For LED control	VESM	20V	+/-10V	4Ω@4.0V
SSM3J35AMFV	For LED control	VESM	-20V	+/-10V	1.1Ω@-4.5V

2.4. L-MOS Logic IC

This design uses the following L-MOS logic IC. Click the part number for details.

Product Number	Package	Function	Vcc
TC7SH34FU	USV	Non-Inverting Buffer	2.0V to 5.5V

2.5. Zener Diode

This design uses the following Zener diode. Click the part number for details.

Product Number	Package	V _z (V) (Typ.)	VESD
CEZ6V8	US2H	$6.8V@I_Z = 10mA$	±30kV



3. Specifications and Block Diagram

3.1. Specifications

Table 3.1 and Table 3.2 list the main specifications of this circuit.

Table 3.1 Module Board Specifications

Board Name	Input Voltage	Rated Output Current
eFuse Application Circuit	Min. 2.7V	1.4A (Typ.),
(with Enhanced Overcurrent	Typ. 5V	up to 4A with appropriate
Protection)	Max. 6V	resistor setting

Table 3.2 Base Board Specifications

Input/Output	Description
Input	VINA input (VINA 2.7V to 6V) VINB input (not used) Drive power supply (VDD 5V to 12V)
Output	Output load A to D (LOAD-A to LOAD-D, each Load can have both resistive load and capacitive load, Max current is 4A for the module board of this design) FLAG output (H-level (approximately 5V) is output when VINA is input)

2024-06-24



3.2. Block Diagrams

3.2.1. Module Board Block Diagram

Fig. 3.1 shows the block diagram of the module board.

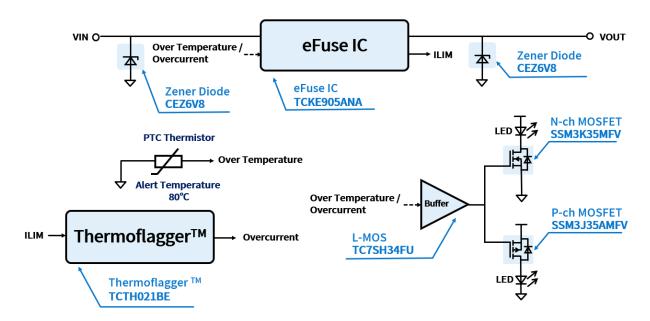


Fig. 3.1 Module Board Block Diagram

2024-06-24



3.2.2. Base Board Block Diagram

Fig. 3.2 shows the block diagram of the base board.

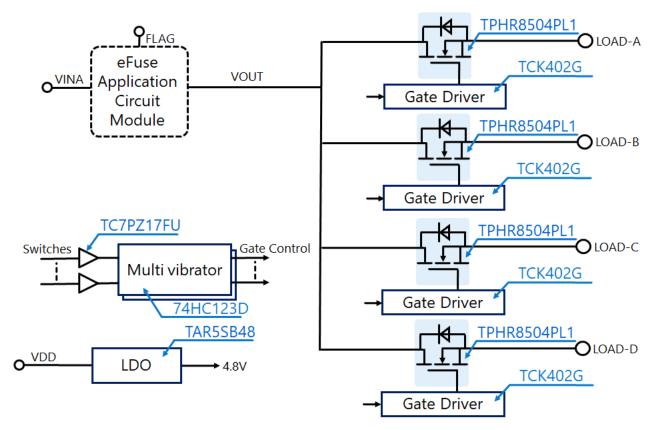


Fig. 3.2 Base Board Block Diagram



4. Circuit Design

4.1. Module Board

The circuit of the module board (eFuse Application Circuit (with Enhanced Overcurrent Protection)) is shown below.

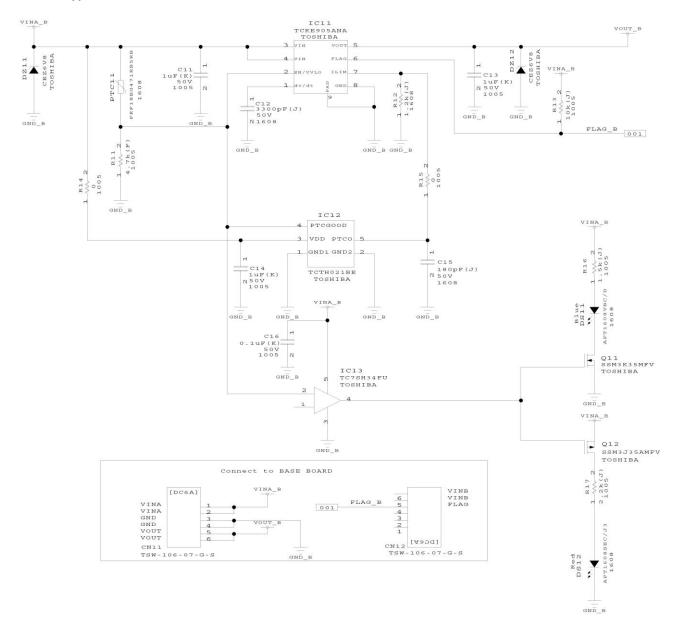


Fig. 4.1 Module Board Circuit Diagram



4.1.1. Over Temperature Detection

A voltage obtained by dividing the supply voltage by a PTC thermistor (PTC11) and a $4.7k\Omega$ resistor (R11) is applied to EN/UVLO terminal of TCKE905ANA (IC11). When PTC thermistor (PTC11) heats up, its resistance rises, the voltage of EN/UVLO terminal falls, and the output of TC7SH34FU (IC13) becomes Low level. This causes SSM3K35MFV (Q11) to turn off, SSM3J35AMFV (Q12) to turn on, blue LED (DS11) to turn off, and red LED (DS12) to turn on. In addition, TCKE905ANA (IC11) output current is cut off.

4.1.2. Overcurrent Detection

TCTH021BE (IC12) is used for overcurrent detection. The output limit current monitor gain G_{IMON} ($I_{\text{ILIM}}/I_{\text{OUT}}$) of TCKE905ANA (IC11) is 290 μ A/A (Typ.). Therefore, the relation between I_{OUT} and I_{ILIM} is as follows.

$$I_{OUT} A = \frac{1A}{290\mu A} \times I_{ILIM} A \cong 3448 \times I_{ILIM} A$$

The output current of the PTCO terminal of the TCTH021BE (IC12) is 10μ A (typ.) and the detection voltage VDET is 0.5V (typ.), therefore TCTH021BE (IC12) judges overcurrent when following condition is met:

$$(I_{ILIM} A + 10 \,\mu A) \times 1200\Omega \ge 0.5V$$

Therefore,

$$I_{ILIM} A \ge \frac{0.5V}{1200\Omega} - 10\mu A \cong 407\mu A$$

At this time, the output current of TCKE905ANA (IC11) VOUT is:

$$I_{OUT} A \cong 3448 \times I_{ILIM} A = 3448 \times 407 \mu A \cong 1.4A$$

Therefore, when the output current of the VOUT terminal of TCKE905ANA (IC11) is approximately 1.4A, TCTH021BE (IC12) judges it to be overcurrent, and PTCGOOD terminal of TCTH021BE (IC12) becomes Low level.

The minimum value of the overcurrent is determined by considering the charactersitic variation of TCTH021BE (IC12), i.e. the maximum value of the output current of the PTCO terminal is $12.2\mu A$ and the minimum value of the detection voltage V_{DET} is 0.42V. In this case the overcurrent is detected when following condition is met:

$$(I_{ILIM} A + 12.2\mu A) \times 1200\Omega \ge 0.42V$$

Therefore,

$$I_{ILIM} A \ge \frac{0.42V}{1200\Omega} - 12.2\mu A \cong 338\mu A$$

© 2024



At this time, the output current of TCKE905ANA (IC11) VOUT is:

$$I_{OUT} A \cong 3448 \times I_{ILIM} A = 3448 \times 338 \mu A \cong 1.17 A$$

Therefore, when the output current of VOUT terminal of TCKE905ANA (IC11) is approximately 1.17A, TCTH021BE (IC12) judges it to be overcurrent, and PTCGOOD terminal of TCTH021BE (IC12) becomes Low level.

As the PTCGOOD terminal goes to Low level, the EN/UVLO terminal of TCKE905ANA (IC11) goes to Low level and VOUT is cut off. In this case the output of TC7SH34FU (IC13) also becomes Low level, and therefore the MOSFET SSM3K35MFV (Q11) is turned off, the MOSFET SSM3J35AMFV (Q12) is turned on, the blue LED (DS11) is turned off and the red LED (DS12) is turned on.

For a stable operation, the resistance of the external resistor R_{ILIM} connected to ILIM terminal should be 1.5k Ω or less.

4.1.3. Setting the Slew Rate

The slew rate of VOUT can be set by connecting a capacitor to dV/dT terminal of TCKE905ANA (IC11).

VOUT slew rate of TCKE905ANA (IC11) in this design is:

$$SR_{ON} V / ms = \frac{42000}{C_{dV/dT} pF} = \frac{42000}{3300} \cong 12.7V / ms$$



4.2. Base Board

4.2.1. All Circuits on the Base Board

All circuits on the base board are shown below.

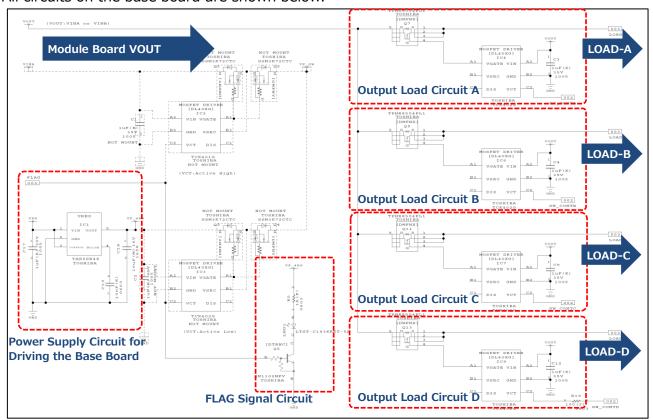


Fig. 4.2 Base Board Circuit (1)

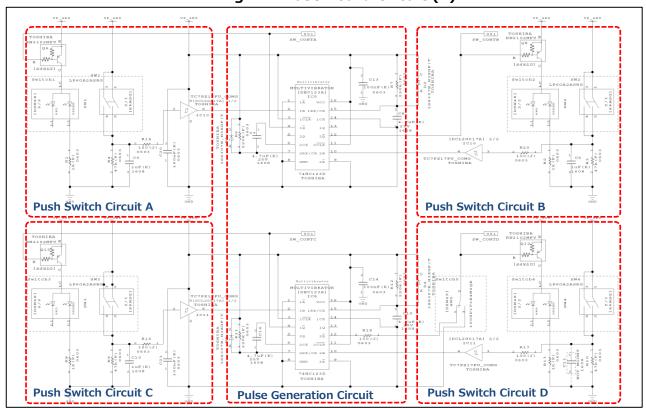


Fig. 4.3 Base Board Circuit (2)



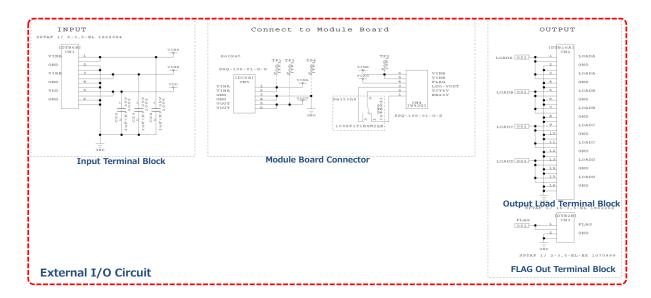


Fig. 4.4 Base Board Circuit (3)

The base board consists of the following circuits:

- (1) Power supply circuit for driving the base board

 It generates the power supply required to operate each circuit on the base board. The drive power supply VDD (5V to 12V) supplied to the input terminal block (CN1) is used to generate the internal power supply VP_4R8 (approximately 4.8V) via LDO TAR5SB48.
- (2) FLAG signal-on circuit

 The built-in resistor transistor (BRT) RN1102MFV lights the LED when FLAG output signal from the module board is High level (approximately 3.3V).
- (3) Output load circuit (A to D)
 High-side switches are configured with power MOSFET <u>TPHR8504PL1</u> and MOSFET gate driver IC <u>TCK402G</u>. The power-out VOUT of the module board is used to power TCK402G.
- (4) Push switch circuit (A to D)

 Four push switches are used to generate the trigger signals for pulse signal generation circuit.

 Resistor, capacitor and schmitt trigger input buffer TC7PZ17FU are used for removing fluctuations. While the pulse signal generated by the pulse generator is at High level, the LED in the key switch is lit and driven by the built-in resistor transistor RN2102MFV.
- (5) Pulse generation circuit

 Monostable multi-vibrator <u>74HC123D</u> uses the trigger signals from four push switches to generate a single-shot pulse of approximately 1 second for that system.
- (6) External I/O circuit Following connectors are used during the evaluation of the eFuse application circuit module board. The input terminal block (CN1) takes VINA input, and VDD input. The output load terminal block (CN2) allows to connect four loads (LOAD-A, LOAD-B, LOAD-C, LOAD-D). The terminal block (CN3) outputs FLAG signal. And connectors (CN4, CN5) are used for connecting the module board to the base board.



4.2.2. Output Load Energizing Method

Four pulse energization switches that output current to the load for approximately 1 second after pressing the switch and one DC energization/pulse energization switch are mounted on the base board.

There are four output loads (LOAD-A, LOAD-B, LOAD-C, LOAD-D) on the base board. When the corresponding pulse energization switch is pressed, one-shot pulse of the following duration is generated by the monostable multi-vibrator 74HC123D, and the high-side switch of the output load circuit is turned on and current flows to the output load while this pulse is at the High level.

$$t_{wout} = 1 \times Cx \times Rx = 1 \times 4.7 \mu F \times 220 k\Omega$$
 (approximately 1.03sec)

As for LOAD-D output, if DC energization/pulse energization switch is switched to DC energization, DC energization takes precedence over pulse energization, and current is continuously output. Therefore, be careful not to overheat or burn the load when DC energization is enabled.

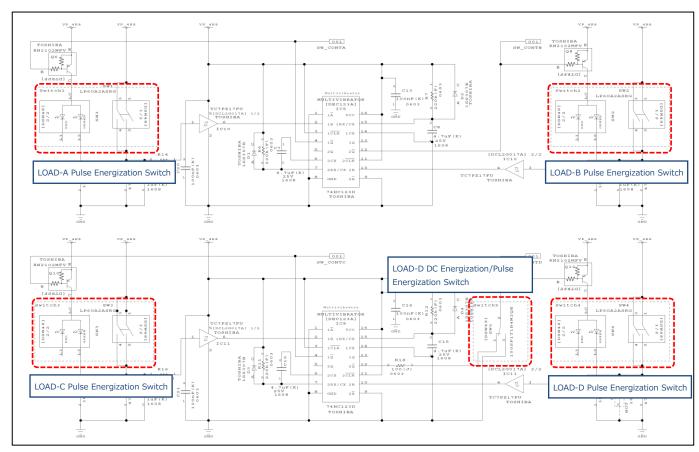


Fig. 4.5 Switches Related to Output Load Energization on Base Board Circuit



5. PCB Designs

5.1. Module Board

Fig. 5.1 shows an example of the component layout of the module board (eFuse Application Circuit (with Enhanced Overcurrent Protection)).

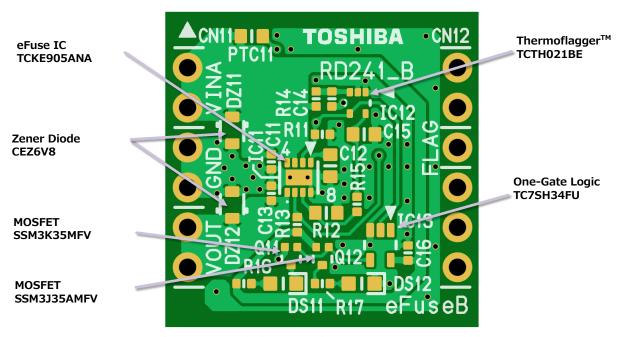


Fig. 5.1 Module Board Component Layout



5.2. Base Board

Fig. 5.2 shows an example of the component layout of the base board.

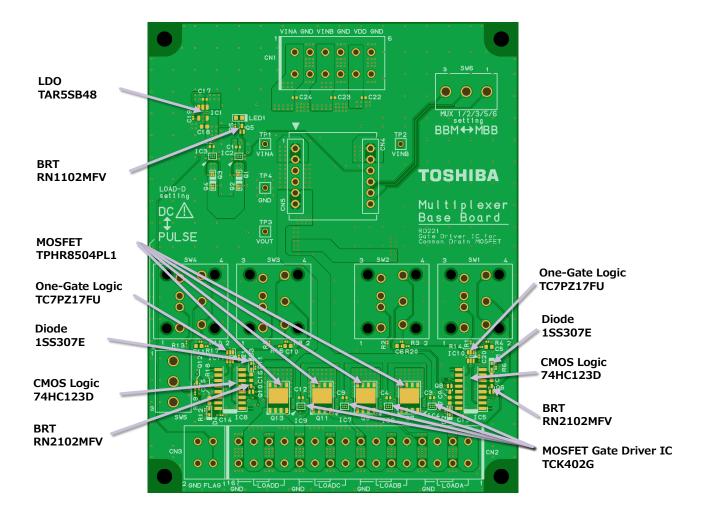


Fig. 5.2 Base Board Component Layout



5.3. Design Considerations

Points to consider during PCB pattern design:

- Pattern Design Considering Current
 - Since the base board and the module board have circuits in which large currents flow, a sufficient pattern width must be ensured in designing the pattern to prevent problems due to temperature rise or voltage drop caused by the pattern when the maximum current with added margin is applied.
- Ground peripheral pattern design
 - In order to suppress the voltage drop when current flows, it is necessary to consider good GND wiring, such as providing a ground plane or minimizing the pattern length.



Terms of Use

This terms of use is made between Toshiba Electronic Devices and Storage Corporation ("We") and Customer who downloads or uses this Reference Design. Customer shall comply with this terms of use. This Reference Design means all documents and data in order to design electronics applications on which our semiconductor device is embedded.

Section 1. Restrictions on usage

- 1. This Reference Design is provided solely as reference data for designing electronics applications. Customer shall not use this Reference Design for any other purpose, including without limitation, verification of reliability.
- 2. Customer shall not use this Reference Design for sale, lease or other transfer.
- 3. Customer shall not use this Reference Design for evaluation in high or low temperature, high humidity, or high electromagnetic environments.
- 4. This Reference Design shall not be used for or incorporated into any product or system whose manufacture, use, or sale is prohibited under any applicable laws or regulations.

Section 2. Limitations

- 1. We reserve the right to make changes to this Reference Design without notice.
- 2. This Reference Design should be treated as a reference only. WE ARE NOT RESPONSIBLE FOR ANY INCORRECT OR INCOMPLETE DATA AND INFORMATION.
- 3. Semiconductor devices can malfunction or fail. When designing electronics applications by referring to this Reference Design, Customer is responsible for complying with safety standards and for providing adequate designs and safeguards for their hardware, software and systems which minimize risk and avoid situations in which a malfunction or failure of semiconductor devices could cause loss of human life, bodily injury or damage to property, including data loss or corruption. Customer must also refer to and comply with the latest versions of all relevant our information, including without limitation, specifications, data sheets and application notes for semiconductor devices, as well as the precautions and conditions set forth in the "Semiconductor Reliability Handbook".
- 4. Designing electronics applications by referring to this Reference Design, Customer must evaluate the whole system sufficiently. Customer is solely responsible for applying this Reference Design to Customer's own product design or applications. WE ASSUME NO LIABILITY FOR CUSTOMER'S PRODUCT DESIGN OR APPLICATIONS.
 5. WE SHALL NOT BE RESPONSIBLE FOR ANY INFRINGEMENT OF PATENTS OR ANY OTHER INTELLECTUAL PROPERTY RIGHTS OF THIRD PARTIES THAT MAY RESULT FROM THE USE OF THIS REFERENCE DESIGN. NO LICENSE TO ANY INTELLECTUAL PROPERTY RIGHT IS GRANTED BY THIS TERMS OF USE, WHETHER EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE.
- 6. THIS REFERENCE DESIGN IS PROVIDED "AS IS". WE (a) ASSUME NO LIABILITY WHATSOEVER, INCLUDING WITHOUT LIMITATION, INDIRECT, CONSEQUENTIAL, SPECIAL, OR INCIDENTAL DAMAGES OR LOSS, INCLUDING WITHOUT LIMITATION, LOSS OF PROFITS, LOSS OF OPPORTUNITIES, BUSINESS INTERRUPTION AND LOSS OF DATA, AND (b) DISCLAIM ANY AND ALL EXPRESS OR IMPLIED WARRANTIES AND CONDITIONS RELATED TO THIS REFERENCE DESIGN, INCLUDING WITHOUT LIMITATION, WARRANTIES OR CONDITIONS OF FUNCTION AND WORKING, WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, ACCURACY OF INFORMATION, OR NONINFRINGEMENT.

Section 3. Terms and Termination

It is assumed that Customer agrees to any and all this terms of use if Customer downloads or uses this Reference Design. We may, at its sole and exclusive discretion, change, alter, modify, add, and/or remove any part of this terms of use at any time without any prior notice. We may terminate this terms of use at any time and without any cause. Upon termination of this terms of use, Customer shall eliminate this Reference Design. Furthermore, upon our request, Customer shall submit to us a written confirmation to prove elimination of this Reference Design.

Section 4. Export Control

Customer shall not use or otherwise make available this Reference Design for any military purposes, including without limitation, for the design, development, use, stockpiling or manufacturing of nuclear, chemical, or biological weapons or missile technology products (mass destruction weapons). This Reference Design may be controlled under the applicable export laws and regulations including, without limitation, the Japanese Foreign Exchange and Foreign Trade Act and the U.S. Export Administration Regulations. Export and re-export of this Reference Design is strictly prohibited except in compliance with all applicable export laws and regulations.

Section 5. Governing Laws

This terms of use shall be governed and construed by laws of Japan, without reference to conflict of law principle.

Section 6. Jurisdiction

Unless otherwise specified, Tokyo District Court in Tokyo, Japan shall be exclusively the court of first jurisdiction for all disputes under this terms of use.

19 / **19** 2024-06-24