32-bit RISC Microcontroller
Reference Manual

Asynchronous Serial Communication Circuit (UART-C)

Revision 2.3

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Toshiba Electronic Devices & Storage Corporation

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Conventions

- Numeric formats follow the rules as shown below:
  Hexadecimal: 0xABC
  Decimal: 123 or 0d123 - Only when it needs to be explicitly shown that they are decimal numbers.
  Binary: 0b111 - It is possible to omit the "0b" when the number of bits can be distinctly understood from a sentence.
- "_N" is added to the end of signal names to indicate low active signals.
- It is called "assert" that a signal moves to its active level, "deassert" to its inactive level.
- When two or more signal names are referred, they are described like as [m:n].
  Example: S[3:0] shows four signal names S3, S2, S1 and S0 together.
- The characters surrounded by ***[ ]*** defines the register.
  Example: ***[ABCD]***
- "N" substitutes suffix number of two or more same kind of registers, fields, and bit names.
  Example: ***[XYZ1]***, ***[XYZ2]***, ***[XYZ3]*** → ***[XYZn]***
- "x" substitutes suffix number or character of units and channels in the register list.
- In case of unit, "x" means A, B, and C, ...
  Example: ***[ADACR0]***, ***[ADBCR0]***, ***[ADCCR0]*** → ***[ADxCR0]***
- In case of channel, "x" means 0, 1, and 2, ...
  Example: ***[T32A0RUNA]***, ***[T32A1RUNA]***, ***[T32A2RUNA]*** → ***[T32AxRUNA]***
- The bit range of a register is written like as [m: n].
  Example: Bit[3: 0] expresses the range of bit 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.
  Example: ***[ABCD]***<EFG> = 0x01 (hexadecimal), ***[XYZn]***<VW> = 1 (binary)
- Word and byte represent the following bit length.
  Byte: 8 bits
  Half word: 16 bits
  Word: 32 bits
  Double word: 64 bits
- Properties of each bit in a register are expressed as follows:
  R: Read only
  W: Write only
  R/W: Read and write are possible.
- Unless otherwise specified, register access supports only word access.
- The register defined as "Reserved" must not be rewritten. Moreover, do not use the read value.
- The value read from the bit having default value of "-" is unknown.
- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value, In the cases that default is "-", follow the definition of each register.
- Reserved bits of the write-only register should be written with their default value. In the cases that default is "-", follow the definition of each register.
- Do not use read-modified-write processing to the register of a definition which is different by writing and read out.

Terms and Abbreviations

Some of abbreviations used in this document are as follows:

ACK	Acknowledgement
CTS	Clear to Send
DMA	Direct Memory Access
FIFO	First-In First-Out
LSB	Least Significant Bit
MSB	Most Significant Bit
RTS	Request to Send
TRGSEL	Trigger Selection Circuit
UART	Universal Asynchronous Receiver Transmitter

1. Outlines

The asynchronous serial communication circuit (UART) can operate as a transmission / reception circuit of 1 channel (UTxTXDA / UTxTXDB / UTxRXD) per unit. The following is a list of functions.

Function classification	Function	Operation explanation
Baud rate control	Frequency dividing ratio of prescaler	Selectable from 1/1 to 1/512 of the ΦT0 frequency for prescaler clock.
	Baud rate generator	N dividing or N + (64 - K) / 64 (N = 1 to 65535 and K = 0 to 63) dividing of the source clock frequency are possible.
Data format	Data length	Selectable 7, 8, or 9-bit.
	Parity	Parity control: Enable or disable selection Parity type: Even or odd parity is selectable
	Stop bit length	Selectable 1-bit or 2-bit.
	Data transfer order	Selectable LSB first or MSB first.
	Data signal inversion	Inversion control of the input and output data signal. Selectable disabled or enabled.
Transmission / reception control	FIFO storage stages	Reception: 8 stages Transmission: 8 stages
	Noise canceling function	Reception: Noise canceling function is enabled or disabled for UTxRXD.
	Error detection	Reception: Parity error, framing error, break error, overrun error Transmission: Trigger transmission error
	Handshake function	Transmission / reception control by handshake with UTxCTS_N / UTxRTS_N signal is possible.
	Wake-up function	The wakeup operation of the slave controller is enabled in the 9-bit mode is possible.
Interlocking control	Interrupt	Reception interrupt, transmission interrupt, and error interrupt.
	DMA request	Reception DMA request: burst transfer or single transfer Transmission DMA request: burst transfer or single transfer
Special control	Half clock mode (Transmission / reception)	Transmission and reception with half width of low width of the normal UART waveform is possible.
	Loopback function (Test function)	The transmission data is connected to the reception data and the loopback test is possible.
	Software reset	Initialization can be done by software.

UTxTXDA can be exchanged for UTxRXD and UTxCTS_N can be exchanged for UTxRTS_N, too. This is done by a port setting. Refer to "Input/Output Ports" of the reference manual.

2. Configuration

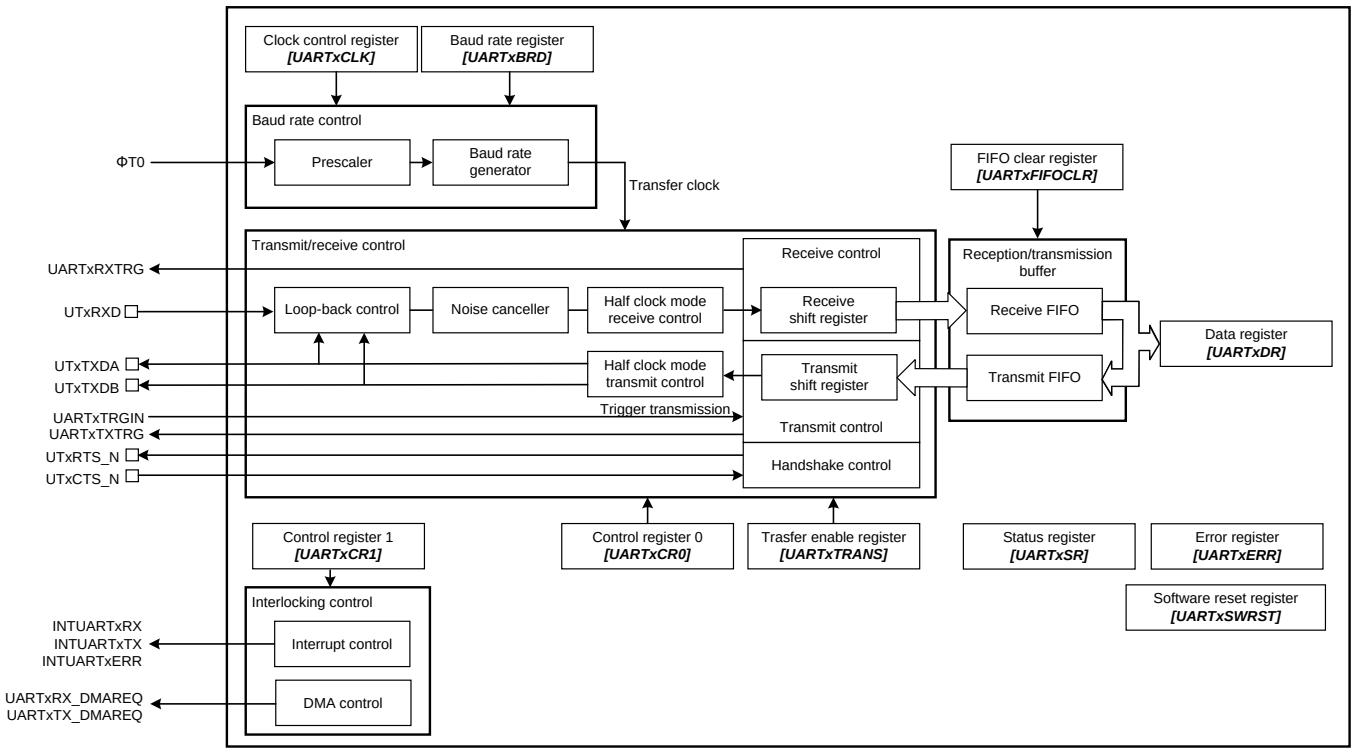

Figure 2.1 UART Block Diagram

Table 2.1 List of Signals

No	Symbol	Signal name	I/O	Related reference manual
1	ΦT0	Prescaler clock	Input	Clock Control and Operation Mode
2	UTxRXD	Data input pin	Input	Data Sheet
3	UTxTXDA	Data output pin A	Output	Data Sheet
4	UTxTXDB	Data output pin B	Output	Data Sheet
5	UTxRTS_N	Request to send signal pin	Output	Data Sheet
6	UTxCTS_N	Clear to send signal pin	Input	Data Sheet
7	UARTxTRGIN	Trigger transmission signal input pin	Input	Product Information
8	INTUARTxRX	Reception interrupt	Output	Exception
9	INTUARTxTX	Transmission interrupt	Output	Exception
10	INTUARTxERR	Error interrupt	Output	Exception
11	UARTxRXTRG	Reception completion trigger	Output	Product Information
12	UARTxTXTRG	Transmission completion trigger	Output	Product Information
13	UARTxRX_DMAREQ	Reception DMA request	Output	Product Information
14	UARTxTX_DMAREQ	Transmission DMA request	Output	Product Information

3. Function and Operation

3.1. Clock Supply

When UART is used, the corresponding clock enable bits should be set to "1" (Clock supply) in fsys supply stop register A (***[CGFSYSENA]*** and ***[CGFSYSMENA]***), fsys supply stop register B (***[CGFSYSENB]*** and ***[CGFSYSMENB])***, fsys supply stop register C (***[CGFSYSMENC]***), and fc supply stop register (***[CGFCEN]***).

The corresponding registers and the bit locations depend on a product. Some products do not have all registers. For the details, refer to "Clock Control and Operation Mode" in Reference manual.

When attempting to stop supplying the clock, make sure to check whether the UART has been stopped. Note that when the MCU enters STOP mode, make sure to check whether the UART has been stopped as well.

3.2. Transfer Clock (Baud Rate Generator)

The following shows the diagram of the transfer clock generator.

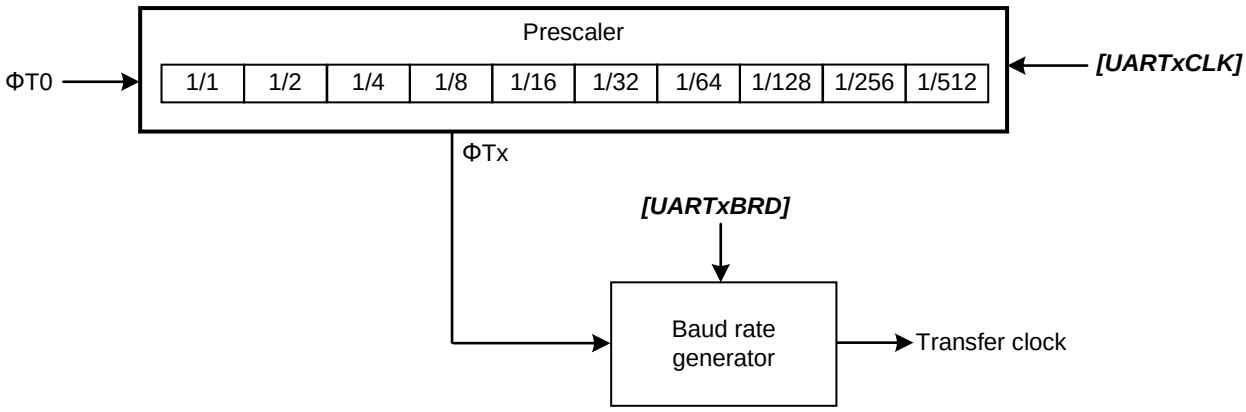

Figure 3.1 Transfer Clock Generator

The prescaler divides the frequency of the prescaler clock (ΦT0) into 1/1 to 1/512. The dividing value is selected by ***[UARTxCLK]*** <PRSEL>.

The baud rate generator divides the frequency of the input clock into N dividing or N + (64 - K) /64 dividing. The setting of the dividing value is done in ***[UARTxBRD]***. The transfer clock frequency is 16 times the baud rate.

The baud rate is calculated as follows:

$$\text{Baud rate} = \frac{\Phi Tx}{N + \frac{(64 - K)}{64}} / 16$$

The baud rate of the N dividing is calculated as follows:

$$\text{Baud rate} = \frac{\Phi Tx}{N} / 16$$

Note: The maximum baud rate is different depending on the product, please refer to the datasheet or "Product Information" of the reference manual.

3.3. Data Format

The summary of the data formats is shown in Table 3.1 and Figure 3.2.
A data length, a data transfer order, a parity, a STOP bit length, and a data signal inversion can be selected.

Table 3.1 Transfer Mode

Data length	Data transfer order	Parity	STOP bit length (transmission)	Data signal inversion
7 bits	LSB first / MSB first	Presence / absence Even / odd	1 bit or 2 bits	Performed / not performed
8 bits				
9 bits				

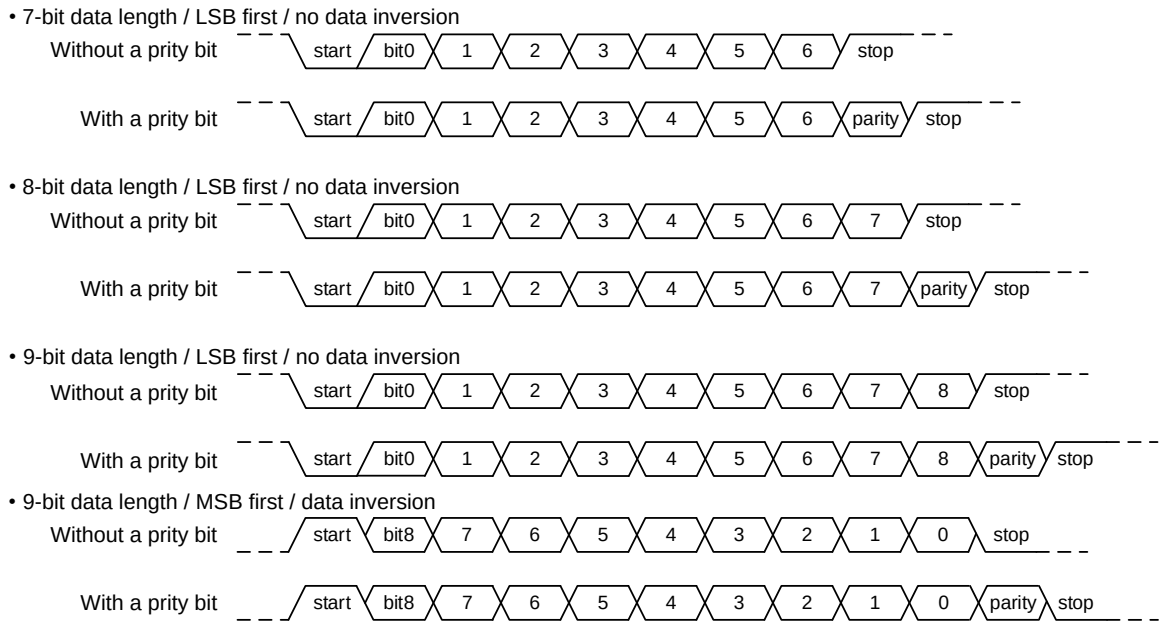

Figure 3.2 Data Format

(1) Data length
Selected from among 7, 8, and 9-bit.

(2) Parity control
When ***[UARTxCR0]***<PE> is set to "1", the parity is enabled. The even or odd parity can be selected by ***[UARTxCR0]***<EVEN>.

The parity control circuit generates automatically a parity for the data in the transmission buffer at data transmission. The settings of <PE> and <EVEN> should be done before the transmission data is written to ***[UARTxDR]***<DR> (Transmission data).

The parity is automatically generated from the reception data at data reception. The generated parity is compared with the received parity. If they are not identical, the parity error is generated.

(3) STOP bit length
[UARTxCR0]<SBLEN> (STOP bit length select) can set the STOP bit length in the UART transmission mode to 1-bit or 2-bit. At data reception, the STOP bit length is handled as 1 bit regardless of the setting value of this bit.

(4) Transmission signals
In the standard UART communication, the signals are output on the UTxTXDA pin.
In the half clock mode, the signals are output on the UTxTXDA pin and the UTxTXDB pin. For the details, refer to "3.9 Half Clock Mode".

(5) Data signal inversion
The data inversion is set by ***[UARTxCR0]***<IV> (Data signal inversion). When it is set to "1", the input and output data are inverted.

(6) Data exchange
The function of UTxTXDA, UTxRXD, UTxCTS_N, and UTxRTS_N can be exchanged. This is done by a port setting. Refer to "Input/Output Ports" of the reference manual.

3.4. Reception Buffer/Transmission Buffer

Received data / transmitted data is stored in reception buffer / transmission buffer.

The reception buffer and the transmission buffer consist of a shift register and a FIFO. The stage count of the receive FIFO and transmit FIFO are "8", respectively.

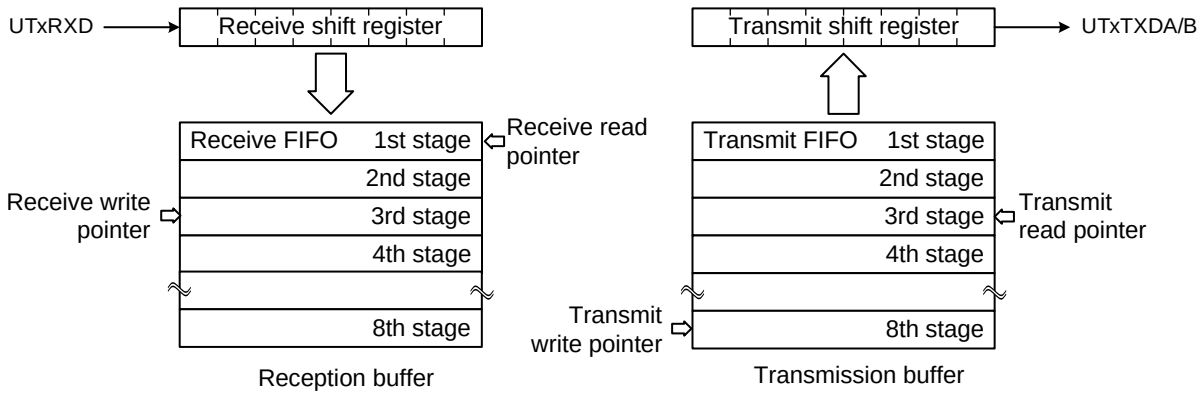

Figure 3.3 Data Buffer Configuration

3.4.1. Reception Buffer

When all bits (one frame) of data input from UTxRXD are stored in the receive shift register, the data is transferred to the receive FIFO and the receive write pointer is moved to the next stage. When the receive FIFO is read, the receive read pointer moves to the next stage. The data in the receive FIFO is read through ***[UARTxDR]*** (Data register).

The stage count of the data stored in the receive FIFO is shown in ***[UARTxSR]***<RLVL> (Receive FIFO data storage level). The register ***[UARTxDR]*** should not be read when the receive FIFO is empty.

When the stage count of the data stored in the receive FIFO becomes identical with the count value set in the register ***[UARTxCR1]***<RIL> (Reception Fill level setting), ***[UARTxSR]***<RXFF> (Receive FIFO flag) is set to "1". Then, a reception interrupt is generated if ***[UARTxCR1]***<INTRXFE> is set to "1" to enable a reception interrupt (Note). If receive FIFO interrupt control is enabled. The value of ***[UARTxCR1]***<RIL> can be set to "1" to "8".

If ***[UARTxFIFOCLR]***<RFCLR> is set to "1", the read/write pointer of the receive FIFO is initialized.

Note: Do not set the reception complete interrupt control enable (<INTRXWE> =1) and the receive FIFO interrupt control enable (<INTRXFE> =1) at the same time.

3.4.2. Transmission Buffer

The data written to ***[UARTxDR]*** (Data register) is stored in the transmit FIFO, and the transmit write pointer moves to the next stage. When data transmission is enabled, the data in the transmit FIFO is transferred to the transmission shift register. Then, the data is output on UTxTXDA/B pins. When the transmit FIFO is transferred, the transmit read pointer moves to the next stage.

The stage count of the data in the transmit FIFO is shown in ***[UARTxSR]***<TLVL> (Transmit FIFO data storage level).

When the data in the transmit FIFO is transferred to the transmission shift register and the stage count of the data in the transmit FIFO becomes identical with the count value set in ***[UARTxCR1]***<TIL> (Transmission Fill level setting), ***[UARTxSR]***<TXFF> (Transmit FIFO flag) is set to "1". Then, a transmission interrupt is generated if ***[UARTxCR1]***<INTTXFE> is set to "1" to enable a transmission interrupt. The value of ***[UARTxCR1]***<TIL> can be set to "0" to "7".

If ***[UARTxFIFOCLR]***<TFCLR> (Transmission buffer clear) is set to "1", the read/write pointer of the transmit FIFO is initialized.

3.5. Data Reception

3.5.1. Basic Operation

If ***[UARTxTRANS]***<RXE> is set to "1", the data reception is enabled. When the START bit is detected, the data reception starts. The data bits and the STOP bit is received. When ***[UARTxTRANS]***<RXE> =1 is set and UTxRXD is "Low", it is regarded immediately as start bit detection.

After one frame data is received completely, the data is transferred from the receive shift register to the receive FIFO. The reception completion flag is set. If the reception completion interrupt control is enabled by ***[UARTxCR1]***<INTRXWE> =1, the reception interrupt is generated.

If the reception FIFO interrupt control is enabled by ***[UARTxCR1]***<INTRXFE> =1, the receive interrupt is generated when the amount of the data in the receive FIFO reaches the Fill level which is set in ***[UARTxCR1]*** <RIL> (Reception Fill level setting).

Note: Do not set the reception complete interrupt control enable (<INTRXWE> =1) and the receive FIFO interrupt control enable (<INTRXFE> =1) at the same time.

The followings are examples to generate the reception interrupt.

- When the Fill level is "1" (***[UARTxCR1]***<RIL> =001):
  One frame data is received completely when the receive FIFO is empty. And the received data is transferred from the receive shift register to the receive FIFO. Then, the storage stage count in the receive FIFO becomes "1".

- When the Fill level is "8" (***[UARTxCR1]***<RIL> =000):
  One frame data is received completely when the receive FIFO stores 7-stage data. And the received data is transferred from the receive shift register to the receive FIFO. Then, the storage stage count in the receive FIFO becomes "8".

If ***[UARTxTRANS]***<RXE> is set to "0" during the data reception, the data reception completes and the operation stops.

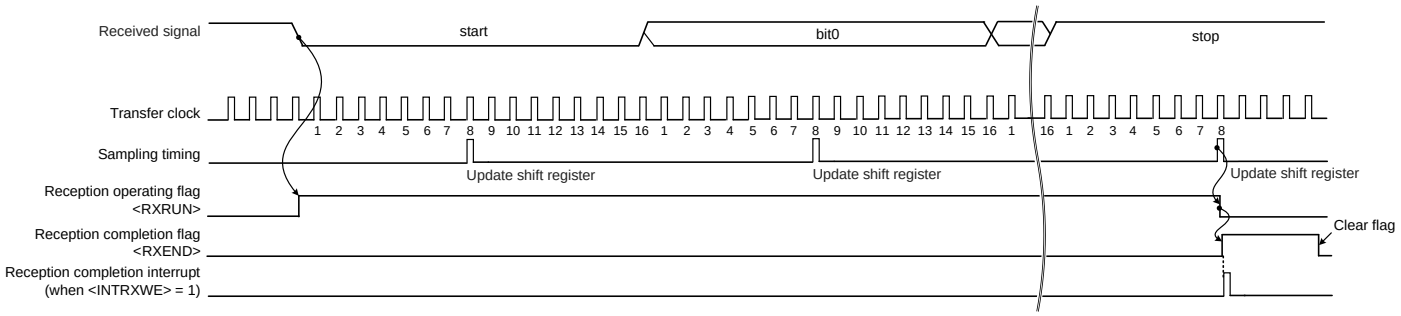

Figure 3.4 Receive Timing

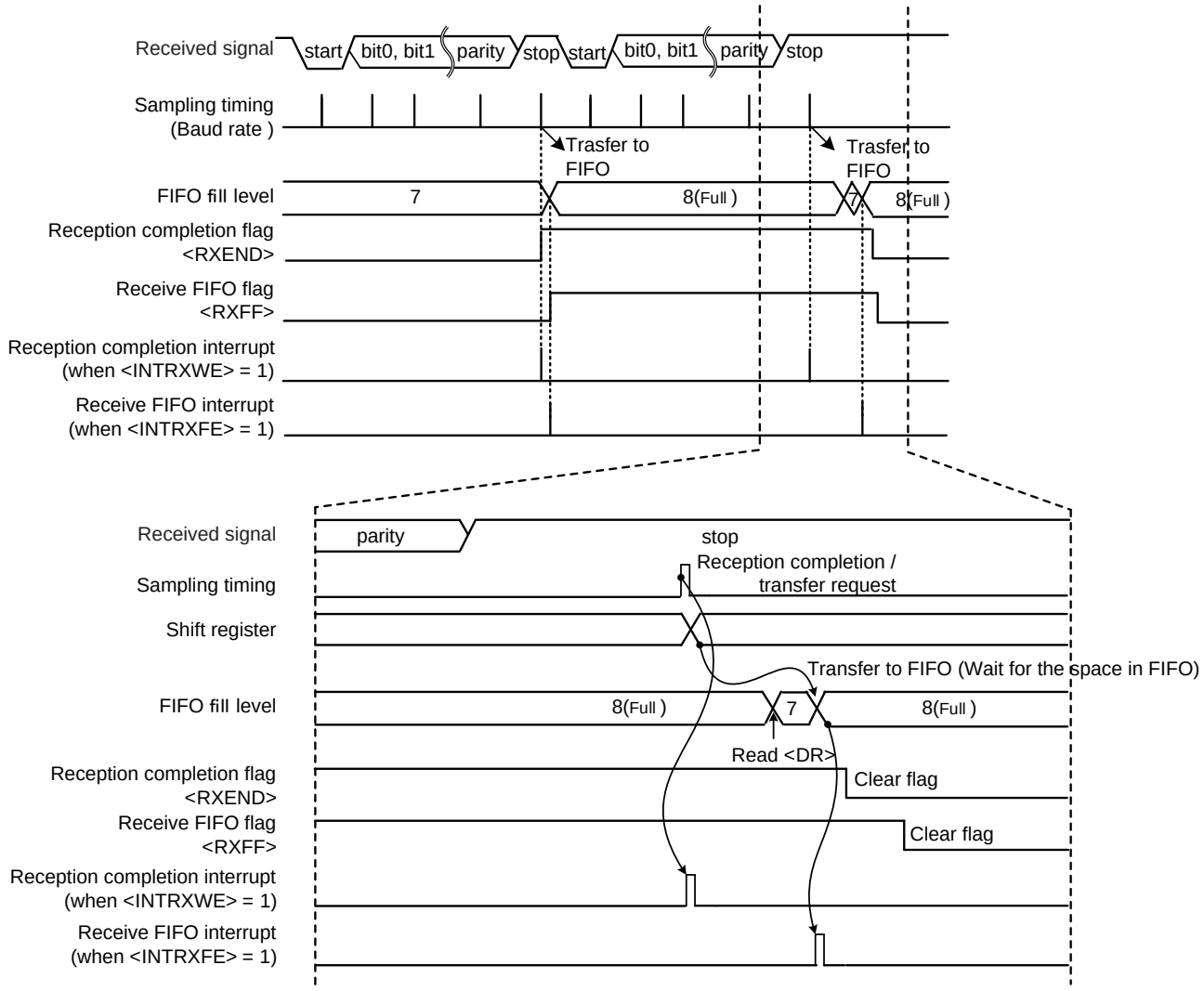

Figure 3.5 Reception Buffer Full Operation Timing

3.5.2. Reception Error Handling

If an error is detected, "1" is set to the corresponding error flag bit in ***[UARTxERR]*** (Error register) and ***[UARTxDR]*** (Data register). When the error occurs, please process appropriately. Also, if error interrupt control is enabled (***[UARTxCR1]***<INTERR> =1), an error interrupt occurs.

Note: If at least one error flag is set, the error interrupt is output. To cancel the error interrupt, clear all error flags with ***[UARTxERR]***

The following error detections are done during the data reception.

- Parity error
  When the parity addition function is enabled (***[UARTxCR0]***<PE>=1), after all bits of the data are received, the parity data generated from the reception data is compared with the received parity bit. If they are not identical, the parity error occurs. This error is masked when a break error occurs.

- Framing error
  If the received STOP bit is "0", the framing error occurs. This error is masked when a break error occurs.

- Break error
  When all data are "0" between the START bit and the STOP bit, the break error occurs.

- Overrun error
  All stages in the receive FIFO store data and the receive shift register has data. Then, if the START bit of the next frame is detected, the overrun error occurs.
  Even when the overrun error occurs, the data reception continues. But the received data is discarded. The data in the receive shift register remains. When ***[UARTxDR]*** (the receive data) is read and some space is generated in the receive FIFO, the data in the receive shift register is transferred to the receive FIFO. While the overrun flag is set, the reception completion interrupt is not generated.

  When the overrun error occurs, take the following actions.
  (1) Disable reception control (***[UARTxTRANS]***<RXE> =0)
  (2) Read received all data ***[UARTxDR]***
  (3) Check completion of data reception stop (***[UARTxSR]***<RXRUN> =0)
  (4) ***[UARTxERR]***<OVRERR> should be cleared.
  (5) Re-enable reception control (***[UARTxTRANS]***<RXE> =1)

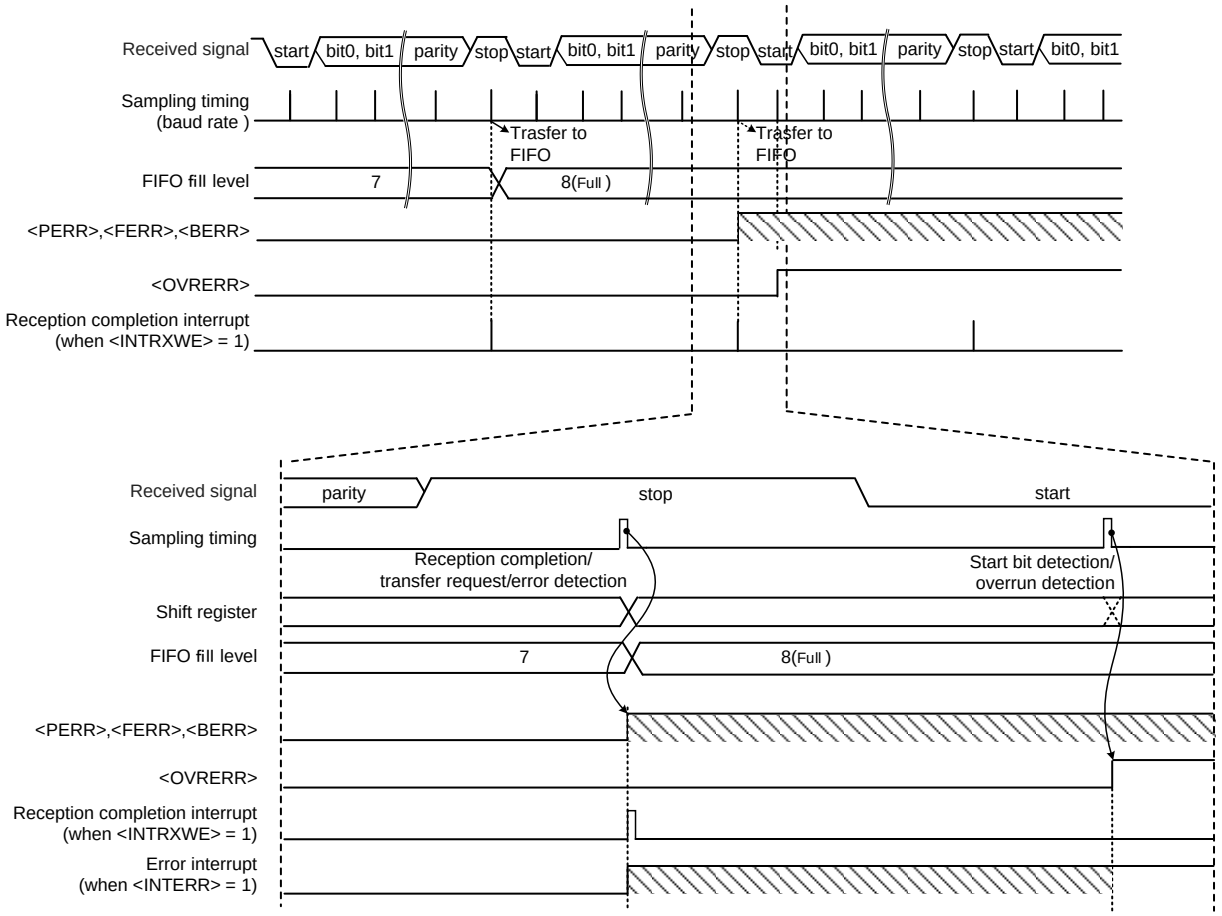

Figure 3.6 Error Flag Update Timing

If the overrun flag is cleared with reception enabled when an overrun error occurs, the latest value of the shift register is stored in the FIFO upon reception of the first STOP bit after clearing the flag, and the receiving operation is continued thereafter. At this time, data stored just before overrun error occurrence and by the first STOP bit reception after the flag clearing is not guaranteed.

3.5.3. Noise Removal of RXD Input

UTxRXD input has a noise filter function that operates with ΦT0 clock or transfer clock. The noise removal time should be set with ***[UARTxCR0]***<NF> (UTxRXD noise removal time).

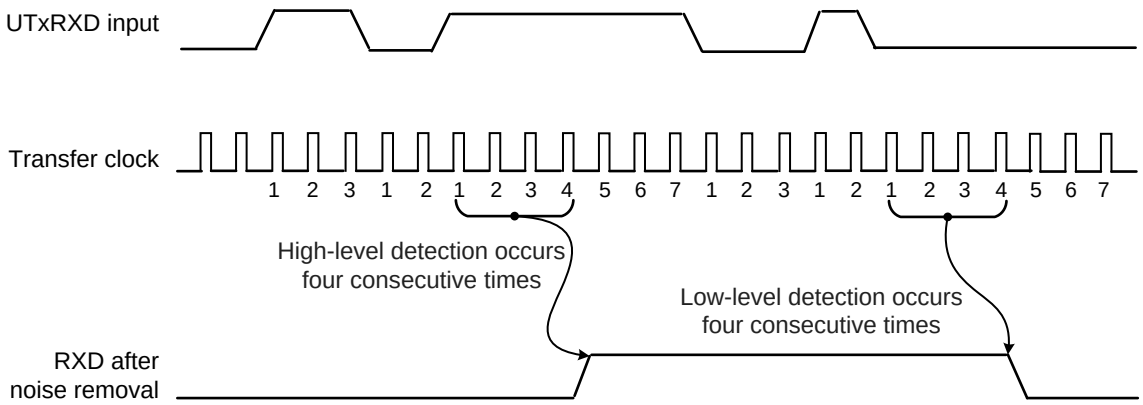

Figure 3.7 Noise Removal Operation (When <NF>=101)

3.6. Data Transmission

3.6.1. Basic Operation

Transmission operation has normal data transmission and data transmission using the trigger function.

- Normal data transmission

  [UARTxTRANS]<TXE> should be set to "1" to enable the data transmission. If data exists in the transmit FIFO, the transmission starts. Or, if data is written to the transmit FIFO, the transmission starts.
  For normal transmission without the trigger function, ***[UARTxTRANS]***<TXTRG> should be set to "0".

  At the start of the transmission, data is transferred from the transmit FIFO to the transmission shift register. The START bit, the data, the parity (when the parity is enabled), and the STOP bit are transmitted in this order. When one frame is transmitted completely, the transmission completion flag is set. The transmission interrupt is generated if the interrupt is enabled by ***[UARTxCR1]***<INTTXWE> =1.

  The data transmission continues until all data in the transmit FIFO are transmitted.

  If the transmission interrupt is enabled by ***[UARTxCR1]***<INTTXFE> =1, the transmit interrupt is generated when the amount of the data in the transmit FIFO reaches the Fill level which is set in ***[UARTxCR1]***<TIL> (Transmission Fill level setting).

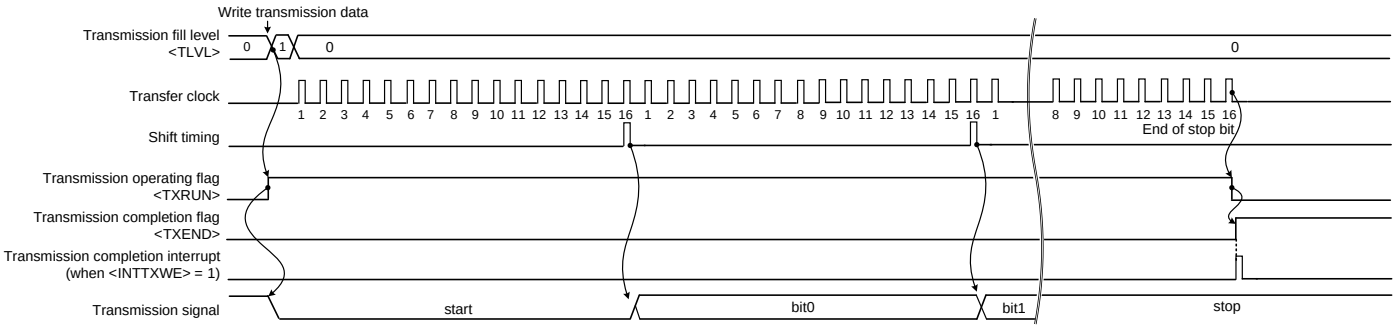

Figure 3.8 Transmission Timing

- Data transmission using the trigger function

  When ***[UARTxTRANS]***<TXTRG> is "1", ***[UARTxTRANS]***<TXE> should be "0".
  When data exists in the transmit FIFO and a trigger is input, ***[UARTxTRANS]***<TXE> becomes "1" automatically and the transmission starts. After the necessary data is transmitted, ***[UARTxTRANS]***<TXE> should be set to "0" to wait for a trigger again. Transmission operation is the same as normal data transmission.
  A new trigger is ignored during the data transmission

  When no data exists in the transmit FIFO and a trigger is input, the trigger is ignored. Then, the error interrupt is generated and ***[UARTxERR]***<TRGERR> (Trigger transmission error flag) is set. When the error occurs, please process appropriately.

  Note: If at least one error flag is set, the error interrupt is output. To cancel the error interrupt, clear all error flags with ***[UARTxERR]***

  At the start of the transmission, data is transferred from the transmit FIFO to the transmission shift register. The START bit, the data, the parity (when the parity is enabled), and the STOP bit are transmitted in this

order. When one frame is transmitted completely, the transmission completion flag is set. The transmission interrupt is generated if the interrupt is enabled by ***[UARTxCR1]***<INTTXWE> =1.

The data transmission continues until all data in the transmit FIFO are transmitted. When ***[UARTxTRANS]*** <TXTRG> is "1", the transmitter waits for a trigger after all data are transmitted.

If the transmission interrupt is enabled by ***[UARTxCR1]***<INTTXFE> =1, the transmit interrupt is generated when the amount of the data in the transmit FIFO reaches the Fill level which is set in ***[UARTxCR1]***<TIL> (Transmission Fill level setting).

- The followings are examples to generate the transmission interrupt.

  - When the Fill level is "0" (***[UARTxCR1]***<TIL> =000):
    Only one stage data is stored in the transmit FIFO. And the data is transferred from the transmit FIFO to the transmit shift register to transmit the data. The storage stage count in the transmit FIFO becomes "0".

  - When the Fill level is "7" (***[UARTxCR1]***<TIL> =111):
    8 stage data is stored in the transmit FIFO. One stage data is transferred from the transmit FIFO to the transmit shift register to transmit the data. The storage stage count becomes "7".

- Disable of transmission control

  When ***[UARTxTRANS]***<TXE> is set to "0" during the data transmission, the transmitter stops after the current frame data transmission completes. The data in the transmit FIFO is maintained. Also, when re-enabling transmission control, set ***[UARTxTRANS]***<TXE> to "1" after confirming transmission completion with ***[UARTxSR]***<TXRUN>=0.

3.6.2. Transmission of Break Error

When ***[UARTxTRANS]***<BK> (Break transmission) is set to "1", UTxTXDA/B output the Low level regardless of the value in ***[UARTxTRANS]***<TXE> (Transmission control) and the enable/disable of the half clock mode. If ***[UARTxTRANS]***<BK> is set to "1" during the data transmission, the Low level is output after the current frame is completely transmitted. Also, when the CTS handshake is enabled (***[UARTxCR0]***<CTSE> =1) and the UTxCTS_N pin is "High", output of "Low" level is started.

[UARTxTRANS]<BK> should be set to "0" to stop the output of the Low level.

3.7. Handshake Function

The CTS/RTS handshake function controls the communication using the UTxCTS_N pin for the data transmission and the UTxRTS_N pin for the data reception. The CTS handshake function is enabled by ***[UARTxCR0]***<CTSE> (CTS handshake function), and the RTS function is enabled by ***[UARTxCR0]***<RTSE> (RTS handshake function).

When the CTS is enabled, the following operation is done. If the UTxCTS_N pin becomes "High" during the data transmission, the current data transmission completes and then the transmission stops until the UTxCTS_N pin becomes "Low". The transmission interrupt is generated as a normal operation. So, owing to this function, the next transmission data can be written to the transmission buffer and the transmitter can stay in the transmission wait state.

When the RTS is enabled, the UTxRTS_N pin outputs the Low level if the data reception is available, that is, the following conditions are valid:

- ***[UARTxTRANS]***<RXE> (Reception control) is "1", which shows the data reception availability.
- The data reception is not operating.
- Receive FIFO has enough space or the receive shift register is empty.

3.8. Wakeup Function

In the 9-bit mode, the wakeup operation of the slave controller is enabled when the wakeup function control bit ***[UARTxCR0]***<WU> (Wake-up function) is set to "1".

A reception interrupt is generated only when the MSB bit of the reception data (***[UARTxDR]***<DR[8]> (Reception data)) is "1".

Note: The UTxTXDA pins in the slave controllers should be in the open drain output mode.

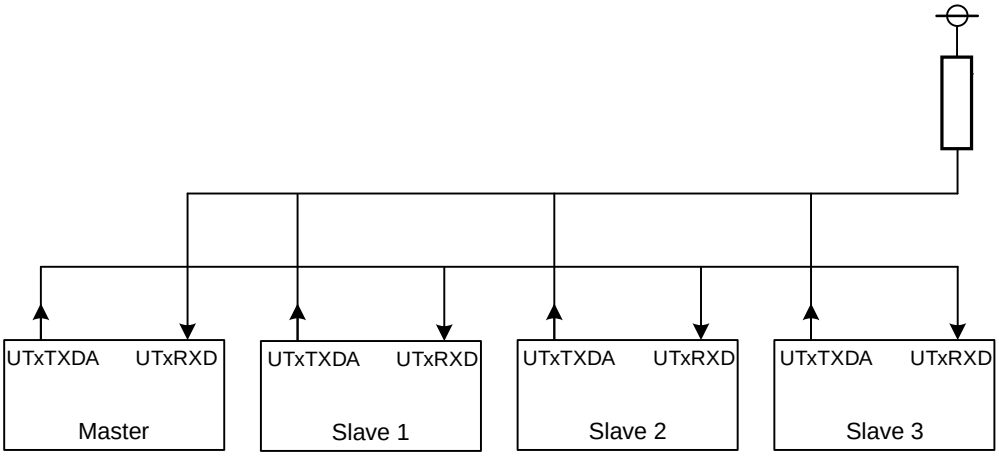

Figure 3.9 Serial Link of Wakeup Function

The execution procedure of the wakeup function is as follows:

The master and slave controllers should be set to the 9-bit mode. Each slave controller should set ***[UARTxCR0]***<WU> to "1" to enable the data reception. Prepare the Select code (8 bits) for each slave controller beforehand.

The master controller transmits one frame data which includes the Select code (8 bits) of the slave controller. The MSB bit ***[UARTxDR]***<DR[8]> (Transmission data) should be set to "1".

Each slave controller receives the frame. If a select code of each slave controller is identical with the received one, it clears its own ***[UARTxCR0]***<WU> to "0". Comparison of select code is executed by software.

The master controller transmits data to the specified slave controller (the controller with ***[UARTxCR0]***<WU> =0). At this time, the MSB bit ***[UARTxDR]***<DR[8]> should be set to "0".

The slave controller whose <WU> is "1" ignores the reception data. The reception interrupt is not generated because the MSB bit ***[UARTxDR]***<DR[8]> (Reception data) is "0". The slave controller with ***[UARTxCR0]***<WU> =0 can transmit data to the master controller. So, the slave controller can notify the master controller of the completion of reception.

3.9. Half Clock Mode

[UARTxCR0]<HBSEN> should be set to "1" to enable the half clock mode. In the half clock mode, the width of the data "0" becomes half of the Low width of the normal UART waveform.

3.9.1. Data Reception in Half Clock Mode

The Low level of the input data (UTxRXD) is detected and an appropriated width of "0" is generated to use an UART reception data in the half clock mode.

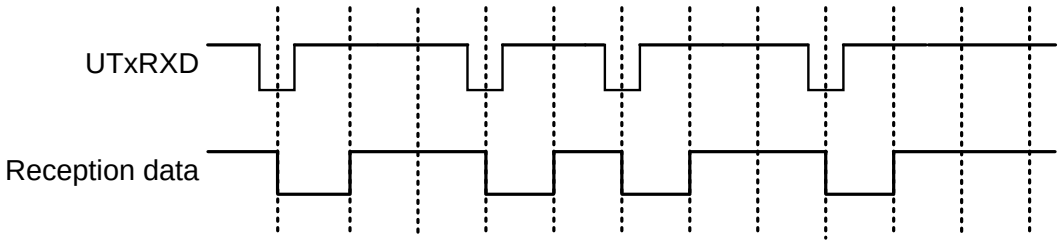

Figure 3.10 Reception Data in Half Clock Mode

3.9.2. Data Transmission in Half Clock Mode

The data "0" width in the half clock mode is half of the width of the normal UART communication as shown in Figure 3.11.

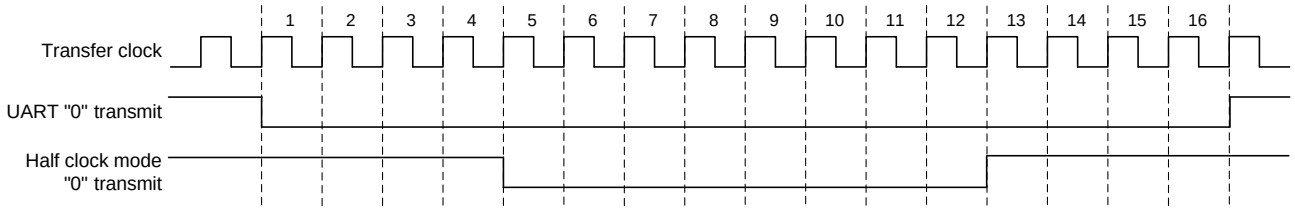

Figure 3.11 Data 0 Transmission in Half Clock Mode

There are two transmission signal pins in the half clock mode. When ***[UARTxCR0]***<HBSMD> is set to "0" (1-pin mode), these two pins output the same signal. When it is set to "1" (2-pin mode), these pins output the data "0" alternately. ***[UARTxCR0]***<HBSST> sets which pin should output the data "0" first.

(1) 1-pin mode

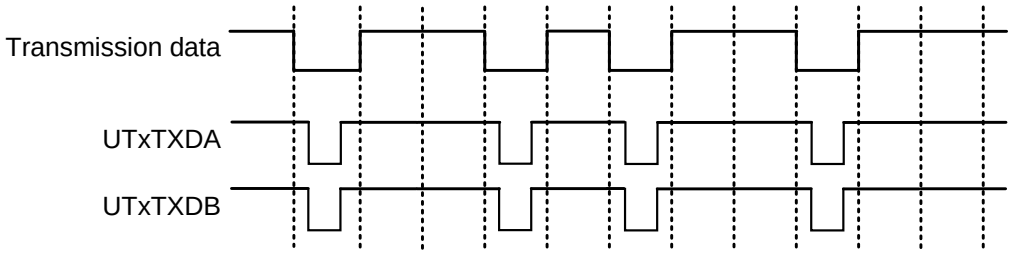

Figure 3.12 Transmission Waveform in 1-pin Mode

(2) 2-pin mode (***[UARTxCR0]***<HBSST> =0: UTxTXDA outputs "0" first.)

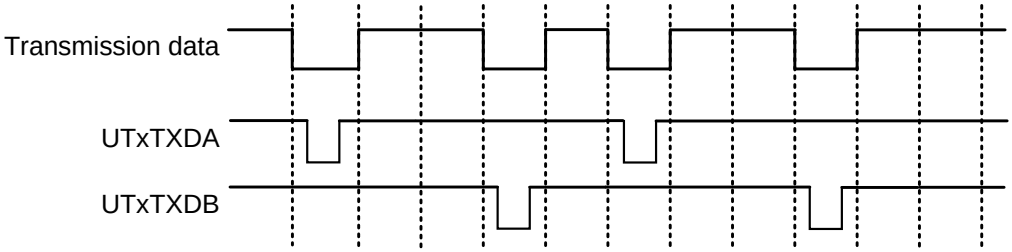

Figure 3.13 Transmission Waveform in 2-pin Mode

3.10. DMA Request

There are a single request and a burst request in the transmission.

- Reception DMA request

  [UARTxCR1]<DMARE> should be set to "1" to enable them.

  When one data or more exist in the receive FIFO, the single request is generated.

  The burst request is generated when the value of ***[UARTxSR]***<RLVL> which shows the stage count of the currently stored data becomes equal to or more than the reception interrupt generation level (Fill level) set in ***[UARTxCR1]***<RIL>. When the DMA transfer completes, the burst request is generated if the stored data level is equal to or more than the Fill level.

- Transmission DMA request

  [UARTxCR1]<DMATE> should be set to "1" to enable them.

  When one data stage space or more exist in the transmit FIFO, the single request is generated.

  The burst request is generated when the value of ***[UARTxSR]***<TLVL> which shows the stage count of the currently stored data becomes equal to or less than the transmission interrupt generation level (Fill level) set in ***[UARTxCR1]***<TIL>. When the DMA transfer completes, a burst request is generated if the stored data level is equal to or less than the Fill level.

3.11. Loopback Function (Test Function)

[UARTxCR0]<LPB> (Loopback function) should be set to "1" to enable the loopback function. When the loopback function is enabled, the transmission data is connected to the reception data and the loopback test is possible.

The connection destination changes depending on the half clock mode control setting (***[UARTxCR0]***<HBSEN>).

When the half clock communication is disabled (<HBSEN> =0), UTxTXDA is connected to the reception data.

When the half clock communication is enabled (<HBSEN> =1), the signal of the logical AND of UTxTXDA and UTxTXDB is connected to the reception data.

3.12. Software Reset

The sequence of the write of "10" to ***[UARTxSWRST]***<SWRST> (Software reset) and the next write of "01" generates the software reset.

The software reset stops the data transfer and initializes the read/write pointers of the receive/transmit FIFO and the error flags. The registers ***[UARTxTRANS]*** (Transfer Enable Register), ***[UARTxDR]*** (Data Register), ***[UARTxSR]*** (Status Register), and ***[UARTxERR]*** (Error Register) are initialized.

The data in the registers ***[UARTxCR0]*** (Control Register 0), ***[UARTxCR1]*** (Control Register 1), ***[UARTxCLK]*** (Clock Control Register), and ***[UARTxBRD]*** (Baud Rate Register) are maintained.

The status of the software reset operation is shown in ***[UARTxSWRST]***<SWRSTF> (Software reset flag). If the software reset is asserted, the next operation should be done after <SWRSTF> is checked to be "0".

4. Registers

4.1. List of Registers

The control registers and their addresses are shown as follows:

Function	Function name	Channel / unit	Base address		
			TYPE1	TYPE2	TYPE3
Asynchronous Serial Communication Circuit	UART	ch0	0x400BB000	0x400CE000	0x4006E000
		ch1	0x400BB100	0x400CE400	0x4006E400
		ch2	0x400BB200	0x400CE800	0x4006E800
		ch3	0x400BB300	0x400CEC00	0x4006EC00
		ch4	0x400BBD00	0x400CF000	0x4006F000
		ch5	0x400BBE00	0x400CF400	0x4006F400
		ch6	0x400BC400	0x400CF800	0x4006F800
		ch7	0x400BC500	0x400CFC00	0x4006FC00

Note: The channel/unit and base address type are different by products. Please refer to "Product Information" of the reference manual for the details.

Register name		Address (Base+)
Software Reset Register	***[UARTxSWRST]***	0x0000
Control Register0	***[UARTxCR0]***	0x0004
Control Register1	***[UARTxCR1]***	0x0008
Clock Control Register	***[UARTxCLK]***	0x000C
Baud Rate Register	***[UARTxBRD]***	0x0010
Transfer Enable Register	***[UARTxTRANS]***	0x0014
Data Register	***[UARTxDR]***	0x0018
Status Register	***[UARTxSR]***	0x001C
FIFO Clear Register	***[UARTxFIFOCLR]***	0x0020
Error Register	***[UARTxERR]***	0x0024

4.2. Details of Registers

4.2.1. *[UARTxSWRST]* (Software Reset Register)

Bit	Bit symbol	After reset	Type	Function
31:8	-	0	R	Reads as "0".
7	SWRSTF	0	R	Software reset flag 0: Software reset is not asserted. 1: Software reset is asserted.
6:2	-	0	R	Reads as "0".
1:0	SWRST[1:0]	00	W	Software reset The sequence of the write of "10" and the next write of "01" generates the software reset. The software reset initializes the registers ***[UARTxTRANS]***, ***[UARTxDR]***, ***[UARTxSR]***, and ***[UARTxERR]***. And, the transmission and reception circuit is also initialized. The read/write pointers of the receive/transmit FIFO are initialized, too. When this field is read, "00" is returned.

4.2.2. *[UARTxCR0]* (Control Register0)

Bit	Bit symbol	After reset	Type	Function
31:19	-	0	R	Reads as "0".
18	HBSST	0	R/W	Half clock mode communication start control 0: Output starts at UTxTXDA pin. 1: Output starts at UTxTXDB pin.
17	HBSMD	0	R/W	Half clock mode communication output control 0: 1-pin mode 1: 2-pin mode
16	HBSEN	0	R/W	Half clock mode control 0: Disabled. 1: Enabled.
15	LPB	0	R/W	Loopback function 0: Disabled. 1: Enabled.
14:12	NF[2:0]	000	R/W	UTxRXD noise removal time 000: None. 001: A signal with 2 cycles or less with ΦT0 clock is removed as noise, and a signal with 3 cycles or more is valid. 010: A signal with 4 cycles or less with ΦT0 clock is removed as noise, and a signal with 5 cycles or more is valid. 011: A signal with 8 cycles or less with ΦT0 clock is removed as noise, and a signal with 9 cycles or more is valid. 100: A signal with 2 cycles or less with transfer clock is removed as noise, and a signal with 3 cycles or more is valid. 101: A signal with 3 cycles or less with transfer clock is removed as noise, and a signal with 4 cycles or more is valid. 110: A signal with 4 cycles or less with transfer clock is removed as noise, and a signal with 5 cycles or more is valid. 111: A signal with 5 cycles or less with transfer clock is removed as noise, and a signal with 6 cycles or more is valid. For the details of the Noise removal, refer to "3.5.3 Noise Removal of RXD Input".
11	-	0	R	Reads as "0".
10	CTSE	0	R/W	CTS handshake function 0: Disabled. 1: Enabled.
9	RTSE	0	R/W	RTS handshake function 0: Disabled. 1: Enabled.
8	WU	0	R/W	Wake-up function 0: Disabled. 1: Enabled. This setting is available only for the 9-bit mode. It is ignored in the other modes. If it is set to "1" (Enabled) and the 9th bit of the reception data is "1", the corresponding reception interrupt is generated.
7	-	0	R	Reads as "0".
6	IV	0	R/W	Data signal inversion 0: Disabled. 1: Enabled.
5	DIR	0	R/W	Data transfer order 0: LSB first 1: MSB first

Bit	Bit symbol	After reset	Type	Function
4	SBLEN	0	R/W	STOP bit length 0: 1-bit 1: 2-bit
3	EVEN	0	R/W	Even parity selection 0: Odd parity 1: Even parity
2	PE	0	R/W	Parity addition 0: Disabled. 1: Enabled.
1:0	SM[1:0]	00	R/W	Data length 00: 7-bit 01: 8-bit 10: 9-bit 11: Reserved.

Note: This register cannot be rewritten during the data transmission and the data reception. This register is rewritable if ***[UARTxSR]*** <SUE> =0 (Setting is enabled).

4.2.3. *[UARTxCR1]* (Control Register1)

Bit	Bit symbol	After reset	Type	Function
31:15	-	0	R	Reads as "0".
14:12	TIL[2:0]	000	R/W	Transmission Fill level setting 000: 0 stages 001: 1 stage : 111: 7 stages This sets the Fill level where the transmission interrupt is generated.
11	-	0	R	Reads as "0".
10:8	RIL[2:0]	001	R/W	Reception Fill level setting 000: 8 stages 001: 1 stage : 111: 7 stages This sets the Fill level where the reception interrupt is generated.
7	INTTXFE	0	R/W	Transmit FIFO interrupt control 0: Disabled. 1: Enabled.
6	INTTXWE	0	R/W	Transmission completion interrupt control 0: Disabled. 1: Enabled.
5	INTRXFE	0	R/W	Receive FIFO interrupt control (Note 1) 0: Disabled. 1: Enabled.
4	INTRXWE	0	R/W	Reception completion interrupt control (Note 1) 0: Disabled. 1: Enabled.
3	-	0	R	Reads as "0".
2	INTERR	0	R/W	Error interrupt control 0: Disabled. 1: Enabled.
1	DMATE	0	R/W	Transmission DMA control 0: Disabled. 1: Enabled.
0	DMARE	0	R/W	Reception DMA control 0: Disabled. 1: Enabled.

Note 1: Please do not enable <INTRXWE> and <INTRXFE> at the same time.

Note 2: This register cannot be rewritten during the data transmission and the data reception. This register is rewritable if ***[UARTxSR]*** <SUE> =0 (Setting is enabled).

4.2.4. *[UARTxCLK]* (Clock Control Register)

Bit	Bit symbol	After reset	Type	Function
31:8	-	0	R	Reads as "0".
7:4	PRSEL[3:0]	0000	R/W	Prescaler dividing ratio selection 0000: 1/1 0110: 1/64 0001: 1/2 0111: 1/128 0010: 1/4 1000: 1/256 0011: 1/8 1001: 1/512 0100: 1/16 1010 to 1111: Inhibited setting. 0101: 1/32
3:2	-	0	R	Reads as "0".
1:0	-	00	R/W	Always write "00".

Note: This register cannot be rewritten during the data transmission and the data reception. This register is rewritable if ***[UARTxSR]*** <SUE> =0 (Setting is enabled).

4.2.5. *[UARTxBRD]* (Baud Rate Register)

Bit	Bit symbol	After reset	Type	Function
31:24	-	0	R	Reads as "0".
23	KEN	0	R/W	N + (64 - K) /64 dividing control 0: Disabled. 1: Enabled.
22	-	0	R	Reads as "0".
21:16	BRK[5:0]	000000	R/W	K value setting of the N + (64 - K) /64 dividing 000000: K =0 000001: K =1 000010: K =2 : 111111: K =63
15:0	BRN[15:0]	0x0000	R/W	N value setting of the N + (64 - K) /64 dividing or N dividing. 0x0000: Inhibited setting. 0x0001: N =1 0x0002: N =2 : 0xFFFF: N =65535

Note: This register cannot be rewritten during the data transmission and the data reception. This register is rewritable if ***[UARTxSR]*** <SUE> =0 (Setting is enabled).

4.2.6. *[UARTxTRANS]* (Transfer Enable Register)

Bit	Bit symbol	After reset	Type	Function
31:4	-	0	R	Reads as "0".
3	BK	0	R/W	Break transmission 0: No transmission is done. 1: Transmission is done. When this bit is set to "1", the Low level is output. When this bit is set to "0", the transmission stops. If ***[UARTxCR1]***<IV> is "1" to invert the data, the High level is output.
2	TXTRG	0	R/W	Trigger transmission control 0: Disabled. 1: Enabled. Do not change <TXTRG> during transmission. Set <TXE> to "0" and check ***[UARTxSR]*** <TXRUN> =0 (operation stop) and then change. For the selection of the trigger input, refer to "Product Information" of the reference manual.
1	TXE	0	R/W	Transmission control 0: Disabled. 1: Enabled.
0	RXE	0	R/W	Reception control 0: Disabled. 1: Enabled.

4.2.7. *[UARTxDR]* (Data Register)

Bit	Bit symbol	After reset	Type	Function
31:19	-	0	R	Reads as "0".
18	PERR	0	R	Parity error (Note) 0: No errors. 1: Error occurs. The write to this bit is ignored.
17	FERR	0	R	Framing error (Note) 0: No errors. 1: Error occurs. The write to this bit is ignored.
16	BERR	0	R	Break error flag 0: No errors. 1: Error occurs. The write of this bit is ignored.
15:9	-	0	R	Reads as "0".
8:0	DR[8:0]	Undefined.	R	Reception data read. This field should not read when no reception data is present.
			W	Transmission data write.

Note: <PERR>,<FERR> are masked when a break error occurs.

4.2.8. *[UARTxSR]* (Status Register)

<table>
<tr><th>Bit</th><th>Bit symbol</th><th>After reset</th><th>Type</th><th>Function</th></tr>
<tr><td>31</td><td>SUE</td><td>0</td><td>R</td><td>Setting enable status flag
0: Setting is enabled.
1: Setting is disabled.
When <SUE> is "0", the UART does neither data transmission nor data reception. The registers can be updated.
Note: Target registers are following.
[UARTxCR0], [UARTxCR1], [UARTxCLK], [UARTxBRD], and [UARTxFIFOCLR].
<SUE> becomes "0" when the followings occur.
1. Reset is input.
2. Software reset is asserted.
3. The data transmission and the data reception complete after [UARTxTRANS]<TXE> and <RXE> are set to "0", respectively.</td></tr>
<tr><td>30:16</td><td>-</td><td>0</td><td>R</td><td>Reads as "0".</td></tr>
<tr><td>15</td><td>TXRUN</td><td>0</td><td>R</td><td>Transmission operating flag
0: Stop
1: Operating
This bit is the status flag which shows the transmission is operating. The following status is set by the combination of <TXRUN> and <TLVL> bits.
<table>
<tr><th><TXRUN></th><th><TLVL></th><th>Status</th></tr>
<tr><td rowspan="2">0</td><td>Other than 0000</td><td>Stop or wait for the next transmission</td></tr>
<tr><td>0000</td><td>Transmission completes and the transmit FIFO is empty.</td></tr>
<tr><td>1</td><td>-</td><td>Transmission is operating.</td></tr>
</table>
<TXRUN> is set when data is present in the transmission shift register even though the transmit FIFO is empty.</td></tr>
<tr><td rowspan="2">14</td><td rowspan="2">TXEND</td><td rowspan="2">0</td><td>R</td><td>Transmission completion flag
0: -
1: Transmission completion
This flag is set when one frame transmission completes.</td></tr>
<tr><td>W</td><td>Flag clear
0: -
1: Flag clear.
Write of "1" clears this bit.</td></tr>
<tr><td rowspan="2">13</td><td rowspan="2">TXFF</td><td rowspan="2">0</td><td>R</td><td>Transmit FIFO flag
0: -
1: Data count reaches the set transmission Fill level.
This bit is set when the stage count of the stored data becomes the set value of Fill level (the [UARTxCR1]<TIL> value) from <TIL>+1.</td></tr>
<tr><td>W</td><td>Flag clear
0: -
1: Flag clear.
Write of "1" clears this bit.</td></tr>
<tr><td>12</td><td>-</td><td>0</td><td>R</td><td>Reads as "0".</td></tr>
<tr><td>11:8</td><td>TLVL[3:0]</td><td>0000</td><td>R</td><td>Transmit FIFO data storage level
This field shows the current stage count of the data stored in the transmit FIFO.</td></tr>
</table>

<table>
<tr><th>Bit</th><th>Bit symbol</th><th>After reset</th><th>Type</th><th>Function</th></tr>
<tr><td>7</td><td>RXRUN</td><td>0</td><td>R</td><td>Reception operating flag
0: Stop
1: Operating
Status flag which shows the reception is operating.
The following status is set by the combination of <RXRUN> and <RLVL> bits.
<table>
<tr><th><RXRUN></th><th><RLVL></th><th>Status</th></tr>
<tr><td rowspan="2">0</td><td>Other than 1000</td><td>Stop or wait for the next reception</td></tr>
<tr><td>1000</td><td>Receive FIFO is full, and the reception completes.</td></tr>
<tr><td>1</td><td>-</td><td>Reception is operating.</td></tr>
</table></td></tr>
<tr><td rowspan="2">6</td><td rowspan="2">RXEND</td><td rowspan="2">0</td><td>R</td><td>Reception completion flag
0: -
1: Reception completion
This flag is set to "1" when one frame reception completes.</td></tr>
<tr><td>W</td><td>Flag clear
0: -
1: Flag clear.
Write of "1" clears this bit.</td></tr>
<tr><td rowspan="2">5</td><td rowspan="2">RXFF</td><td rowspan="2">0</td><td>R</td><td>Receive FIFO flag
0: -
1: Data count reaches the set reception Fill level.
This bit is set when the stage count of the stored data stage becomes the [UARTxCR1]<RIL> value (the set value of Fill level) from <RIL>-1.</td></tr>
<tr><td>W</td><td>Flag clear
0: -
1: Flag clear.
Write of "1" clears this bit.</td></tr>
<tr><td>4</td><td>-</td><td>0</td><td>R</td><td>Reads as "0".</td></tr>
<tr><td>3:0</td><td>RLVL[3:0]</td><td>0000</td><td>R</td><td>Receive FIFO data storage level
This field shows the current stage count of the data stored in the receive FIFO.</td></tr>
</table>

4.2.9. *[UARTxFIFOCLR]* (FIFO Clear Register)

Bit	Bit symbol	After reset	Type	Function
31:2	-	0	R	Reads as "0".
1	TFCLR	0	W	Transmission buffer clear 0: - 1: Clear When this bit is written to "1", the read/write pointer of the transmit FIFO are initialized. When it is read, "0" is returned.
0	RFCLR	0	W	Reception buffer clear 0: - 1: Clear When this bit is written to "1", the read/write pointer of the receive FIFO are initialized. When it is read, "0" is returned.

Note: This register cannot be rewritten during the data transmission and the data reception. This register is rewritable if ***[UARTxSR]*** <SUE> =0 (Setting is enabled).

4.2.10. *[UARTxERR]* (Error Register)

Bit	Bit symbol	After reset	Type	Function
31:5	-	0	R	Reads as "0".
4	TRGERR	0	R	Trigger transmission error flag 0: No errors. 1: Error occurs. This is set to "1" when the data transmission cannot be started by the trigger because of no data in the transmit FIFO.
			W	Flag clear 0: - 1: Flag clear. Write of "1" clears this bit.
3	OVRERR	0	R	Overrun error flag 0: No errors. 1: Error occurs. This is set to "1" when an overrun error occurs.
			W	Flag clear 0: - 1: Flag clear. Write of "1" clears this bit. (Note3)
2	PERR	0	R	Parity error flag (Note 1) 0: No errors. 1: Error occurs. This is set to "1" when a parity error occurs.
			W	Flag clear 0: - 1: Flag clear. Write of "1" clears this bit.
1	FERR	0	R	Framing error flag (Note 1) 0: No errors. 1: Error occurs. This is set to "1" when a framing error occurs.
			W	Flag clear 0: - 1: Flag clear. Write of "1" clears this bit.
0	BERR	0	R	Break error flag 0: No errors. 1: Error occurs. This is set to "1" when a break error occurs.
			W	Flag clear 0: - 1: Flag clear. Write of "1" clears this bit.

Note 1: <PERR>,<FERR> are masked when a break error occurs.

Note 2: If error occurrence and flag clearing are simultaneous, clearing takes precedence.

Note 3: For the procedure for clearing the overrun flag, refer to "3.5.2 Reception Error Handling".

5. Usage Example

5.1. Baud Rate Setting Value

The following shows samples of the baud rate setting values using the clock frequency ΦTx. The deviation of ΦTx is not included.

Table 5.1 Setting Example at ΦTx =40MHz, <PRSEL> =0000, and <KEN> =1

Baud rate (bps)	<BRK>	<BRN>	Calculated value (bps)
9600	0x25	0x104	9600
	0x26		
19200	0x32	0x082	19198
	0x33		19201
38400	0x39	0x041	38397
	0x3A		38406
57600	0x26	0x02B	57595
	0x27		57616
62500	0x00	0x027	62500
76800	0x1C	0x020	76775
	0x1D		76812
115200	0x13	0x015	115191
	0x14		115274
128000	0x1E	0x013	128000

Table 5.2 Setting Example at ΦTx =80MHz, <PRSEL> =0000, and <KEN> =1

Baud rate (bps)	<BRK>	<BRN>	Calculated value (bps)
9600	0x0A	0x208	9600
	0x0B		
19200	0x25	0x104	19200
38400	0x32	0x082	38397
	0x33		38402
57600	0x0C	0x056	57595
	0x0D		57606
62500	0x00	0x04F	62500
76800	0x39	0x041	76794
	0x3A		76812
115200	0x26	0x02B	115191
	0x27		115232
128000	0x3C	0x027	128000

6. Precautions

- In some products, the UTxRTS_N pin or the UTxCTS_N pin may not be assigned. The corresponding functions should not be used in those products.
- The registers which are not assigned should not be accessed.
- The trigger input depends on the product when the trigger transmission control is used. Refer to "Product Information" of the reference manual.

7. Revision History

Table 7.1 Revision History

Revision	Date	Description
1.0	2017-09-11	- First release
2.0	2018-06-05	- "Outlines" Error detection/Operation explanation cell Transmission term: Deleted "Break error," - "Figure 2.1", "3.4.", "Figure 3.5" receive buffer→reception buffer, transmit buffer →transmission buffer - "Table 2.1" Separate Signal name term into symbol term and Signal name term Related Reference manual: "Clock Control Circuit" → "Clock Control" - "3.1.Clock Supply" Modified register name - "3.2. Transfer Clock" Added Note - "3.4. Reception Buffer / Transmission Buffer" receive buffer / transmit buffer → reception buffer / transmission buffer - "3.5.2." Reception Error Handling Added "If the overrun flag is cleared with reception enabled when an overrun error ..." - "4.1.List of Registers" Base address table: Added "ch6" and "ch7" row. Added "TYPE3" column - "4.2.5." BRN/Function: N + (64 - K) /64 dividing → N + (64 - K) /64 dividing or N dividing - "4.2.8." SUE/Function: Deleted ***[UARTxERR]*** - "4.2.10" Deleted "Note2: This register cannot be rewritten during the ...." Added Note2,Note3
2.1	2019-07-26	- 1. modified the Operation explanation of Baud rate control. - 3.5.2 modified the contents of taking actions when the overrun error occurs. - 4.2.8 modified the "0" writing operation of bit 14/13/6/5 (Don't care → -) - 4.2.9 modified the "0" writing operation of bit 1/0 (Don't care → -) - 4.2.10 modified the "0" writing operation of bit 4/3/2/1/0 (Don't care → -) - revised the page of "RESTRICTIONS ON PRODUCT USE"
2.2	2020-12-14	- Modified top page and header and footer (added New Family) - Revised the page of "Conventions" - Modified description of trademark - modified 1. Outline - Modified 3.1. Clock Supply - 3.4. Reception Buffer / Transmission Buffer Modified description - 3.5.2. Reception Error Handling Modified description - 3.9.1. Data Reception in Half Clock Mode Modified description - "4.1. List of Registers" "ch6" and "ch7" of "TYPE1" column: Added base address
2.3	2024-05-10	- Data sheet is added in the related document. - The reference manuals for the UTxRXD, UTxTXDA, UTxTXDB, UTxRTS_N, and UTxCTS_N are changed in Table 2.1. - Appearance updated

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