For high-speed differential interface 32Gbps MUX/DEMUX bus switch TDS4A212MX, TDS4B212MX Application Notes

Overview

This document describes the guidelines and precautions for using MUX (multiplexer) /DEMUX (demultiplexer) bus switch TDS4A212MX, TDS4B212MX for high-speed differential interfaces. Recommended data rates can be used for interfaces such as 1 to 32Gbps, PCIe® 5.0, PCIe® 4.0, CXL.2.0, USB4® Version2, Thunderbolt™4 and DisplayPort™ 2.0.

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1. Introduction

In recent years, PCIe, USB, Thunderbolt and other high-speed communication interfaces have been widely adopted in PCs, servers, and other electronic devices, and these interfaces have been used to connect and expand CPU, peripheral chips, graphics boards, peripheral devices, and other devices.

However, if the frequency increases as the communication speed increases, the signal loss on the transmission path tends to occur. This loss occurs even when the signal passes through the board wiring, and it is necessary to design the circuit design to reduce the loss.

Therefore, MUX/DEMUX used when expanding the differential interface also requires high-frequency and low-loss products. We have recently developed a high-frequency, low-loss 2:1 MUX/1:2 DEMUX bus-switch TDS4A212MX, TDS4B212MX that can be used in PCIe5, USB4, Thunderbolt 4 and other applications.

This document explains applications using TDS4A212MX, TDS4B212MX and precautions for designing the circuit board.

2. About TDS4A212MX, TDS4B212MX

2.1. Overview

TDS4A212MX and TDS4B212MX are high-speed differential 2:1 MUX (multiplexer) /1:2 DEMUX (demultiplexer) bus switches. The differential signal operating range is 0 to 2.0 V for common mode voltage and a 0 to 1.8 Vpp for differential voltage swing, supporting a wide range of differential interfaces.

The recommended data rates are from 1 to 32Gbps. They can be used for high-speed differential interfaces such as PCIe 5.0, CXL 2.0, USB4 Version2, Thunderbolt 4, DisplayPort 2.0.

-3-dB bandwidth is 26.2 GHz for TDS4A212MX, 27.5 GHz for TDS4B212MX.

XQFN16(1.6 × 2.4 mm) is used for the packaging, contributing to the miniaturization of the mounting board.

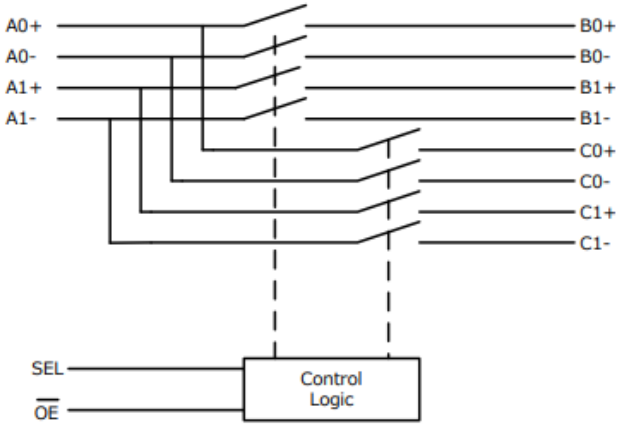

Fig. 1 Block Diagram1

(Common in TDS4A212MX, TDS4B212MX)

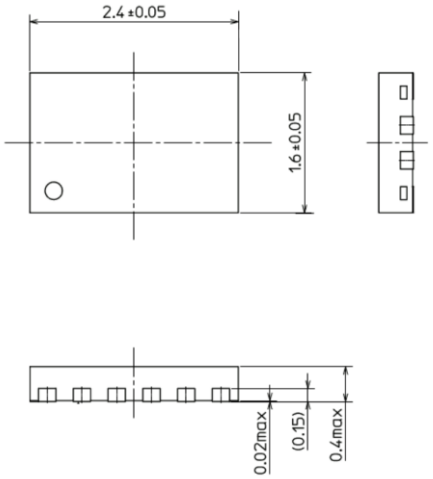

Fig. 2 Packaging Dimensions (unit:mm)2

(Common in TDS4A212MX, TDS4B212MX)

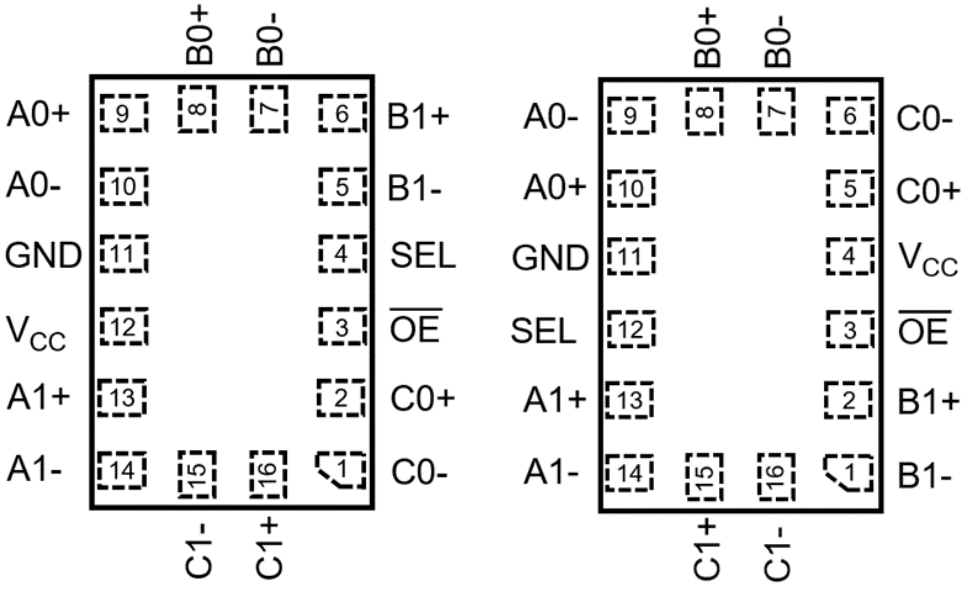

Fig. 3 Pinout Diagram (Top View) Left: TDS4A212MX Right: TDS4B212MX3

2.2. Pin Layout

TDS4A212MX and TDS4B212MX have the same function but different terminal arrangements. TDS4A212MX has a terminal layout that makes it easier to design boards, and TDS4B212MX has a terminal layout that emphasizes high-frequency properties.

Fig. 4 illustrates the use of TDS4A212MX and TDS4B212MX to exclusively connect System A with Systems B and C.

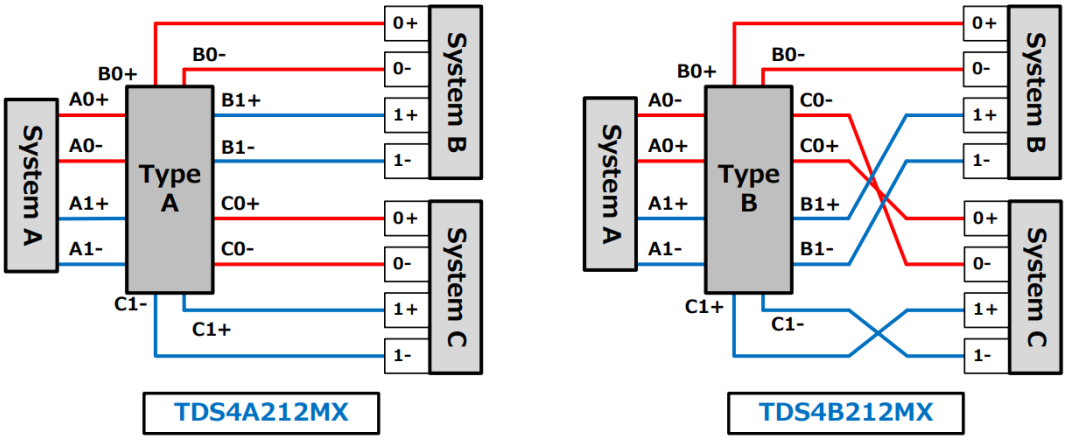

Fig. 4 Typical Wiring of TDS4A212MX, TDS4B212MX4

As shown in Fig. 4, TDS4A212MX does not have crossing of wires, but TDS4B212MX requires crossing of wires.

2.3. Function

TDS4A212MX and TDS4B212MX can be combined with a SEL to select either port B or port C as the A port connection destination, and to transmit differential signals bidirectionally between the connected ports.

Setting $\overline{OE}$ to the low level (L), the unit enters the active mode. By setting SEL to the low level (L), ports A and B are connected. By setting SEL to the high level (H), ports A and C are connected.

Setting $\overline{OE}$ to the high level (H), the unit enters the standby mode. The unit is unconnected irrespective of SEL.

The maximum current consumption in the active mode is 150 μA. However, in the standby mode, the current consumption can be reduced to a maximum of 10 μA.

Table. 1 Port Connections and Control Input Logic (n = 0, 1)1

Input$\overline{OE}$	Input SEL	Function (n = 0, 1)
L	L	An+ Port = Bn+ Port, An- Port = Bn- Port
L	H	An+ Port = Cn+ Port, An- Port = Cn- Port
H	Don't care	An, Bn and Cn Port Disconnect

3. Eye pattern

3.1. What is Eye Pattern?

An eye pattern is a method for visually assessing the transmission waveform of a differential signal. It is called an eye pattern because it is visualized by cutting and overlapping signal waveforms for each bit, resulting in an eye-like shape.
Eye patterns are a useful tool in the analysis of differential signals. They allow you to assess signal integrity during the design and testing of semiconductor devices, communication systems, and boards.

Non Return to Zero (NRZ) typically used in differential signaling has an ideally shaped eye pattern, as shown in Fig. 5, with constant oscillation and short rise and fall times.

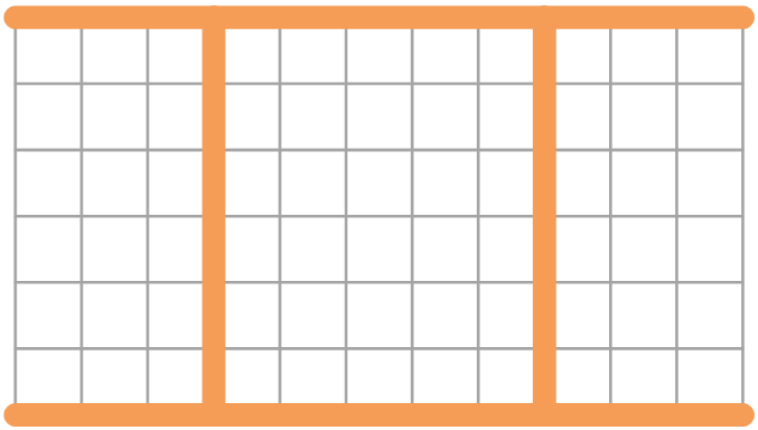

Fig. 5 Ideal eye pattern5

In reality, however, factors such as signal attenuation and noise affect this, resulting in deteriorations like a narrower eye opening and increased rise and fall times, as shown in Fig. 6.
This degradation becomes more pronounced with increased attenuation and noise, allowing for the evaluation of the differential signal's waveform quality from the eye pattern.

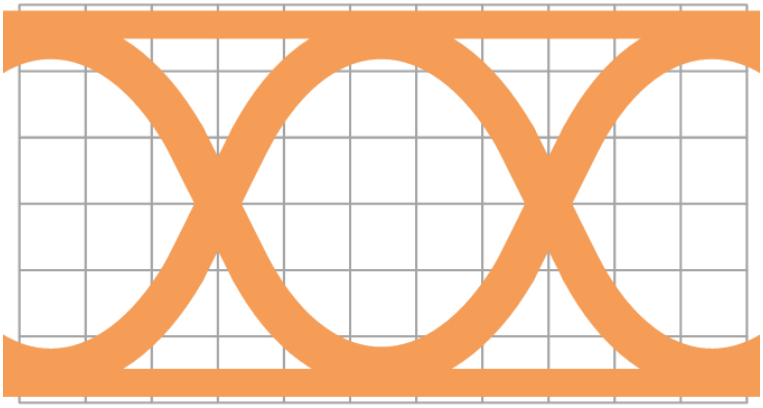

Fig. 6 Typical Differential Signal Eye Patterns6

One eye pattern is equivalent to one bit, and this is referred to as a Unit Interval (UI).
Below, we explain the evaluation items in the eye pattern.

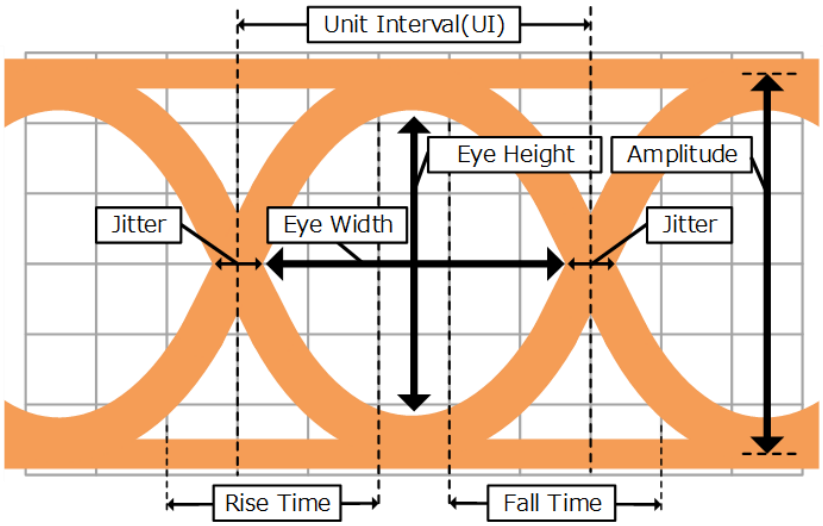

Fig. 7 Typical measured values on the eye pattern7

Eye Height: Eye Height refers to the vertical-eye opening. If Eye Height is equal to the amplitude of the eye, the eye can be considered ideal. However, in actual measuring, Eye Height is reduced due to factors such as signal attenuation and noise. Therefore, signal attenuation and noise effects can be compared on the basis of eye-height.

Eye Width: Eye Width refers the horizontal-eye opening. It can be calculated from the difference between rising and falling intersections. As jitter worsens, Eye Width also worsens, allowing a visual assessment of jitter.

Jitter: Jitter is the time lag between the rising and falling edges at a rising and falling intersection.

Visually, it corresponds to the thickness of the horizontal line at the intersection. Large jitter causes large fluctuations between the rising and falling edges of a signal, affecting the timing and making it difficult to send and receive signals. Jitter is therefore an important measurement parameter in eye patterns. Jitter is caused by various factors and is collectively referred to as TJ (total jitter).

Rise Time (rise time): The rise time is the specified time for the voltage transitions from L (0) → H (1).

Fall Time (fall time): The fall time is the specified time for the voltage transitions from H (1) → L (0).

For details, refer to the standards of the interface used.

There is also a method employ a mask test to quantitatively evaluate the opening of the eye.
Mask testing is a method that displays masks, which are specified for each communication standard, on the eye pattern and assesses compliance with the standard if there is no overlap with the eye pattern. Masks typically have rhombic or hexagonal shapes and can be utilized to identify errors, thereby offering insights into signal improvement.

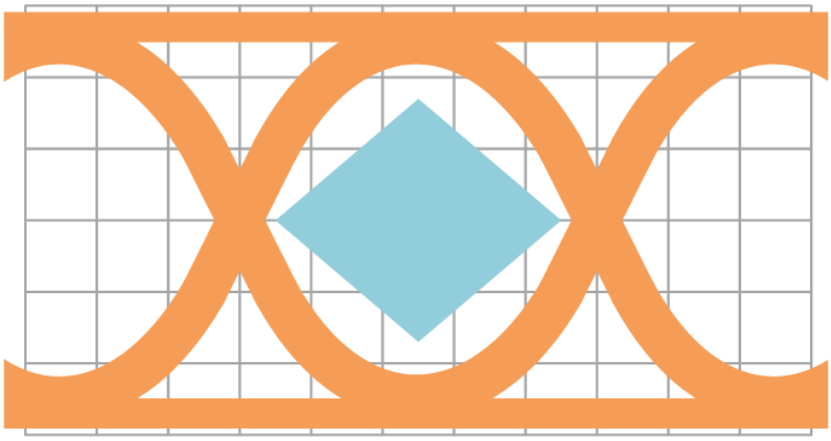

Fig. 8 Mast test example on eye pattern8

3.2. TDS4A212MX, TDS4B212MX eye pattern

Eye pattern evaluations were performed using evaluation boards that had TDS4A212MX, TDS4B212MX mounted on them.

Consequently, we obtained the eye pattern from the actual measurement board of the product by conducting de-embedding to remove the transmission line loss from the evaluation board's data (product-mounted board). Similarly, we obtained the eye pattern of the board used for evaluating substrate characteristics (through board).

The board is made of MEGTRON6 material. A 1.95mm V-connector was utilized for connecting the board to the cabling.

This board is designed with the shortest possible wiring, including the product, which allows measurements only between the A0± and C0± ports.

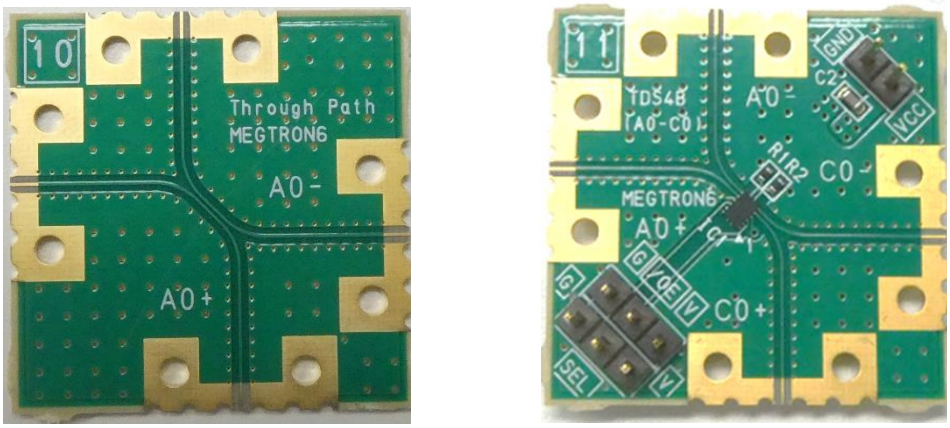

Fig. 9 Evaluation board used for eye pattern9

(Left: Through board Right: Product-mounted board)

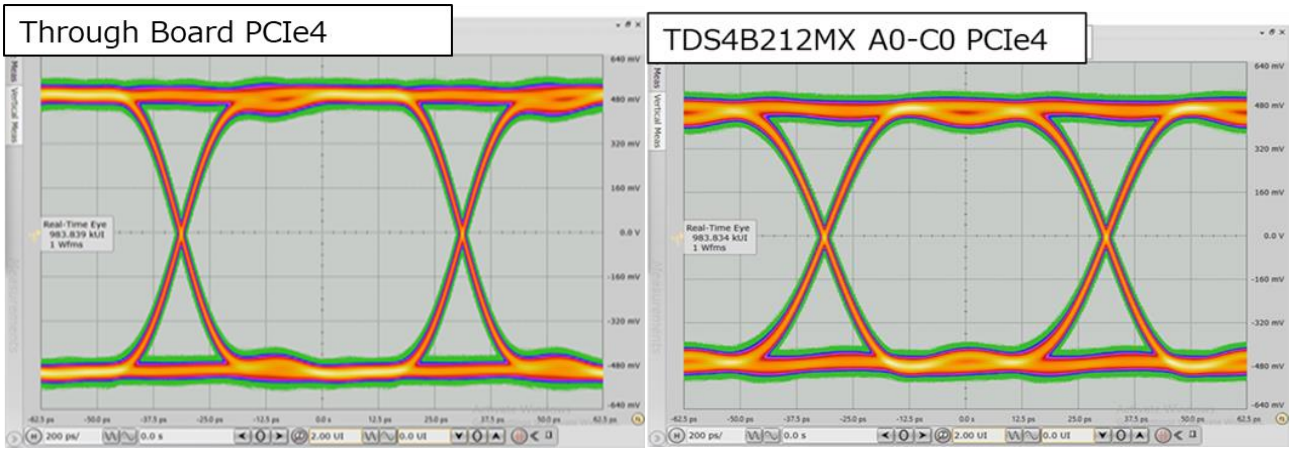

Fig. 10 Measured PCIe4 eye pattern10

(Left: Through board Right: TDS4B212MX)

We subsequently measured the Eye Height, Eye Width, and Total Jitter (TJ) for both the product mounting board and the through board. Afterward, we deducted the values for the through board from those of the product mounted board to determine the Eye Height attenuation (Δ Eye Height), Eye Width attenuation (Δ Eye Width), and TJ increment (Δ TJ) associated with the product.

Table. 2 PCIe4 Eye Pattern Evaluation Details2

Evaluation details	Eye Height (mV)	**ΔEye Height (mV)**	Eye Width (ps)	**ΔEye Width (ps)**	TJ (ps)	**ΔTJ (ps)**
Through board	839	-	59.86	-	4.55	-
TDS4B212MX	758	**-81**	59.28	**-0.59**	5.41	**0.86**

4. Application

4.1. Available interfaces

TDS4A212MX and TDS4B212MX are high-speed differential 2:1 MUX(Multiplexer)/1:2 DEMUX (demultiplexer) that can be used to switch signals into two distinct paths.
Our proprietary SOI processing "TarfSOI™" and small packaging enable us to achieve excellent high-frequency properties and use them at data rates up to 32Gbps.
It also achieves a wide common-mode voltage range (0 ~ 2.0 V) and differential-signal voltage swing (0 ~ 1.8 Vpp), allowing it to be used in various high-speed data protocols.
Typically, it is available on the following interfaces:

PCIe Gen 5.0, 4.0, 3.0, 2.0, 1.0
CXL 2.0, 1.0
USB4 Version2
USB4 Gen 3, Gen 2
USB 3.2 Gen 2, Gen 1
Thunderbolt 4, 3, 2
Display Port 2.0, 1.4, 1.3, 1.2
SAS 3.0

4.2. PCIe Use

The following shows how MUX/DEMUX switches the connectivity between the CPU and several PCIe slots.

Depending on the specifications of the PC and server, the PCIe lanes on the CPU may not be sufficient if there is a need to expand the PCIe slots. In such cases, a MUX/DEMUX can be used to connect the CPU to several PCIe slots. For instance, if you have 8 lanes of CPU with 16 lanes each of TX and RX directly connected to PCIe slot 1, and you want to use the remaining 8 lanes exclusively with PCIe slot 1 and PCIe slot 2, connect the 2:1 MUX/1:2 DEMUX as depicted in the figure below.

TDS4A212MX/TDS4B212MX can be switched between two lanes per device, thus it can be connected by placing eight devices between the CPU and PCIe slots.

Use AC coupling capacitors on the MUX/DEMUX to provide the appropriate common mode as follows.

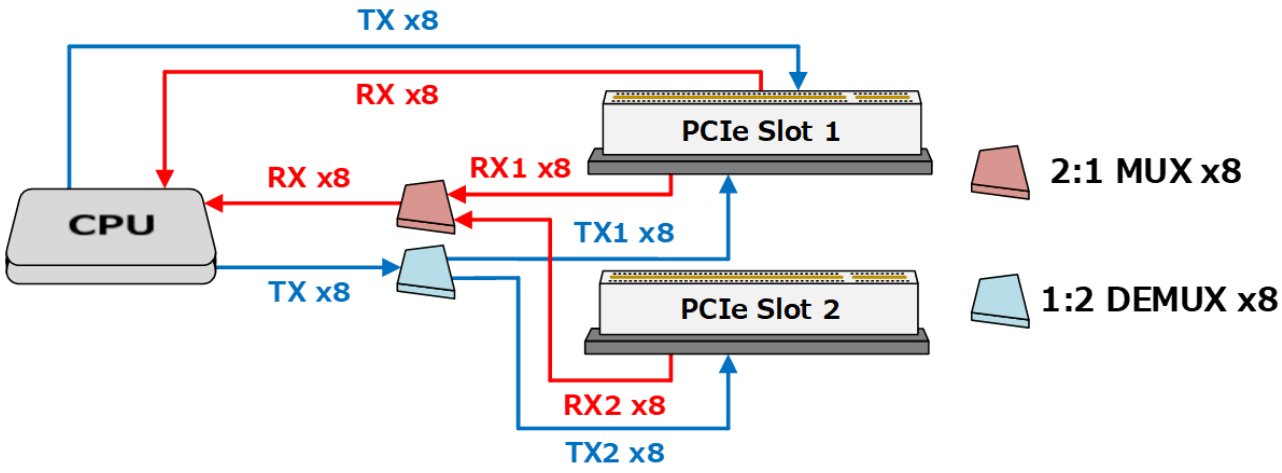

Fig. 11 MUX/DEMUX PCIe Use Case11

The Eye Pattern Assessment for PCIe5 is shown below.

PCIe5
32Gbps NRZ
1Vp-p(Diff)
PRBS-7

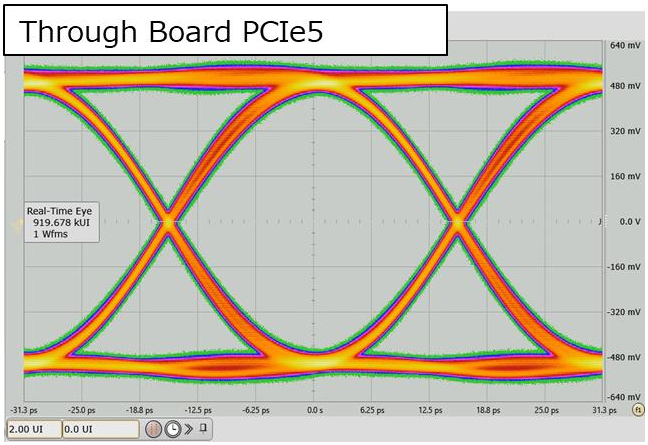

Fig. 12 PCIe5 Through Board Assessment12

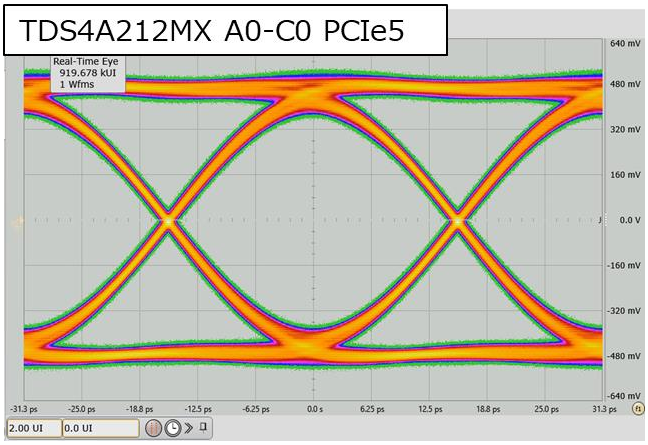

Fig. 13 PCIe5 TDS4A212MX assessment13

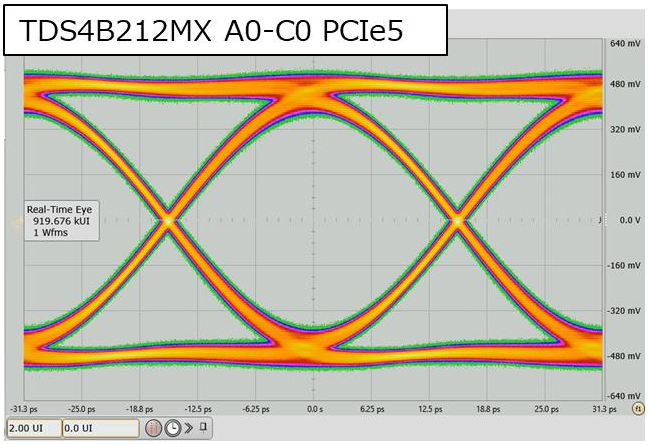

Fig. 14 PCIe5 TDS4B212MX assessment14

Table. 3 PCIe5 Eye Pattern Evaluation Details3

Evaluation details	Eye Height (mV)	ΔEye Height (mV)	Eye Width (ps)	ΔEye Width (ps)	TJ (ps)	ΔTJ (ps)
Through board	826	-	28.81	-	4.14	-
TDS4A212MX	675	-151	28.76	-0.05	4.33	0.19
TDS4B212MX	678	-148	28.91	0.10	4.20	0.06

The Eye Pattern Assessment for PCIe4 is shown below.

PCIe4
16Gbps NRZ
1Vp-p(Diff)
PRBS-7

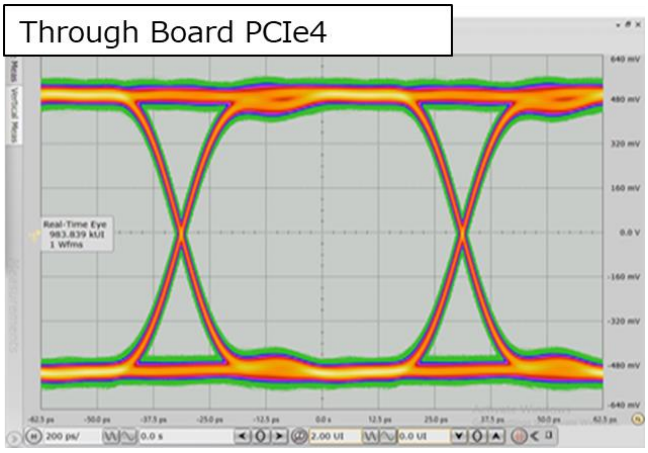

Fig. 15 PCIe4 Through Board Assessment15

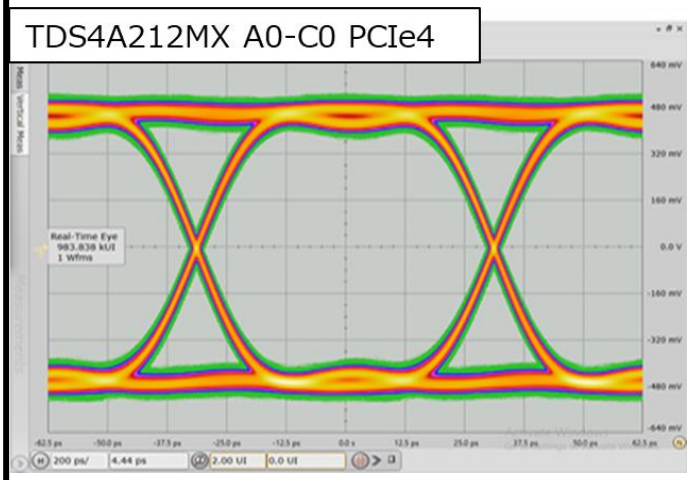

Fig. 16 PCIe4 TDS4A212MX assessment16

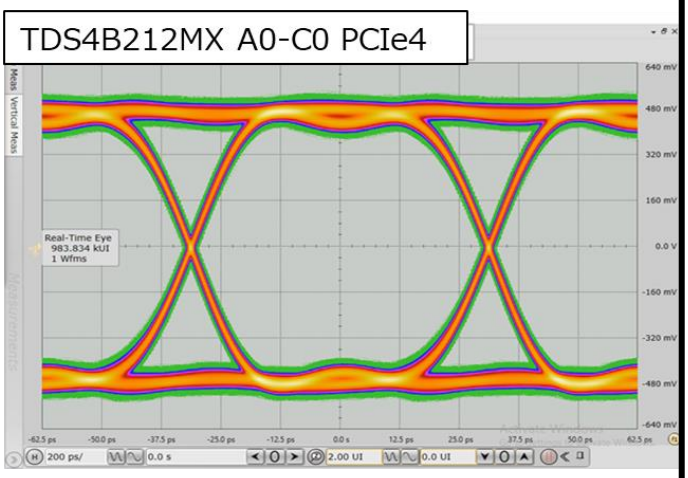

Fig. 17 PCIe4 TDS4B212MX assessment17

Table. 4 PCIe4 Eye Pattern Evaluation Details4

Evaluation details	Eye Height (mV)	ΔEye Height (mV)	Eye Width (ps)	ΔEye Width (ps)	TJ (ps)	ΔTJ (ps)
Through board	839	-	59.86	-	4.55	-
TDS4A212MX	758	-81	59.28	-0.59	5.41	0.86
TDS4B212MX	741	-98	59.18	-0.68	5.69	1.14

4.3. USB TypeC Use

When USB TypeC requires plug flip, the following is a sample connection. Since USB TypeC has no front and back terminals, and signals must be transmitted and received in either direction, a MUX/DEMUX is used to switch between front and back. The orientation is determined by the CC terminal, and the USB control IC selects the MUX/DEMUX port connection. The following shows an example where the host board and device board are connected using TypeC cables on both sides.

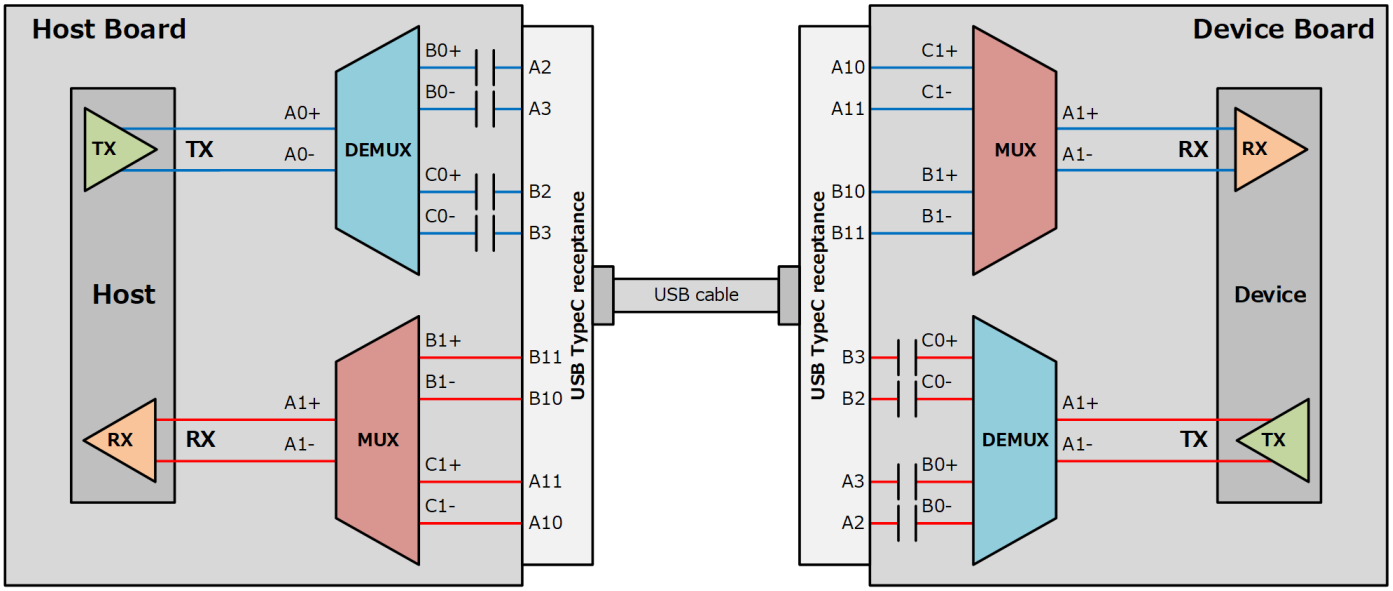

Fig. 18 USB TypeC MUX/DEMUX Use Case18

The Eye Pattern Assessment for USB4 Version2 is shown below.

USB4 Version2
40Gbps PAM3
1Vp-p(Diff)
PRBS-7

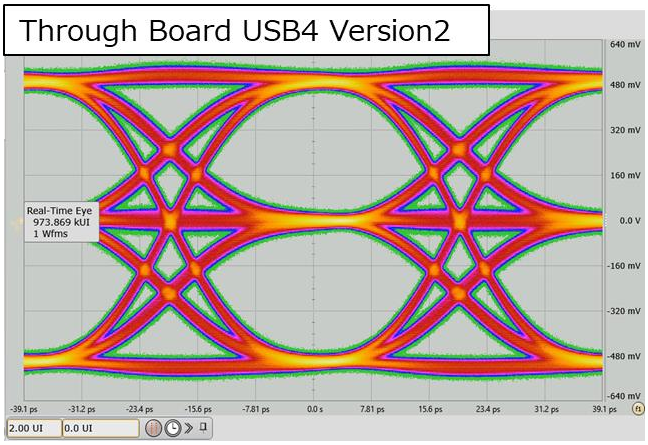

Fig. 19 USB4 Version2 Through Board Assessment19

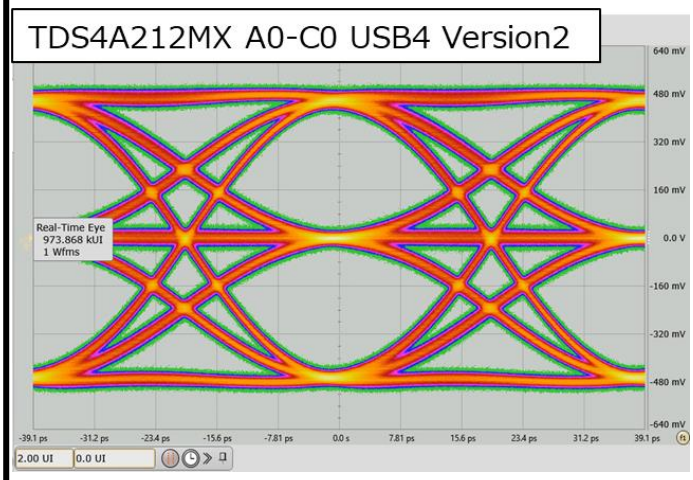

Fig. 20 USB4 Version2 TDS4A212MX assessment20

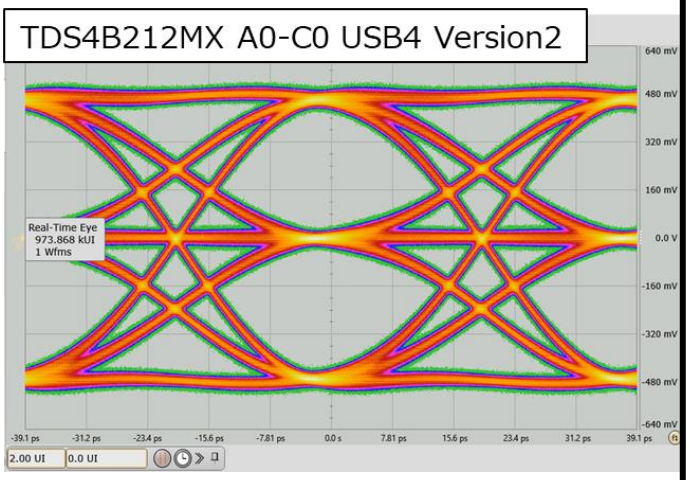

Fig. 21 USB4 Version2 TDS4B212MX assessment21

Table. 5 USB4 Version2 Eye Pattern Evaluation Details5

Evaluation details	Eye	Eye Height (mV)	ΔEye Height (mV)	Eye Width (ps)	ΔEye Width (ps)	TJ (ps)	ΔTJ(ps)
Through board	High	406	-	24.84	-	14.49	-
	Low	404	-	25.02	-	14.25	-
TDS4A212MX	High	370	-36	22.16	-2.69	17.35	2.86
	Low	370	-34	22.52	-2.50	17.11	2.87
TDS4B212MX	High	380	-26	22.22	-2.62	17.38	2.89
	Low	376	-28	22.22	-2.81	17.11	2.86

The Eye Pattern assessment for USB4 is shown below.

USB4
20Gbps NRZ
1Vp-p(Diff)
PRBS-7

Through Board USB4

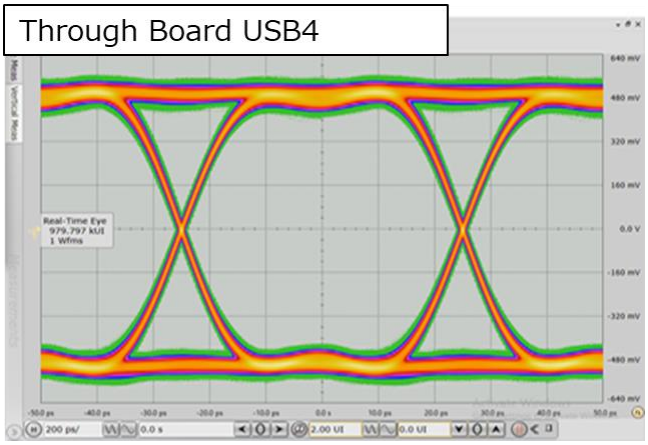

Fig. 22 USB4 Through Board Assessment22

TDS4A212MX A0-C0 USB4

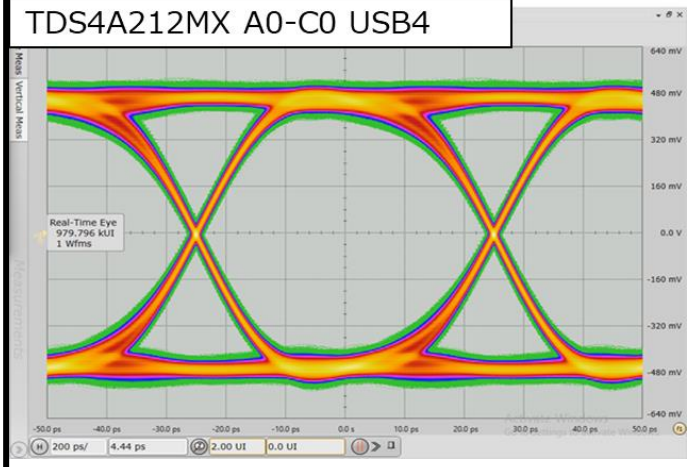

Fig. 23 USB4 TDS4A212MX assessment23

TDS4B212MX A0-C0 USB4

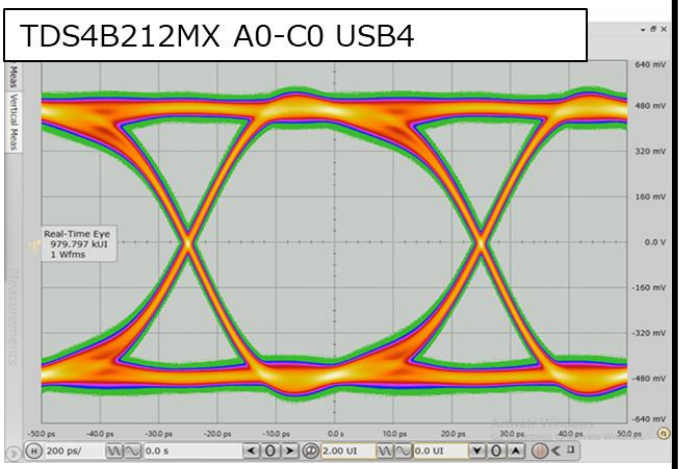

Fig. 24 USB4 TDS4B212MX assessment24

Table. 6 USB4 Eye Pattern Evaluation Details6

Evaluation details	Eye Height (mv)	ΔEye Height (mV)	Eye Width (ps)	ΔEye Width (ps)	TJ (ps)	ΔTJ (ps)
Through board	810	-	47.81	-	3.78	-
TDS4A212MX	743	-67	47.19	-0.63	4.79	1.01
TDS4B212MX	728	-82	46.88	-0.94	4.74	0.96

4.4. AC coupling

Many high-speed differential interfaces signaling require a capacitor (AC coupling capacitor) to provide an AC coupling between the TX (transmitter) and the RX (receiver).
When a high-speed differential signal passes through an AC coupling capacitor, the DC components of the signal are removed, enabling signal transmission even when the common-mode voltage differs between the TX and the RX.
The figure below shows an example where the host board and the device board are connected by a connector. In many high-speed differential interfaces, if the TX and the RX are connected by connectors, it is recommended that AC coupling capacitors be placed between the TX and the connectors. Therefore, an AC coupling capacitor is placed in the position shown in Fig. 25.
If this happens, the high-speed differential signal passes through an AC coupling capacitor, which removes the DC components, so that the common-mode voltage is supplied from the TX prior to passing through an AC coupling capacitor, and the common-mode voltage is supplied from the RX after passing through an AC coupling capacitor.

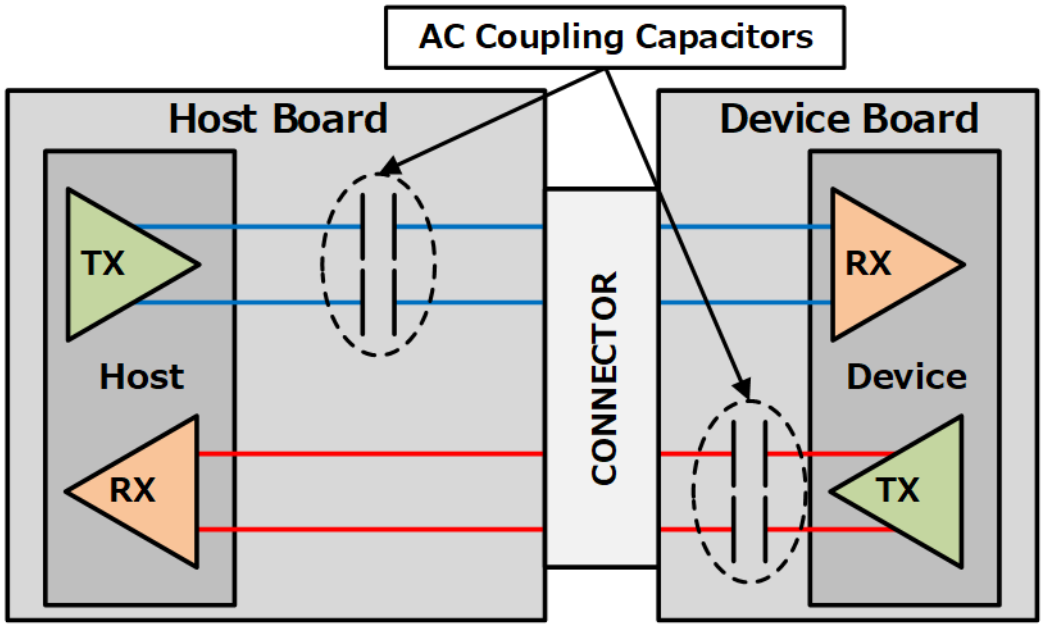

Fig. 25 AC Coupling Capacitor Layout25

In addition, an AC coupling capacitor needs to select an appropriate capacitance according to the interface. For the same differential pair, place symmetrically with the same capacity and the same package size.
Package sizes of 201 and 402 are recommended, while 603 and 805 are not recommended, considering the effect on differential wiring length.

The following example shows an exclusive connection between the host board and two device boards. The MUX/DEMUX is located on the host board. The switching is controlled by the host. Three typical arrangement patterns are shown below.

(a)Place a capacitor between MUX/DEMUX and the device*

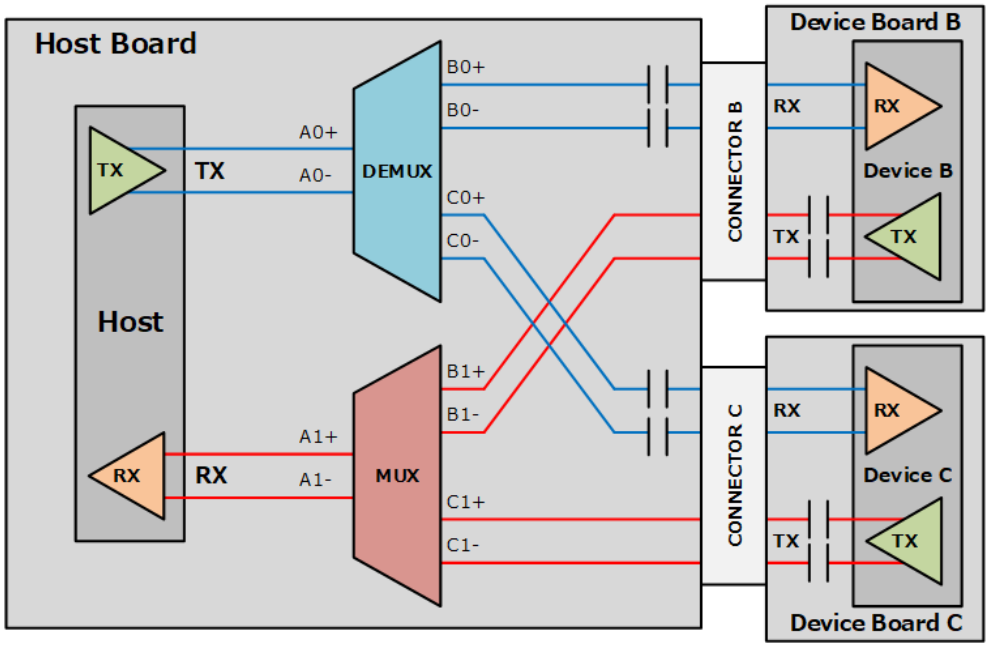

Fig. 26 An arrangement where a capacitor is placed between MUX/DEMUX and the device.26

*Check that the common-mode voltage of the host's TX and RX is within MUX/DEMUX's operating limits.

In the path passing through the DEMUX (blue line), an AC coupling capacitor is placed between the DEMUX and the connector.
Since the differential signal passes through the DEMUX prior to passing through the AC coupling capacitor, the DEMUX is supplied with the common-mode voltage from the host's TX.
In the path passing through the MUX (red line), an AC coupling capacitor is placed between the TX of the device and the connector.
Since the differential signal passes through the MUX after passing through the AC coupling capacitor, the MUX is supplied with the common-mode voltage from the host's RX.

Since it is recommended that the AC coupling capacitor be placed between the TX and the connector, the position to be placed is limited to this position.

(b)Place a capacitor between TX and MUX/DEMUX *

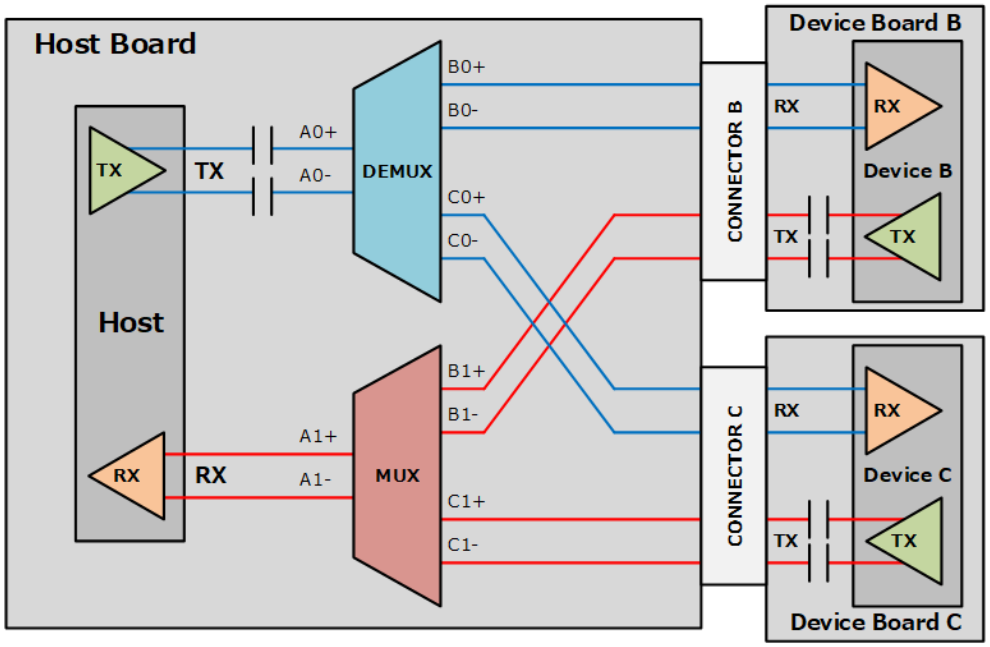

Fig. 27 An arrangement where a capacitor is placed between TX and MUX/DEMUX27

*It can be used when the RX common mode voltage of the device is within the operating range of the DEMUX, and the RX common mode voltage of the device is within the operating range of the MUX.

In the path passing through the DEMUX (blue line), an AC coupling capacitor is placed between the TX and the DEMUX.
Since the differential signal passes through the AC coupling capacitor and then through the DEMUX, the RX of the device provides a common-mode voltage.
In the path passing through the MUX (red line), an AC coupling capacitor is placed between the TX of the device and the connector.
Since the differential signal passes through the MUX after passing through the AC coupling capacitor, the MUX is supplied with the common-mode voltage from the host's RX.

Since it is recommended that the AC coupling capacitor be placed between the TX and the connector, the position to be placed is limited to this position.

(c)Place capacitors on both sides of MUX/DEMUX *

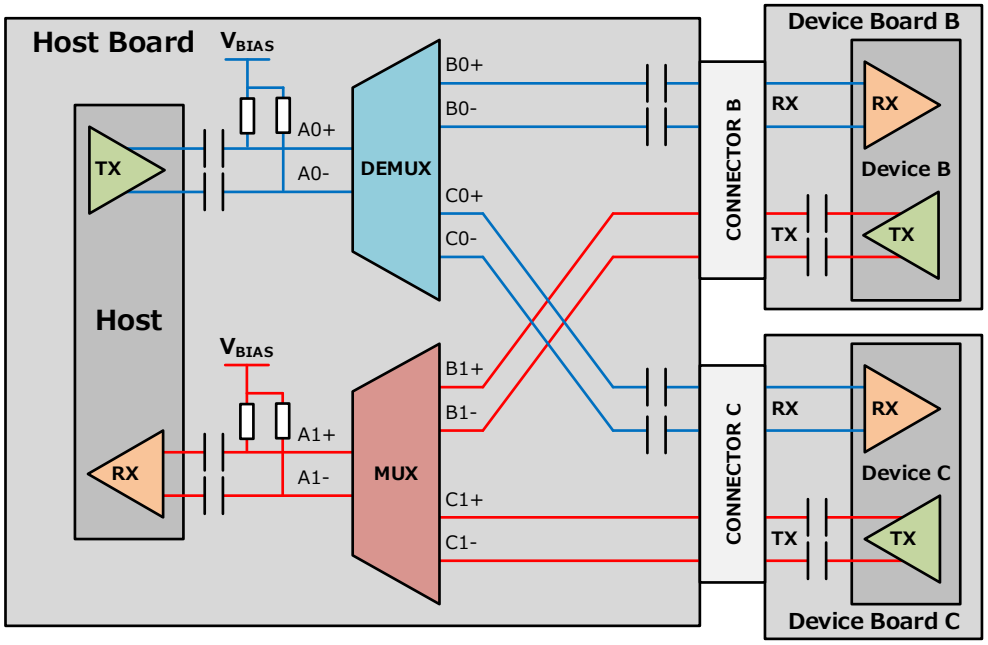

Fig. 28 An arrangement where capacitors are located on both sides of MUX/DEMUX28

*This configuration is used when the common-mode voltage of the TX and RX of the host/device is outside of the operating limits of the MUX/DEMUX.

An AC coupling capacitor is placed on both sides of the MUX/DEMUX for both the path passing through the MUX and the path passing through the DEMUX.
In such an arrangement, the MUX/DEMUX will not receive common-mode power from both the host and the device.
Therefore, as shown in the diagram, apply a common-mode voltage between 0 and 2.0 V with a resistor of 10 kΩ or more.

5. Summary

This document describes our MUX/DEMUX bus-switch, the TDS4A212MX and the TDS4B212MX, for high-speed differential interfaces.
If you need a MUX, DEMUX for a PCIe, USB, Thunderbolt or other high-speed interfaces, we would like you to consider TDS4A212MX, TDS4B212MX. Please Refer to the data sheet for other detailed characteristics.

For TDS4A212MX product pages and data sheets, see → Click Here

For TDS4B212MX product pages and data sheets, see → Click Here

For a list of bus switches, see → Click Here

Here is an introduction to the Toshiba bus switch in the mini catalog → Click Here

Application notebook switch basics here → Click Here

This is FAQ for the bus switch → Click Here

Handling Precautions

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The hardware, software and systems described in this document are called "this product."

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