

MOSFETs Silicon N-Channel MOS (U-MOSIII)

# SSM3K79CTC

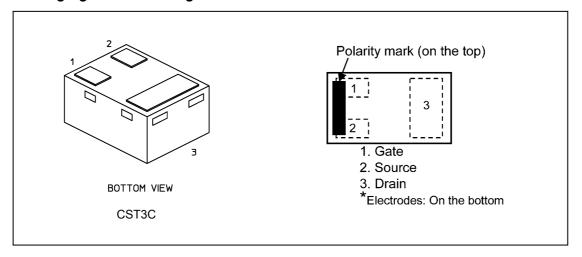
#### 1. Applications

· Load Switches

#### 2. Features

- (1) 2.5 V drive
- (2) Low drain-source on-resistance
  - :  $R_{DS(ON)}$  = 3.6  $\Omega$  (max) (@ $V_{GS}$  = 4 V)
  - $R_{DS(ON)} = 6.0 \Omega \text{ (max) } (@V_{GS} = 2.5 \text{ V})$
- (3) Low leakage current

# 3. Packaging and Pin Assignment





## 4. Absolute Maximum Ratings (Note) (Unless otherwise specified, Ta = 25 °C)

Characteristics		Symbol	Rating	Unit
Drain-source voltage		V <sub>DSS</sub>	30	V
Gate-source voltage		V <sub>GSS</sub>	±20	
Drain current (DC)	(Note 1)	I <sub>D</sub>	100	mA
Drain current (pulsed)	(Note 1)	I <sub>DP</sub>	400	
Power dissipation	(Note 2)	$P_{D}$	500	mW
Channel temperature		T <sub>ch</sub>	150	°C
Storage temperature		T <sub>stg</sub>	-55 to 150	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Ensure that the channel temperature does not exceed 150 °C.

Note 2: Device mounted on a 25.4 mm × 25.4 mm × 1.6 mm FR4 glass epoxy board (Cu pad: 645 mm<sup>2</sup>)

Note: This transistor is sensitive to electrostatic discharge and should be handled with care.

Note: The MOSFETs in this device are sensitive to electrostatic discharge. When handling this device, the worktables,

operators, soldering irons and other objects should be protected against anti-static discharge.

Note: The channel-to-ambient thermal resistance, R<sub>th(ch-a)</sub>, and the drain power dissipation, P<sub>D</sub>, vary according to the board material, board area, board thickness and pad area. When using this device, be sure to take heat dissipation fully into account.



#### 5. Electrical Characteristics

#### 5.1. Static Characteristics (Unless otherwise specified, T<sub>a</sub> = 25 °C)

Characteristics		Symbol	Test Condition	Min	Тур.	Max	Unit
Gate leakage current		I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 5 \text{ V}$	_	_	±0.05	μА
			$V_{DS}$ = 0 V, $V_{GS}$ = ±16 V	_	_	±1	
Drain cut-off current		I <sub>DSS</sub>	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V	_	_	0.06	
Drain-source breakdown voltage		V <sub>(BR)DSS</sub>	I <sub>D</sub> = 0.1 mA, V <sub>GS</sub> = 0 V	30	_	_	V
Drain-source breakdown voltage	(Note 1)	V <sub>(BR)DSX</sub>	I <sub>D</sub> = 0.1 mA, V <sub>GS</sub> = -10 V	16	_	_	
Gate threshold voltage	(Note 2)	V <sub>th</sub>	$V_{DS} = 3 \text{ V}, I_{D} = 0.1 \text{ mA}$	0.8	_	1.5	
Drain-source on-resistance	(Note 3)	R <sub>DS(ON)</sub>	I <sub>D</sub> = 10 mA, V <sub>GS</sub> = 2.5 V	_	3.5	6.0	Ω
			I <sub>D</sub> = 10 mA, V <sub>GS</sub> = 4 V	_	2.3	3.6	
Forward transfer admittance	(Note 3)	Y <sub>fs</sub>	V <sub>DS</sub> = 3 V, I <sub>D</sub> = 10 mA	35	_	_	mS

Note 1: If a reverse bias is applied between gate and source, this device enters  $V_{(BR)DSX}$  mode. Note that the drain-source breakdown voltage is lowered in this mode.

Note 2: Let  $V_{th}$  be the voltage applied between gate and source that causes the drain current ( $I_D$ ) to below (0.1 mA for this device). Then, for normal switching operation,  $V_{GS(ON)}$  must be higher than  $V_{th}$ , and  $V_{GS(OFF)}$  must be lower than  $V_{th}$ . This relationship can be expressed as:  $V_{GS(OFF)} < V_{th} < V_{GS(ON)}$ .

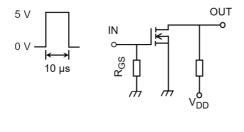
Take this into consideration when using the device.

Note 3: Pulse measurement.

#### 5.2. Dynamic Characteristics (Unless otherwise specified, T<sub>a</sub> = 25 °C)

Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Input capacitance	C <sub>iss</sub>	$V_{DS} = 3 \text{ V}, V_{GS} = 0 \text{ V},$	_	13.5	_	pF
Reverse transfer capacitance	C <sub>rss</sub>	f = 1 MHz		6.5		
Output capacitance	C <sub>oss</sub>			8.0		
Switching time (turn-on time)	t <sub>on</sub>	$V_{DD}$ = 5 V, $I_{D}$ = 10 mA, $V_{GS}$ = 0 to 5 V, $R_{GS}$ = 50 $\Omega$		5.5		ns
Switching time (turn-off time)	t <sub>off</sub>	Duty $\leq$ 1 %,V <sub>IN</sub> : $t_r$ , $t_f$ < 5 ns, Common source, See Chapter 5.3.		35		

#### 5.3. Switching Time Test Circuit



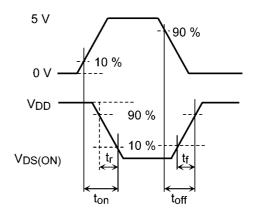


Fig. 5.3.1 Switching Time Test Circuit

Fig. 5.3.2 Input Waveform/Output Waveform

## 5.4. Source-Drain Characteristics (Unless otherwise specified, T<sub>a</sub> = 25 °C)

Characteristics		Symbol	Test Condition	Min	Тур.	Max	Unit
Diode forward voltage	(Note 1)	$V_{DSF}$	$I_D = -100 \text{ mA}, V_{GS} = 0 \text{ V}$		-0.85	-1.2	V

Note 1: Pulse measurement.



# 6. Marking

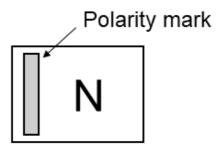
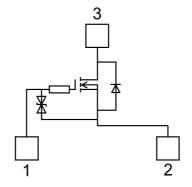


Fig. 6.1 Marking

# 7. Equivalent Circuit





#### 8. Characteristics Curves (Note)

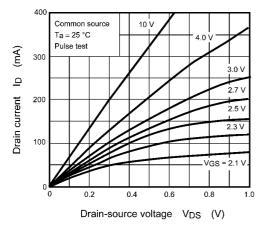
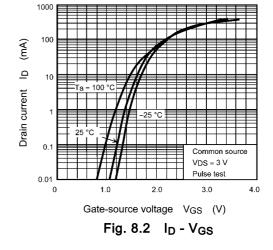


Fig. 8.1 I<sub>D</sub> - V<sub>DS</sub>



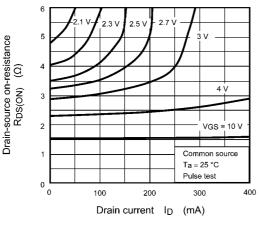


Fig. 8.3 R<sub>DS(ON)</sub> - I<sub>D</sub>

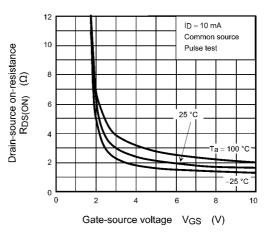


Fig. 8.4 R<sub>DS(ON)</sub> - V<sub>GS</sub>

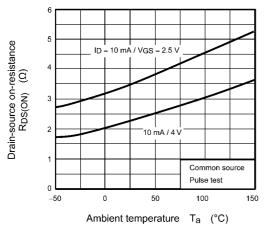


Fig. 8.5 R<sub>DS(ON)</sub> - T<sub>a</sub>

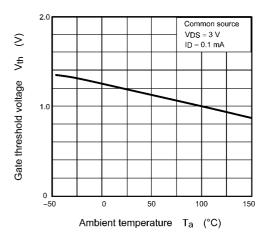
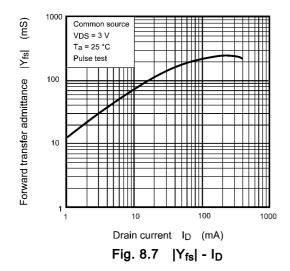


Fig. 8.6 V<sub>th</sub> - T<sub>a</sub>





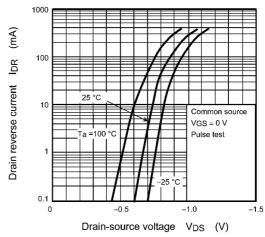
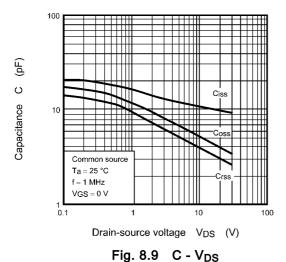
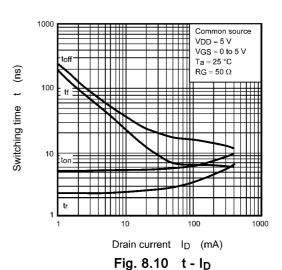


Fig. 8.8 I<sub>DR</sub> - V<sub>DS</sub>





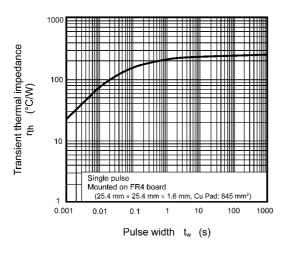


Fig. 8.11 rth - tw

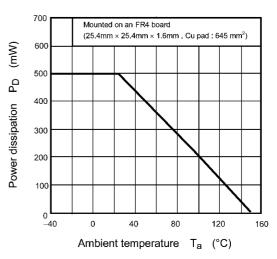


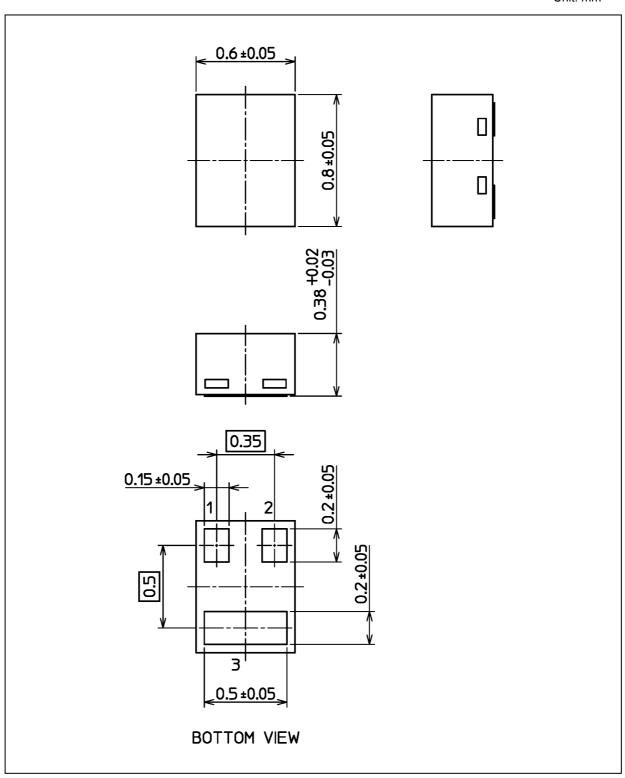
Fig. 8.12 P<sub>D</sub> - T<sub>a</sub>

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.



# **Package Dimensions**

Unit: mm



Weight: 0.55 mg (typ.)

Package Name(s)
Nickname: CST3C



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