Gate Drive Circuit
for SiC MOSFET Module

Design guide

RD237-DGUIDE-02

Toshiba Electronic Devices & Storage Corporation

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1. Introduction

This design guide (hereafter referred to as this guide) describes the design methodology of the Gate Drive Circuit for SiC MOSFET Module (hereafter referred to as this design).

SiC (Silicon Carbide) MOSFETs have been developed in recent years because they allow the reduction of on-resistance while maintaining a higher breakdown voltage compared to the conventional Si (Silicon) MOSFETs. Therefore, these are being evaluated and adopted more and more with the aim of improving inverter efficiency.

SiC MOSFET modules equipped with SiC MOSFET chips are used in power conversion in motor drives used in industrial applications and inverters for railroad cars contributing to a more efficient and compact industrial equipment.

This design uses the pre-driver TLP5231 that is capable of high-current gate drive by using external buffer MOSFETs and has various protection functions to achieve isolated gate drive for high-current and high-voltage SiC MOSFET modules.

This design is optimized for driving the gates of Toshiba's Dual SiC MOSFET modules (MG400V2YMS3, MG600Q2YMS3, MG250YD2YMS3). By using this design, the application circuit of the SiC MOSFET module can be easily configured.

It is equipped with two gate drive circuits to match the above-mentioned SiC MOSFET modules, and in addition it is miniaturized to the same size as that of the module so that it can be mounted directly on top of the module, therefore creating an excellent solution for suppressing parasitic inductance in wiring.

This design features a variety of the protection circuits, including DESAT (desaturation) detection function, active miller clamp function, etc. In addition, each component can be adjusted according to the actual target specifications.

For more details about Toshiba's SiC MOSFET modules, kindly refer to their datasheets and other related documents.

When using a SiC MOSFET module other than the above-mentioned modules, each component needs to be adjusted. Refer to the datasheet and other related documents of TLP5231, the design guide of this reference design, etc. for adjusting each component.

When applying this design to an actual application, refer to the TLP5231 data sheet and design it to meet the safety standards to which the operating conditions and environment apply.

* Each Dual SiC MOSFET module has been tested under the following conditions.

MG400V2YMS3: VDS ≦ 800V, ID ≦ 600A

MG600Q2YMS3: VDS ≦ 1200V, ID ≦ 400A

MG250YD2YMS3: VDS ≦ 1200V, ID ≦ 250A

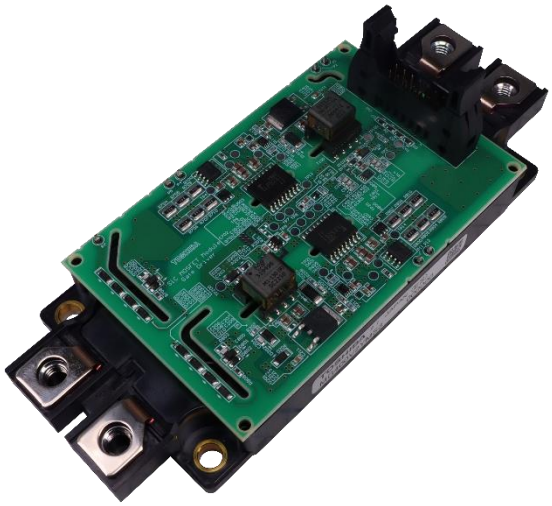

Image of this design attached directly to Toshiba’s Dual SiC MOSFET Module

2. Main Components Used

2.1. Pre-Driver Coupler TLP5231

This design uses TLP5231 pre-drive photocouplers that are capable of high-current gate-drive by using an external buffer MOSFET and incorporates various protection functions. The main features of TLP5231 are as follows.

- Output peak current: ±2.5A (Max.)
- Operating temperature: -40 to 110°C
- Threshold input current: 3.5mA (Max.)
- Propagation delay time: 300ns (Max.)
- Common-mode transient immunity: ±25kV/μs (Min.)
- Isolation voltage: 5000Vrms (Min.)
- Dual output for external complementary type MOS buffer
- Under Voltage Lock-Out (UVLO) protection for positive and negative gate power supply
- Safety Standards

  UL recognized: UL 1577, File No. E67349

  cUL recognized: CSA Component Acceptance Service No.5A File No. E67349

  VDE approved: EN 60747-5-5, EN 62368-1 (Note 2.1)

  CQC approved: GB4943.1, GB8898 Japan Factory

  Note: When a VDE approved type is needed, please designate the "Optional (D4)".
- Structural parameter: Minimum creepage and clearance 8mm

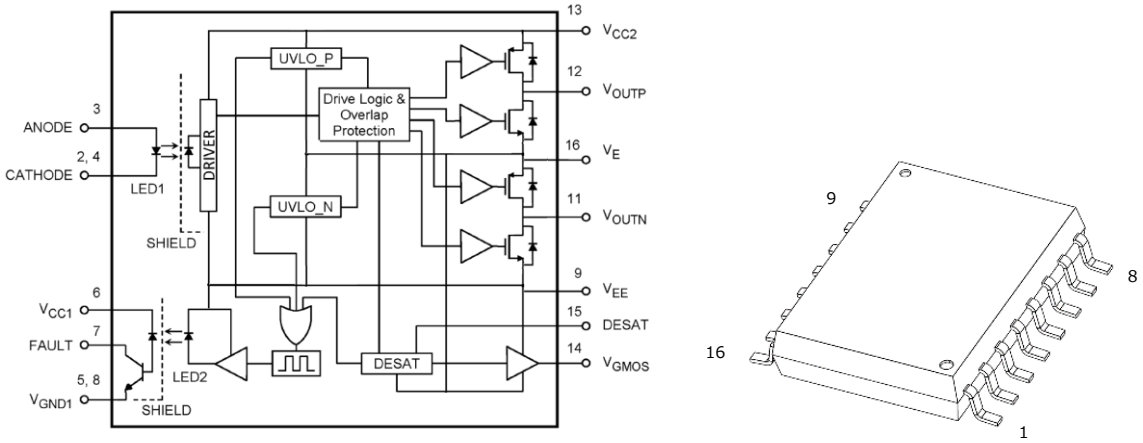

Fig. 2.1 TLP5231 Internal Circuit Configuration and Package (SO16L)

2.2. LDO Regulator IC TCR1HF50B

This design uses TCR1HF50B LDO regulators for producing the internal 5V power supply. The main features of TCR1HF50B are as follows.

- High maximum input voltage: 40V (Max.), Operation input voltage range: 4V to 36V
- Low quiescent current I_{BON} = 1μA (Typ.) @ I_{OUT} = 0mA
- High response load transient
  -60mV/+50mV @ 3.3V output, I_{OUT} = 0mA ↔ 10mA
- High accuracy output voltage: ±1% (Ta = 25°C)
- Built-in overcurrent protection circuit
- Built-in overheat protection circuit
- Built-in inrush current reduction circuit
- Pull up connection between CONTROL and VIN
- Ceramic capacitors can be used
- General package SMV (SOT-25) (2.9mm x 2.8mm x 1.1mm)

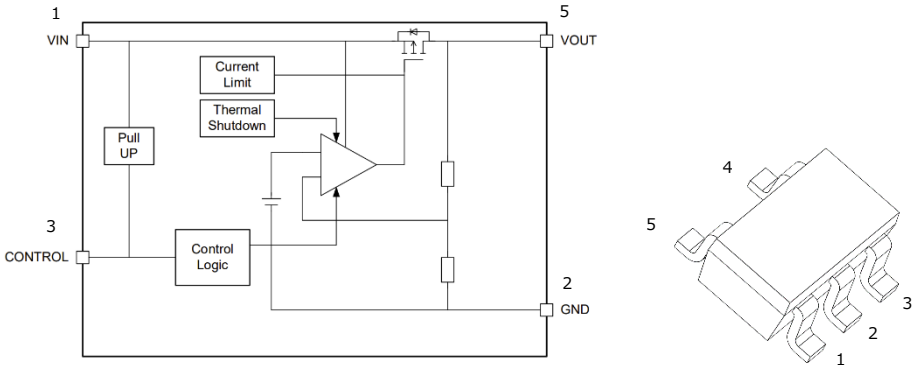

Fig. 2.2 TCR1HF50B Internal Circuit Configuration and Package (SOT-25)

2.3. High-Speed Comparator IC TC75S57FU

This design uses CMOS type general-purpose single comparators (TC75S57FU) in active miller clamp circuits. The main features of TC75S57FU are as follows.

- Low current consumption: I_{DD} = 100μA (Typ.)
- Single power supply operation: V_{DD} = ±0.9 to ±3.5V or 1.8 to 7V
- Wide common mode input voltage range: V_{SS} to V_{DD} - 0.9V
- Push-pull output circuit
- Low input bias current
- Small package

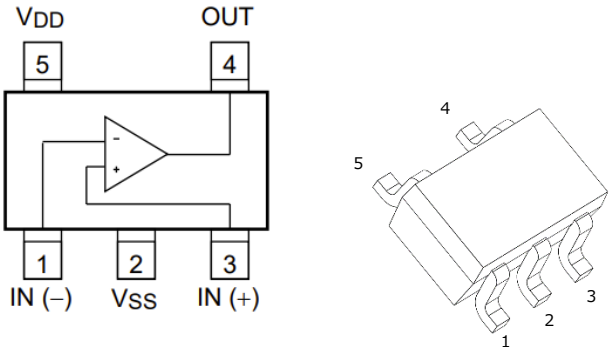

Fig. 2.3 TC75S57FU Internal Circuit Configuration and Package (SOT-353)

2.4. Small Package MOSFET TPC8132

This design uses TPC8132 P-ch MOSFETs as buffer for gate-drive of TLP5231. The main features of TPC8132 are as follows.

- Small footprint due to small and thin package
- Low drain-source on-resistance: $R_{DS(ON)}$ = 20mΩ (Typ.) (V_{GS} =-10V)
- Low leakage current: I_{DSS} =-10μA (Max.) (V_{DS} =-40V)
- Enhancement mode: V_{th} = -0.8 to -2.0V (V_{DS} = -10V, I_D = -0.2mA)

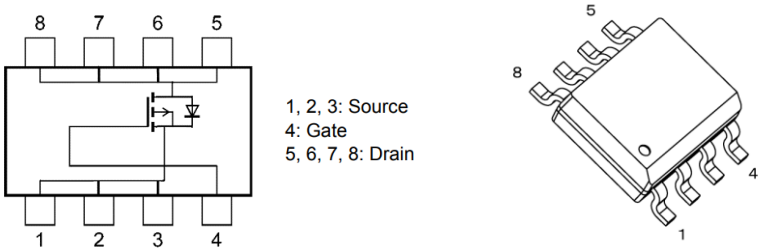

Fig. 2.4 TCP8132 Internal Circuit Configuration and Package (SOP-8)

2.5. Tiny Package MOSFET SSM6K804R

This design uses SSM6K804R N-ch MOSFETs as buffer for gate-drive of TLP5231 and in the DESAT detection soft turn-off. The main features of SSM6K804R are as follows.

- 175℃ MOSFET
- 4.5V drive
- Low drain-source on-resistance

  $R_{DS(ON)}$ = 12mΩ (Typ.) (@V_{GS} = 4.5V)

  $R_{DS(ON)}$ = 9mΩ (Typ.) (@V_{GS} = 10V)

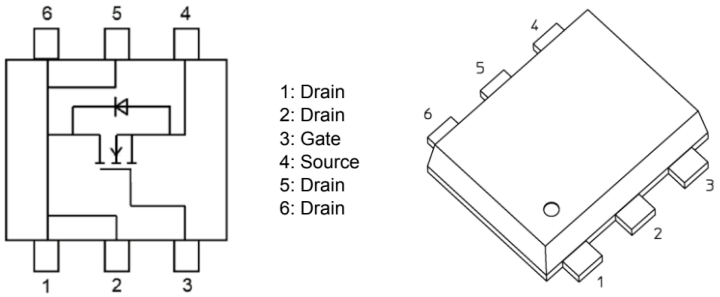

Fig. 2.5 SSM6K804R Internal Circuit Configuration and Package (TSOP6F)

2.6. Small Signal MOSFET SSM3K318R

This design uses SSM3K318R N-ch MOSFET in the active miller clamp circuit. The main features of SSM3K318R are as follows.

- 4.5V gate drive voltage
- Low drain-source on-resistance

  $R_{DS(ON)}$ = 145mΩ (Max.) (@V_{GS} = 4.5V)

  $R_{DS(ON)}$ = 107mΩ (Max.) (@V_{GS} = 10V)

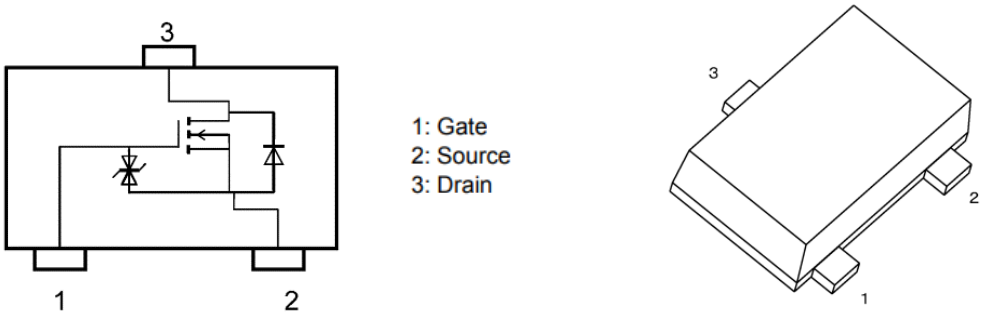

Fig. 2.6 SSM3K318R Internal Circuit Configuration and Package (SOT-23F)

2.7. Small Signal MOSFET SSM3K15AFS

This design uses SSM3K15AFS N-ch MOSFETs in the input-drive (photocoupler) of TLP5231. The main features of SSM3K15AFS are as follows.

- 2.5V drive
- Low on-resistance
  $R_{DS(ON)}$ = 3.6Ω (Max.) (@V_{GS} = 4V)
  $R_{DS(ON)}$ = 6.0Ω (Max.) (@V_{GS} = 2.5V)

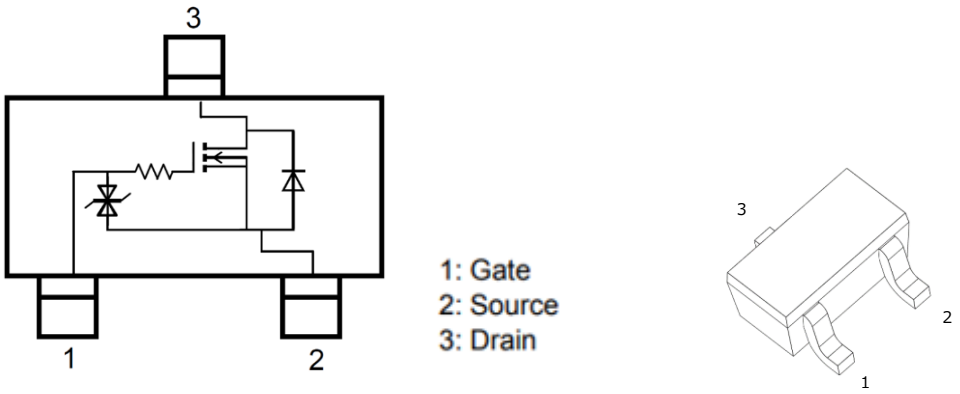

Fig. 2.7 SSM3K15AFS Internal Circuit Configuration and Package (SOT-416)

2.8. Small Signal NPN Bipolar Transistor 2SC6026MFV

This design uses 2SC6026MFV NPN bipolar transistors in the fault detector circuit. The main features of 2SC6026MFV are as follows.

- High withstand voltage: V_{CEO} = 50V
- High collector current: I_C = 150mA (Max.)
- High current amplification factor: h_{FE} = 120 to 400
- Excellent h_{FE} linearity: h_{FE} (IC = 0.1mA)/h_{FE} (IC = 2mA) = 0.95 (Typ.)

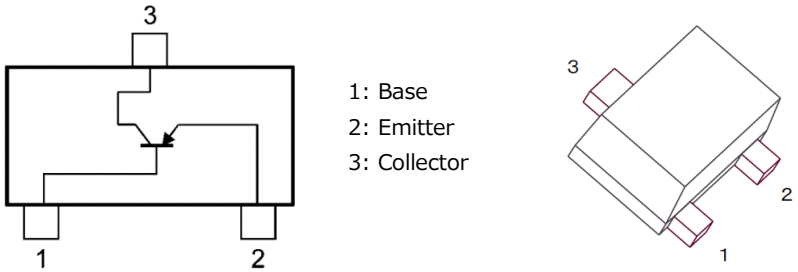

Fig. 2.8 2SC6026MFV Internal Circuit Configuration and Package (SOT-723)

3. Outline of Gate Driver for SiC MOSFET Module

This design is a gate drive circuit that can drive Toshiba's Dual SiC MOSFET Modules. This design is equipped with the gate-drive circuit using the pre-drive photocoupler TLP5231, an insulated power supply, and protection circuits.

3.1. Features

- High-current gate-drive via external buffer MOSFETs
- Single power supply operation with isolated DC-DC circuit
- Short-circuit proof (using DESAT detection)
- Low gate-drive voltage detection (UVLO)
- Active Miller Clamp (AMC)
- Output on/off control
- Fault detection output
- Temperature monitor output

3.2. Pin Description

It features a controller connector (CN1) as the external interface and uses a XG4A-1431 (Omron connector.

Table3.1 Controller Connector (CN1) Specifications

Pin#	Signal Name	I/O	Description	Pin#	Signal Name	I/O	Description
1	GND	-	GND	2	VDD	-	Power supply voltage for control
3	(N.C.)	-		4	B_INA	I	Low-side gate control signal input
5	B_FLT	O	Low-side fault detection output (Resistor collector output)	6	B_ENA	I	Low-side enable signal input
7	A_INA	I	High-side gate control signal input	8	(N.C.)	-	
9	A_ENA	I	High-side enable signal input	10	(5V)	-	External 5V power supply pin (Optional)
11	GND	-	GND	12	A_FLT	O	High-side fault detection output (Resistor collector output)
13	TH1	O	Temperature detection output 1	14	TH2	O	Temperature detection output 2

3.3. Specifications

Table 3.2 lists the recommended operating ranges of the gate drivers for SiC MOSFET modules. Table 3.3 lists the electrical properties of the gate drive output-voltage and the protective functions.

Table 3.2 Recommended Operation Range

Item			Min.	Typ.	Max.	Unit
Power supply voltage for control	V_{DD}		20.0	24	28.0	V
Input signal (gate control signal, enable signal)	INPUT	High Level	4.0	-	5.0	V
		Low Level	0	-	1.8	
Switching Frequency Note 3.1 (SiC MOSFET module gate drive)	f_{sw}		-	-	50	kHz

Note 3.1: Set frequency such that each component remains within its rated temperature range in actual application.

Table 3.3 Electrical Characteristics

Item	Symbol	Conditions	Min	Typ.	Max	Unit
Gate drive output High voltage	V_{CC2}		18.5	20	21.5	V
Gate drive output Low voltage	V_{EE}		-7.2	-6.7	-6.2	V
UVLO_P threshold (V_{CC2}-V_E)	V_{UVLOP-}	Protection operation voltage @IF = 8mA V_{OUTP}-V_E > 5V	11	12	13	V
	V_{UVLOP+}	Protection release voltage @IF = 8mA V_{OUTP}-V_E < 5V	12	13	14	
UVLO_N Threshold (V_E-V_{EE})	V_{UVLON-}	Protection operation voltage @IF = 8mA V_{OUTN}-V_E > 1V	-5.7	-5.0	-4.7	V
	V_{UVLON+}	Protection release voltage @IF = 8mA V_{OUTN}-V_E < 1V	-6	-5.3	-5	
Drain-source voltage when DESAT is detected Note 3.2	V_{DS} (High side)	V_{CC2}-V_E = 20V Ta = 25℃	0.46	-	-	V
	V_{DS} (Low side)					
Thermistor rated resistance	R	Tc = 25℃	3.5	5.0	6.5	kΩ
		Tc = 50℃	125	165	205	Ω
Thermistor B constant	B	TNTC = 25 to 150℃	-	3375	-	K

Note 3.2 When DESAT is detected, the drain-source voltage is equal to DESAT threshold voltage of TLP5231 minus the voltage drop across the diodes (D703, D704, D705, D706) and the resistor (R708).

4. Circuit Design

4.1. Overall Block Diagram

Fig. 4.1 shows the block diagram of the gate driver for SiC MOSFET module. It is equipped with TLP5231 pre-drive photocouplers, isolated DCDC converters, and active miller clamp circuits that enable high-current gate-drive via external buffer MOSFETs. It operates according to the control power supply voltage supplied from VDD.

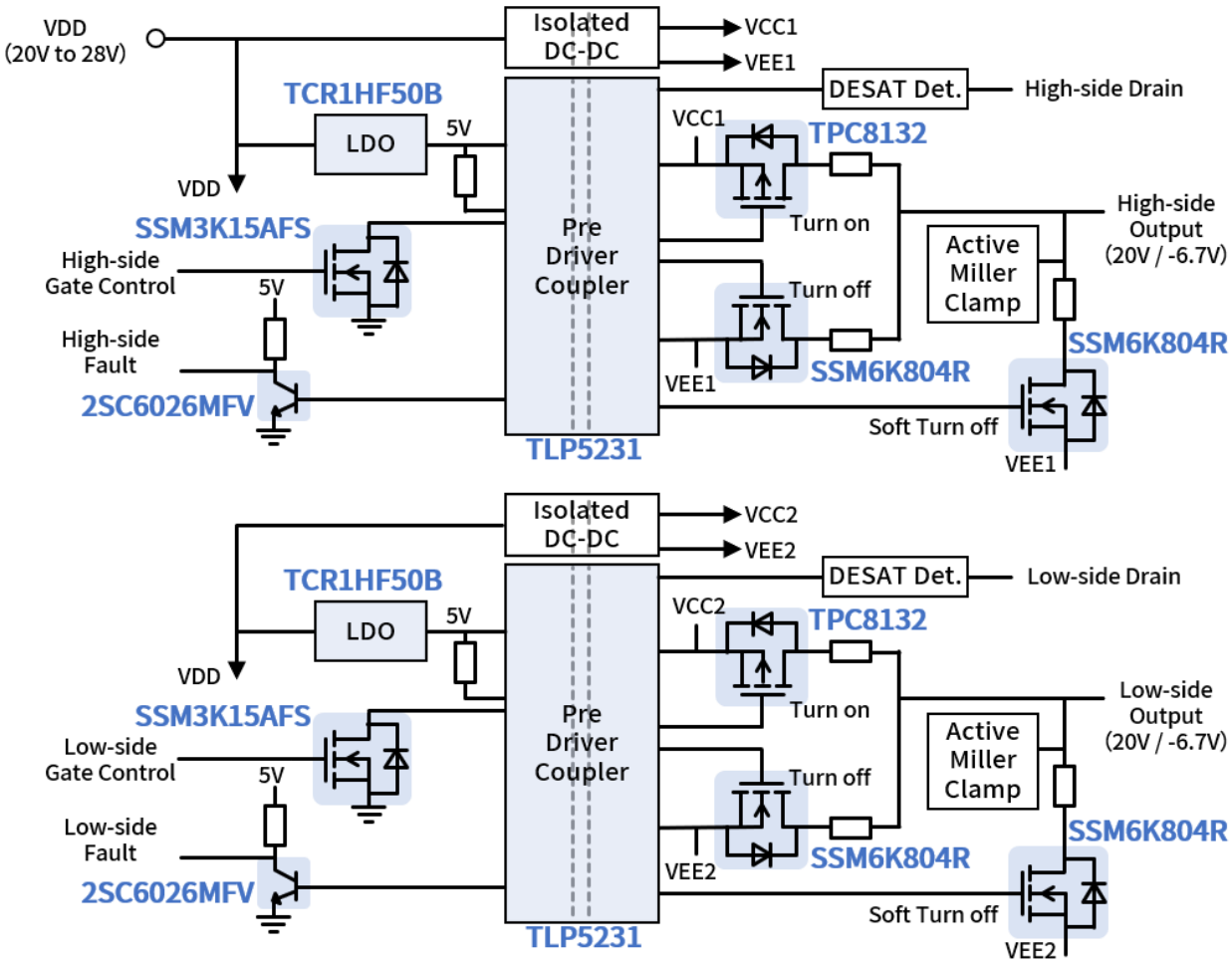

Fig. 4.1 Gate Driver Block Diagram for SiC MOSFET Module

4.2. Gate Control Circuit (Primary Side of TLP5231)

Fig. 4.2 shows the circuit of the primary side (input side) of TLP5231. (NM stands for Not Mounted, not installed)

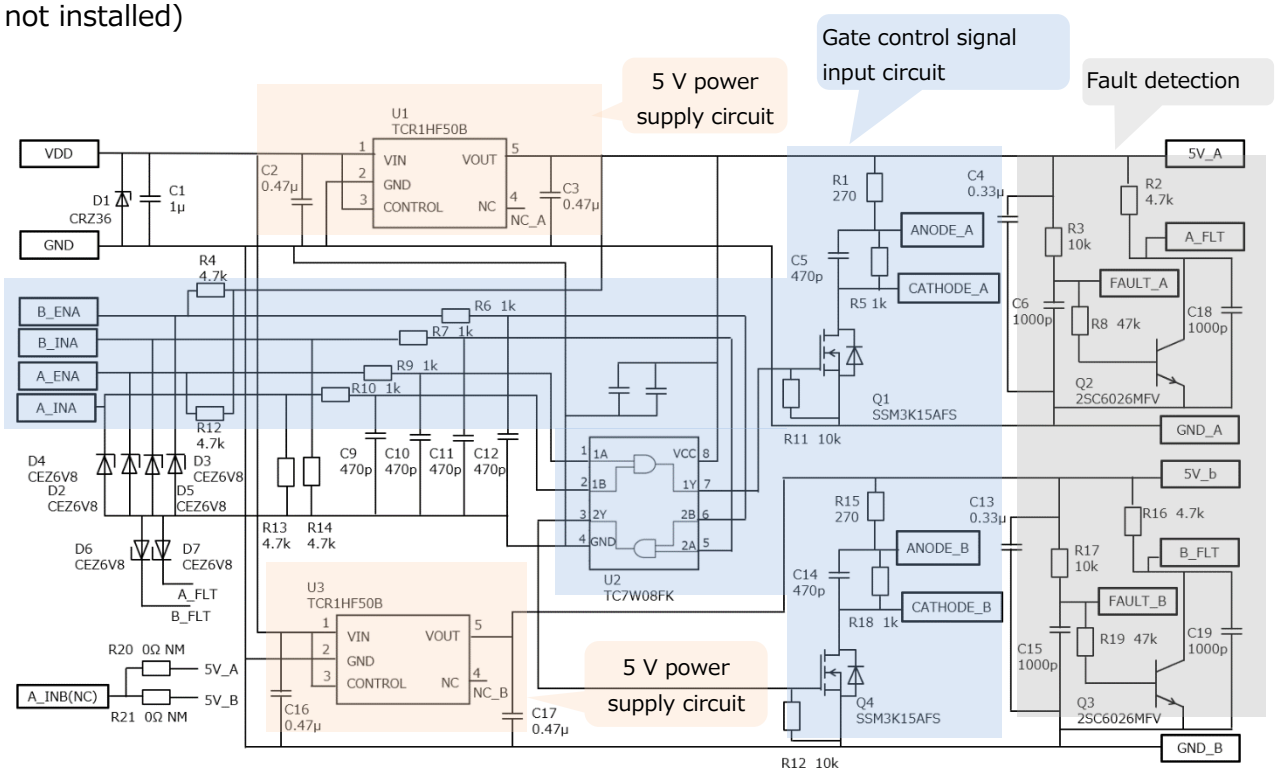

Fig. 4.2 Primary Control Circuit

4.2.1. 5V Power Supply Circuit

Fig. 4.3 shows 5V power supply circuit. It uses TCR1HF50B LDO regulators (U1, U3) to produce 5V from VDD.

The 5V output of TCR1HF50B is supplied to the primary-side power supply input V_{CC1} of TLP5231(U300, U400), the gate-control-signal input circuit, and the fault-detection output circuit. There is no problem if a common TCR1HF50B is used as a power supply for the high-side and low-side drives, but separate TCR1HF50B are used for each high-side and low-side to distribute the losses.

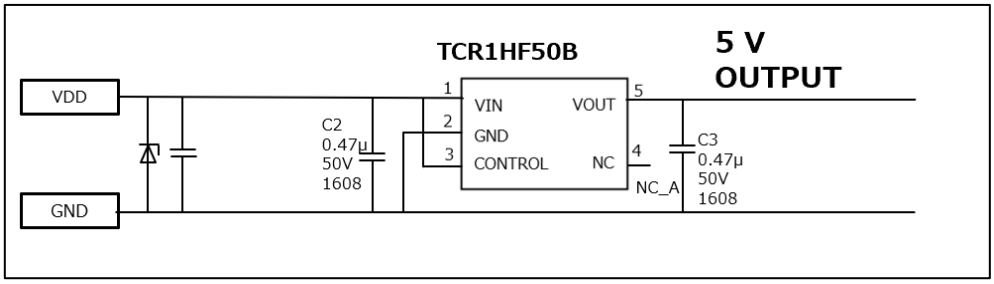

Fig. 4.3 TCR1HF50B (LDO Regulator) Circuit

4.2.2. Gate Control Signal Input

Fig. 4.4 shows the gate control signal input circuit.

A_INA (input signal) and A_ENA (enable) are the gate control signal inputs for the high side. A_ENA can control enable/disable of gate drive output. When enabled, the A_ENA signal is High and when disabled A_ENA signal is Low. When A_ENA is open, it is enabled because it is pulled up by the internal circuit. A_INA and A_ENA are input to TC7W08FK (AND circuit), and the output 1Y is input to the gate of MOSFET Q_1. When both A_INA and A_ENA are H (the output 1Y is H), the MOSFET Q_1 turns on and an input on-current $I_{F(ON)}$ flows between ANODE_A and CATHODE_A of TLP5231 for the high-side. This $I_{F(ON)}$ activates the high-side SiC MOSFET module. When 1Y is Low, there is no I_F flow between ANODE_A and CATHODE_A, so SiC MOSFET module is disabled.

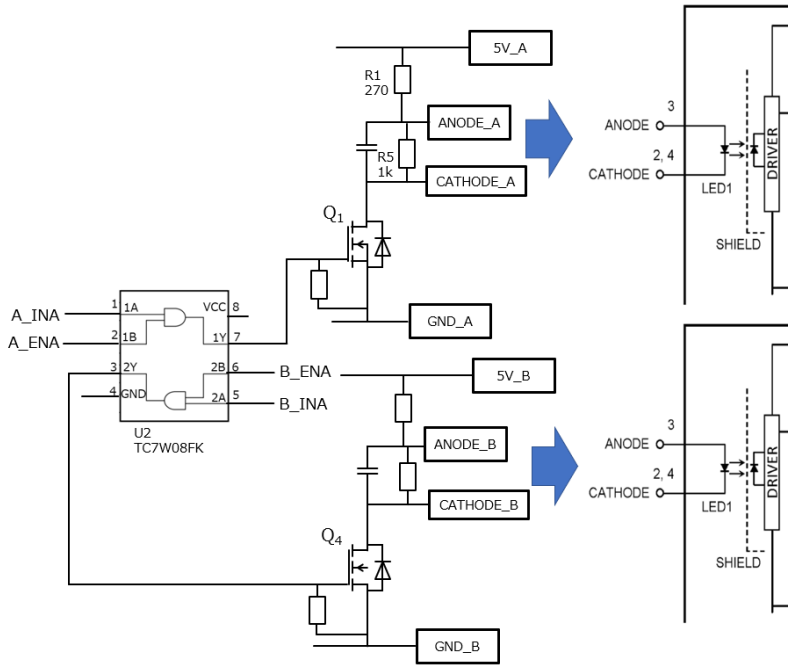

Fig. 4.4 Gate Control Signal Input Circuit

I_F (LED input forward current) between the primary anode and TLP5231 is expressed by the following equation:

$$I_F = \frac{V_{DD} - V_F}{R1} - \frac{V_F}{R5} \qquad (4-1)$$

To set I_F of TLP5231 equal to 11mA, the current flowing through R1 must be 12.6mA. R1 is connected to 5V power supply, and the current flowing to R5 becomes 1.6mA. The typical input forward voltage VF of TLP5231 between anode and cathode is 1.58V. Now, R1 and R5 are determined by the following equations.

$$R1 = \frac{V_{DD} - V_F}{12.6mA} = \frac{5V - 1.58V}{12.6mA} \fallingdotseq 271\Omega$$

$$R5 = \frac{V_F}{1.6\ mA} = \frac{1.58\ V}{1.6\ mA} \fallingdotseq 988\Omega$$

In the actual circuit, R1 of 270Ω and R5 of 1000Ω are selected to be close to the values calculated above.

The I_F can be calculated using these resistance values as follows.

$$I_F = \frac{5V - 1.58V}{270\Omega} - \frac{1.58V}{1000\Omega} = 11.08mA$$

The gate control signal input B_INA (input signal) and B_ENA (enable) for the low side also perform the same operation as the high side. Table 4.1 shows the truth table.

Table 4.1 Truth Table

A_INA (CN1:Pin7)	A_ENA (CN1:Pin9)	$I_{F(ON)}$_A	SiC MOSFET Module _A
L	L	OFF	OFF
H	L	OFF	OFF
H	H	ON	ON
L	H	OFF	OFF

Since a pull-up resistor is connected to the A_ENA terminal in this design, if the A_ENA signal is not input, it will be in the active state. A L-level input is required to set the A_ENA signal to disable state.

4.2.3. Fault Detection Output Circuit

Fig. 4.5 shows the high side fault detection output circuit.

In this design, when a high side fault (Under-voltage protection and DESAT operation) is detected in the SiC MOSFET module, the FAULT_A signal of TLP5231 is inverted and output as A_FLT signal. When a fault is detected, the FAULT_A goes to H level, the transistor Q2 turns on, and the A_FLT goes to L level. The same applies to the low side. A_FLT and B_FLT are resistor pull-up collector outputs; therefore, they allow wired OR configuration. And, according to TLP5231 sequence, when Q702 gate (V_{GMOS}) becomes L level, the normal operation is resumed, and the FLT pin goes from the L level to the H level.

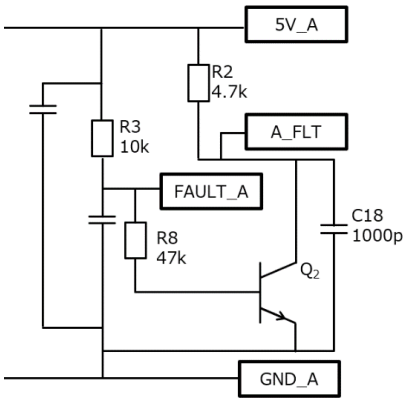

Fig. 4.5 Fault Detection Output Circuit

Table 4.2 Fault Output Truth Table

UVLO (Under Voltage Lock Out)	DESAT Detected	FLT Output (CN1:5pin,12pin)
Normal Operation	No	H Level
Under Voltage Lock Out	No	L Level
Normal Operation	Yes	L Level
Under Voltage Lock Out	Yes	L Level

4.3. Gate Drive Power Supply Circuit

Fig. 4.6 shows the high-side gate drive power supply circuit. The gate-drive power supply consists of an isolated DC-DC converter and a voltage regulator. The isolated DC-DC converter is a flyback converter that converts the control power supply voltage VDD into a positive voltage 24 V (V_{POS}-V_E) and a negative voltage -6.7V (V_{EE}-V_E). The turn-on gate-drive output voltage (V_{CC2}-V_E) is regulated from a positive voltage of 24V to 20V by the voltage regulator (U101). The turn-off gate-drive output voltage (V_{EE}-V_E) is a negative voltage -6.7V.

These gate drive output voltages are set considering the rated gate voltages and the gate switching properties of the used SiC MOSFET Module and the under voltage lock out (UVLO) detection levels of TLP5231. The same applies to the low-side gate drive power supply circuit.

To change the positive or negative voltage, UVLO operation (V_{UVLOP+}, V_{UVLON+}) of TLP5231 used in this design must be adjusted. Note that TLP5231 does not operate unless both positive and negative power supplies are aligned, during evaluation, always apply a negative power supply at less than V_{UVLON+}-6.0V (Min.) even if only the positive power supply is acceptable.

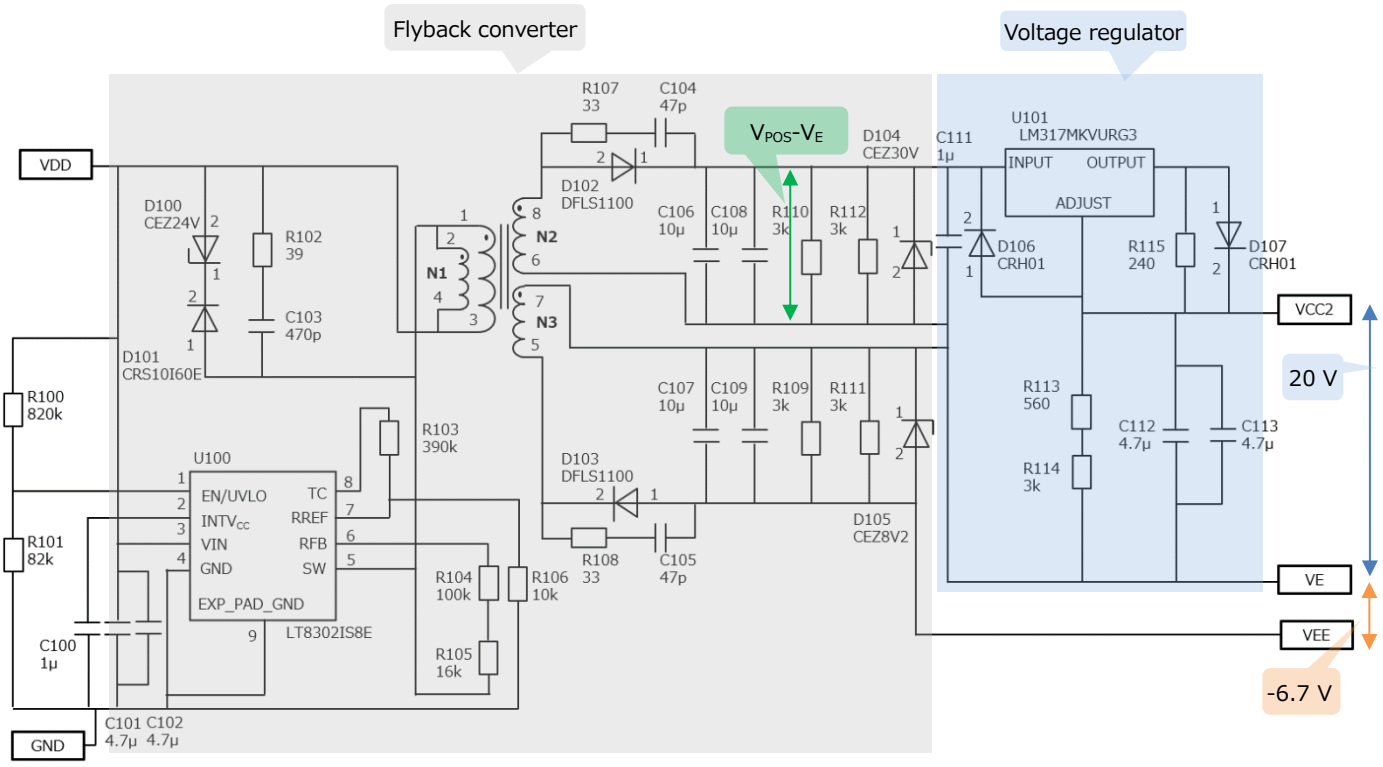

Fig. 4.6 Power Supply Circuit for Gate Drive

LT8302 is used for the control IC of the flyback converter. The output voltage can be set by the following equation using the external resistors (R104, R105, R106) and the transformer winding rate (N_{PS2}, N_{PS3}).

$$V_{POS} - V_E = V_{REF} \times \left(\frac{R104 + R105}{R106}\right) \times \left(\frac{1}{N_{PS2}}\right) - V_F$$

$$V_E - V_{EE} = V_{REF} \times \left(\frac{R104 + R105}{R106}\right) \times \left(\frac{1}{N_{PS3}}\right) - V_F$$

V_{REF} = 1.00V (LT8302 internal reference voltage)

N_{PS2}, N_{PS3} of the transformer must be adjusted to match the actual requirements. The winding ratios of this design are shown in Table 4.3.

Table 4.3 Winding Ratios of Transformer

	Voltage	Winding Ratio
Positive voltage	24V	N_{PS2} = 0.5 (N1:N2)
Negative voltage	-6.7V	N_{PS3} = 1.8 (N1:N3)

If there is an error in the measured output voltage V_E -$V_{EE\ (MEAS)}$ with respect to the target output voltage V_E -V_{EE} of the mounted resistance value (R104, R105), readjust it to the final resistance value ($R104_{(FINAL)}$, $R105_{(FINAL)}$) by using the following equation.

$$R_{104(FINAL)} + R_{105(FINAL)} = \frac{V_E - V_{EE}}{V_E - V_{EE\ \ (MEAS)}} \times R_{106}$$

In this design, R104 = 100kΩ and R105 = 16kΩ are the readjusted values.

A LM317MKVURG3 is used as the voltage regulator IC that regulates the turn-on gate-drive output voltage (V_{CC2}-V_E). V_{CC2}-V_E can be set by the following equation using the external resistors R113, R114, and R115.

In this design, V_{CC2}-V_E is set to 20V.

$$V_{CC2} - V_E = V_{REF} \times \left(1 + \frac{R113 + R114}{R115}\right) + I_{ADJ} \times (R113 + R114)$$

$$V_{CC2} - V_E = 1.25V \times \left(1 + \frac{560\Omega + 3k\Omega}{240\Omega}\right) + 50\mu A \times (560\Omega + 3k\Omega) = 20V$$

V_{REF} = 1.25V (LM317MKVURG3 internal reference voltage)
I_{ADJ} = 50μA (LM317MKVURG3 ADJUST terminal outflow current)
R113 = 560Ω, R114 = 3kΩ, R115 = 240Ω

4.4. Gate Drive Circuit (Secondary Side of TLP5231)

Fig. 4.7 shows the high-side gate drive circuit.

The gate drive circuit consists of buffer MOSFETs (Q700, Q701 for high-current gate drive), gate resistors for controlling turn-on/turn-off, a DESAT detection circuit, and a combination of resistors and a soft turn-off MOSFET for short-circuit protection.

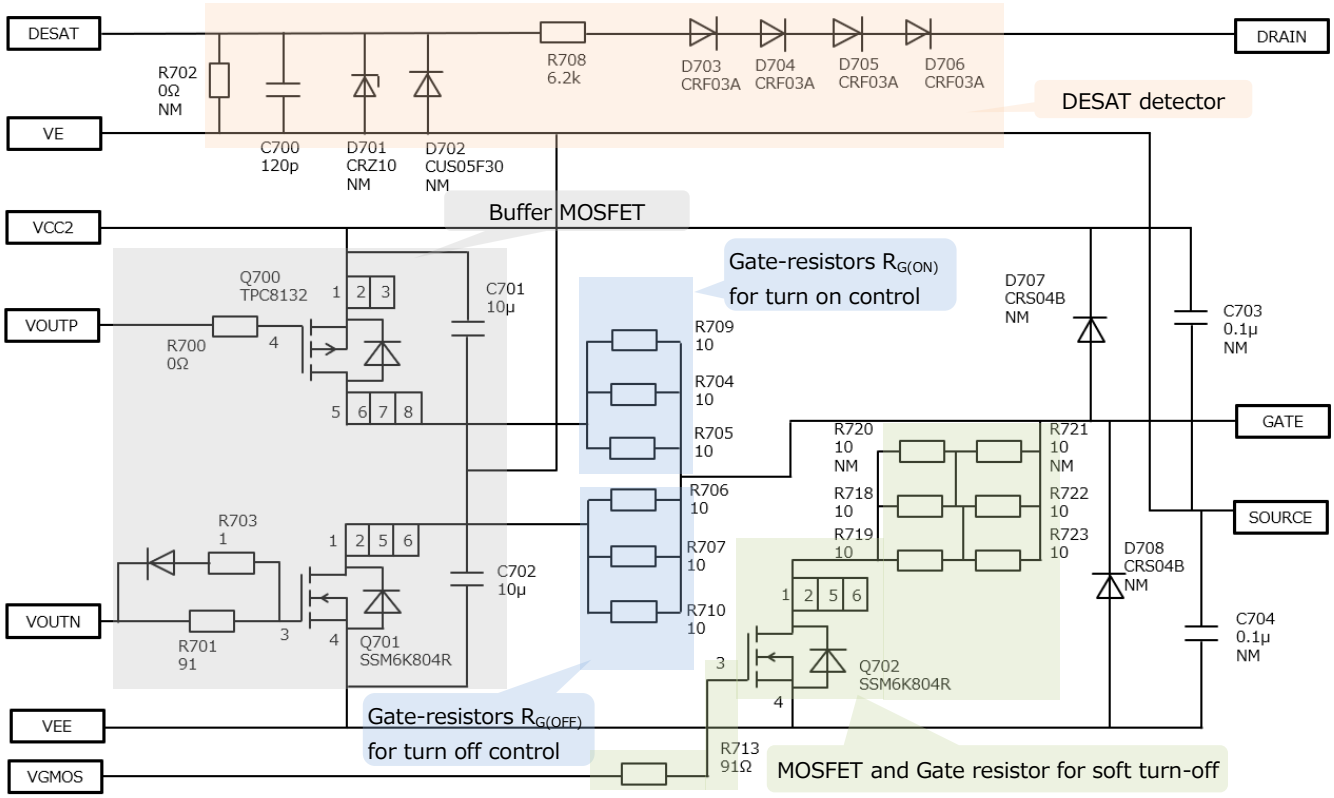

Fig. 4.7 Gate Drive Circuit

When an input on-current $I_{F(ON)}$ flows due to the gate control signal input, the V_{OUTP} output becomes Low (V_{OUTN} is Low) and the buffer P-ch MOSFET Q700 is turned on to charge the gate of the SiC MOSFET module and turn on the SiC MOSFET.

If the input on-current $I_{F(ON)}$ does not flow, the V_{OUTN} output becomes High (V_{OUTP} is High) and the buffer N-ch MOSFET Q701 is turned on to discharge the gate of the SiC MOSFET module and turn off the SiC MOSFET.

4.4.1. Buffer MOSFET

The MOSFETs used as the buffer MOSFETs are shown below.

P-ch MOSFET: TPC8132 (V_{DSS} = 40V, I_D = -7A (DC), I_{DP} = -28A (Pulse))

N-ch MOSFET: SSM6K804R (V_{DSS} = 40V, I_D = 12A (DC), I_{DP} = 50A (Pulse))

The gate-drive average current I_{CHG_SiC} in this design is 0.185A, and the gate drive peak current I_{CHG_PEAK} is 9.9A. The current capability of the selected buffer MOSFET is sufficient to drive the gate.

● Gate-drive average-current I_{CHG} calculation

The gate charge (Q_g) of our Dual SiC MOSFET module (MG600Q2YMS3) is estimated to be 1.85μC with V_{GS} change of -6.7 V to 20 V from Fig. 4.8.

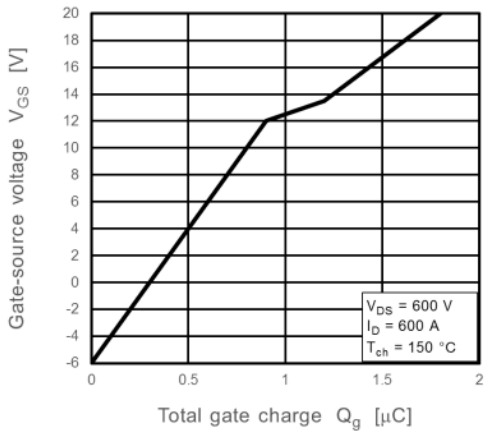

Fig. 4.8 Total Gate Charge

From the following equation, the mean charge current required for gate-drive is 0.093A.

$$I_{CHG\_SiC} = Q_G \times f_{SW} = 1.85\mu C \times 50kHz = 0.093A$$

f_{SW} = 50kHz (Gating control signal frequency)

If the SiC MOSFET module MG400V2YMS3 is used, I_{CHG_SiC} is 0.093A. (Same as MG600Q2YMS3)

● Calculation of gate-drive peak current $I_{CHG\_PEAK\_MAX}$

To calculate the maximum peak current $I_{CHG\_PEAK\_MAX}$ required for gate drive, the gate resistor $R_{G(ON)}$ is considered 0Ω.

From equation (4-1) below, $I_{CHG\_PEAK\_MAX}$ becomes 9.9A. The on-resistance of the gate-drive buffer MOSFET in this design is neglected because it is very small compared to r_{ig}.

$$\boldsymbol{I_{CHG\_PEAK\_MAX} = \frac{V_{GS}}{r_{ig} + R_{G(ON)}} = \frac{26.7V}{2.7\Omega + 0\Omega}} \qquad (4-1)$$

$V_{GS} = V_{CC2} - V_{EE}$ = 20V − (-6.7V) = 26.7V

Inner-gate resistance of r_{ig} = 2.7Ω (MG600Q2YMS3)

If the SiC MOSFET module MG400V2YMS3 is used, $I_{CHG\_PEAK\_MAX}$ is 7.6A.

4.4.2. External Gate Resistor Setting

The gate drive circuit is shown in Fig. 4.9. The current path differs for turn-on and turn-off. Different gate resistor value settings are possible for turn-on and turn-off. The gate resistors are determined by considering the turn-on/turn-off times and resistance-loss based on Qg of SiC MOSFET module. In this design, the turn-on and turn-off gate resistors are set to 3.3Ω (10Ω 3 parallel, 1W, 1632 metric). From Equation (4-1), the gate-drive peak current I_{CHG_PEAK} with gate resistor $R_{G(ON)}$=3.3Ω is 4.45A.

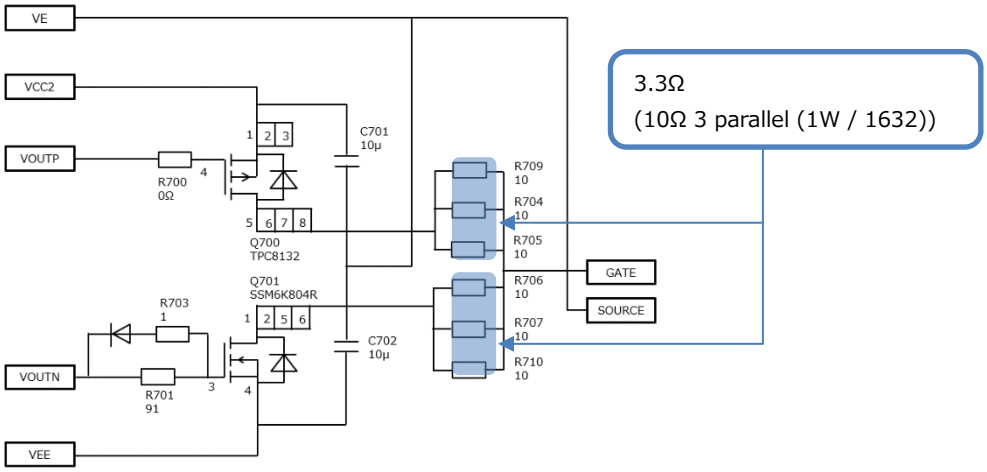

Fig. 4.9 Gate Drive Circuit

We evaluated MG600Q2YMS3 (V_{DS} ≦ 800V, I_D ≦ 600A), MG400V2YMS3 (V_{DS} ≦ 1200V, I_D ≦ 400A), MG250YD2YMS3(V_{DS} ≦ 1200V, I_D ≦ 250A) in this design. When designing an actual product, take the safety standard into consideration. The following table shows the measured results using MG600Q2YMS3.

<Turn-on/Turn-off result>
Measuring conditions: V_{DS} = 800V, I_D = 600A, lead-load 100µH, $R_{G(ON)}$ = $R_{G(OFF)}$ = 3.3Ω, Ta = 25°C

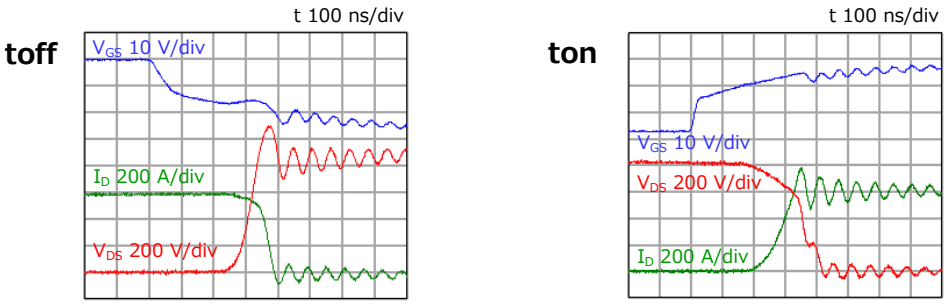

Fig. 4.10 Turn-On/Turn-Off Waveform

<Gate Resistance Loss Characteristics (Calculation)>

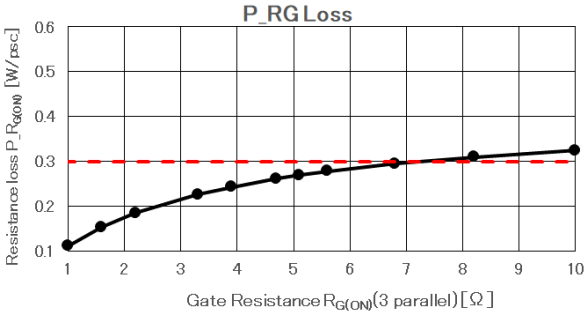

Fig. 4.11 Resistance Loss Characteristics

The calculation the loss $P\_R_{G(ON)}$ for each turn-on gate resistor $R_{G(on)}$ is as shown below. The on-resistance of the gate-drive buffer MOSFET is ignored because it is very small compared to r_{ig}.

$P\_R_{G(ON)} = R_{G(ON)}/(R_{G(ON)} + r_{ig}) \times P_{GATE\_ON}/$(Number of Parallel resistors)

$= R_{G(ON)}/ (R_{G(ON)}+2.7\Omega) \times 2.47W / 3 = 0.23W$

$P_{GATE\_ON} = 1/2 \times V_{GS} \times Q_g \times f_{SW}$ (turn-on charging energy)

r_{ig}: 2.7Ω MG600Q2YMS3 internal resistance

V_{GS}:26.7V VCC2-VEE = 20V-(-6.7V) = 26.7V

Q_g:1.85uC (from MG600Q2YMS3 datasheet)

f_{SW}:50 kHz gate-drive frequency

The turn-off gate-resistor $R_{G(off)}$ is also calculated in the same way.

<Switching loss result>

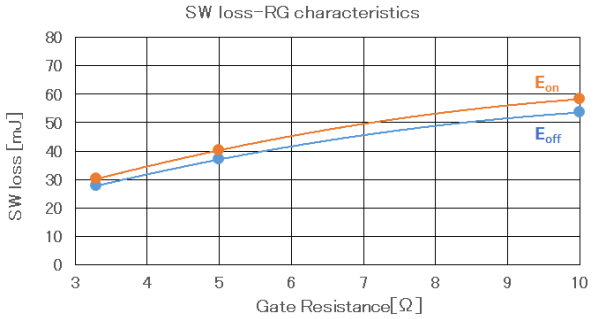

Fig. 4.12 Switching Loss Characteristics

<Switching time result>

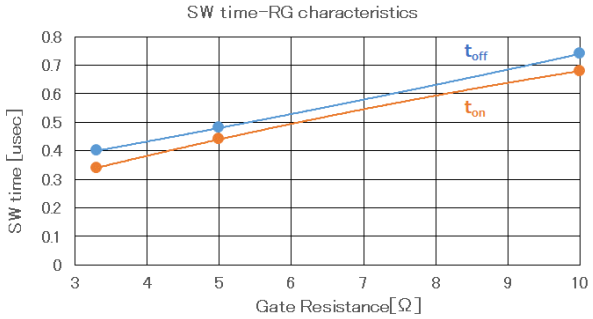

Fig. 4.13 Switching Time Characteristics

<V_{DS} surge voltage result>

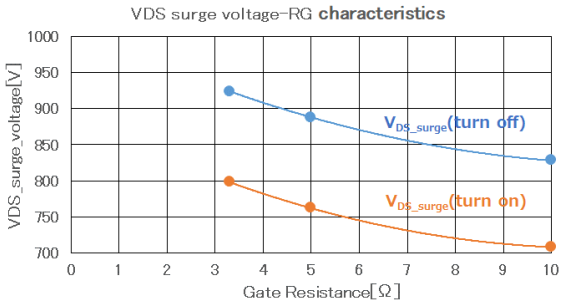

Fig. 4.14 V_{DS} Surge Voltage Characteristics

If the gate resistance is derated 30% with respect to the rated 1W, the gate resistance must be adjusted to be less than or equal to 0.3W. However, if the gate resistance is reduced, the switching-time is shortened and V_{DS} surge voltage is increased. And if the gate resistance is increased, the resistance loss and switching loss increases, resulting in heat generation. When adjusting the gate resistor according to the actual specifications, take into account the heat generation, switching loss,

V_{DS} surge voltage, etc. of the respective components. Refer to the data sheet of the power device to be used (e.g. SiC MOSFET Module) and the related documentation to select the gate resistance value.

4.5. Protection Circuit

4.5.1. DESAT (Desaturation) Detection Circuit Operation

DESAT detect function is designed to protect SiC MOSFET module from being damaged by excessive current. It is done by using the DESAT terminal which monitors the drain-source voltage (V_{DS}) of SiC MOSFET module.

If an abnormal high current flows into the drain current (I_D) of SiC MOSFET module, V_{DS} increases along with I_D according to the static characteristic curve of Drain Current (I_D) and Drain Source-to-Source Voltage (V_{DS}). If the V_{DS} monitored by the DESAT terminal exceeds the threshold voltage V_{DESAT} (TLP5231 V_{DESAT} 8.0 V default), the SiC MOSFET module operation is stopped, and the fault signal is output from FLT terminal of the connector CN1.

DESAT detection method does not allow direct monitoring of the drain current (I_D), and therefore, accuracy cannot be increased. However, it is a relatively simple configuration and is used for an emergency-stop when a large current occurs.

Fig. 4.15 shows the current loop used for monitoring DESAT.

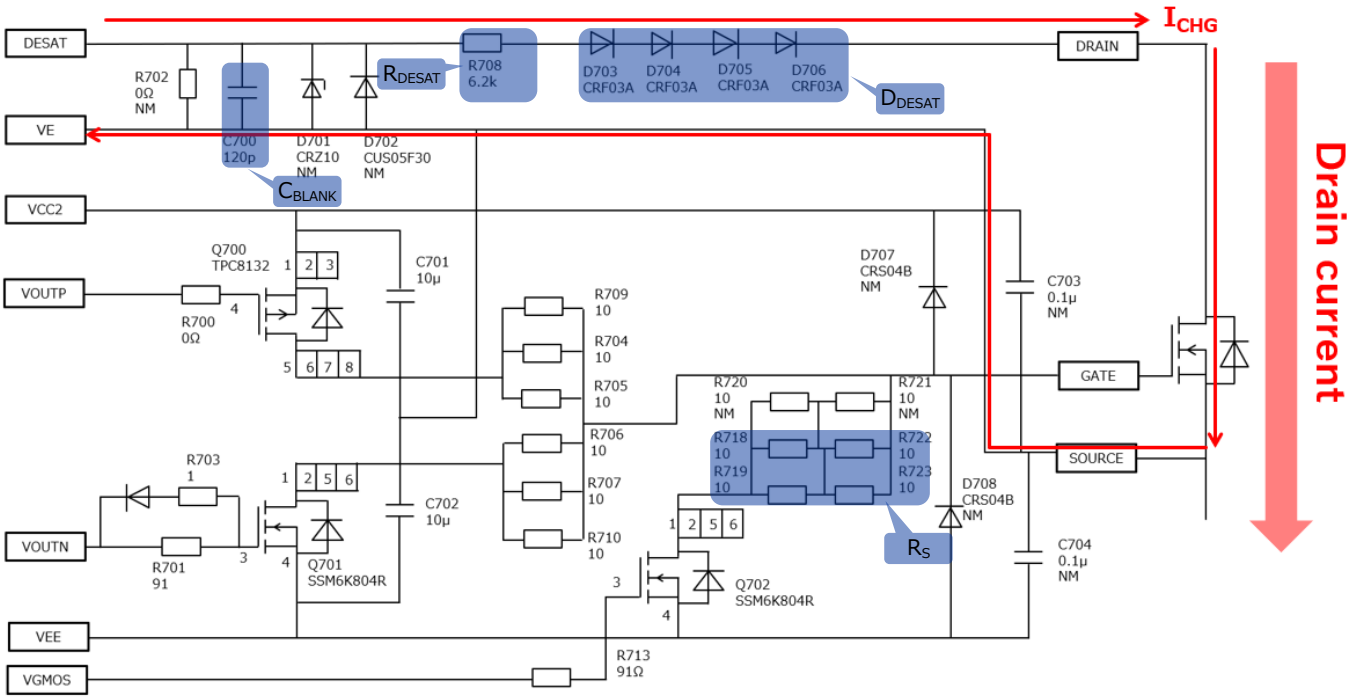

Fig. 4.15 DEDAT detecting operation

When SiC MOSFET is on, DESAT terminal acts as a constant current source and outputs a blanking capacitance charging current I_{CHG} of approximately 0.5mA, and charges and the blanking capacitance C_{BLANK} connected between DESAT pin and VE pin. The voltage generated by C_{BLANK} is equal to the

sum of voltage drops when I_{CHG} flows through the resistor R_{DESAT} (R708) and the high voltage tolerant diode D_{DESAT} (D703, D704, D705, D706) and the drain-source voltage V_{DS} of SiC MOSFET module. The voltage between DESAT and V_E ($V_{DESAT(ON)}$) at that time is expressed by the following equation.

$$V_{DESAT(ON)} = V_{DS} + VF(D_{DESAT}) + I_{CHG} \times R_{DESAT}$$

$$V_{DESAT(ON)} = V_{DS} + VF(D703 + D704 + D705 + D706) + I_{CHG} \times R708$$

Since SiC MOSFET module is on, I_{CHG} is superimposed on the drain current I_D several 10A through the drain source. For this reason, the above V_{DS} is a voltage generated according to the I_D-V_{DS} static characteristic curve of the SiC MOSFET module. The voltage drop of a small current I_{CHG} is included in the voltage drop of I_D and is not visible.

V_{DS} of the normally-on SiC MOSFET module is voltage according to I_D, but V_{DS} increases when an overcurrent occurs. If V_{DS} increases and $V_{DESAT(ON)}$ exceeds DESAT threshold voltage V_{DESAT} (TLP5231 V_{DESAT} 8.0V (Typ.)), the soft turn-off MOSFET (Q702) is turned on. This is judged to be an abnormal condition. The resistive R_S connected to the drains of Q702 gently pull out the gate charge. This suppresses the spike-voltage generated between the drain and the source, and soft shutdown occurs to prevent the destruction of the SiC MOSFET module. DESAT is detected by the following equation.

$$V_{DESAT} = V_{DESAT(ON)} = V_{DS} + V_F(D703 + D704 + D705 + D706) + I_{CHG} \times R708 \qquad (4-2)$$

From equation (4-2), R708 at DESAT detection can be written as Equation (4-3).

$$R708 = \frac{\left(V_{DESAT\_MIN} - V_F(D703 + D704 + D705 + D706) - V_{DS\_MIN}\right)}{I_{CHG\_MAX}} \qquad (4-3)$$

When DESAT is detected, the value of V_{DS} is determined from the drain-source voltage (V_{DS}) and drain current (I_D) characteristics of SiC MOSFET module to be used, after first determining the abnormal current. In this design, based on MG600Q2YMS3 specifications, the minimum fault detection current I_{DESAT_MIN} when a DESAT is detected is set to I_D = 276A at T_{CH} = 25°C, and for this the V_{DS} can be read as 0.46V from Fig. 4.16. Adjust R708 so that $V_{DESAT(ON)}$ is equal to DESAT threshold V_{DESAT}.

In this design, R708 is adjusted by setting 0.46V to the lowest V_{DS_MIN} of the drain-to-source voltage V_{DS} when a DESAT is detected.

SiC MOSFET Module Drain-Source V_{DS_MIN}: 0.46V (Min.)
DESAT Threshold V_{DESAT_MIN}: 7.5V (Min.)
Blanking Capacitance Charge Current I_{CHG_MAX}: 0.82mA (Max.)
High Voltage Diode D_{DESAT} (D703～D706) Forward Voltage V_F: 1.96V (Typ.)

$$R708 = \frac{(7.5V - 1.96V - 0.46V)}{0.82mA} = 6200\Omega$$

R708 is selected as 6.2kΩ and therefore the lowest DESAT detection V_{DS} is approximately 0.46V and I_D is 276A. Kindly do appropriate design according to the actual specifications and then do enough evaluation of the real circuit.

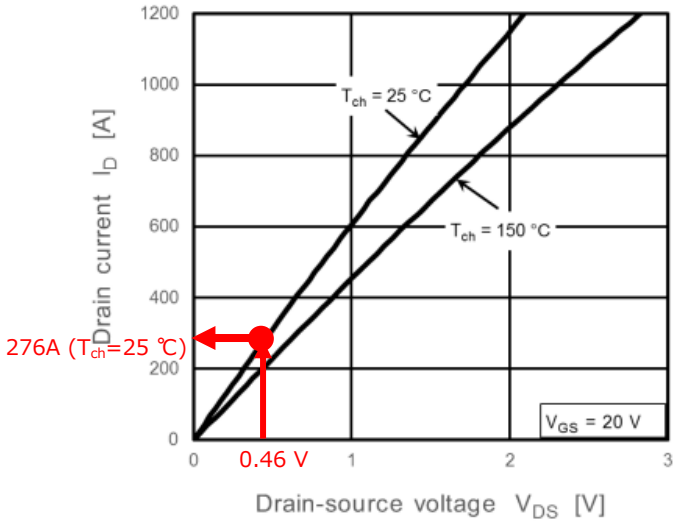

Fig. 4.16 I_D-V_{DS} Characteristic

DESAT terminal is connected to the drain terminal of SiC MOSFET module through a high-voltage diode (D_{DESAT}). If the drain voltage of SiC MOSFET module fluctuates due to external noises while SiC MOSFET module in ON, DESAT voltage may fluctuate. If DESAT voltage fluctuation exceeds DESAT threshold (8.0V Typ.), the protection operation will be initiated and the soft shutdown of the SiC MOSFET module will occur. Since the noise generated by the high-voltage inverter circuit is large, a blanking capacitor C_{BLANK} (C700) is added to form a low-pass filter.

A trade-off due to the addition of this C_{BLANK} (C700) is the blanking time t_{BLANK} in which $V_{DESAT(ON)}$ reaches V_{DESAT} when a short-circuit fault occurs.

The blanking-time t_{BLANK} is given by the following equation:

$$t_{BLANK} = \{C_{BLANK} \times (V_{DESAT} - V_{DESAT(ON)})\} / I_{CHG}$$

$$t_{BLANK} = \{C700 \times (V_{DESAT} - V_{DS} - VF(D703 + D704 + D705 + D704) - I_{CHG} \times R708)\} / I_{CHG} \qquad (4-4)$$

After the blanking time t_{BLANK}, the soft shutdown of SiC MOSFET module occurs. The gate-voltage V_G at soft shutdown decreases exponentially over time, as shown by the following equation:

$$V_G = (V_{CC2} + |V_{EE}|) \times \exp\left(\frac{-t}{C_{in} \times R_S}\right) - |V_{EE}|$$

If the time to fall to $V_{G(OFF)}$ is set to be the soft turn-off time t_{STO}, the following equation is used.

$$t_{STO} = -C_{in} \times R_S \times \ln\left(\frac{V_{G(OFF)} + |V_{EE}|}{V_{CC2} + |V_{EE}|}\right) \quad (4-5)$$

t_{STO} can be adjusted with the resistance value of Rs (consisting of R718 to R723).

The t_{DESAT_TOTAL} from the time of fault to the time of soft shutdown is the sum of t_{BLANK}, t_{STO}, and $t_{DESAT(FILTER)}$.

$$t_{DESAT\_TOTAL} = t_{BLANK} + t_{STO} + t_{DESAT(FILTER)} \quad (4-6)$$

In this design, the maximum blanking time t_{BLANK_MAX} is used to calculate the maximum $t_{DESAT\_TOTAL\ (Max)}$ to be 2.86μs from the following equation. V_{DS} is set to V_{DS}=0.46V during normal operation.

$t_{DESAT\_TOTAL(MAX)} = \{120\text{pF} \times (9.0\text{V} \quad - 0.46\text{V} - 1.96\text{V} - 0.29\text{mA} \times 6.2\text{k}\Omega)\} / 0.29\text{mA} - 53\text{nF} \times 10\Omega \times \ln\left(\frac{2\text{V}+|-6.7\text{V}|}{20\text{V}+|-6.7\text{V}|}\right) + 0.29\mu\text{s} = 1.98\mu\text{s} + 0.594\mu\text{s} + 0.29\mu\text{s} = 2.86\mu\text{s}$

Blanking capacitance C_{BLANK}: 120pF
DESAT threshold V_{DESAT}: 9.0V (Max.)
Blanking capacitance Charge Current I_{CHG}: 0.29mA (Min.)
Input capacitance C_{in}: 53nF for SiC MOSFET Modules (MG600Q2YMS3) (Typ.)
Drain resistance R_S of MOSFET for soft turn-off: 10Ω (Typ.) (R718, R719, R722, R723:10Ω, 2 series in 2 parallel, R720, R721: not mounted)
Positive power supply voltage V_{CC2}: 20V (Typ.)
Negative power supply voltage V_{EE}: -6.7V (Typ.)
SiC MOSFET Module (MG600Q2YMS3) Gate Threshold Voltage $V_{G(OFF)}$: 2V (Set to a value less than 3.6V)

Note that the capacitance of the pins of the protective diodes which are connected in parallel to the blanking capacitor C_{BLANK} (C700) will affect t_{BLANK}.

C_{BLANK} (C700) and R_{DESAT} (R708) must be adjusted carefully because they also affect V_{DS} of SiC MOSFET module and the noise tolerance of DESAT terminal (CR filter parameter) when DESAT is detected. Depending on actual use conditions, if the parasitic inductance (Ls) of the electric wiring generates a large surge voltage when the current is cut off and exceeds the component rated voltage, it may result in damage. To reduce the surge-voltage caused by Ls, the snubber circuit must be connected as close as possible to SiC MOSFET module. Verify DESAT detection operation sufficiently using an actual device.

4.5.2. UVLO Function (Under Voltage Lock Out)

TLP5231 incorporated in this design has a built-in UVLO function. The voltages of the positive power supply (V_{CC2}–V_E) and the negative power supply (V_E–V_{EE}) on the secondary side are monitored. When the positive voltage is lower than the UVLO threshold voltage (V_{UVLOP-}), or if the negative voltage is more than the UVLO threshold voltage (V_{UVLON-}), the operation is stopped. When the positive power supply voltage exceeds V_{UVLOP+} and the negative power supply voltage drops below V_{UVLON+}, normal operation is resumed. This function prevents SiC MOSFET module from passing current between the drain/source at inadequate gate voltage. It is intended to prevent damage due to overheating. Note that TLP5231 does not operate unless both the positive and negative power supplies are aligned, so be sure to apply a negative power supply even if only the positive power supply is acceptable. UVLO takes precedence over all functions because TLP5231 starts operation after UVLO is released.

Positive power supply voltage undervoltage protection (UVLO_P)

When the positive power supply voltage (V_{CC2}–V_E) on the secondary side of TLP5231 drops below the threshold voltage V_{ULVOP-}, the gate drive output is stopped, and FLT pins (pins 5 and 12 of CN1) of this design go from H level to L level. When the positive power supply voltage (V_{CC2}–V_E) on the secondary side rises above the threshold voltage V_{ULVOP+}, the gate drive output is enabled, and FLT pins go from L level to H level (only when the negative power supply voltage is below the UVLO threshold).

Negative power supply voltage undervoltage protection (UVLO_N)

When the negative supply voltage (V_E–V_{EE}) on the secondary side of TLP5231 rises above the threshold voltage V_{ULVON-}, the gate drive output is stopped, and FLT pins (pins 5 and 12 of CN1) of this design go from H level to L level. When the negative power supply voltage (V_E–V_{EE}) on the secondary side drops below the threshold voltage V_{ULVON+}, the gate-drive output is enabled, and FLT pins go from L level to H level (only when the positive power supply voltage is above the UVLO threshold).

Table4.4 shows UVLO threshold voltages.

Table 4.4 UVLO Threshold Voltages

UVLO_P threshold	V_{UVLOP+}	13 V (Typ.)
	V_{UVLOP-}	12 V (Typ.)
UVLO_N threshold	V_{UVLON+}	-5.3 V (Typ.)
	V_{UVLON-}	-5.0 V (Typ.)

4.5.3. Active Miller Clamp (AMC)

In a bridge configuration in which devices are connected in series at the top and bottom, when one of the devices turns on, then the voltage across its drain and source changes quickly (higher dV/dt). This will lead to current flow from drain to gate of another device via its drain to gate capacitance (C_{DG}), which can cause the gate voltage to rise and turn on the MOSFET accidently. This is a malfunction called as self-turn on. Active Miller Clamp (AMC) is a function that prevents this malfunction.

Fig. 4.18 shows AMC operation of this design, and Fig. 4.19 shows the operation waveforms. When the gate control signal of this design goes to L level (V_{OUTN} goes to H level), the gate voltage of SiC MOSFET module drops, the MOSFET for AMC turns on, and the gate voltage is clamped to negative voltage (V_{EE}) without using the gate resistor $R_{G(OFF)}$. Through these measures, self-turning on can be prevented by controlling the rise of the gate voltage.

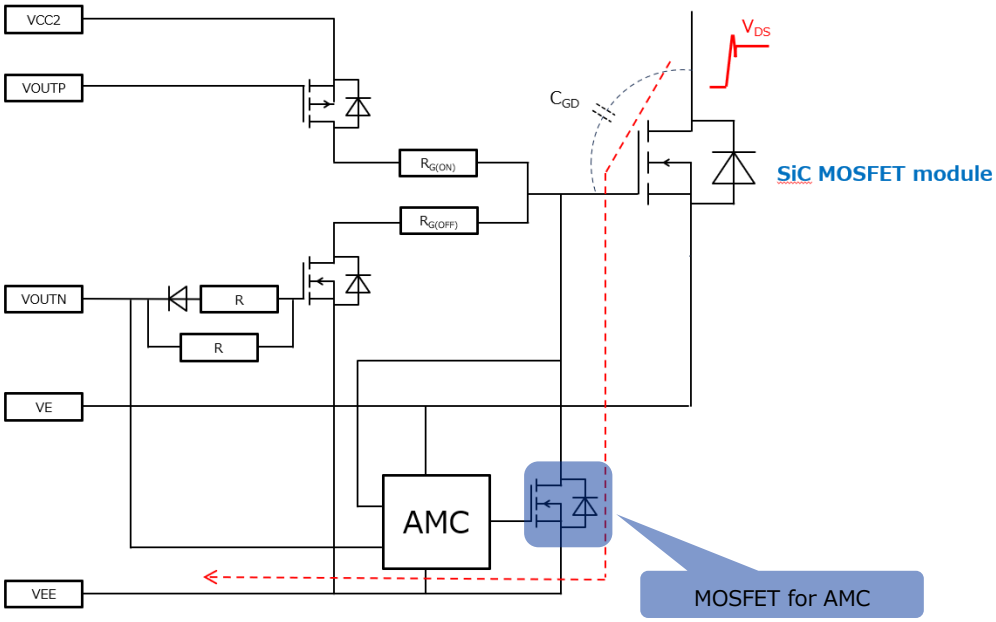

Fig. 4.18 Active Miller Clamp Operation

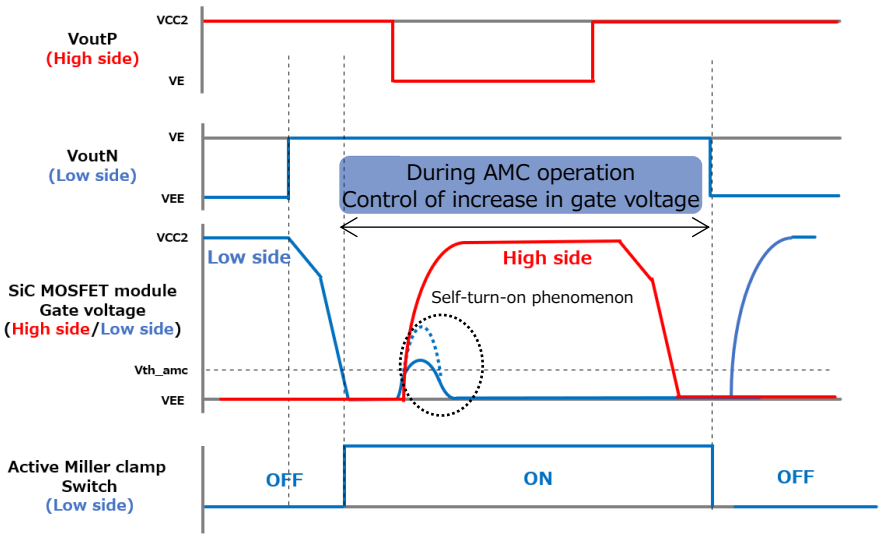

Fig. 4.19 Active Miller Clamp Operation Waveform Image

4.6. Temperature Detection Output

The connector (CN1) of this design provides a connection pin which is connected to the thermistor output built into SiC MOSFET module. It can be used to monitor the temperature of the SiC MOSFET module. This design is not equipped with a temperature detection circuit; therefore, the user can add an external detection circuit if necessary. Refer to the Table 3.3 for the rated resistance and the B constant of the thermistor in SiC MOSFET module MG600Q2YMS3.

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