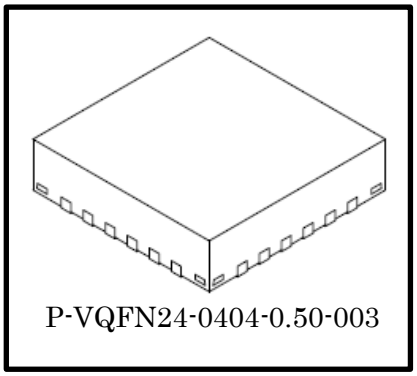
CDMOS Linear Integrated Circuit Silicon

TB9103FTG

Automotive 1-channel H-bridge(2-channel half-bridge) gate driver

1. OUTLINE

TB9103FTG is 2-channel half-bridge gate driver for automotive applications. It can also be used as 1-channel H-bridge gate driver. It can realize low power consumption in sleep mode. Having various fault detection functions, the product shuts down the gate drive and notifies faults from the DIAG terminals (open drain).



P-VQFN24-0404-0.50-003

Weight: 0.04g (typ.)

2. APPLICATIONS

Used in combination with an N-channel MOSFET, TB9103FTG is suitable for latching motor applications such as sliding doors and back doors, as well as drive motor applications such as seats and windows, which are used in automobiles.
In addition, the product is suitable for migrating motor control parts from mechanical relays to semiconductors.

3. FEATURES

- Equipped with two control modes: Half-bridge mode, H-bridge mode
- Can be used as 2-channel independent half-bridge.
  - Dead time control and shutdown control for each channel
- Can be used as H-bridge by combining half-bridges.
  - Dead time control and shutdown control as H-bridge
- Low power sleep mode
- Equipped with various fault detections:
  - VB low voltage detection, VCC low voltage detection, VCP high voltage detection
  - Gate-source voltage detection, gate voltage fault shutdown
  - Drain-source voltage detection (can set detection levels), overcurrent shutdown
  - Overheat detection, shutdown
  - Notification from the open-drain output terminal when a fault is detected.
- Operating voltage range: 7-18 V
- AEC-Q100 Rev-J (will conform to): Grade 1
- Small package (VQFN24: 4 mm square)

Start of commercial production
2025-02

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4. BLOCK DIAGRAM

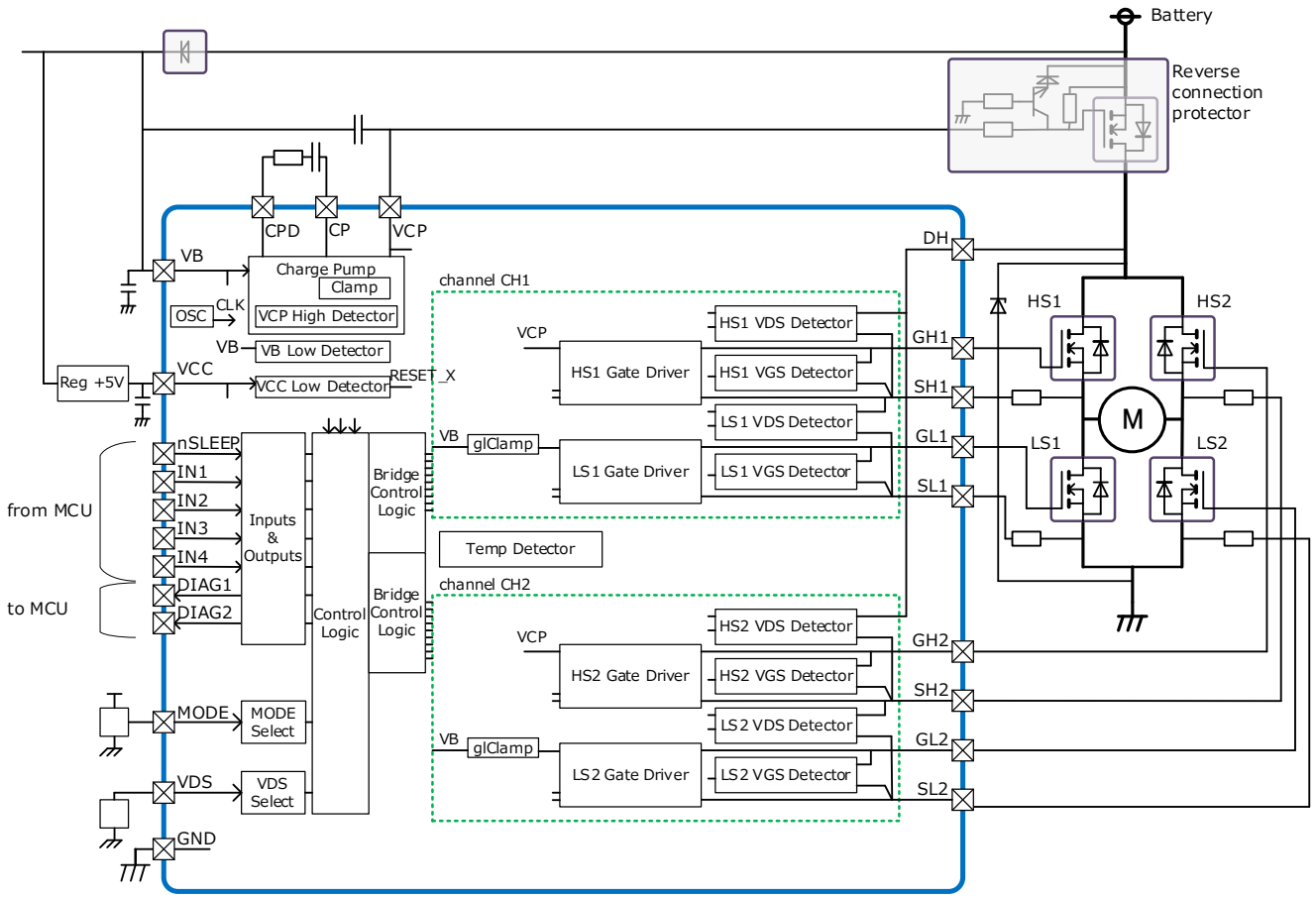


Fig. 1 TB9103FTG functional block diagram

5. TERMINAL LAYOUT

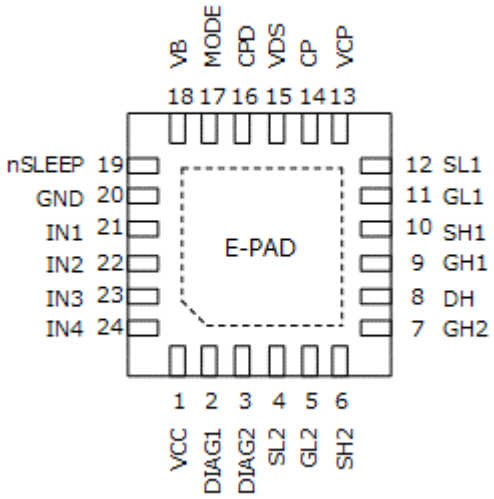


Fig. 2 Terminal layout (top view)

6. TERMINALS

Table 1 Terminals

No.	Name	I/O	Description
1	VCC	-	This is a power supply terminal of the IC.
2	DIAG1	OUT	This is an output terminal of the diagnostic outcome by the fault detection function.
3	DIAG2	OUT	This is an output terminal of the diagnostic outcome by the fault detection function.
4	SL2	IN	This is a standard terminal of the gate driver for LS2 low-side FET.
5	GL2	OUT	This is a standard terminal used for VDS detection of LS2 low-side FET.
6	SH2	IN	This is an output terminal of the gate driver for LS2 low-side FET.
7	GH2	OUT	This is a standard terminal of the gate driver for HS2 high-side FET.
8	DH	IN	This is a monitor standard terminal used for VDS detection of HS2 high-side FET.
9	GH1	OUT	This is an output terminal of the gate driver circuit for HS2 high-side FET.
10	SH1	IN	This is a standard terminal used for VDS detection of HS1 and HS2 high-side FETs.
11	GL1	OUT	This is an output terminal of the gate drive signal for HS1 high-side FET.
12	SL1	IN	This is a source terminal voltage of HS1 high-side FET.
13	VCP	-	This is a gate drive signal output terminal of LS1 low-side FET.
14	CP	-	This is the input terminal of the standard potential used for VDS detection of LS1 low-side FET.
15	VDS	IN	This is a power supply terminal of the IC. It is the final input/output terminals of the charge pump circuit.
16	CPD	-	Connect it to the smoothing capacitor.
17	MODE	IN	This is a power supply terminal of IC. It is the boosting terminal for the charge pump circuit.
18	VB	-	This is a voltage input terminal for setting the detection voltage of VDS detection.
19	nSLEEP	IN	This is a power supply terminal of the IC. It is the drive output terminal of the charge pump circuit.
20	GND	-	This is a voltage input terminal that sets the bridge operation mode.
21	IN1	IN	This is a power supply terminal of the IC. Apply the battery voltage.
22	IN2	IN	This is a voltage input terminal that sets the IC into sleep mode. Setting the voltage to logic level Low will make the IC enter sleep mode.
23	IN3	IN	This is a GND terminal.
24	IN4	IN	This is the logic level signal input terminal 1 that controls the ON/OFF of the power FET composing the bridge.

7. FUNCTIONAL OPERATIONS

Table 2 shows the operating states that TB9103FTG may assume.

TB9103FTG goes into reset state when VCC detects low voltage.

When VCC is a normal voltage and the nSLEEP pin is Low, TB9103FTG goes into sleep state, and the operation of each part stops.

In sleep state, the DIAG output goes into High-Z state, but the latch that stores abnormal state keeps its value without initializing it. The DIAG output operates according to the abnormal states when sleep state is released. After indicating the sleep state, keep it in the sleep state for at least the tSLEEP time.

After shifting to the normal operation state, TB9103FTG checks the MODE terminal and sets an operation mode, half-Bridge or H-Bridge. The condition to hold the operation mode setting is when the "Reset release state and the sleep release state (nSLEEP = High)" are established at the same time.

At the time of reset or sleep state, set all of nSLEEP, IN1, IN2, IN3, and IN4 to Low.

During the tWAKE period after releases, set IN1, IN2, IN3, IN4 to Low ("High-Z").

The gate drive section receives the MCU instructions from IN1, IN2, IN3, and IN4 and makes the gate output (GH1, GL1, GH2, and GL2) according to the instructions. The gate drive section automatically confirms that both the external high-side FET and low-side FET are turned OFF every time the instructions from the MCU are changed.

Table 2 Operation state

Operation states of IC	Charge pump	Bridge Control Logic	DIAG output (DIAG1, DIAG2)	Gate output (GH1, GL1, GH2,GL2)	Operation states of the external FET
VCC drop detection release state nSLEEP=H (Sleep release state)	In operation	In operation	In operation	In operation	In operation (Operation according to gate outputs)
VCC drop detection release state nSLEEP=L (Sleep state)	In stopped state	In stopped state (Note2)	High-Z (Note1) (Note3)	RL	High-Z (OFF at both high and low sides)
VCC drop detection release state nSLEEP=H (Sleep release state)	In stopped state	In stopped state In initial state	L	RL	High-Z (OFF at both high and low sides)
VCC drop detection release state nSLEEP=L (Sleep state)	In stopped state	In stopped state In initial state	High-Z (Note3)	RL	High-Z (OFF at both high and low sides)

Explanation of symbols:
RL: Low by resistor; L: Low; H: High; High-Z: High impedance state

Note1: The internal latch that stores abnormal states retains its values.
Note2: Any instruction from IN1, IN2, IN3, or IN4 in sleep state will not be executed.
Note3: High output by external pull-up

7.1. VCC Low Voltage Detection Circuit

The VCC low voltage detection circuit monitors the voltage of the VCC terminal and detects voltage drops.

When the voltage drops below VCCLOd, the circuit enters reset state, suspending all circuits and turning OFF all external FET gate drives (shutdown). Reset state is released when the voltage rises above VCCLOr. Normal operation starts after releasing reset.

In addition, the detection comparator has a hysteresis of VCCLOHYS to prevent chattering, and also has a built-in filter at the latter part of the comparator for eliminating pulses of less than tVCCLO.

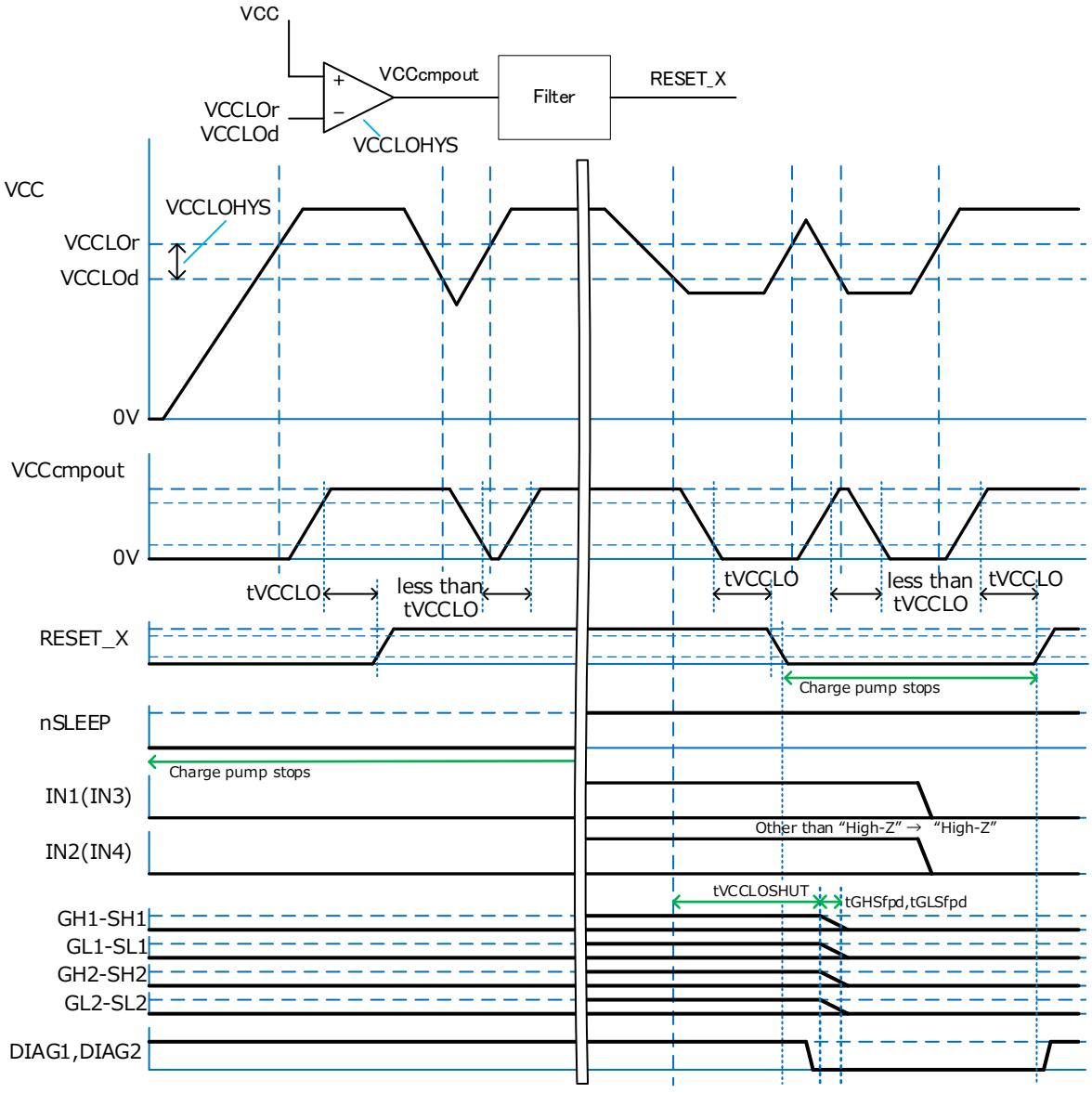


Fig. 3 Terminal layout (top view)

Note: The above diagram is partially omitted and simplified in order to explain the functions and operations of the IC.

7.2. VB Low Voltage Detection Circuit

The voltage detection circuit monitors the voltage of the VB terminal and detects voltage drops.

When the voltage drops below VBLOd, the charge pump circuit stops, turning OFF all external FET gate drives (shutdown). When the voltage rises above VBLOr, shutdown is released, and normal operation begins. To resume gate drive, in half-bridge mode, set all INx terminals to Low; in H-bridge mode, set IN1 and IN2 terminals to Low. The shutdown can then be released, the DIAG1 and DIAG2 pins can be returned to normal, and normal operation can resume after the tWAKE time.

In addition, the detection comparator has hysteresis of VBLOHYS to prevent chattering.

Note: INx = IN1, IN2, IN3, IN4

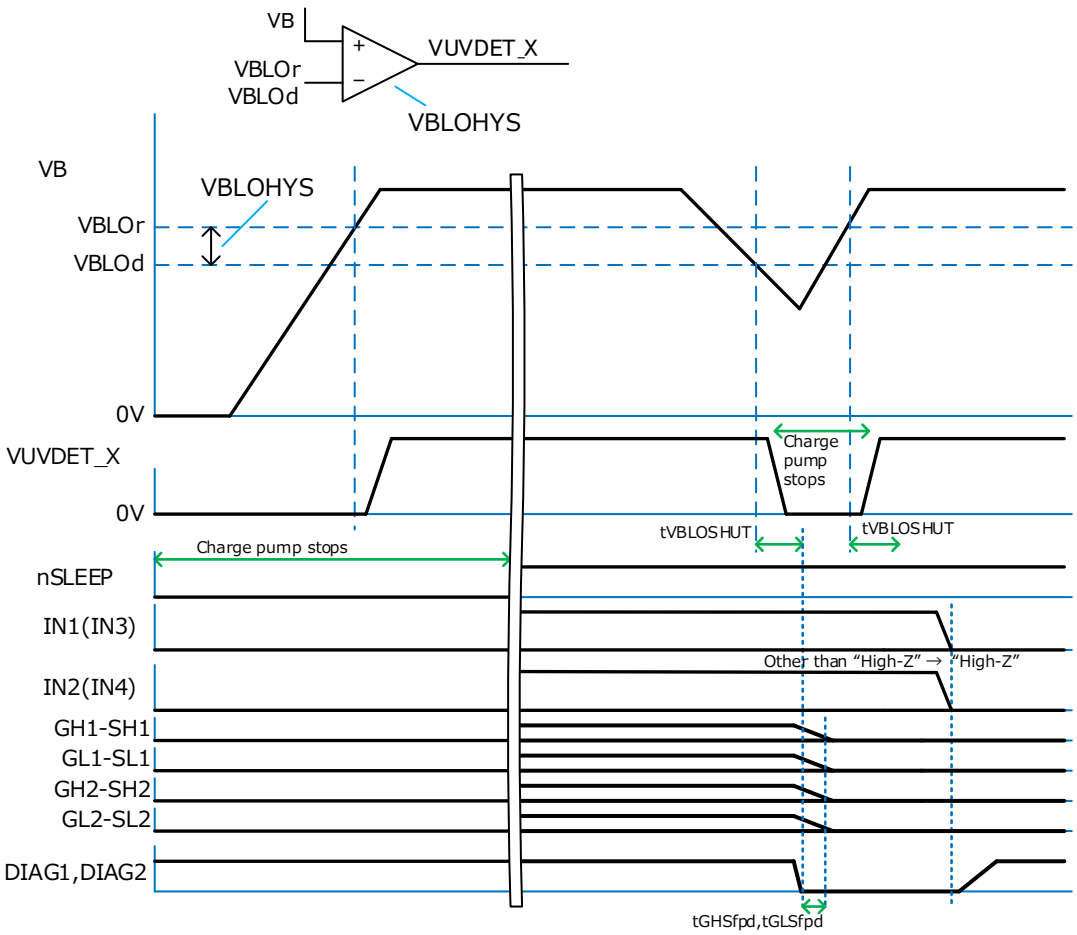


Fig. 4 VB low voltage detection operation

Note: The above diagram is partially omitted and simplified in order to explain the functions and operations of the IC.

7.3. Charge Pump Circuit

TB9103FTG has a built-in charge pump circuit to drive the gate of the external high-side N-channel MOSFET. Its drive is performed at 200kHz (typ.).

The charge pump operation stops when it is at nSLEEP=Low, internal reset period, and VB low voltage detection period. When the charge pump voltage exceeds the clamp voltage of VCPCL1d, it immediately stops boosting.

Do not apply external voltage to the VCP terminal.

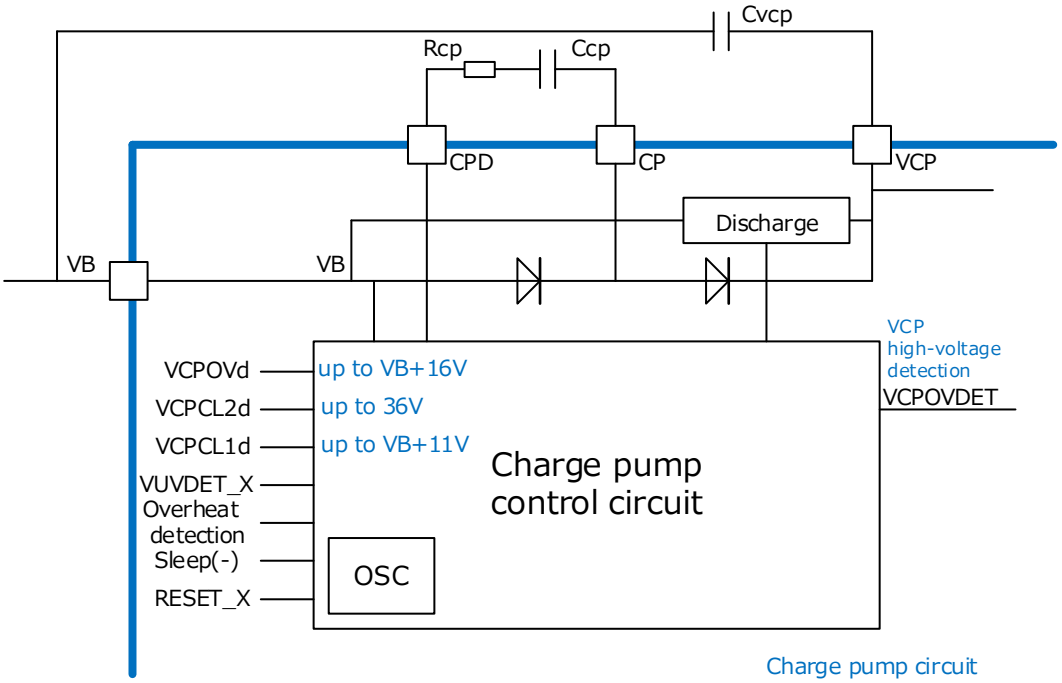


Fig. 5 Example of charge pump circuit

Note: The above diagram is partially omitted and simplified in order to explain the functions and operations of the IC.

Table 3 Charge pump circuit operation definition

Operation state of IC	Charge pump operation	VCP discharge operation
Reset (VCC low voltage detection)	In stopped state	In stopped state
Sleep (nSLEEP=Low)	In stopped state	In stopped state
VB Low voltage detection (VUVDET_X=0)	In stopped state	In stopped state
VCP Clamp 1 excessive voltage (VCPCL1d<VCP)	In stopped state	In stopped state
VCP Clamp 2 excessive voltage (VCPCL2d<VCP)	In stopped state	Discharge
VCP high voltage detection excessive voltage (VCPOVd<VCP)	In stopped state	Discharge
Overheat detection	In stopped state	In stopped state
Those other than the above	In operation	In stopped state

7.3.1. Charge pump high voltage clamp circuit

Besides immediately suspending boosting voltage to prevent the TB9103FTG from exceeding the withstand voltage of its elements in the case of exceeding VPCCL2d, the charge pump voltage also conducts discharge of the externally connected smoothing capacitor C_{VCP}.

7.3.2. Charge pump high voltage detection circuit

To prevent excessive, withstand voltages between the gate and source of the external FET, this circuit immediately suspends boosting voltage and carries out discharge of the externally connected smoothing capacitor C_{VCP} in the case of exceeding VCPOVd.

Furthermore, the circuit turns OFF (shutdown) all external FETs and outputs an error to DIAG1 and DIAG2 terminals. Then, when the voltage drops below VCPOVd, the charge pump starts operating.

To resume operation after turning OFF the external FETs based on the assesment of high-voltage detection in half-bridge mode, set all the INx terminals to Low. In H-bridge mode, set the IN1 and IN2 terminals to Low. Then, the shutdown can be released, the DIAG1 and DIAG2 pins can be returned to normal, and normal operation can resume after the tWAKE time.

Note: INx = IN1, IN2, IN3, IN4

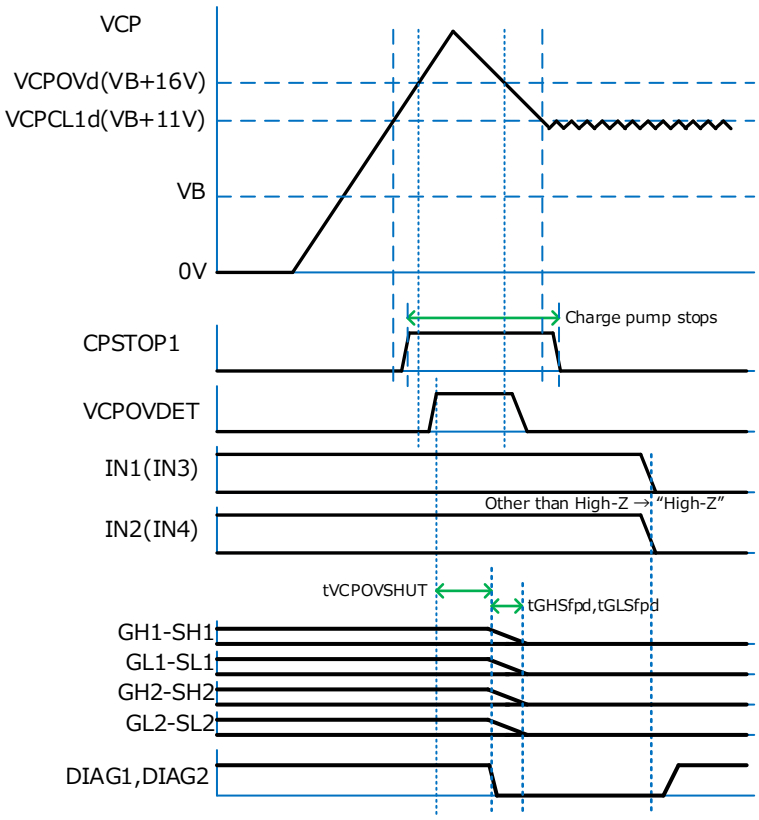


Fig. 6 Charge pump high voltage detection and shutdown operation

7.4. Gate Drive Circuit

Fig. 7 shows the block diagram of the gate drive.

The high-side gate driver outputs enough voltage to turn ON the external high-side N-channel MOSFET, and its output resistor, Ronhssrc, is 500Ω (typ.). When the external MOSFET is turned OFF, it shunts the section between the gate and the source through the output resistor, Ronhssnk, of 50Ω (typ.).

The low-side gate driver outputs enough voltage to turn ON the external low-side N-channel MOSFET. However, the gate driver outputs voltage clamped inside the IC to keep the gate voltage of the external FET below a rated value. Its output resistor, Ronlssrc, is 500Ω (typ.). When the external MOSFET is turned OFF, the gate driver shunts the section between the gate and the source through the output resistor, Ronhssnk, of 50Ω (typ.).

When the IC is in reset or sleep state, the gate driver output shunts the section between the gate and the source with the pull-down resistors, RHSOFF and RLSOFF, which are 150kΩ (typ.).

In addition, please make sure that GH1, GL1, GH2, GL2 do not stack to VCC or GND.

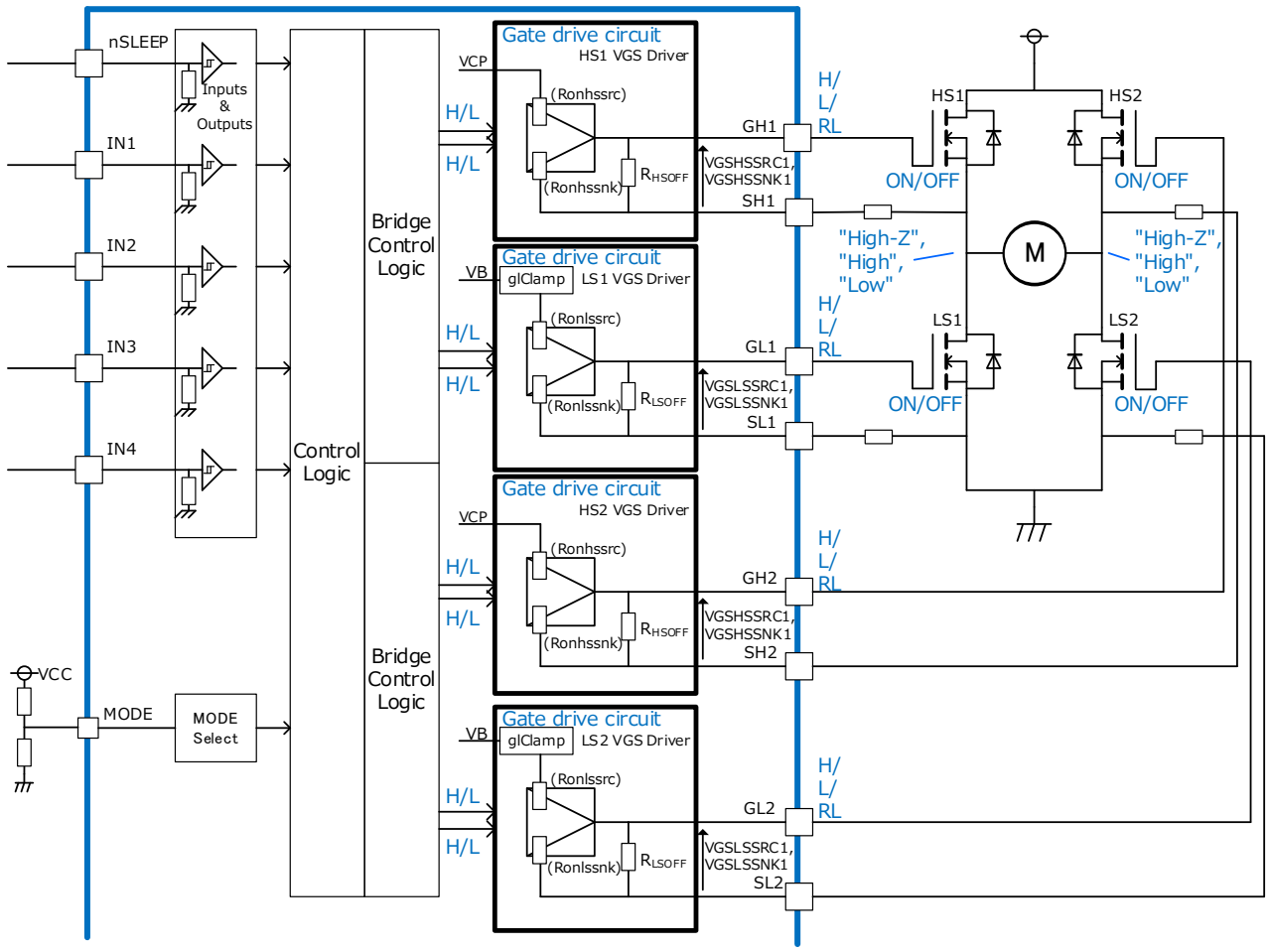


Fig. 7 Block diagram of gate drive circuit

Note: The above diagram is partially omitted and simplified in order to explain the functions and operations of the IC.

7.4.1. Gate-source voltage detection circuit

To judge the end of dead time, the circuit compares the gate-source voltage with VGSDEAD.

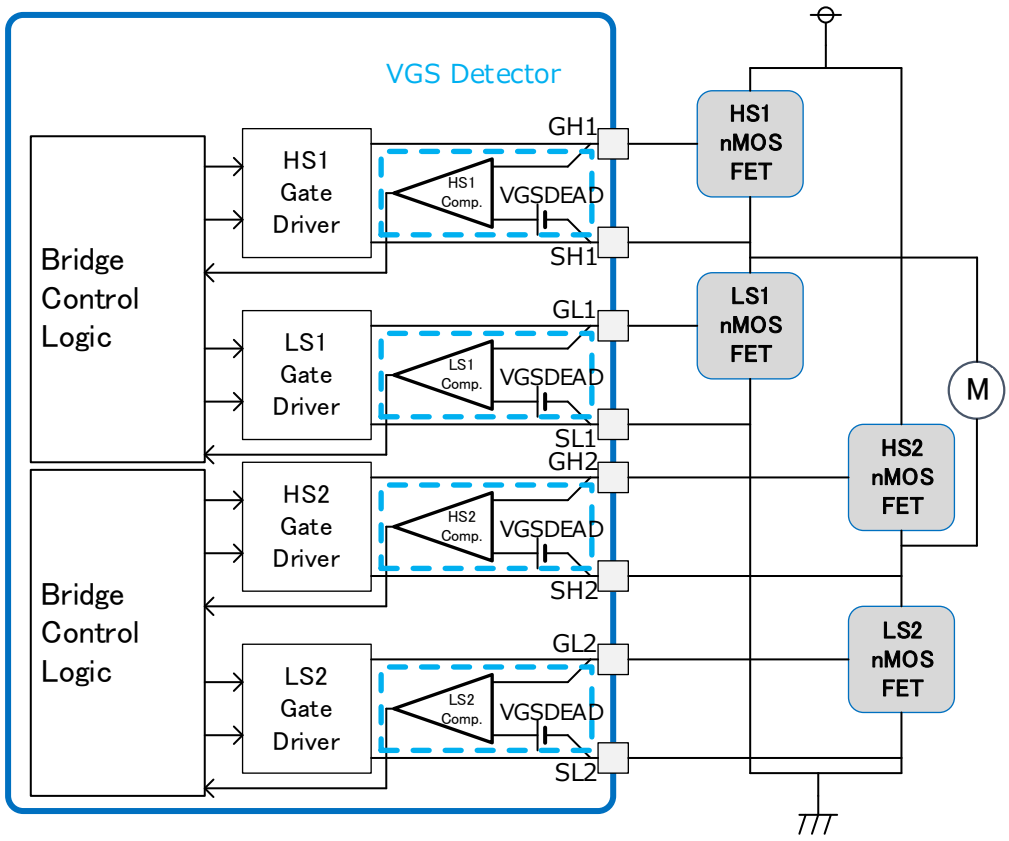


Fig. 8 Dead time control circuit—Section for VGS voltage detection

Note: The above diagram is partially omitted and simplified in order to explain the functions and operations of the IC.

7.5. Control Logic (Control Logic and Bridge Control Logic)

TB9103FTG has five input terminals (nSLEEP and IN1, IN2, IN3, and IN4) for bridge control and one input terminal (MODE) for selecting half-bridge/H-bridge. The input signal to nSLEEP is the control signal input section, which eliminates glitches. The five input signals have pull-down resistors to stop the function in the IC in the event of a pin open failure.

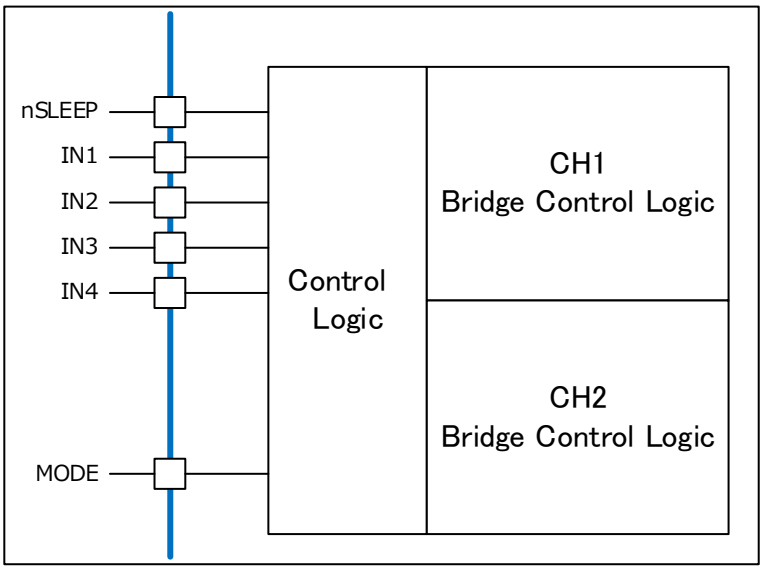


Fig. 9 Block configuration example of control logic

Note: The above diagram is partially omitted and simplified in order to explain the functions and operations of the IC.

7.5.1. Mode setting

TB9103FTG can select its operating mode according to voltages at the MODE terminal. This setting is selected by either pulling up the MODE terminal to VCC or pulling it down to GND; however, when making this setting through a resistor, it is necessary to select a resistance value that is sufficiently smaller than the resistance value within the IC. The selected mode latches when the power supply VCC exceeds VCCLOr and the condition nSLEEP=High are met at the same time.

Fig. 10 shows the interface circuit for the MODE terminal.

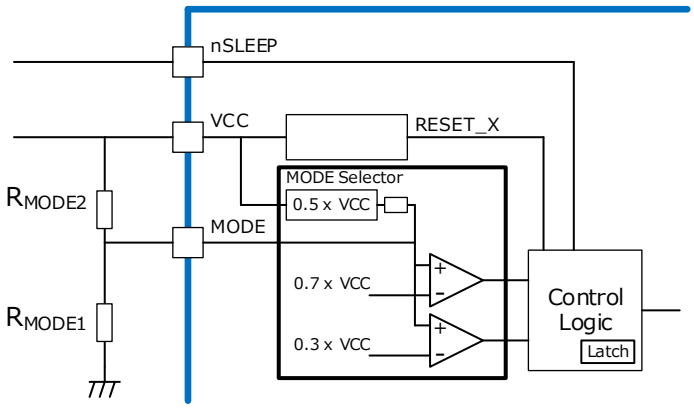


Fig. 10 MODE terminal interface circuit

Note: The above diagram is partially omitted and simplified in order to explain the functions and operations of the IC.

Table 4 MODE terminal settings

R_{MODE2}, R_{MODE1} Setting		MODE terminal voltage	Bridge mode
R_{MODE2}	R_{MODE1}		
<47kΩ+10%	Open	MODE2set	Half-bridge mode (two independent channels)
Open	<47kΩ+10%	MODE1set	H-bridge mode
Open	Open	Those other than the above	Error (Refer to Table 8 Detection function mode terminal open)

7.5.1.1. Mode setting terminal open detection circuit

When TB9103FTG detects that the MODE terminal is open, it turns OFF (shuts down) all external FETs and outputs an error to the DIAG1 and DIAG2 terminals.

The error output is updated at the timing to latch the mode state again (after releasing reset or nSLEEP).

7.5.2. Half-bridge mode

7.5.2.1. Operation description

TB9103FTG operates as two independent channels in half-bridge mode.

The first half-bridge CH1 is controlled by the signals of IN1 and IN2 terminals. In half-bridge mode, dead time is automatically inserted when the drive instructions by the IN1 and IN2 terminals are changed so that the high-side external FET HS1 and the low-side external FET LS1 are not turned ON at the same time. The gate voltage fault detection function monitors the voltage between GH1 and SH1 and the voltage between GL1 and SL1 and compares the difference with the indication of the IN1 and IN2 terminals when it is outside the monitoring mask time. The drain-current overcurrent detection function monitors the voltage between DH and SH1 as well as the voltage between SH1 and SL1 and monitors and judges whether the external FET is in a sufficiently ON state when it is outside the monitoring mask time.

The second half-bridge CH2 is controlled by the signals of IN3 and IN4 terminals. In half-bridge mode, dead time is automatically inserted when the drive instructions by the IN3 and IN4 terminals are changed so that the high-side external FET HS2 and the low-side external FET LS2 are not turned ON at the same time. The gate voltage fault detection function monitors the voltage between GH2 and SH2 and the voltage between GL2 and SL2 and compares the difference with the indication of the IN3 and IN4 terminals when it is outside the monitoring mask time. The drain-current overcurrent detection function monitors the voltage between DH and SH2 as well as the voltage between SH2 and SL2 and monitors and judges whether the external FET is in a sufficiently ON state when it is outside the monitoring mask time.

The TB9103FTG does not have the ability to measure motor current. When installing an external monitor resistor, use it within the absolute maximum rating.

Set unused channels' INx to Low.

Note: INx = IN1, IN2, IN3, IN4

7.5.2.2. Truth table

Tables 5 and 6 show possible operating states in half-bridge mode.

Table 5 Truth table for first half-bridge CH1

Internal	Inputs			Outputs		Descriptions
H=Reset	nSLEEP	IN1	IN2	GH1	GL1	
H	X	X	X	RL	RL	IC is in reset state. Motor phase input is High-Z.
L	L	X	X	RL	RL	IC is in sleep mode. Motor phase input is High-Z.
L	H	L	L	L	L	Motor phase input is High-Z.
L	H	H	L	H	L	Motor phase input is High.
L	H	L	H	L	H	Motor phase input is Low.
L	H	H	H	L	L	Motor phase input is High-Z. (Note1)

Table 6 Truth table for second half-bridge CH2

Internal	Inputs			Outputs		Descriptions
H=Reset	nSLEEP	IN3	IN4	GH2	GL2	
H	X	X	X	RL	RL	IC is in reset state. Motor phase input is High-Z.
L	L	X	X	RL	RL	IC is in sleep mode. Motor phase input is High-Z.
L	H	L	L	L	L	Motor phase input is High-Z.
L	H	H	L	H	L	Motor phase input is High.
L	H	L	H	L	H	Motor phase input is Low.
L	H	H	H	L	L	Motor phase input is High-Z. (Note1)

Explanation of symbols:
X: Do not care; RL: Low via resistor; L: Low via active element
H: High by active element; High-Z: High impedance state

Note1: Release operation is not performed when a fault is detected.

7.5.2.3. Definition of current path

In half-bridge mode, the current path of the external N-channel MOSFET used for TB9103FTG is defined as shown in Fig. 11. The solid line shows the current path when driving. In addition, the dotted line indicates the path of regenerative current.

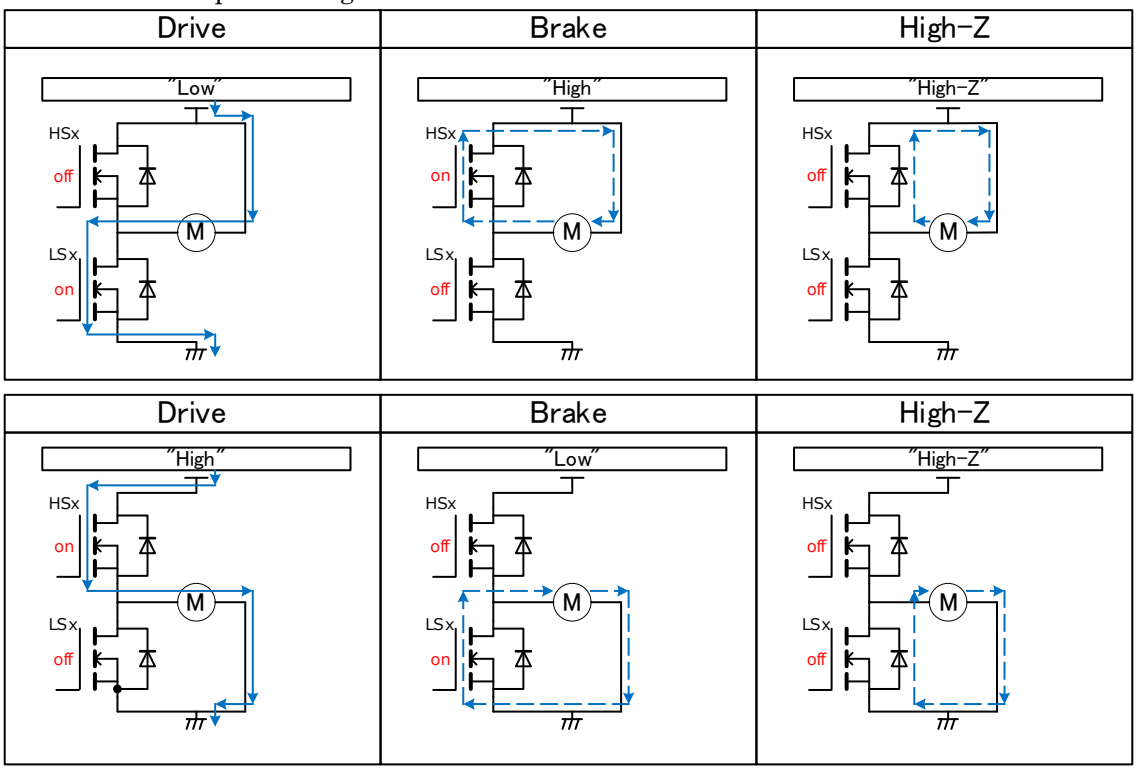


Fig. 11 Definition of current path

Note: The above diagram is partially omitted and simplified in order to explain the functions and operations of the IC.

7.5.2.4. Drive control flowchart

Fig. 12 shows the drive control flowchart in half-bridge mode.
Fig. 13 shows drive control combinations which are not shown in Fig. 12.

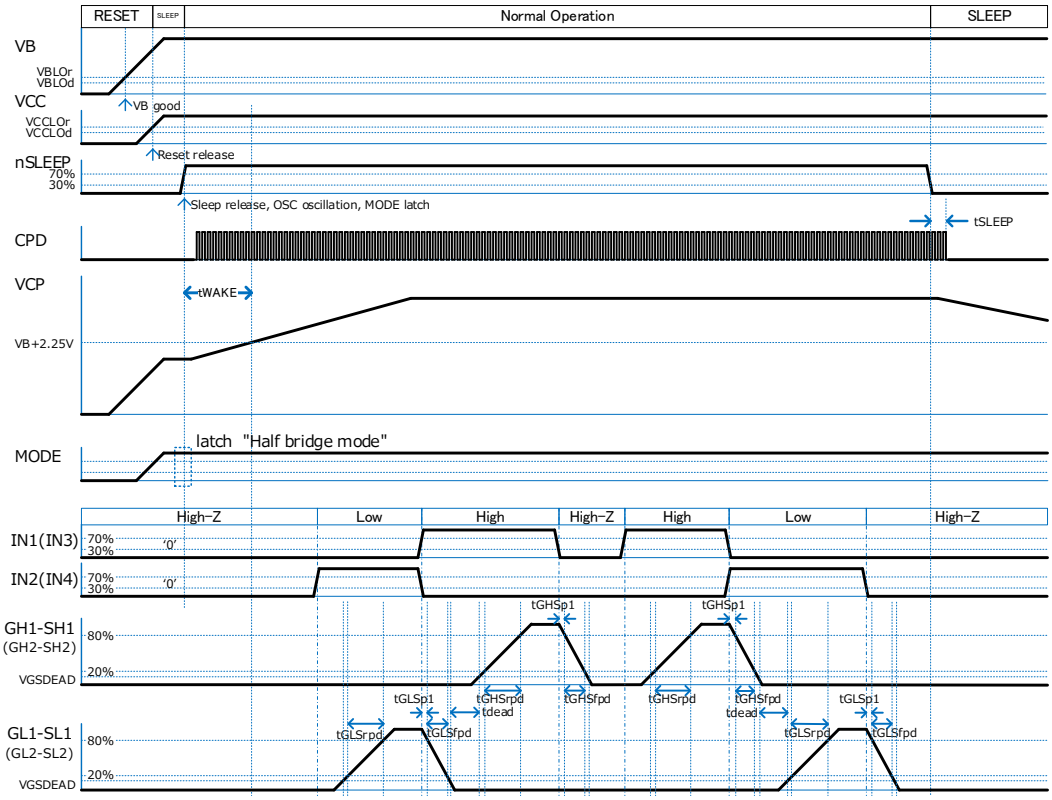


Fig. 12 Half-bridge flowchart 1 (for each channel)

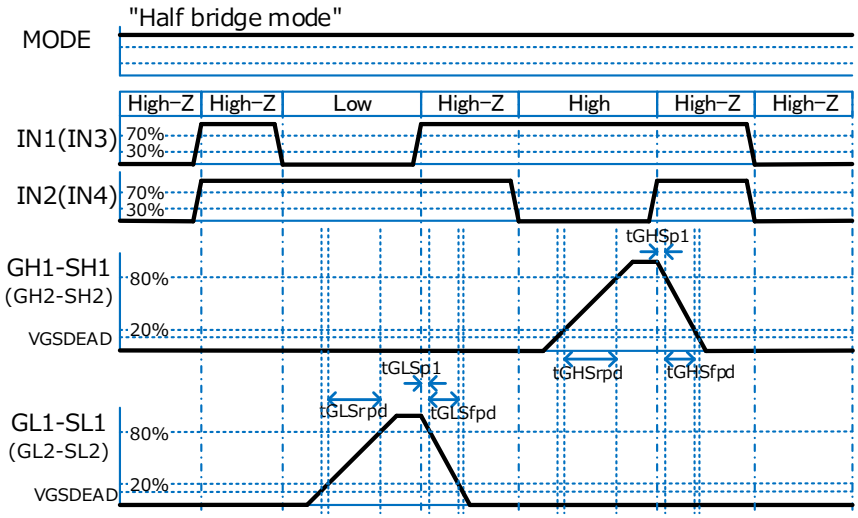


Fig. 13 Half-bridge flowchart 2—Other drive control combinations

Note: The above diagram is partially omitted and simplified in order to explain the functions and operations of the IC.

7.5.3. H-bridge mode

7.5.3.1. Operation description

TB9103FTG operates as a one-channel H-bridge in H-bridge mode.

Control is performed by the signals of the IN1 and IN2 terminals. It is recommended that the IN3 and IN4 terminals be connected to GND. In H-bridge mode, dead time is automatically inserted when the drive instructions by the IN1 and IN2 terminals are changed so that the high-side external FETs—HS1 and HS2—and the low-side external FETs—LS1 and LS2—are not turned ON at the same time. The gate voltage fault detection function monitors the voltage between GH1 and SH1, the voltage between GL1 and SL1, the voltage between GH2 and SH2, and the voltage between GL2 and SL2, and compares the difference with the indication of the IN1 and IN2 terminals when it is outside the monitoring mask time. The drain-current overcurrent detection function monitors the voltage between DH and SH1, the voltage between SH1 and SL1, the voltage between DH and SH2, and the voltage between SH2 and SL2 and monitors and judges whether the external FETs are in the ON state when it is outside the monitoring mask time.

The TB9103FTG does not have the ability to measure motor current. When installing an external monitor resistor, use it within the absolute maximum rating.

7.5.3.2. Truth table

Table 7 shows possible logical states in H-bridge mode.

Table 7 Truth table for H-bridge mode

Internal	Inputs			Outputs				Descriptions
H=Reset	nSLEEP	IN1	IN2	GH1	GL1	GH2	GL2	
H	X	X	X	RL	RL	RL	RL	IC is in reset state. Motor phase input is High-Z.
L	L	X	X	RL	RL	RL	RL	IC is in sleep mode. Motor phase input is High-Z.
L	H	L	L	L	L	L	L	Motor phase input is High-Z.
L	H	H	L	H	L	L	H	Motor phase input is Forward drive (SH1→SH2)
L	H	L	H	L	H	H	L	Motor phase input is Reverse drive (SH2→SH1)
L	H	H	H	L	H	L	H	Motor phase input is Brake

Explanation of symbols:
X: Do not care; RL: Low through resistor; L: Low through active element
H: High by active element; High-Z: High impedance state

It is recommended that the IN3 and IN4 terminals be connected to GND.

7.5.3.3. Definition of current path

In H-bridge mode, the current path of the external N-channel MOSFETs used for TB9103FTG is defined as shown in Fig. 14.

The red solid line indicates the current path in forward drive, and the blue solid line indicates the current path in reverse drive.

The dotted line indicates the regenerative current path in forward drive, and the two-dot chain line indicates the regenerative current path in reverse drive.

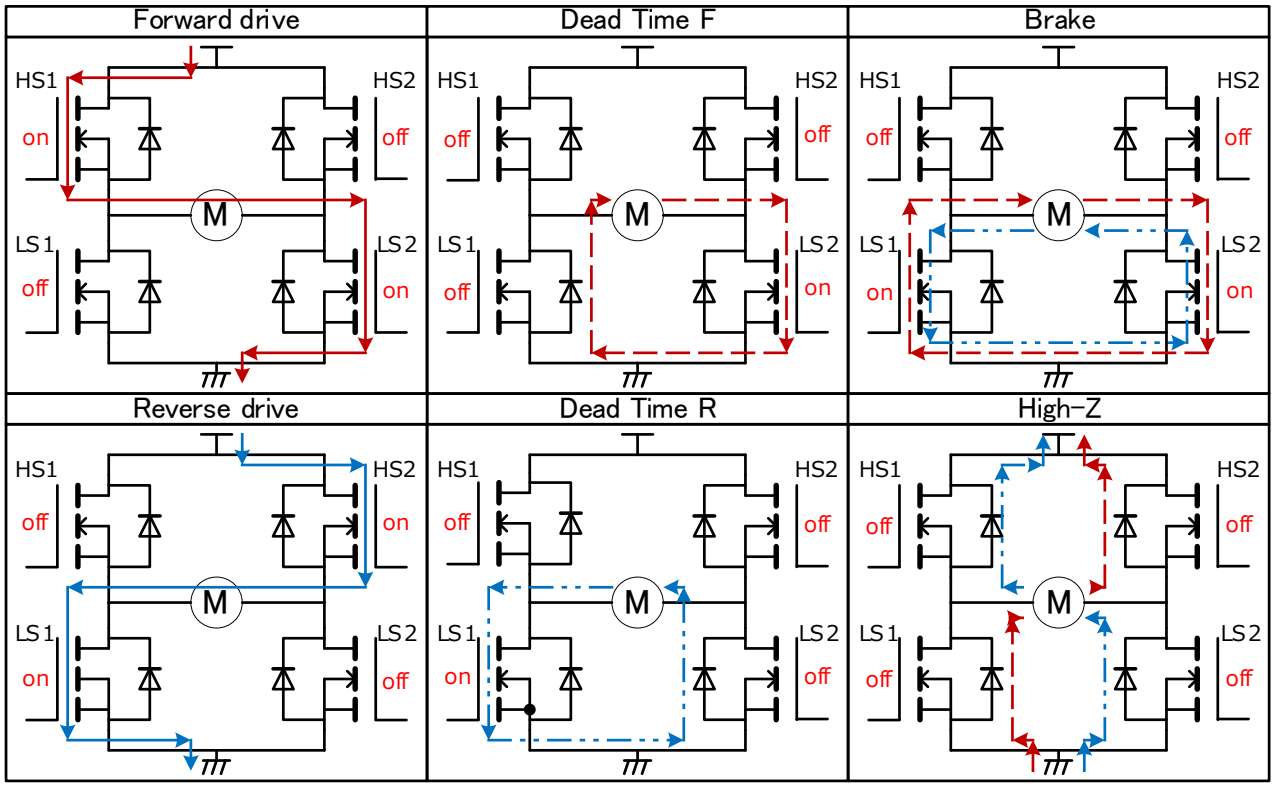


Fig. 14 Definition of current path

Note: The above diagram is partially omitted and simplified in order to explain the functions and operations of the IC.

Disconnecting the current to the motor will generate a back electromotive force in the motor.

At the time of the High-Z state, the back EMF is regenerated through the power supply.

If the sink capability of the power supply is not available, the power and output terminals of the IC may rise above the rated rate.

The back electromotive force of the motor depends on the conditions of use and the characteristics of the motor.

Please make sure that there is no risk of damage or malfunction of the IC and that there is no risk of destruction or malfunction in the peripheral circuits under the customer's usage conditions.

7.5.3.4. Drive control flowchart

Fig. 15 shows the bridge drive control flowchart in H-bridge mode.
Fig. 16 shows drive control combinations which are not shown in Fig. 15.

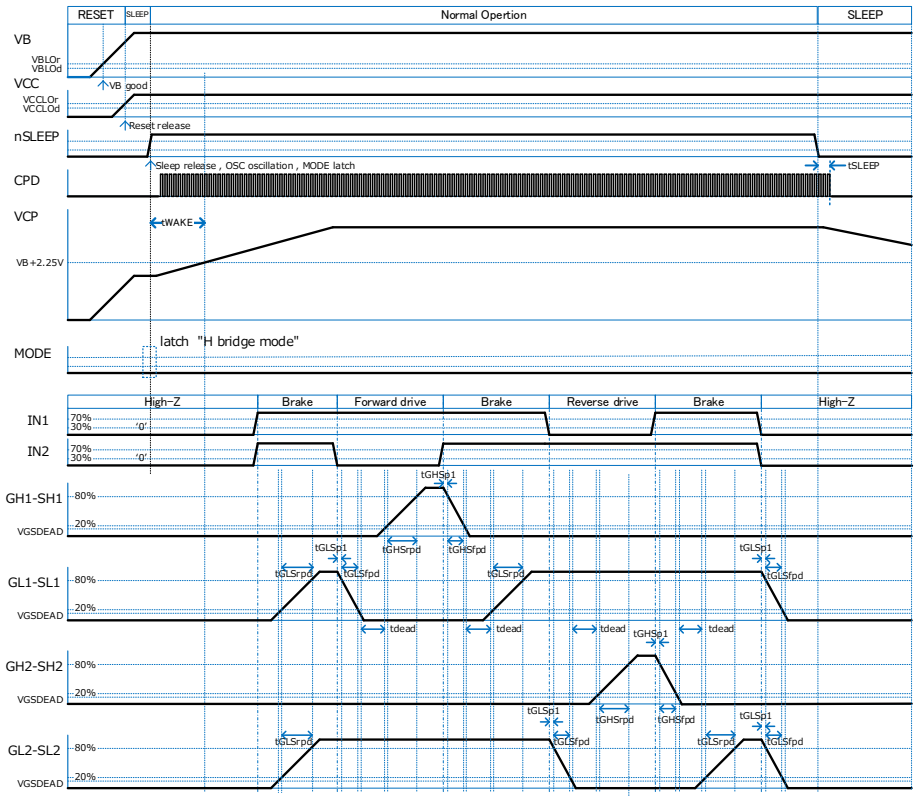


Fig. 15 H-bridge flowchart 1

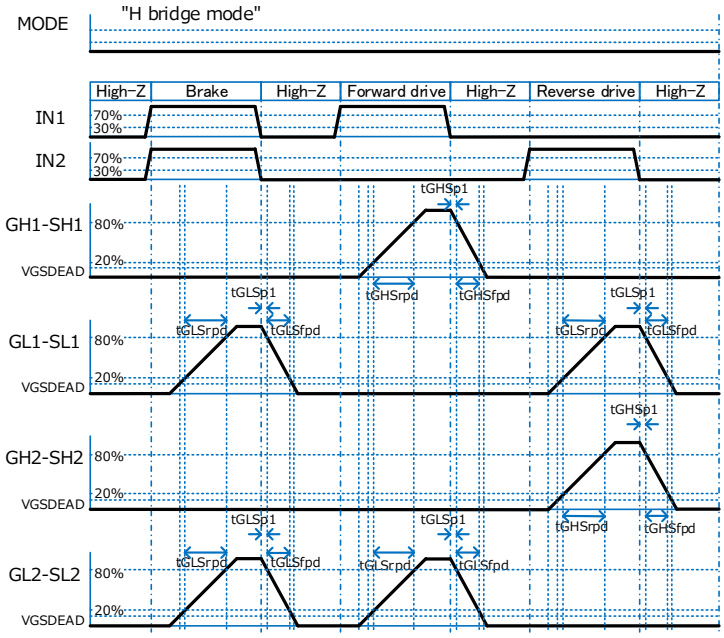


Fig. 16 H-bridge flowchart 2—Other drive control combinations

Note: The above diagram is partially omitted and simplified in order to explain the functions and operations of the IC.

7.6. Fault Detection Functions

TB9103FTG has various fault detection functions. This chapter describes them. As for the following functions, refer to each chapter in parenthesis: VCC low voltage detection (Chapter 7.1), VB low voltage detection (Chapter 7.2), charge pump high voltage detection circuit (Chapter 7.3.2), mode setting pin open detection circuit (Chapter 7.5.1.1). VDS detection threshold setting pin open detection circuit (Chapter 7.6.5.1) and overheat shutdown (Chapter 7.6.6).

7.6.1. Types of fault detection functions and corresponding operations

TB9103FTG has functions to detect fault states shown in Table 8, shut down the gate drive, and output to the DIAG1 and DIAG2 terminals according to the fault conditions shown in Table 9.

Anomaly detection can occur more than once at the same time.In addition, if an abnormality is detected while the gate is being driven and shut down, the gate drive abnormality judgment may occur at the same time due to the shutdown.The output to the DIAG1 and DIAG2 pins prioritizes abnormal conditions and outputs corresponding to the highest priority abnormal conditions.

Table 8 Detection functions and corresponding operations

No.	Detection function	Gate drive output (VGS), Charge pump operating state	Release condition
1	CH1 (HS1, LS1) IDS overcurrent judgment (Voltage monitoring between DS)	In half-bridge mode: GH1=GL1=Low In H-bridge mode: GH1=GL1=GH2=GL2=Low Charge pump=Operation	In half-bridge mode: Change IN1 and IN2 terminals from others to Low In H-bridge mode: Change IN1 and IN2 terminals from others to Low
2	CH1 (HS1, LS1) Gate drive fault judgment (Voltage monitoring between GS)	In half-bridge mode: GH1=GL1=Low In H-bridge mode: GH1=GL1=GH2=GL2=Low Charge pump=Operation	In half-bridge mode: Change IN1 and IN2 terminals from others to Low In H-bridge mode: Change IN1 and IN2 terminals from others to Low
3	CH2 (HS2, LS2) IDS overcurrent judgment (Voltage monitoring between DS)	In half-bridge mode: GH2=GL2=Low In H-bridge mode: GH1=GL1=GH2=GL2=Low Charge pump=Operation	In half-bridge mode: Change IN3 and IN4 terminals from others to Low In H-bridge mode: Change IN1 and IN2 terminals from others to Low
4	CH2 (HS2, LS2) Gate drive fault judgment (Voltage monitoring between GS)	In half-bridge mode: GH2=GL2=Low I n H-bridge mode: GH1=GL1=GH2=GL2=Low Charge pump=Operation	In half-bridge mode: Change IN3 and IN4 terminals from others to Low In H-bridge mode: Change IN1 and IN2 terminals from others to Low
5	MODE terminal open	GH1=GL1=GH2=GL2=Low Charge pump=Operation	Recovery when nSLEEP=High and reset release by VCC are satisfied
6	VDS terminal open	GH1=GL1=GH2=GL2=Low Charge pump=Operation	Recovery when released
7	Overheat detection	GH1=GL1=GH2=GL2=Low Charge pump=Stop	The Charge Pump will be restored as soon as it is resolved. In half-bridge mode: Change IN1, IN2, IN3, IN4 terminals from others to Low In H-bridge mode: Change IN1 and IN2 terminals from others to Low (Note2), (Note3)
8	VB low voltage detection	GH1=GL1=GH2=GL2=Low Charge pump=Stop	The Charge Pump will be restored as soon as it is resolved. In half-bridge mode: Change IN1, IN2, IN3, IN4 terminals from others to Low In H-bridge mode: Change IN1 and IN2 terminals from others to Low (Note2), (Note3)

No.	Detection function	Gate drive output (VGS), Charge pump operating state	Release condition
9	VCC low voltage detection	GH1=GL1=GH2=GL2=RL Charge pump=Stop	Recovery when low voltage is released (Note1)
10	VCP high voltage detection	GH1=GL1=GH2=GL2=Low Charge pump=Stop	The Charge Pump will be restored as soon as it is resolved. In half-bridge mode: Change IN1, IN2, IN3, IN4 terminals from others to Low In H-bridge mode: Change IN1 and IN2 terminals from others to Low (Note2), (Note3)
11	No detection	Normal operation	-

RL: Low through a shunt resistor between the gate and the source

Note1: When VCC low voltage is detected, the internal of TB9103FTG goes into reset state.
Note2: When released while in the fault detection state, all gate drivers will go Low and the charge pump will stop.
Note3: After performing the release operation by the IN1,IN2, it is necessary to wait for the tWAKE period.

Table 9 Detection details and DIAG1, DIAG2 terminals

No.	Detected contents	DIAG Output Priority	DIAG1 terminal output	DIAG2 terminal output	Remarks
1	CH1 (HS1, LS1) IDS overcurrent judgment (monitoring voltage between DS)	Middle	Low	High	Fault detected on CH1
2	CH 1(HS1, LS1) Gate drive fault judgment (monitoring voltage between GS)	Middle	Low	High	Fault detected on CH1
3	CH2 (HS2, LS2) IDS overcurrent judgment (monitoring voltage between DS)	Low	High	Low	Fault detected on CH2
4	CH2 (HS2, LS2) Gate drive fault judgment (monitoring voltage between GS)	Low	High	Low	Fault detected on CH2
5	MODE terminal open	High	Low	Low	Fault common to both CHs detected
6	VDS terminal open	High	Low	Low	Fault common to both CHs detected
7	Overheat detection	High	Low	Low	Fault common to both CHs detected
8	VB low voltage detection	High	Low	Low	Fault common to both CHs detected
9	VCC low voltage detection	High	Low	Low	Fault common to both CHs detected
10	VCP high voltage detection	High	Low	Low	Fault common to both CHs detected
11	No detection	-	High	High	-

Note: The output to the DIAG1 and DIAG2 pins prioritizes abnormal conditions and outputs corresponding to the highest priority abnormal conditions.

7.6.2. DIAG1 and DIAG2 terminals

DIAG1 and DIAG2 terminals, which are open drain outputs, must be connected to the power supply (VCC) through an external resistor. Connect the pull-up to the power supply terminal of the circuit (MCU, etc.) used for judgment by inputting the DIAG signal.

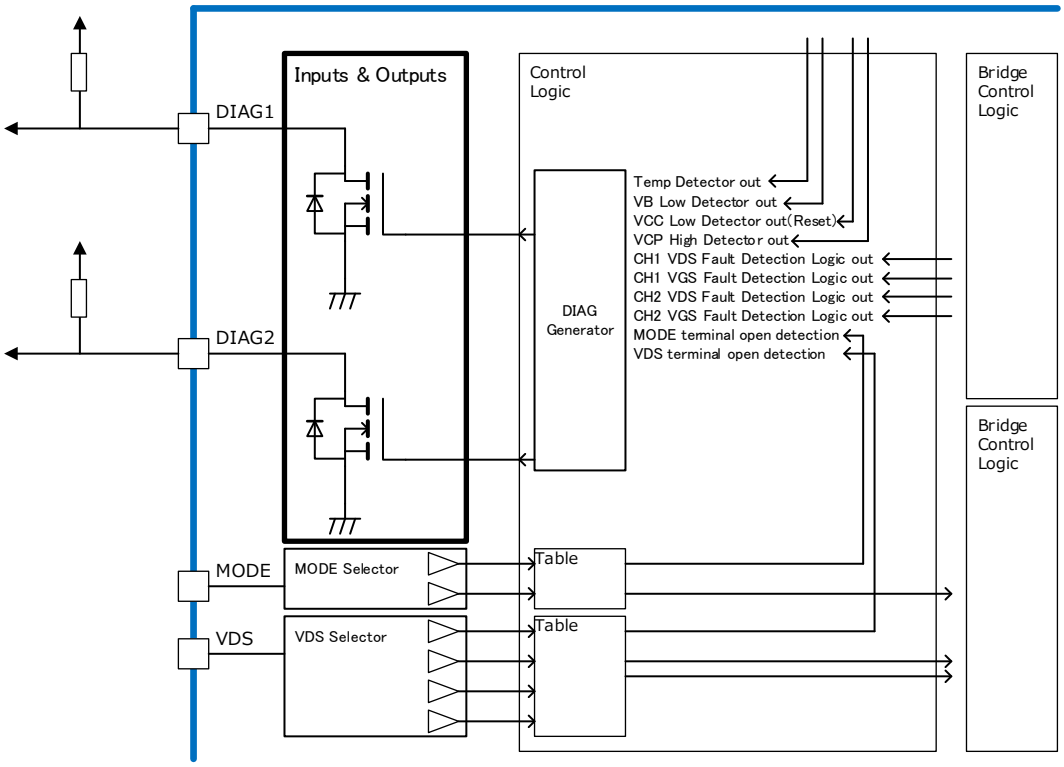


Fig. 17 DIAG1 and DIAG2 terminals

Note: The above diagram is partially omitted and simplified in order to explain the functions and operations of the IC.

7.6.3. VGS monitoring, gate driver fault detection, and shutdown operation

TB9103FTG diverts part of the dead time control circuit to monitor whether the drive instructions of the IN1, IN2, IN3 and IN4 terminals are consistent with the states of the GH1, GH2, GL1 and GL2 terminals. When the drive instruction is changed, judgment is not made until tVGSF has passed since the change. If the state is different from those indicated in Tables Table 5, Table 6 and Table 7 when it is outside of the tVGSF time, a gate driver fault is assessed to have occurred.

When the gate driver fault is assessed to have occurred, the DIAGx terminal is set to the states shown in No.2 and 4 of Table 9, and all the external FETs of the channel judged to be faulty are turned OFF (shutdown) in half-bridge mode. All the external FETs are turned OFF (shutdown) in H-bridge mode.

To restore the operation after gate driver fault and turning OFF the external FETs, in half-bridge mode, set all the INx terminals of the channel judged to be faulty to Low. In H-bridge mode, set the IN1 and IN2 terminals to Low.

Note: INx = IN1, IN2, IN3, IN4 , DIAGx = DIAG1, DIAG2

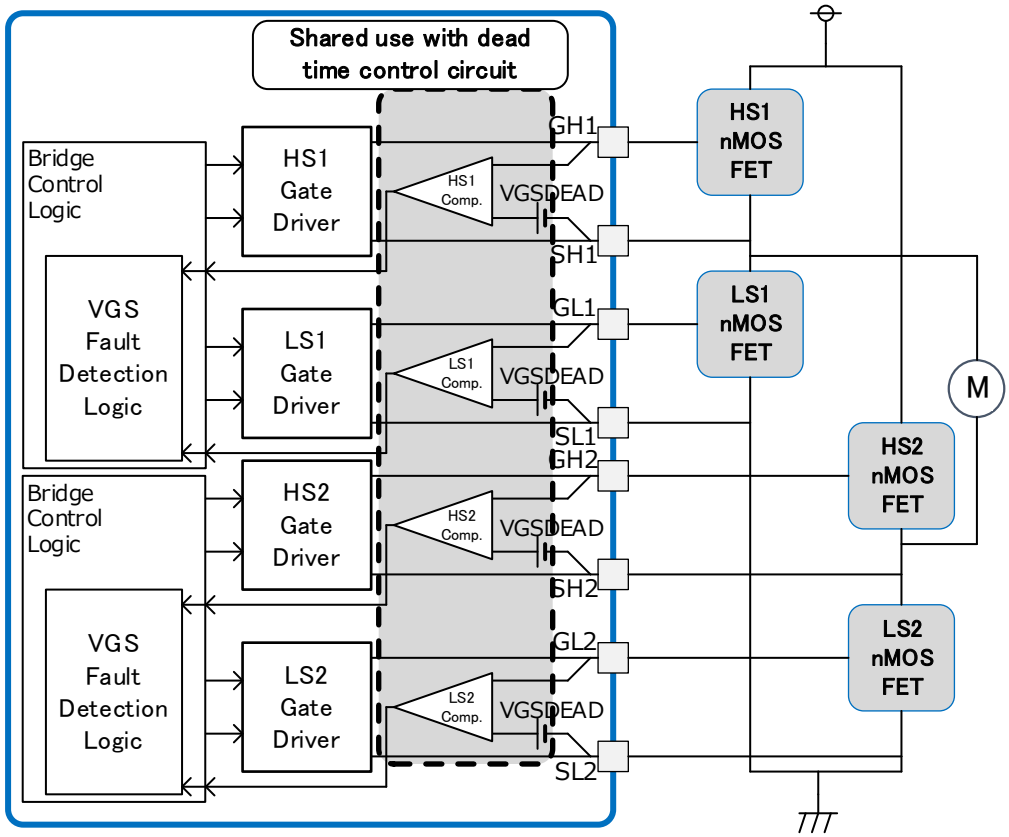


Fig. 18 VGS monitoring and fault detection circuit block diagram

Note: The above diagram is partially omitted and simplified in order to explain the functions and operations of the IC.

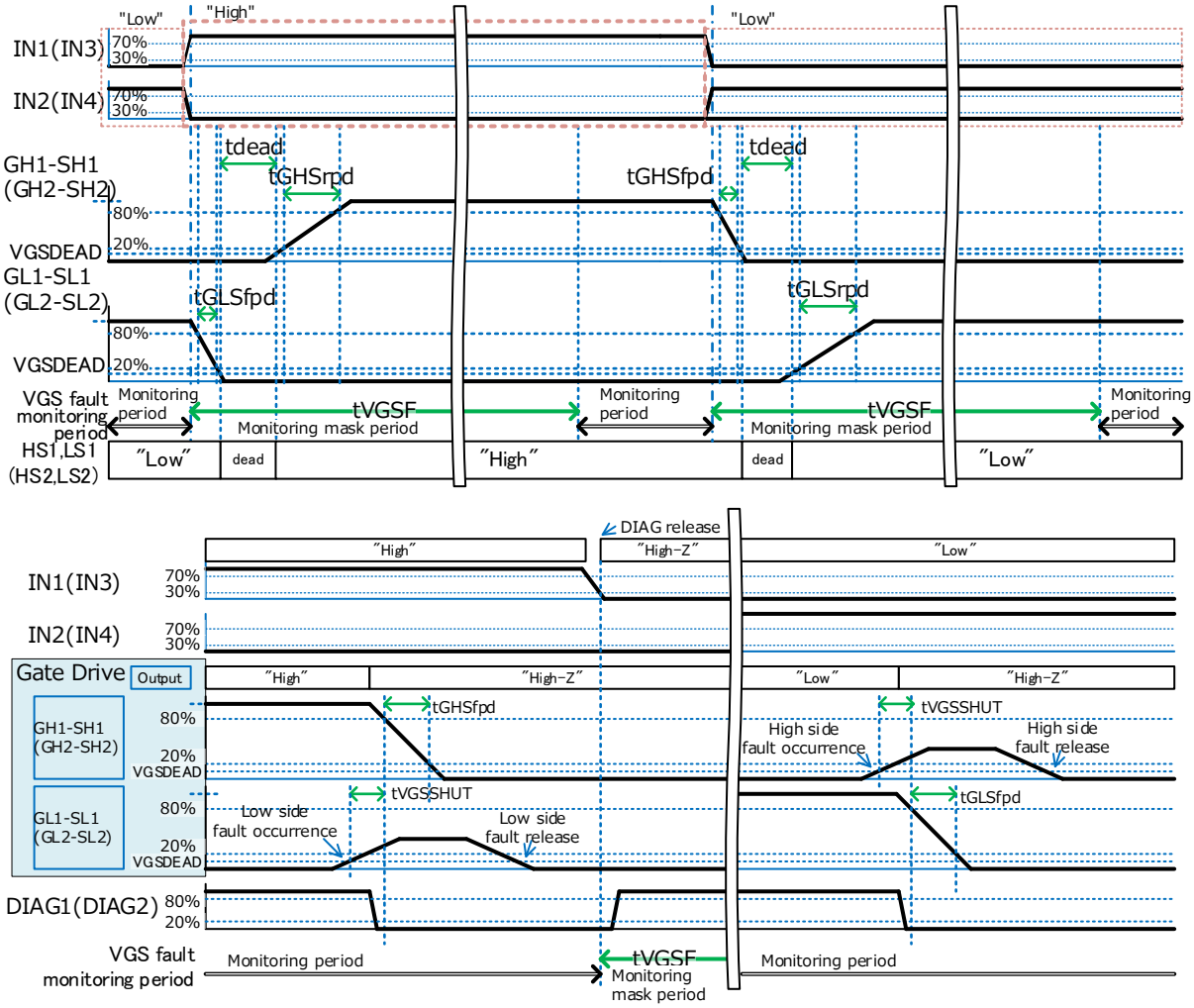


Fig. 19 VGS monitoring, fault detection, and shutdown operation

Note: The above diagram is partially omitted and simplified in order to explain the functions and operations of the IC.

7.6.4. VDS monitoring, IDS overcurrent detection, and shutdown operation

Fig. 20 shows the concept of connection to external FETs.

TB9103FTG monitors whether the drain-source voltage VDS is lower than the set voltages of HS_Vref and LS_Vref while the external FET gate is being driven.

When the drive instruction is changed, TB9103FTG does not monitor until tVDSF has passed since the change. If the VDS is higher than the set voltages of HS_Vref and LS_Vref while the gate of the external FET is being driven ON when it is outside the tVDSF time, TB9103FTG will judge it as overcurrent.

When overcurrent is judged, the DIAG terminals are set to the states shown in No.1 and 3 of Table 9, and in half-bridge mode, all the external FET drives of the channel judged to be faulty are turned OFF (shutdown). In H-bridge mode, all the external FET drives are turned OFF (shutdown).

To restore operation after overcurrent is judged and the external FETs are turned OFF (shutdown), in half-bridge mode, set all the INx terminals of the channel judged to be faulty to Low. Set the IN1 and IN2 terminals to Low in H-bridge mode.

Note: INx = IN1, IN2, IN3, IN4

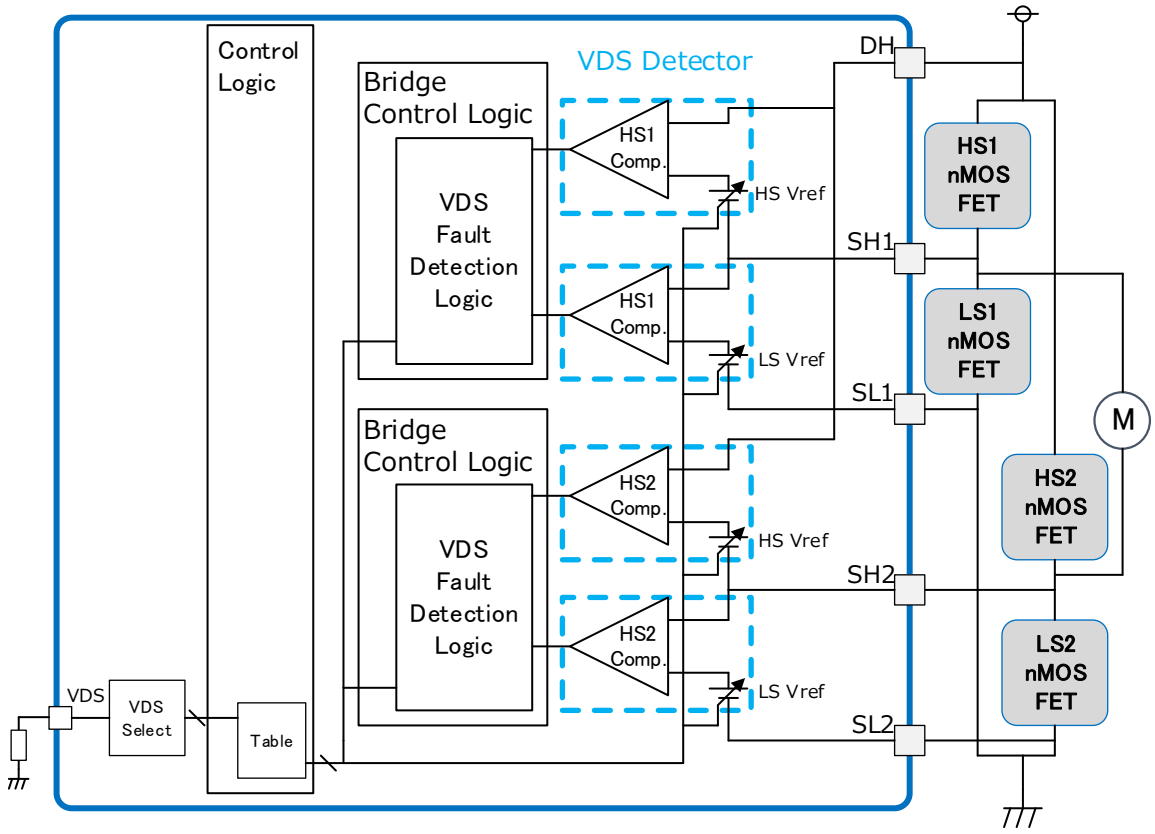


Fig. 20 Block diagram of IDS overcurrent detection by VDS monitoring

Note: The above diagram is partially omitted and simplified in order to explain the functions and operations of the IC.

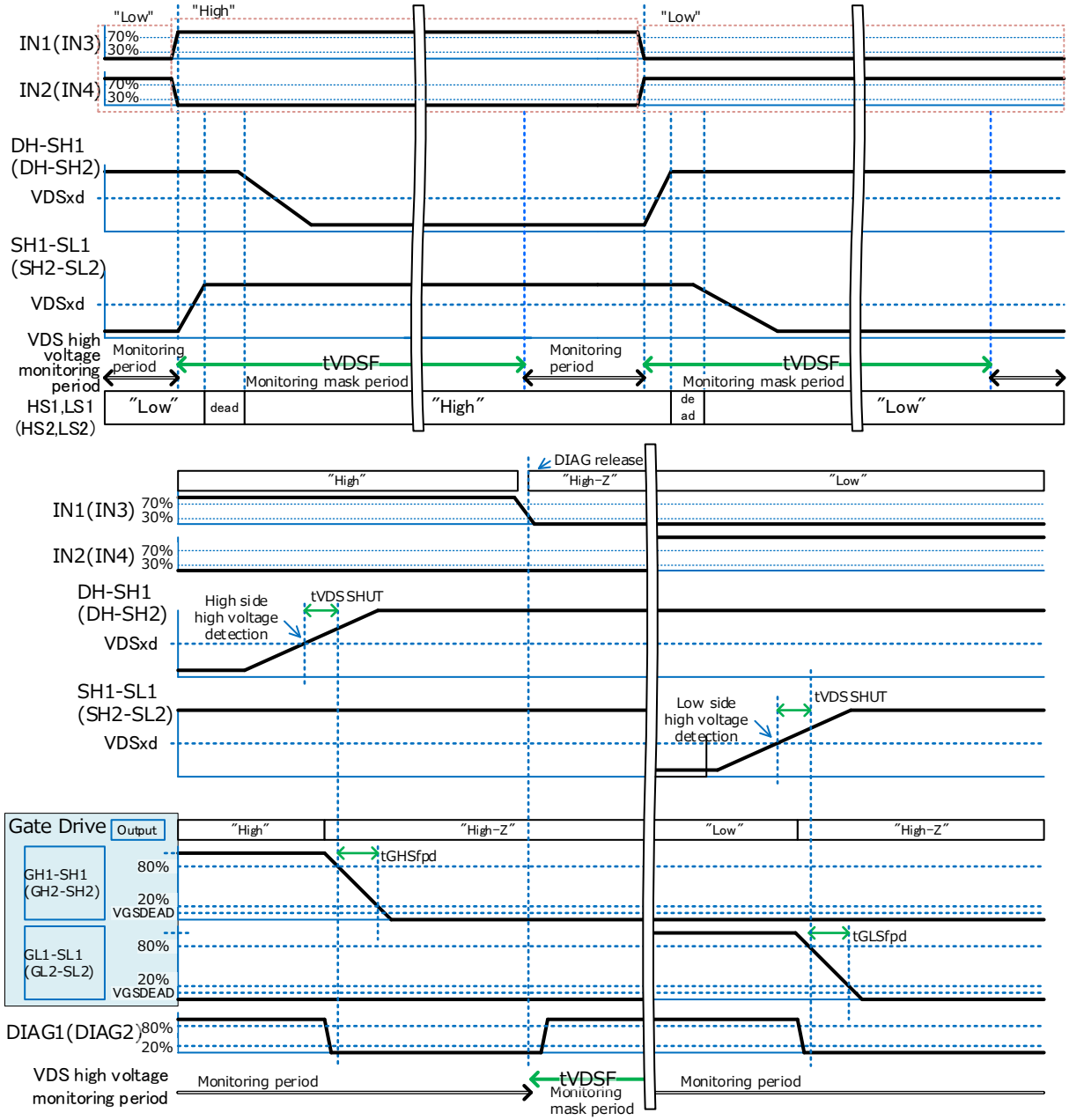


Fig. 21 Timing chart of IDS overcurrent detection by VDS monitoring

Note: The above diagram is partially omitted and simplified in order to explain the functions and operations of IC.

7.6.5. VDS detection threshold voltage setting

High-side threshold voltage "HS Vref" and low-side threshold voltage "LS Vref" used for VDS detection can be set by the voltage applied to the VDS terminal. They also have the function disabling VDS monitoring.

This setting, which is selected with an external resistor, needs to be set using a relatively high resistance in order to minimize VCC current consumption.

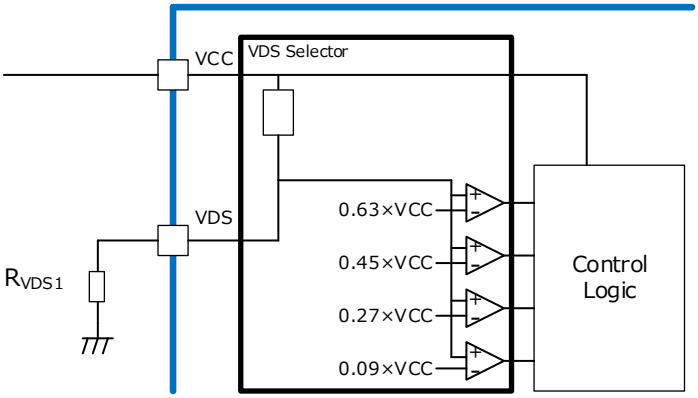


Fig. 22 VDS terminal interface circuit

Note: The above diagram is partially omitted and simplified in order to explain the functions and operations of the IC.

Table 10 VDS threshold voltage setting

Example of R_{VDS1}	VDS terminal voltage	VDS terminal voltage setting (HS_Vref, LS_Vref)
R_{VDS1}		
Open	VDS4dset	Error
270kΩ ±10%	VDS3dset	VDS3d
130kΩ ±10%	VDS2dset	VDS2d
51kΩ ±10%	VDS1dset	VDS1d
≤1kΩ ±10%	VDS0dset	VDS detection disabled

7.6.5.1. VDS detection threshold setting terminal open detection circuit

When TB9103FTG detects that the VDS terminal is open, it turns OFF (shuts down) all the external FETs and outputs an error to the DIAG1 and DIAG2 terminals. It automatically recovers after the error output is canceled.

7.6.6. Overheat shutdown

When the controller chip exceeds the overheat detection temperature of TTSDd, TB9103FTG turns OFF (shuts down) all the external FETs and outputs an error to the DIAG1 and DIAG2 terminals.

When the chip temperature drops below the release threshold temperature of TTSDr start the charge pump operation. To resume gate drive, set all INx pins to Low in half-bridge mode, and set IN1 and IN2 pins Low (High-Z indication) in H-bridge mode. Then, the shutdown is released, the DIAG1 and DIAG2 pins are returned to normal, and normal operation can resume after the tWAKE.

Note: INx = IN1, IN2, IN3, IN4

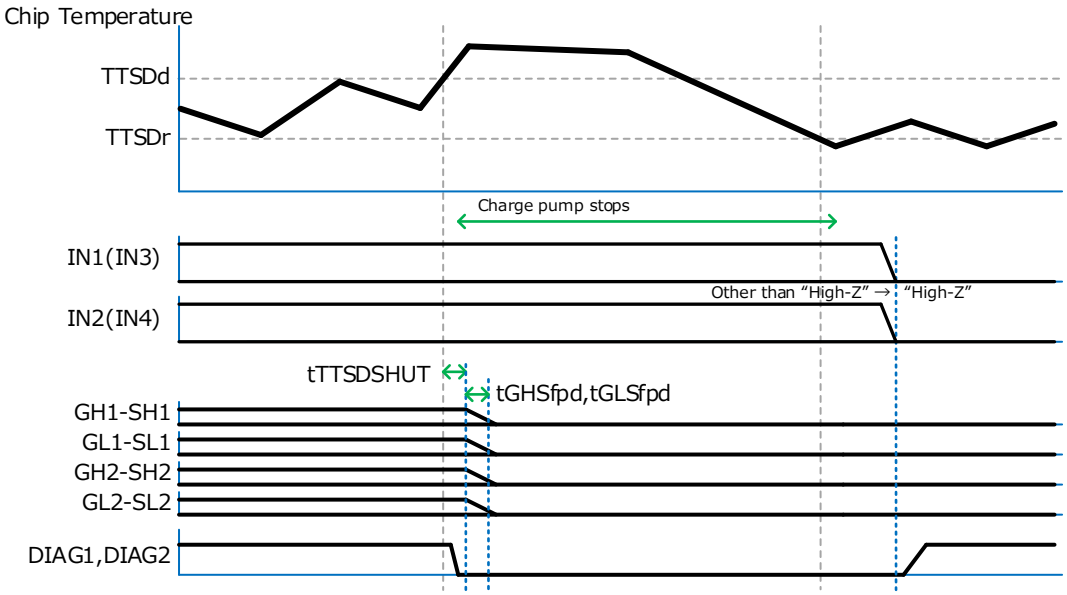


Fig. 23 Overheating detection timing chart

Note: The above diagram is partially omitted and simplified in order to explain the functions and operations of the IC.

8. PRODUCT SPECIFICATIONS/RATINGS

8.1. Absolute Maximum Ratings

Unless otherwise specified, Ta=-40 to 125°C, voltage is based on GND, and the direction of current flowing into the terminal is positive.

Spec No.	Characteristics	Condition	Symbol	Rating	Unit
8.1.1	Power supply voltage 1 VB		Vb	-0.3 to Vcp+0.3 (≤18)	V
8.1.2		≤1sec		to Vcp+0.3 (≤40)	V
8.1.3	Power supply voltage 2 VCC		Vcc	-0.3 to 6	V
8.1.4	Charge pump voltage1 CPD		Vcp1	-0.3 to Vb+0.3 (≤36)	V
8.1.5		≤1sec		to Vb+0.3 (≤40)	V
8.1.6	Charge pump voltage2 CP		Vcp2	-0.3 to Vcp+0.3 (≤36)	V
8.1.7		≤1sec		to Vcp+0.3 (≤40)	V
8.1.8	Charge pump voltage3 VCP		Vcp3	-0.3 to 36	V
8.1.9		≤1sec		to 40	V
8.1.10	High-side gate terminal voltage GH1, GH2		Vgh	-0.3 to Vcp+0.3 (≤40)	V
8.1.11	Low-side gate terminal voltage GL1, GL2		Vgl	-0.3 to Vb+0.3 (≤40)	V
8.1.12	High-side drain terminal voltage DH		Vdh	-0.3 to Vcp+0.3 (≤40)	V
8.1.13	High-side source terminal voltage SH1, SH2		Vsh	-0.3 to Vcp+0.3 (≤40)	V
8.1.14		≤0.1msec		-2 to	V
8.1.15	Low-side source terminal voltage SL1, SL2		Vsl	-0.3 to Vb+0.3 (≤40)	V
8.1.16		≤0.1msec		-2 to	V
8.1.17	Terminal voltage nSLEEP		Vin3	-0.3 to 6	V
8.1.18	Terminal voltage IN1,IN2,IN3,IN4		Vin1	-0.3 to Vcc+0.3 (≤6)	V
8.1.19	Terminal voltage MODE		Vin4	-0.3 to 40	V
8.1.20	Terminal voltage VDS		Vin2	-0.3 to Vb+0.3 (≤40)	V
8.1.21	Terminal voltage DIAG1,DIAG2		Vod1	-0.3 to 6	V
8.1.22	Differential voltage between terminals VB, DH	VB-DH	Vdif1	-2 to 2	V
8.1.23	Differential voltage between terminals DH, SH1, SH2	SH1-DH, SH2-DH	Vdif3	to 2	V
8.1.24	Differential voltage between terminals SH1, SH2,SL1, SL2	SL1-SH1, SL2-SH2	Vdif4	to 2	V
8.1.25	Ambient temperature		Ta	-40 to 125	°C
8.1.26	Junction temperature		Tj	-40 to 150	°C
8.1.27	Storage temperature		Tstg	-55 to 150	°C

The absolute maximum ratings are standard values that must not be exceeded even momentarily.

When any absolute maximum rating is exceeded, it may cause destruction, degradation, or damage to the IC and/or other parts. Design systems so that absolute maximum ratings are not exceeded in any operating condition.

Please use this IC within the operating ranges described above.

8.2. Operating Ranges

Spec No.	Characteristics	Symbol	Condition	Min	Typ	Max	Unit
8.2.1	Power supply voltage operating range 1	VBrng	VBrng≥VCCrng	7	-	18	V
8.2.2	Power supply voltage operating range 2	VCCrng	VBrng≥VCCrng	4.5	-	5.5	V
8.2.3	Junction temperature operating range	Tjrng		-40	-	150	°C

8.3. Thermal Resistance

Spec No.	Characteristics	Symbol	Condition	Min	Typ	Max	Unit
8.3.1	Thermal resistance	R_{thJA}	-	-	39.9	-	°C/W

8.4. Electrical Characteristics

Unless otherwise specified, VB=7 to 18 V, VCC=4.5 to 5.5 V (VB≥VCC), and Ta=-40 to 125°C.
All the voltages are referenced to GND, and the current direction that flows into the terminal is positive.

8.4.1. Power

Spec No.	Characteristics	Symbol	Condition	Min	Typ	Max	Unit
8.4.1.1	Operating power supply current	IVB	nSLEEP=High, no load (not connected with external FET), Rcp=10Ω, Ccp=0.1μF, Cvcp=2.2μF	-	-	10	mA
8.4.1.2	Operating power supply current	IVCC	nSLEEP=High	-	-	2.5	mA
8.4.1.3	Power supply current in Sleep mode VB	ISLEEP1	nSLEEP=Low, Ta=25°C	-	-	14	μA
8.4.1.4	Power supply current in Sleep mode VCC	ISLEEP2	nSLEEP=Low, Ta=25°C	-	-	14	μA
8.4.1.5	Transition time to sleep mode	tSLEEP	At VB=7V, From nSLEEP terminal H->L to GLx=0.9×VB Refer to Fig. 12, Fig. 15	-	-	15	μs
8.4.1.6	Restoration time from sleep mode	tWAKE	From nSLEEP terminal L ->H to VCP=VB+2.25 V IVCP=-2mA, Rcp=10Ω, Ccp=0.1μF, Cvcp=2.2μF Refer to Fig. 12, Fig. 15	-	-	0.5	ms

Note: GLx = GL1, GL2

8.4.2. Charge pump

Spec No.	Characteristics	Symbol	Condition	Min	Typ	Max	Unit
8.4.2.1	Charge pump voltage	VCP1	VB=7V to 18V,IVCP=-2mA GHx and GLx are at no load. Rcp=10Ω, Ccp=0.1μF Cvcp=2.2μF	VB+5	VB+11	VB+14	V
8.4.2.2	Charge pump switching frequency	fCP		100	200	400	kHz
8.4.2.3	Charge pump clamp voltage	VCPCL1d	Refer to Fig. 5, Fig. 6	VB+10	VB+11	VB+14	V
8.4.2.4		VCPCL2d	Refer to Fig. 5	33	36	39	V
8.4.2.5	Charge pump high voltage detection	VCPOVd	Refer to Fig. 5, Fig. 6	VB+15	VB+16	VB+18	V
8.4.2.6	Charge pump high voltage detection, shutdown time	tVCPOVSHUT	no load VCPOVd<VCP -> VGS=80% Refer to Fig. 6	-	-	15	μs
8.4.2.7	Charge pump voltage Discharge current	IVCPDIS	VB=18V, VCP=32V	10	70	200	mA

Note: GHx = GH1, GH2 GLx = GL1, GL2

8.4.3. Control input/output

Spec No.	Characteristics	Symbol	Condition	Min	Typ	Max	Unit
8.4.3.1	Low level input voltage nSLEEP,IN1,IN2,IN3,IN4	VIL		-	-	0.3×VCC	V
8.4.3.2	High level input voltage nSLEEP,IN1,IN2,IN3,IN4	VIH		0.7×VCC	-	-	V
8.4.3.3	Input voltage hysteresis nSLEEP,IN1,IN2,IN3,IN4	VIHYS		0.1	-	-	V
8.4.3.4	Low level input current nSLEEP,IN1,IN2,IN3,IN4	IIL	VCC=5.0V, VIN=0V	-5	-	5	μA
8.4.3.5	High level input current nSLEEP,IN1,IN2,IN3,IN4	IIH	VCC=5.0V, VIN=5.0V	25	50	100	μA
8.4.3.6	MODE terminal setting voltage	MODE2set	Half-bridge mode	0.7×VCC	-	-	V
8.4.3.7		MODE1set	H-bridge mode	-	-	0.3×VCC	V
8.4.3.8	MODE terminal setting current	IMODE2	Refer to Fig. 4	1.5	8	20	μA
8.4.3.9		IMODE1	Refer to Fig. 4	-20	-8	-1.5	μA
8.4.3.10	DIAG High-Z Output current	IDIAGOFF	DIAGx=VCC	-	-	10	μA
8.4.3.11	DIAG Low level Output voltage	VDIAGLO	IDIAGLO=1mA	-	-	0.5	V

Note: DIAGx = DIAG1, DIAG2

8.4.4. FET gate driver

Spec No.	Characteristics	Symbol	Condition	Min	Typ	Max	Unit
8.4.4.1	Between high-side GSs Drive voltage	VGSHSSRC1	VB=7 to 18V SHx=VB, no load GHx-SHx	VCP-VB -0.2	-	VCP-VB	V
8.4.4.2		VGSHSSNK1	SHx=VB, no load GHx-SHx	-	-	0.5	V
8.4.4.3	Between low-side GSs Drive voltage	VGSLSSRC1	VB=9 to 18V SLx=GND, no load GLx-SLx	8.9	11	14	V
8.4.4.4		VGSLSSRC2	VB=7 to 9V SLx=GND, no load GLx-SLx	VB-0.1	-	VB	V
8.4.4.5		VGSLSSNK1	SLx=GND, no load GLx-SLx	-	-	0.5	V
8.4.4.6	Between high-side GSs Drive output resistance Source direction	Ronhssrc	SHx=VB, IGLOAD=-1mA GHx-SHx	250	500	1000	Ω
8.4.4.7	Between high-side GSs Drive output resistance Sink direction	Ronhssnk	SHx=VB, IGLOAD=1mA GHx-SHx	20	50	150	Ω
8.4.4.8	Between low-side GSs Drive output resistance Source direction	Ronlssrc	SLx=GND, IGLOAD=-1mA GLx-SLx	250	500	1000	Ω
8.4.4.9	Between low-side GSs Drive output resistance Sink direction	Ronlssnk	SLx=GND, IGLOAD=1mA GLx-SLx	20	50	150	Ω
8.4.4.10	High side Turn-ON time	tGHSrpd	SHx=VB, Rl=10Ω, Cl=10nF Refer to Fig. 19	1	8	20	µs
8.4.4.11	High side Turn-OFF time	tGHSfpd	SHx=VB, Rl=10Ω, Cl=10nF Refer to Fig. 19	0.1	0.8	5	µs
8.4.4.12	Low side Turn-ON time	tGLSrpd	SLx=GND, Rl=10Ω, Cl=10nF Refer to Fig. 19	1	8	20	µs
8.4.4.13	Low side Turn-OFF time	tGLSfpd	SLx=GND, Rl=10Ω, Cl=10nF Refer to Fig. 19	0.1	0.8	5	µs
8.4.4.14	Input propagation delay time	tGHSp1	SLx=GND, Rl=10Ω, Cl=10nF Refer to Fig. 12	0.1	0.5	2	µs
8.4.4.15	Input propagation delay time	tGLSp1	SLx=GND, Rl=10Ω, Cl=10nF Refer to Fig. 12	0.1	0.5	2	µs
8.4.4.16	Minimum dead time	tdead	SHx=VB, SLx=GND Rl=10Ω, Cl=10nF Refer to Fig. 19	0.5	1.5	6	µs

Spec No.	Characteristics	Symbol	Condition	Min	Typ	Max	Unit
8.4.4.17	For dead time judgment VGS voltage	VGSDEAD	Refer to Fig. 19	0.6	1.5	1.8	V
8.4.4.18	High side Hold off resistance	RHSOFF	Shunt resistance between gate and source SHx=GND	75	150	300	kΩ
8.4.4.19	Low side Hold off resistance	RLSOFF	Shunt resistance between gate and source	75	150	300	kΩ

Note: GHx = GH1, GH2　GLx = GL1, GL2　SHx = SH1, SH2　SLx = SL1, SL2

8.4.5. State detection

Spec No.	Characteristics	Symbol	Condition	Min	Typ	Max	Unit
8.4.5.1	VCC low voltage detection	VCCLOd	VCC drop detection	3.9	-	4.3	V
8.4.5.2		VCCLOr	VCC up release	4.0	-	4.5	V
8.4.5.3	VCC low voltage detection hysteresis	VCCLOHYS	VCCLOd < VCCLOr	0.1	-	-	V
8.4.5.4	VCC low voltage detection Filter time	tVCCLO	Refer to Fig. 3	3	4	12	µs
8.4.5.5	VCC low voltage detection Shutdown time	tVCCLOSHUT	no load VCC<VCCLOd -> VGS=80% Refer to Fig. 3	3	10	25	µs
8.4.5.6	VB low voltage detection	VBLOd	VB drop detection	5.1	-	5.7	V
8.4.5.7		VBLOr	VB up release	5.2	-	6.0	V
8.4.5.8	VB low voltage detection hysteresis	VBLOHYS	VBLOd < VBLOr	0.1	-	-	V
8.4.5.9	VB low voltage detection Shutdown time	tVBLOSHUT	no load VB<VBLOd -> VGS=80% Refer to Fig. 4	-	-	15	µs
8.4.5.10	VGS gate drive Fault detection mask time	tVGSF	Refer to Fig. 19	134	268	536	µs
8.4.5.11	VGS gate drive Fault detection shutdown time	tVGSSHUT	no load Fault state -> VGS=80% Refer to Fig. 19	-	-	5	µs
8.4.5.12	VDS detection level setting	VDS4dset	VDS detection function setting error	0.65× VCC	-	VCC	V
8.4.5.13		VDS3dset	VDS3d selection	0.47× VCC	-	0.61× VCC	V
8.4.5.14		VDS2dset	VDS2d selection	0.29× VCC	-	0.43× VCC	V
8.4.5.15		VDS1dset	VDS1d selection	0.11× VCC	-	0.25× VCC	V
8.4.5.16		VDS0dset	VDS detection function disable	0	-	0.07× VCC	V
8.4.5.17	VDS terminal input current	IVDS		-38	-28	0.1	µA
8.4.5.18	VDS detection level setting Shutdown time	tVDS4dSHUT	no load VDS terminal=VDS4dset -> VGS=80%	-	-	5	µs
8.4.5.19	VDS detection level	VDS3d		0.76	0.9	1.04	V
8.4.5.20		VDS2d		0.51	0.6	0.69	V
8.4.5.21		VDS1d		0.25	0.3	0.35	V
8.4.5.22	VDS detection mask time	tVDSF	Refer to Fig. 21	134	268	536	µs
8.4.5.23	VDS high voltage detection Shutdown time	tVDSSHUT	no load VDSxd<VDS -> VGS=80% Refer to Fig. 21	3	10	25	µs
8.4.5.24	Overheat shutdown Detected temperature	TTSDd	Detection	155	175	195	°C
8.4.5.25		TTSDr	Release	110	130	150	°C

Spec No.	Characteristics	Symbol	Condition	Min	Typ	Max	Unit
8.4.5.26	Overheat detection Shutdown time	tTTSDSHUT	no load TTSDd<Tj -> VGS=80% Refer to Fig. 23	-	-	15	µs

Note: TSD standards are by design only and have not been subjected to shipment testing.
Overheat shutdown circuitry is intended to avoid abnormal condition temporarily.
This does not warrant preventing the IC from being damaged.

8.5. Measurement Circuit

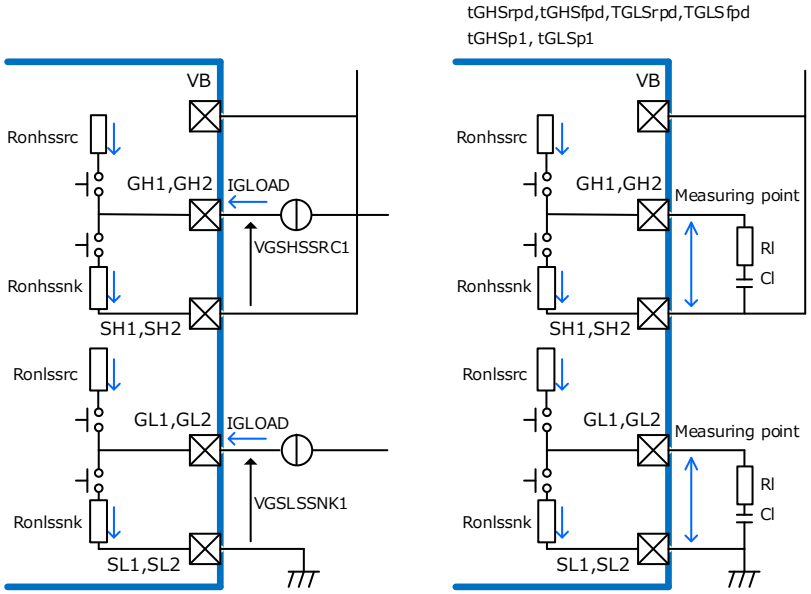


Fig. 24 Measurement of gate drive section

Note: The above diagram is partially omitted and simplified in order to explain the functions and operations of the IC.

9. Application circuit example

The information shown below is used only as an implementation guide for this device and does not guarantee the functional operation or performance. It is necessary to fully evaluate the functionality at the time of actual use.

9.1. Application circuit example

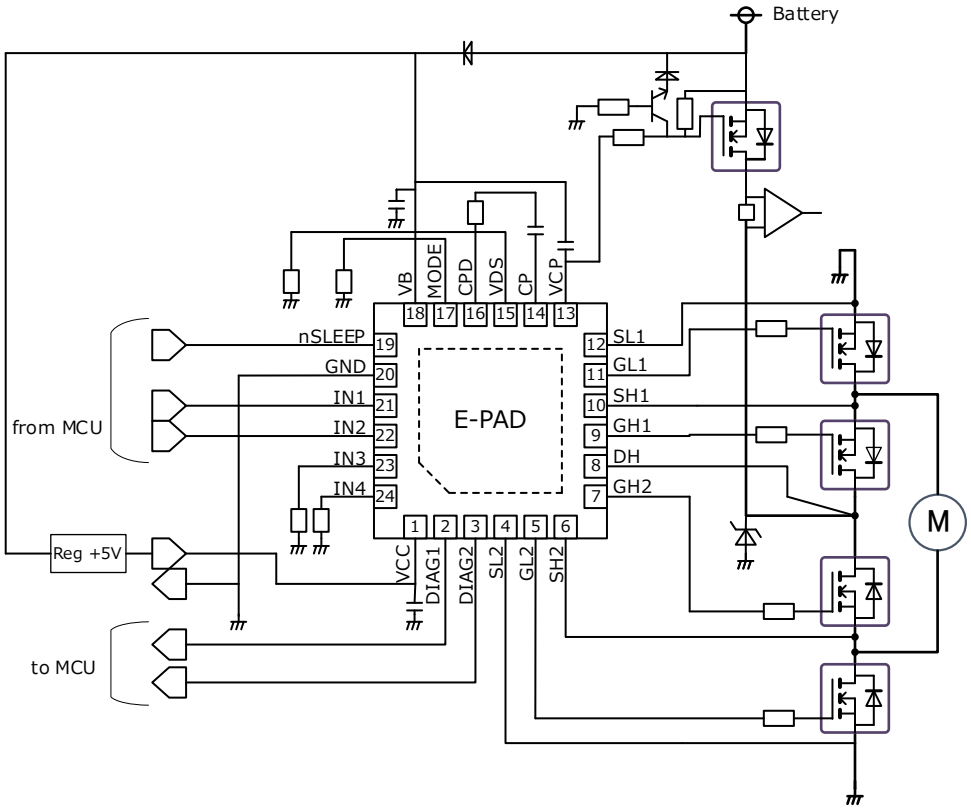


Fig. 25 TB9103FTG H-bridge mode (Application circuit example)

Note1: The above figure is just an example of the application, and it is necessary to fully evaluate the functionality at the time of actual use.

Note2: The above diagram is partially omitted and simplified in order to explain the functions and operations of the IC.

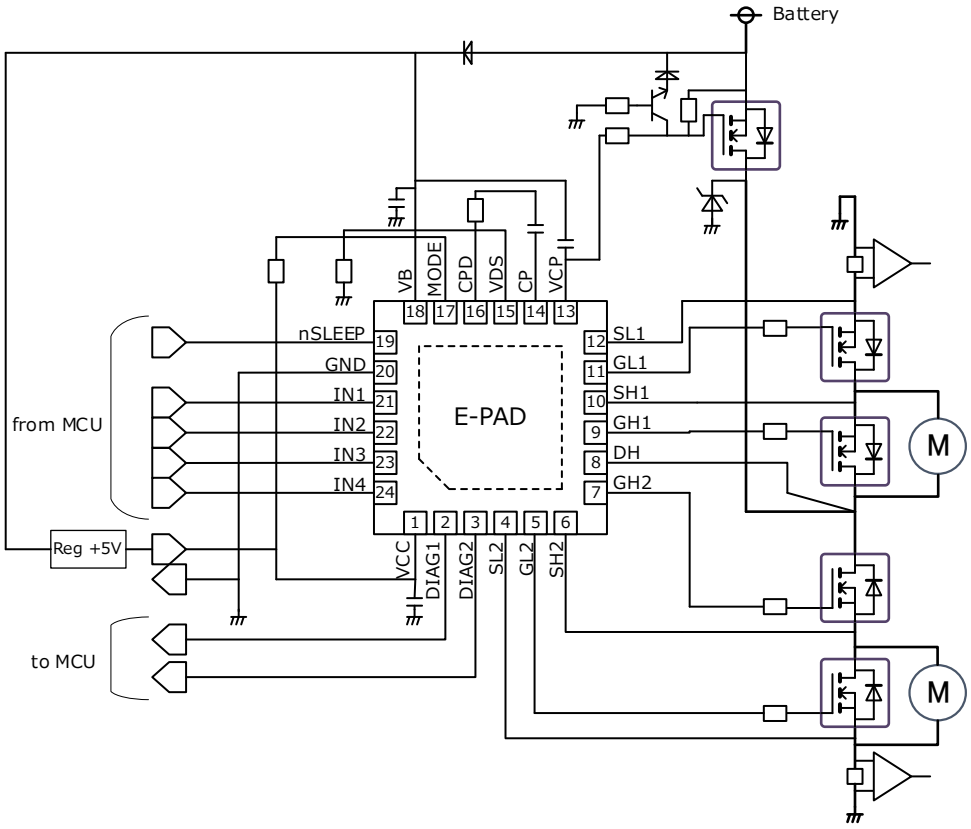


Fig. 26 TB9103FTG Half-bridge mode (Application circuit example)

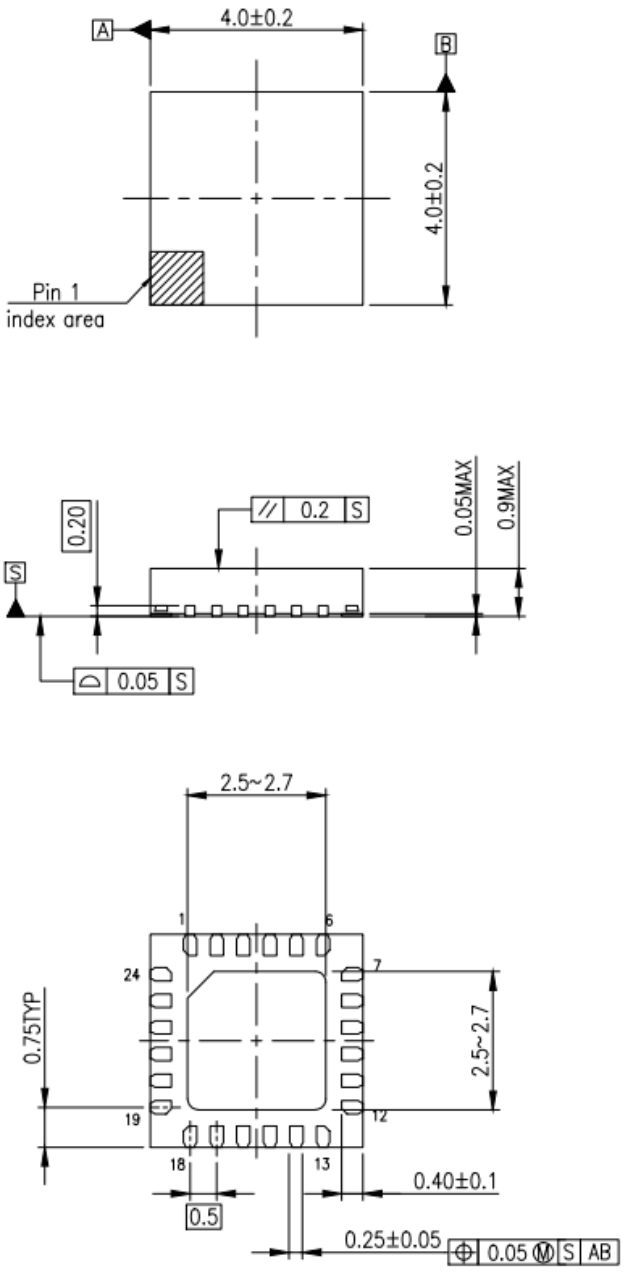
Note1: The above figure is just an example of the application, and it is necessary to fully evaluate the functionality at the time of actual use.

Note2: The above diagram is partially omitted and simplified in order to explain the functions and operations of the IC.

10. Outline drawing

Package dimensions

P-VQFN24-0404-0.50-003 "Unit:mm"



Weight: 0.04g(Typ.)

11. Revision history

Specification Ver.	Specification changes	Date of creation/changes
1.0	Initial Release	2024-08-21

12. IC Usage Considerations

12.1. Notes on Handling of ICs

(1) The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment.

(2) Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure.

12.2. Points to Remember on Handling of ICs

(1) Over current Protection Circuit
Over current protection circuits (referred to as current limiter circuits) do not necessarily protect ICs under all circumstances. If the Over current protection circuits operate against the over current, clear the over current status immediately.

(2) Thermal Shutdown Circuit
Thermal shutdown circuits do not necessarily protect ICs under all circumstances. If the thermal shutdown circuits operate against the over temperature clears the heat generation status immediately.

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