HIGH SPEED DUAL CHANNEL DIGITAL ISOLATORS

DCL52xx00

DCL520C00 / DCL520D00 / DCL521C00 / DCL521D00

1. Applications

- Industrial automation systems
- Motor control
- Inverter
- Switching power supply

2. Description

DCL520C00/DCL520D00/DCL521C00/DCL521D00 are dual-channel digital isolators based on Toshiba complementary metal-oxide semiconductor (CMOS) technology. High reinforced insulation is achieved by Toshiba CMOS technology and the magnetic coupling structure.
DCL520C00/DCL520D00/DCL521C00/DCL521D00 data channels are available in a variety of configuration with a withstand isolation voltage of 3000 Vrms.
DCL520C00/DCL520D00/DCL521C00/DCL521D00 can operate with a temperature range of -40 to 125 °C and a wide supply voltage of 2.25 to 5.5 V.

3. Features

Data rate	: Up to 150 Mbps
Supply voltage	: 2.25 V to 5.5 V
Temperature Range	: -40 °C to 125 °C
Propagation Delay	:10.9 ns Typical (5.0 V operation)
Default Output	: High and Low Options
High CMTI(Typ.)	: 150 kV/μs
Withstand Isolation Voltage	: 3.0 kVrms
Package	: SOIC8-N
Safety-Related Certification	:

UL	: UL1577, File No. E519997
cUL	: CSA Component Acceptance Service Notice No. 5A, File No. E519997
VDE	: DIN EN IEC 60747-17 (VDE V 0884-17) (Planning)
CQC	: (Planning)

Note: When a VDE approved type is needed, please contact your Toshiba sales representative.

Start of commercial production
2025-08

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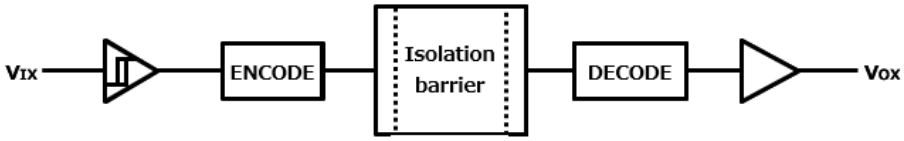
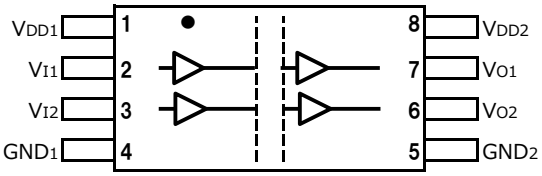
4. Internal Circuit (Simplified Schematic)

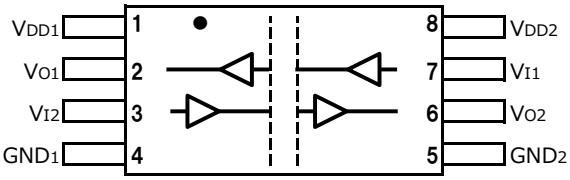


5. Pin configuration and Functions

DCL520C00 / DCL520D00



DCL521C00 / DCL521D00



5.1. Pin Functions

PIN			I/O	DESCRIPTION
NAME	DCL520C00 DCL520D00	DCL521C00 DCL521D00		
V_{DD1}	1	1	—	Power Supply, side 1
V_{I1}	2	7	I	Input, Channel1
V_{I2}	3	3	I	Input, Channel2
GND_1	4	4	—	GND connection for VDD_1, side 1
GND_2	5	5	—	GND connection for VDD_2, side 2
V_{O2}	6	6	O	Output, Channel2
V_{O1}	7	2	O	Output, Channel1
V_{DD2}	8	8	—	Power Supply, side 2

6. Functional Description

(1) DCL520C00/ DCL520D00

V_{DDI}	V_{DDO}	INPUT (V_{Ix})	OUTPUT (V_{Ox})	COMMENTS
PU	PU (Note1)	L	L	Normal Operation
		H	H	
		OPEN	Default	Default mode: When INPUT is open, the corresponding channel output goes to its default logic status. DCL520C00=L, DCL520D00=H
PD		L or OPEN		
PU	PD	X	Undetermined	When VDD_2 is unpowered, a channel output is undetermined.
PD		L or OPEN		
PD	X	H	-	Don't use, since a certain voltage will be output through the internal ESD circuit.

PU= Powered up (VDD≥2.25 V), PD=Powered down (VDD≤1.7 V), H=High Level, L=Low Level, X=don't care
Note1 : The state of the output pin is fixed after 20μs from the time the power supply voltage V_{DDO} is turned on(PD⇒PU).

(2) DCL521C00/ DCL521D00

V_{DDI}	V_{DDO}	INPUT (V_{Ix})	OUTPUT (V_{Ox})	COMMENTS
PU	PU (Note1)	L	L	Normal Operation
		H	H	
		OPEN	Default	Default mode: When INPUT is open, the corresponding channel output goes to its default logic status. DCL521C00=L, DCL521D00=H
PD		L or OPEN		
PU	PD	X	Undetermined	When VDD_2 is unpowered, a channel output is undetermined.
PD		L or OPEN		
PD	X	H	-	Don't use, since a certain voltage will be output through the internal ESD circuit.

PU= Powered up (VDD≥2.25 V), PD=Powered down (VDD≤1.7 V), H=High Level, L=Low Level, X=don't care
Note1 : The state of the output pin is fixed after 20μs from the time the power supply voltage V_{DDO} is turned on(PD⇒PU).

7. Absolute Maximum Ratings (T_a = 25 °C)

PARAMETER	SYMBOL	MIN	MAX	UNIT
Power supply voltage	V_{DD1}, V_{DD2}	-0.5	6.0	V
Input Voltage	V_I	-0.5	V_{DD1}+0.5 (Note1)	V
Output Voltage	V_O	-0.5	V_{DD2}+0.5 (Note1)	V
Output Current	I_O	-15	15	mA
Storage Temperature	T_{stg}	-65	150	°C
Operating Temperature	T_{opr}	-40	125	°C
Soldering Temperature (10 s)	T_{sol}	—	260	°C
Maximum Withstanding Isolation Voltage (60 s)	BV_S	—	3000	Vrms

Note1: Maximum voltage must not exceed 6 V.

8. Recommended Operating Conditions (Note)

PARAMETER	SYMBOL	MIN	MAX	UNIT
Power supply voltage	V_{DD1}, V_{DD2}	2.25	5.5	V
Junction Temperature	T_J	-40	150	°C
Ambient Temperature	T_a	-40	125	°C

Note: The recommended operating conditions are given as a design guide necessary to obtain the intended performance of the device. Each parameter is an independent value. When creating a system design using this device, the electrical characteristics specified in this data sheet should also be considered.

Note: A ceramic capacitor (0.1 μF) should be connected between pin 1 (V_{DD1}) and pin 4 (GND_1) for V_{DD1} and between pin 8 (V_{DD2}) and pin 7 (GND2) for V_{DD2}, and should be the layout on the IC as close as possible (less than 10 mm). Otherwise, the IC may not switch properly.

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9. Electrical Characteristics

9.1. Electrical Characteristics – 5 V Supply

All typical specifications are at T_a=25 °C、V_{DD1}=V_{DD2}=5 V. Minimum/maximum specifications apply over the entire recommended operating range of 4.5 V≤V_{DD1}≤5.5 V, 4.5 V≤V_{DD2}≤5.5 V, and -40 °C≤T_a≤125 °C, unless otherwise noted.

PARAMETER	TEST CONDITIONS	Fig.	SYMBOL	MIN	TYP.	MAX	UNIT
DC SPECIFICATIONS							
Under voltage Lockout	Threshold when supply voltage is rising	12-1	V_{DDxUV+}	—	2.1	2.25	V
	Threshold when supply voltage is falling		V_{DDxUV-}	1.7	1.9	—	
	Supply voltage hysteresis		V_{DDxUVH}	0.1	0.2	—	
Output Voltage Logic High	V_{Ix}=H , I_{OH}=-20 μA	12-2	V_{OH}	V_{DDO}-0.1 (Note1)	V_{DDO} (Note1)	—	V
	V_{Ix}=H , I_{OH}=-4 mA			V_{DDO}-0.4 (Note1)	V_{DDO}-0.2 (Note1)	—	
Output Voltage Logic Low	V_{Ix}=L , I_{OL} =20 μA	12-2	V_{OL}	—	0	0.1	V
	V_{Ix}=L , I_{OL} =4 mA			—	0.2	0.4	
Output impedance	—	12-2	Z_O	—	50	—	Ω
High-level input voltage	—	12-3	V_{IH}	0.7*V_{DDI} (Note1)	—	—	V
Low-level input voltage	—	12-3	V_{IL}	—	—	0.3*V_{DDI} (Note1)	V
Input Voltage Hysteresis	—	12-3	V_{HYS}	—	0.37	—	V
Input Current	V_I= V_{DDI}(Note1) or 0 V	-	I_I	—	—	±10	μA
SWITCHING SPECIFICATIONS							
Data Rate	—	-	t_bps	DC	—	150	Mbps
Pulse Width	—	-	PW	6.6	—	—	ns
Propagation Delay	50 kHz,Duty=50 %, t_r=t_f=2 ns,C_L=15 pF	12-4	t_{PHL} , t_{PLH}	—	10.9	18.3	ns
Pulse Width Distortion	|t_{PHL} – t_{PLH}|	12-4	PWD	—	0.8	2.5	ns
Propagation Delay Skew (Between any two units)(Note2)	—	-	$t_{PSK(PP)}$	—	—	10	ns
Channel Matching	Same Direction	12-4	t_{skCD}	—	—	3.2	ns
	Opposing Direction	12-4	t_{skOD}	—	—	3.6	ns
Output Rise Time	10 % - 90 %	12-4	t_r	—	0.9	—	ns
Output Fall Time	90 % - 10 %	12-4	t_f	—	0.9	—	ns
Common mode transient Immunity	VI= V_{DDI} or 0 V , VCM=1500 V , Ta=25 °C	12-5	CMTI	—	150	—	kV/μs

Note1: V_{DDI}=Input-side V_{DDx} , V_{DDO}=Output-side V_{DDx}
Note2: The propagation delay skew, tpsk, is equal to the magnitude of the difference in propagation delay that will be seen between units at the same given conditions (supply voltage, input current, temperature, etc.).

9.2. Electrical Characteristics – 3.3 V Supply

All typical specifications are at T_a=25 °C、V_{DD1}=V_{DD2}=3.3 V. Minimum/maximum specifications apply over the entire recommended operating range of 3.0 V≤V_{DD1}≤3.6 V, 3.0 V≤V_{DD2}≤3.6 V, and -40 °C≤T_a≤125 °C, unless otherwise noted.

PARAMETER	TEST CONDITIONS	Fig.	SYMBOL	MIN	TYP.	MAX	UNIT
DC SPECIFICATIONS							
Under voltage Lockout	Threshold when supply voltage is rising	12-1	V_{DDxUV+}	—	2.1	2.25	V
	Threshold when supply voltage is falling		V_{DDxUV-}	1.7	1.9	—	
	Supply voltage hysteresis		V_{DDxUVH}	0.1	0.2	—	
Output Voltage Logic High	V_{Ix}=H , I_{OH}=-20 μA	12-2	V_{OH}	V_{DDO}-0.1 (Note1)	V_{DDO} (Note1)	—	V
	V_{Ix}=H , I_{OH}=-4 mA			V_{DDO}-0.4 (Note1)	V_{DDO}-0.2 (Note1)	—	
Output Voltage Logic Low	V_{Ix}=L , I_{OL} =20 μA	12-2	I_{OL}	—	0	0.1	V
	V_{Ix}=L , I_{OL} =4 mA			—	0.2	0.4	
Output impedance	—	12-2	Z_O	—	50	—	Ω
High-level input voltage	—	12-3	V_{IH}	0.7*V_{DDI} (Note1)	—	—	V
Low-level input voltage	—	12-3	V_{IL}	—	—	0.3*V_{DDI} (Note1)	V
Input Voltage Hysteresis	—	12-3	V_{HYS}	—	0.32	—	V
Input Current	V_I= V_{DDI}(Note1) or 0 V	-	I_I	—	—	±10	μA
SWITCHING SPECIFICATIONS							
Data Rate	—	-	t_bps	DC	—	150	Mbps
Pulse Width	—	-	PW	6.6	—	—	ns
Propagation Delay	50 kHz,Duty=50 %, t_r=t_f=2 ns,C_L=15 pF	12-4	t_{PHL} , t_{PLH}	—	11.6	19.1	ns
Pulse Width Distortion	|t_{PHL} – t_{PLH}|	12-4	PWD	—	0.8	2.5	ns
Propagation Delay Skew (Between any two units)(Note2)	—	-	$t_{PSK(PP)}$	—	—	10	ns
Channel Matching	Same Direction	12-4	t_{skCD}	—	—	3.3	ns
	Opposing Direction	12-4	t_{skOD}	—	—	3.7	ns
Output Rise Time	10 % - 90 %	12-4	t_r	—	0.8	—	ns
Output Fall Time	90 % - 10 %	12-4	t_f	—	0.8	—	ns
Common mode transient Immunity	VI= V_{DDI} or 0 V , VCM=1500 V , Ta=25 °C	12-5	CMTI	—	150	—	kV/μs

Note1: V_{DDI}=Input-side V_{DDx} , V_{DDO}=Output-side V_{DDx}
Note2: The propagation delay skew, tpsk, is equal to the magnitude of the difference in propagation delay that will be seen between units at the same given conditions (supply voltage, input current, temperature, etc.)

9.3. Electrical Characteristics – 2.5 V Supply

All typical specifications are at T_a=25 °C、V_{DD1}=V_{DD2}=2.5 V. Minimum/maximum specifications apply over the entire recommended operating range of 2.25 V≤V_{DD1}≤2.75 V, 2.25 V≤V_{DD2}≤2.75 V, and -40 °C≤T_a≤125 °C, unless otherwise noted.

PARAMETER	TEST CONDITIONS	Fig.	SYMBOL	MIN	TYP.	MAX	UNIT
DC SPECIFICATIONS							
Under voltage Lockout	Threshold when supply voltage is rising	12-1	V_{DDxUV+}	—	2.1	2.25	V
	Threshold when supply voltage is falling		V_{DDxUV-}	1.7	1.9	—	
	Supply voltage hysteresis		V_{DDxUVH}	0.1	0.2	—	
Output Voltage Logic High	V_{Ix}=H , I_{OH}=-20 μA	12-2	V_{OH}	V_{DDO}-0.1 (Note1)	V_{DDO} (Note1)	—	V
	V_{Ix}=H , I_{OH}=-4 mA			V_{DDO}-0.4 (Note1)	V_{DDO}-0.2 (Note1)	—	
Output Voltage Logic Low	V_{Ix}=L , I_{OL} =20 μA	12-2	I_{OL}	—	0	0.1	V
	V_{Ix}=L , I_{OL} =4 mA			—	0.2	0.4	
Output impedance	—	12-2	Z_O	—	50	—	Ω
High-level input voltage	—	12-3	V_{IH}	0.7*V_{DDI} (Note1)	—	—	V
Low-level input voltage	—	12-3	V_{IL}	—	—	0.3*V_{DDI} (Note1)	V
Input Voltage Hysteresis	—	12-3	V_{HYS}	—	0.32	—	V
Input Current	V_I= V_{DDI}(Note1) or 0 V	-	I_I	—	—	±10	μA
SWITCHING SPECIFICATIONS							
Data Rate	—	-	t_bps	DC	—	150	Mbps
Pulse Width	—	-	PW	6.6	—	—	ns
Propagation Delay	50 kHz,Duty=50 %, t_r=t_f=2 ns,C_L=15 pF	12-4	t_{PHL} , t_{PLH}	—	12.6	21.0	ns
Pulse Width Distortion	|t_{PHL} – t_{PLH}|	12-4	PWD	—	1.0	2.5	ns
Propagation Delay Skew (Between any two units)(Note2)	—	-	$t_{PSK(PP)}$	—	—	10	ns
Channel Matching	Same Direction	12-4	t_{skCD}	—	—	3.5	ns
	Opposing Direction	12-4	t_{skOD}	—	—	3.9	ns
Output Rise Time	10 % - 90 %	12-4	t_r	—	0.8	—	ns
Output Fall Time	90 % - 10 %	12-4	t_f	—	0.8	—	ns
Common mode transient Immunity	VI= V_{DDI} or 0 V , VCM=1500 V , Ta=25 °C	12-5	CMTI	—	150	—	kV/μs

Note1: V_{DDI}=Input-side V_{DDx} , V_{DDO}=Output-side V_{DDx}
Note2: The propagation delay skew, tpsk, is equal to the magnitude of the difference in propagation delay that will be seen between units at the same given conditions (supply voltage, input current, temperature, etc.)

9.4. Supply Current Characteristics – 5 V Supply

All typical specifications are at T_a=25 °C、V_{DD1}=V_{DD2}=5 V. Minimum/maximum specifications apply over the entire recommended operating range of 4.5 V≤V_{DD1}≤5.5 V, 4.5 V≤V_{DD2}≤5.5 V, and -40 °C≤T_a≤125 °C, unless otherwise noted.

(1) DCL520X00

PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP.	MAX	UNIT
Supply Current (DC Signal)	VI=0(DCL520C00), VI=1(DCL520D00)	$I_{DD1(Q)}$	—	1.1	1.7	mA
		$I_{DD2(Q)}$	—	2.6	4	mA
	VI=0(DCL520D00), VI=1(DCL520C00)	$I_{DD1(Q)}$	—	10.5	16	mA
		$I_{DD2(Q)}$	—	2.9	4.3	mA
1 Mbps	f_{CLK}=500 kHz, duty=50 % cycle square wave. C_L=15 pF	$I_{DD1(1)}$	—	5.9	9.2	mA
		$I_{DD2(1)}$	—	2.8	4.4	mA
25 Mbps	f_{CLK}=12.5 MHz, duty=50 % cycle square wave. C_L=15 pF	$I_{DD1(25)}$	—	5.9	8.7	mA
		$I_{DD2(25)}$	—	5.2	7.4	mA
100 Mbps	f_{CLK}=50 MHz, duty=50 % cycle square wave. C_L=15 pF	$I_{DD1(100)}$	—	6.9	9.6	mA
		$I_{DD2(100)}$	—	14	19.4	mA

(2) DCL521X00

PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP.	MAX	UNIT
Supply Current (DC Signal)	VI=0(DCL521C00), VI=1(DCL521D00)	$I_{DD1(Q)}$	—	2.0	3.0	mA
		$I_{DD2(Q)}$	—	2.0	3.0	mA
	VI=0(DCL521D00), VI=1(DCL521C00)	$I_{DD1(Q)}$	—	7.2	10.4	mA
		$I_{DD2(Q)}$	—	7.2	10.4	mA
1 Mbps	f_{CLK}=500 kHz, duty=50 % cycle square wave. C_L=15 pF	$I_{DD1(1)}$	—	4.6	6.8	mA
		$I_{DD2(1)}$	—	4.6	6.8	mA
25 Mbps	f_{CLK}=12.5 MHz, duty=50 % cycle square wave. C_L=15 pF	$I_{DD1(25)}$	—	6.1	8.5	mA
		$I_{DD2(25)}$	—	6.1	8.5	mA
100 Mbps	f_{CLK}=50 MHz, duty=50 % cycle square wave. C_L=15 pF	$I_{DD1(100)}$	—	11.1	15.6	mA
		$I_{DD2(100)}$	—	11.1	15.6	mA

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9.5. Supply Current Characteristics – 3.3 V Supply

All typical specifications are at T_a=25 °C、V_{DD1}=V_{DD2}=3.3 V. Minimum/maximum specifications apply over the entire recommended operating range of 3.0 V≤V_{DD1}≤3.6 V, 3.0 V≤V_{DD2}≤3.6 V, and -40 °C≤T_a≤125° C, unless otherwise noted.

(1) DCL520X00

PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP.	MAX	UNIT
Supply Current (DC Signal)	VI=0(DCL520C00), VI=1(DCL520D00)	$I_{DD1(Q)}$	—	1.1	1.5	mA
		$I_{DD2(Q)}$	—	2.6	3.8	mA
	VI=0(DCL520D00), VI=1(DCL520C00)	$I_{DD1(Q)}$	—	10.4	15.5	mA
		$I_{DD2(Q)}$	—	2.8	4.2	mA
1 Mbps	f_{CLK}=500 kHz, duty=50 % cycle square wave. C_L=15 pF	$I_{DD1(1)}$	—	5.7	9	mA
		$I_{DD2(1)}$	—	2.7	4.2	mA
25 Mbps	f_{CLK}=12.5 MHz, duty=50 % cycle square wave. C_L=15 pF	$I_{DD1(25)}$	—	5.7	8.3	mA
		$I_{DD2(25)}$	—	4.4	6.4	mA
100 Mbps	f_{CLK}=50 MHz, duty=50 % cycle square wave. C_L=15 pF	$I_{DD1(100)}$	—	6.5	8.9	mA
		$I_{DD2(100)}$	—	9.2	15.7	mA

(2) DCL521X00

PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP.	MAX	UNIT
Supply Current (DC Signal)	VI=0(DCL521C00), VI=1(DCL521D00)	$I_{DD1(Q)}$	—	2.0	2.8	mA
		$I_{DD2(Q)}$	—	2.0	2.8	mA
	VI=0(DCL521D00), VI=1(DCL521C00)	$I_{DD1(Q)}$	—	7.1	10.2	mA
		$I_{DD2(Q)}$	—	7.1	10.2	mA
1 Mbps	f_{CLK}=500 kHz, duty=50 % cycle square wave. C_L=15 pF	$I_{DD1(1)}$	—	4.5	6.6	mA
		$I_{DD2(1)}$	—	4.5	6.6	mA
25 Mbps	f_{CLK}=12.5 MHz, duty=50 % cycle square wave. C_L=15 pF	$I_{DD1(25)}$	—	5.5	7.6	mA
		$I_{DD2(25)}$	—	5.5	7.6	mA
100 Mbps	f_{CLK}=50 MHz, duty=50 % cycle square wave. C_L=15 pF	$I_{DD1(100)}$	—	8.7	12.3	mA
		$I_{DD2(100)}$	—	8.7	12.3	mA

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9.6. Supply Current Characteristics – 2.5 V Supply

All typical specifications are at T_a=25 °C、V_{DD1}=V_{DD2}=2.5 V. Minimum/maximum specifications apply over the entire recommended operating range of 2.25 V≤V_{DD1}≤2.75 V, 2.25 V≤V_{DD2}≤2.75 V, and -40 °C≤T_a≤125° C, unless otherwise noted.

(1) DCL520X00

PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP.	MAX	UNIT
Supply Current (DC Signal)	VI=0(DCL520C00), VI=1(DCL520D00)	$I_{DD1(Q)}$	—	0.98	1.5	mA
		$I_{DD2(Q)}$	—	2.52	3.7	mA
	VI=0(DCL520D00), VI=1(DCL520C00)	$I_{DD1(Q)}$	—	10.4	15.4	mA
		$I_{DD2(Q)}$	—	2.8	4.1	mA
1 Mbps	f_{CLK}=500 kHz, duty=50 % cycle square wave. C_L=15 pF	$I_{DD1(1)}$	—	5.6	8.8	mA
		$I_{DD2(1)}$	—	2.7	4.1	mA
25 Mbps	f_{CLK}=12.5 MHz, duty=50 % cycle square wave. C_L=15 pF	$I_{DD1(25)}$	—	5.5	8	mA
		$I_{DD2(25)}$	—	4	5.9	mA
100 Mbps	f_{CLK}=50 MHz, duty=50 % cycle square wave. C_L=15 pF	$I_{DD1(100)}$	—	6.4	8.4	mA
		$I_{DD2(100)}$	—	7.5	13.3	mA

(2) DCL521X00

PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP.	MAX	UNIT
Supply Current (DC Signal)	VI=0(DCL521C00), VI=1(DCL521D00)	$I_{DD1(Q)}$	—	1.9	2.8	mA
		$I_{DD2(Q)}$	—	1.9	2.8	mA
	VI=0(DCL521D00), VI=1(DCL521C00)	$I_{DD1(Q)}$	—	7.1	10.1	mA
		$I_{DD2(Q)}$	—	7.1	10.1	mA
1 Mbps	f_{CLK}=500 kHz, duty=50 % cycle square wave. C_L=15 pF	$I_{DD1(1)}$	—	4.4	6.5	mA
		$I_{DD2(1)}$	—	4.4	6.5	mA
25 Mbps	f_{CLK}=12.5 MHz, duty=50 % cycle square wave. C_L=15 pF	$I_{DD1(25)}$	—	5.2	7.2	mA
		$I_{DD2(25)}$	—	5.2	7.2	mA
100 Mbps	f_{CLK}=50 MHz, duty=50 % cycle square wave. C_L=15 pF	$I_{DD1(100)}$	—	7.6	10.9	mA
		$I_{DD2(100)}$	—	7.6	10.9	mA

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10. Insulation Specifications

PARAMETER	Symbol	TEST CONDITIONS	VALUE	UNIT
Minimum External Clearance	CLR	—	3.8	mm
Minimum External Creepage	CPG	—	3.8	mm
Distance Through The Insulation	DTI	—	17	μm
Comparative Tracking Index	CTI	—	400	V
Material Group	—	According to IEC 60664-1	Ⅱ	—
Overvoltage Category Per IEC 60664-1	—	Related Mains Voltage ≤ 150 V_{RMS}	I-IV	—
	—	Related Mains Voltage ≤ 300 V_{RMS}	I-III	—
DIN EN IEC 60747-17; EN IEC 60747-17				
Maximum Repetitive Peak Isolation Voltage	V_{IORM}	AC voltage (bipolar)	566	V_{PK}
Maximum Transient Isolation Voltage	V_{IOTM}	$V_{TEST} = V_{IOTM}$, t = 60 s (qualification) , $V_{TEST} = 1.2 \times V_{IOTM}$, t = 1 s (100 % production)	4243	V_{PK}
Maximum Impulse Voltage	V_{IMP}	IEC 62368-1 1.2/50 μs waveform	5000	V_{PK}
Maximum surge isolation Voltage	V_{IOSM}	Test method per IEC 62368-1, 1.2/50 μs waveform, $V_{TEST} \geq 1.3 \times VIMP$ (qualification) , min.10 kV	10000	V_{PK}
Apparent charge measuring voltage	$V_{pd(m)}$	Method A, After Input/Output safety test subgroup2&3, VIORM × 1.2 = Vpd (m), tini = 60 sec, tm = 10 sec, partial discharge < 5 pC	679	V_{PK}
		Method A, After environmental tests subgroup 1, VIORM × 1.6 = Vpd (m), tini = 60 sec, tm = 10 sec, partial discharge < 5 pC	906	
		Method B2; At routine test (100 % production) and preconditioning (type test) VIORM × 1.875 = Vpd (m), 100 % production test, tini = tm = 1 sec, partial discharge < 5 pC	1062	
Barrier capacitance, input to output	C_{IO}	f = 1 MHz	0.8	pF
Input Capacitance	C_I	VIx	1.9	pF
Isolation Resistance	R_{IO}	V_{IO} = 500 V, T_A = 25 °C	$>10^{12}$	Ω
		V_{IO} = 500 V, 100 °C ≤ T_A ≤ 125 °C	$\geq 10^{11}$	
		V_{IO} = 500 V at T_S = 150 °C	$\geq 10^{9}$	
Pollution Degree	—	—	2	—
Climatic Category	—	—	40/125/21	—
UL 1577				
Maximum Withstand Isolation Voltage	V_{ISO}	$V_{TEST} = V_{ISO}$, t = 60 s (qualification), $V_{TEST} = 1.2 \times V_{ISO}$, t = 1 s (100 % production)	3000	Vrms

11. Safety Limiting Values

PARAMETER	Symbol	TEST CONDITIONS	Value	Unit
Safety Input, Output Or Supply Current	I_S	V_{DD1}=V_{DD2}=5.5 V, Tj=150 °C,Ta=25 °C	255	mA
		V_{DD1}=V_{DD2}=3.6 V, Tj=150 °C,Ta=25 °C	390	mA
		V_{DD1}=V_{DD2}=2.75 V, Tj=150 °C,Ta=25 °C	510	mA
Safety Input, Output Or Total Power	P_S	Tj=150 °C, Ta=25 °C	1403	W
Maximum Safety Temperature	T_S	-	150	°C

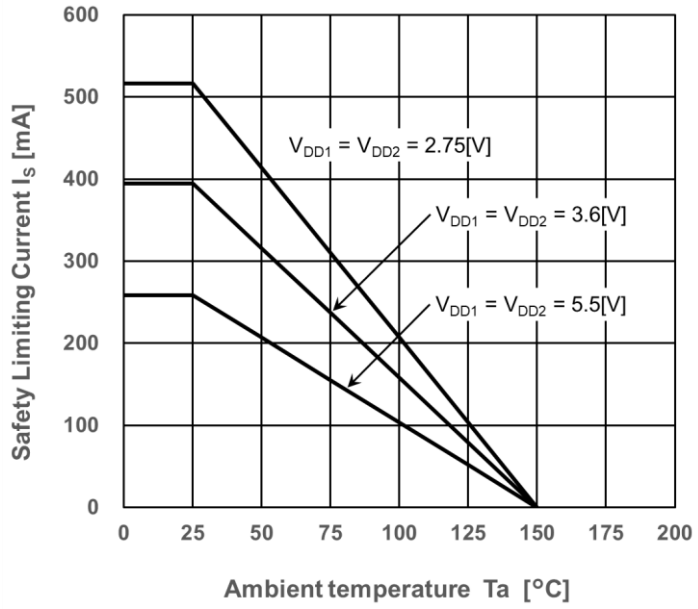
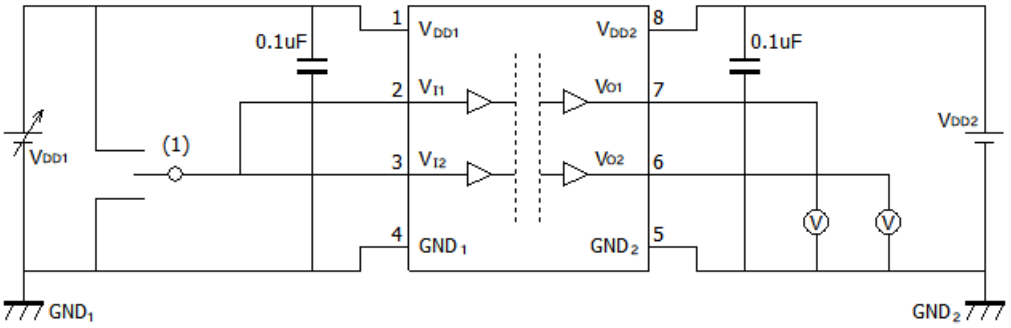


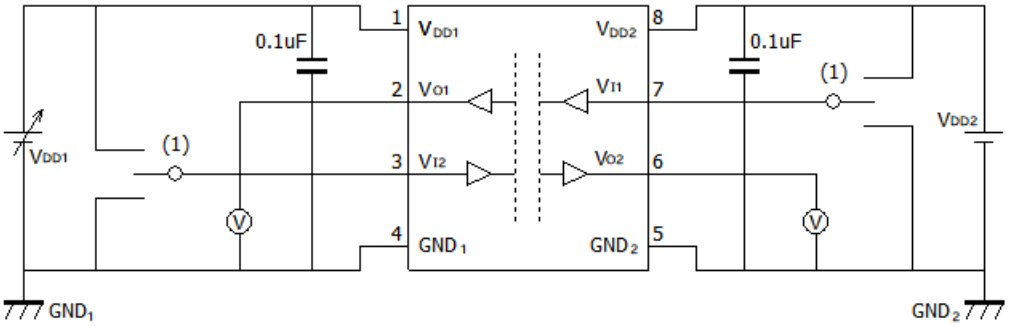
Fig. 11.1 Thermal Derating Curve for Safety Limiting Current−Ta

12. Test Circuit



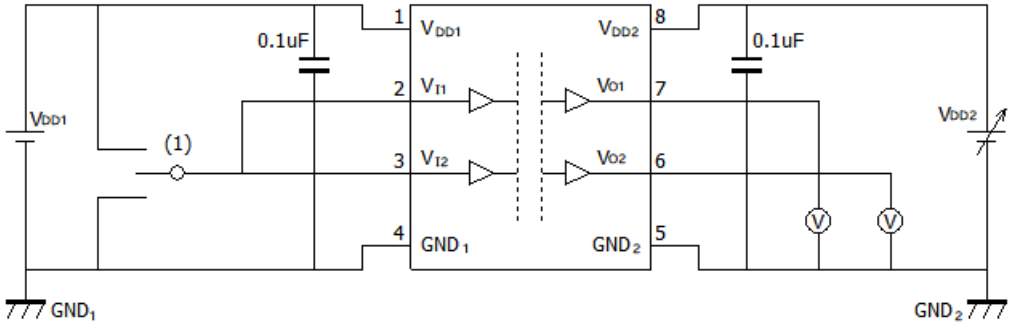
1: Default=L：V_{DD}, Default=H：GND

Fig. 12.1.1 DCL520C00/DCL520D00 V_{DD1UV+}/ V_{DD1UV-} Test Circuit



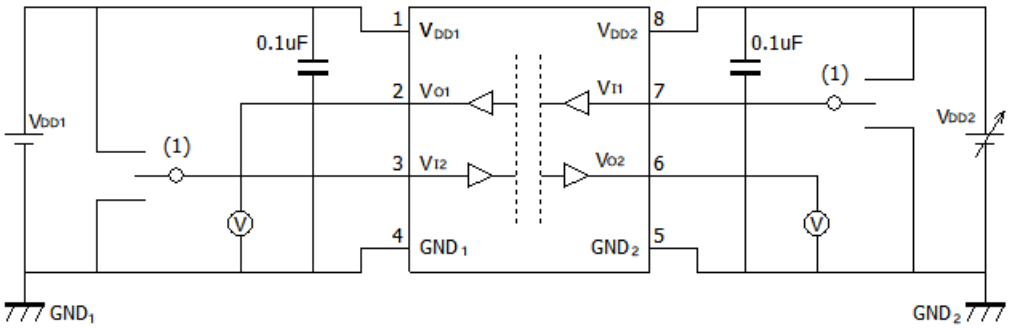
1: Default=L：V_{DD}, Default=H：GND

Fig. 12.1.2 DCL521C00/DCL521D00 V_{DD1UV+}/ V_{DD1UV-} Test Circuit



1: Default=L：V_{DD}, Default=H：GND

Fig. 12.1.3 DCL520C00/DCL520D00 V_{DD2UV+}/ V_{DD2UV-} Test Circuit



1: Default=L：V_{DD}, Default=H：GND

Fig. 12.1.4 DCL521C00/DCL521D00 V_{DD2UV+}/ V_{DD2UV-} Test Circuit

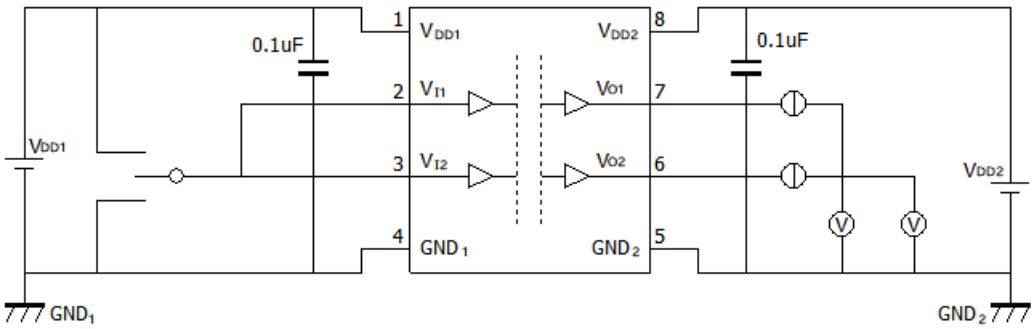


Fig. 12.2.1 DCL520C00/DCL520D00 V_{OH}/V_{OL} Test Circuit

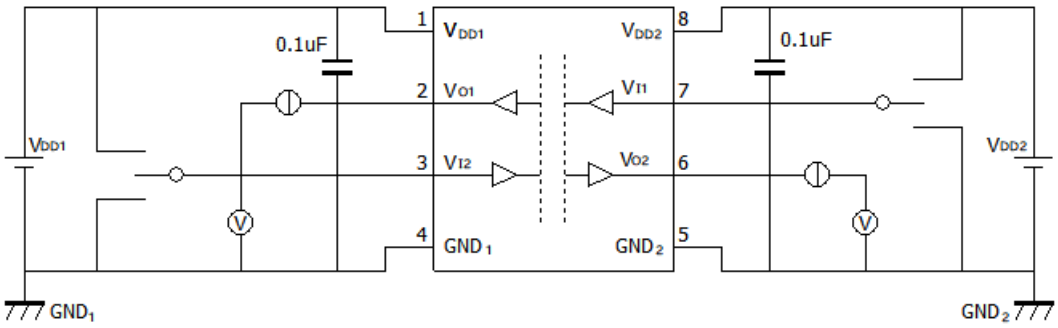


Fig. 12.2.2 DCL521C00/DCL521D00 V_{OH}/V_{OL} Test Circuit

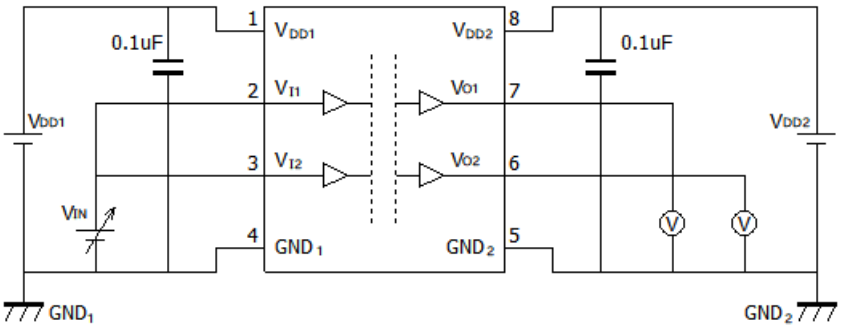


Fig. 12.3.1 DCL520C00/DCL520D00 V_{IH}/V_{IL} Test Circuit

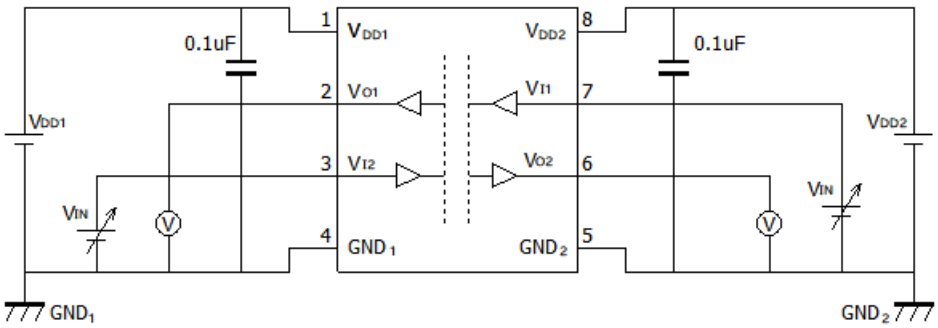
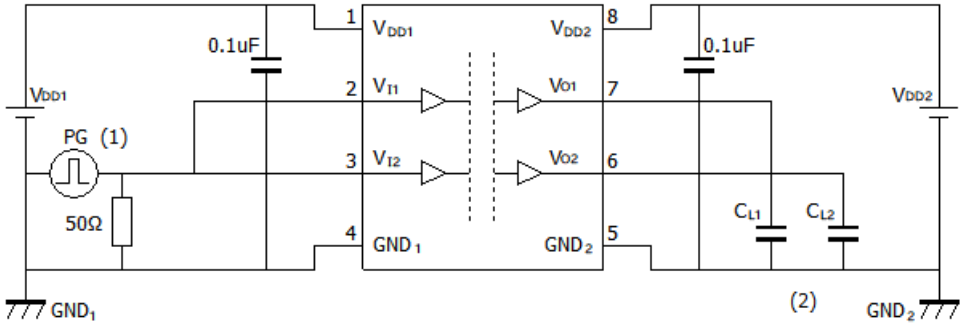
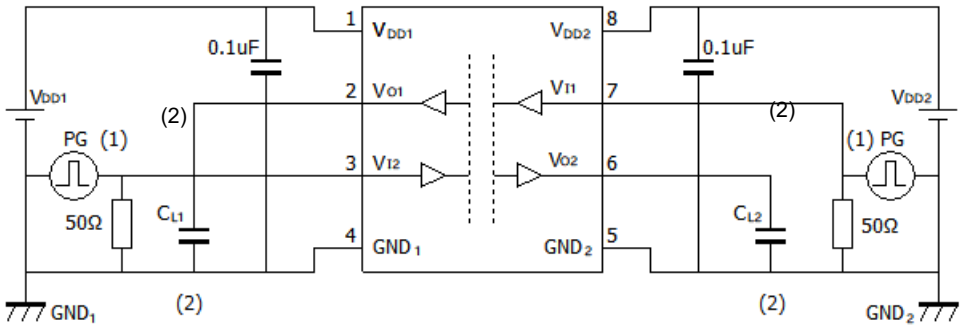


Fig. 12.3.2 DCL521C00/DCL521D00 V_{IH}/V_{IL} Test Circuit



1: The input pulse is supplied by a generator having the following characteristics: PRR≤50 kHz, 50 % duty cycle, tr≤2 ns, tf≤2 ns, Z_O =50 Ω. At the input, 50 Ω resistor is required to terminate input generator signal. It is needed not in actual application.
2: CLx=15 pF includes instrumentation and fixture capacitance.

Fig.12.4.1 DCL520C00/DCL520D00 Switching Test Circuit



1: The input pulse is supplied by a generator having the following characteristics: PRR≤50 kHz, 50 % duty cycle, tr≤2 ns, tf≤2 ns, Z_O =50 Ω. At the input, 50 Ω resistor is required to terminate input generator signal. It is needed not in actual application.
2: CLx=15 pF includes instrumentation and fixture capacitance.

Fig.12.4.2 DCL521C00/DCL521D00 Switching Test Circuit

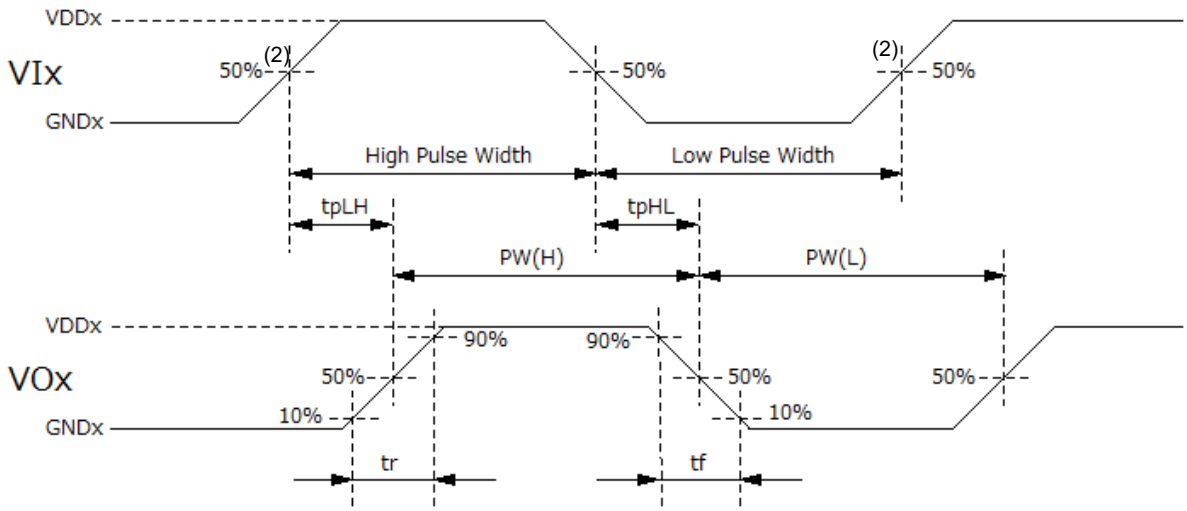
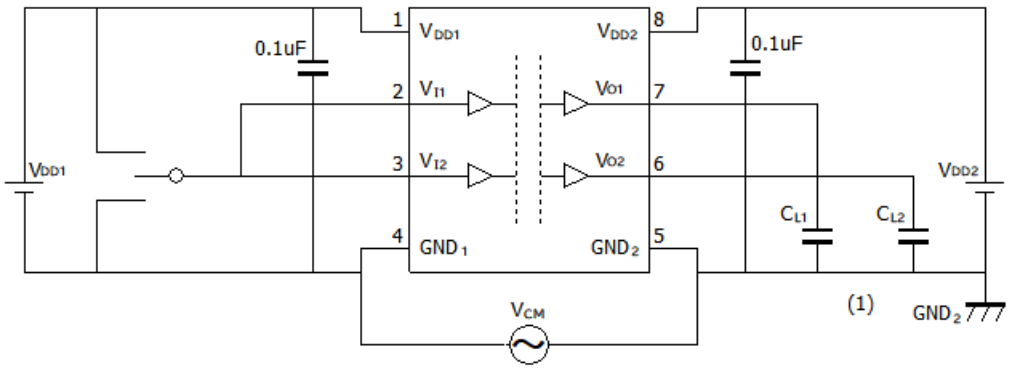
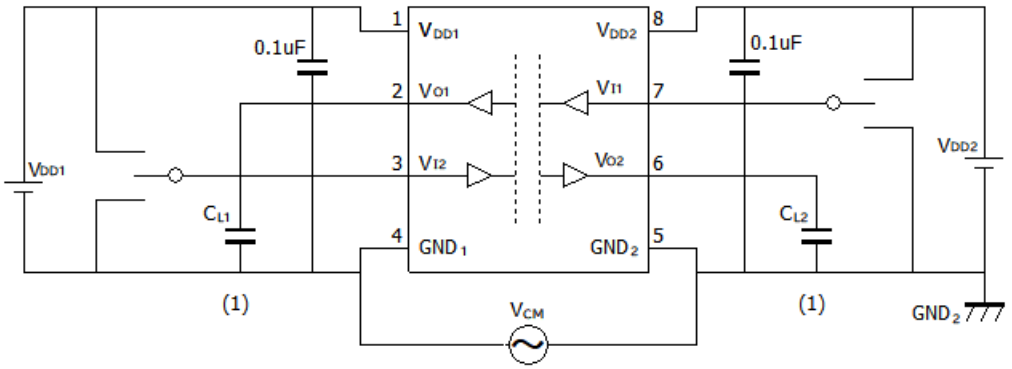


Fig.12.4.3 Switching Test Circuit and Voltage Waveforms



1: CLx=15 pF includes instrumentation and fixture capacitance.

Fig.12.5.1 DCL520C00/DCL520D00 Common-Mode Transient Immunity Test Circuit



1: CLx=15 pF includes instrumentation and fixture capacitance.

Fig.12.5.2 DCL521C00/DCL521D00 Common-Mode Transient Immunity Test Circuit

13. Characteristics Curves

Note: The following characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

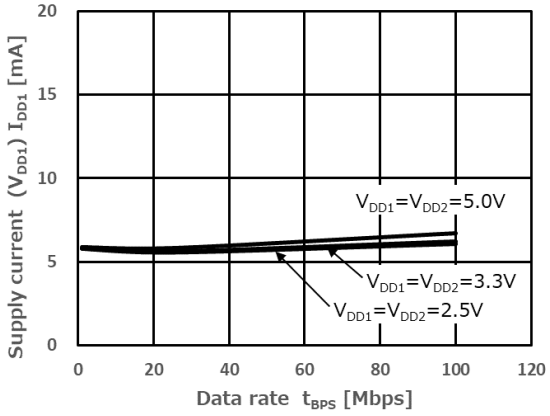


Fig.13.1 DCL520x00 I_{DD1} Supply Current—Data rate

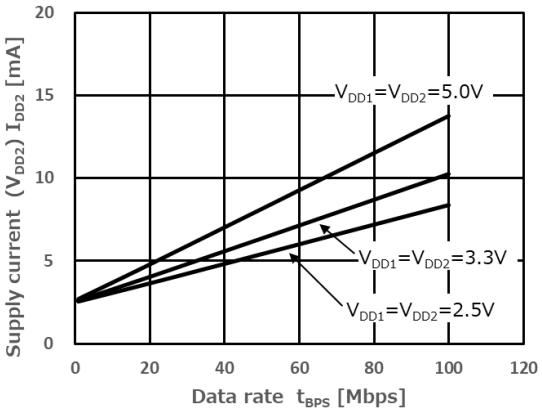


Fig.13.2 DCL520xx00 I_{DD2} Supply Current—Data rate

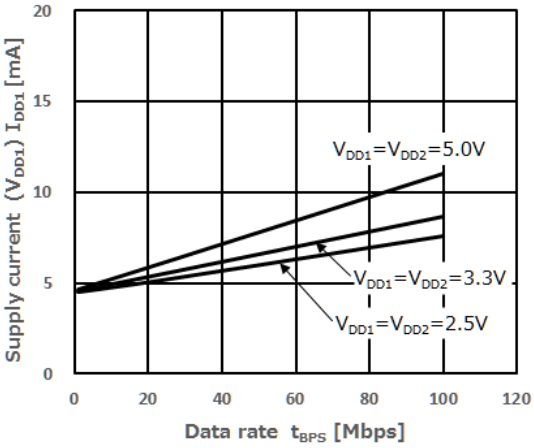


Fig.13.3 DCL521x00 I_{DD1} Supply Current—Data rate

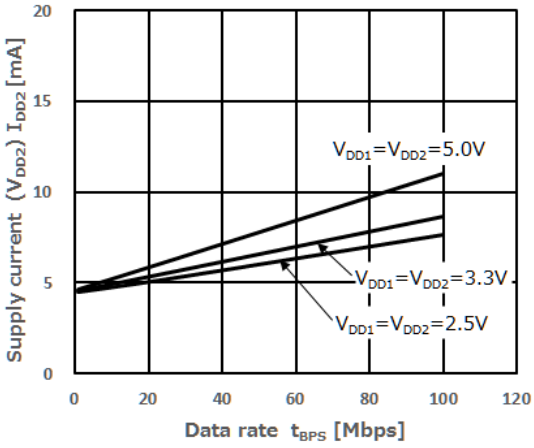


Fig.13.4 DCL521xx00 I_{DD2} Supply Current—Data rate

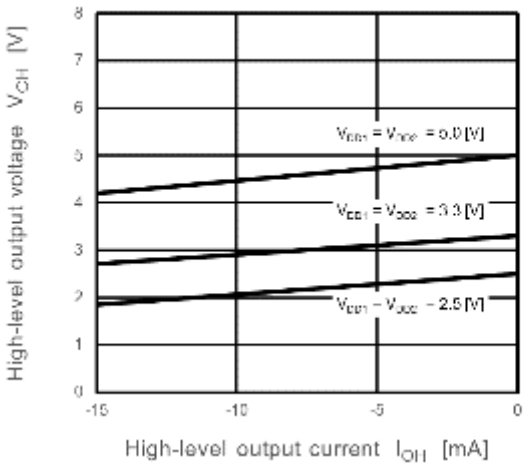


Fig.13.5 VOH-IOH

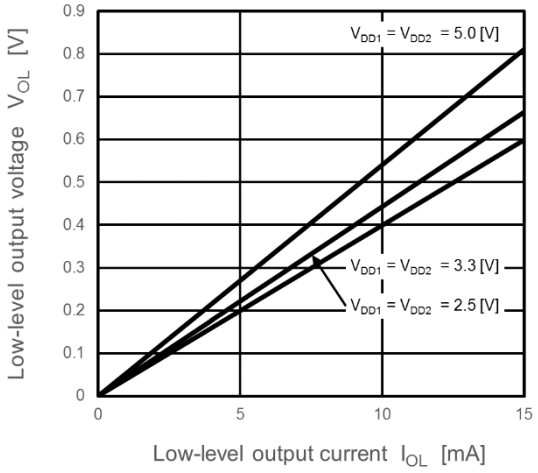


Fig.13.6 VOL-IOL

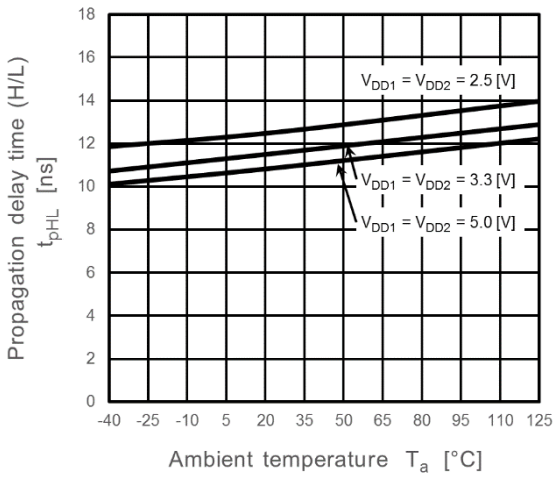


Fig.13.7 Propagation Delay Time t_{PHL} -Ta

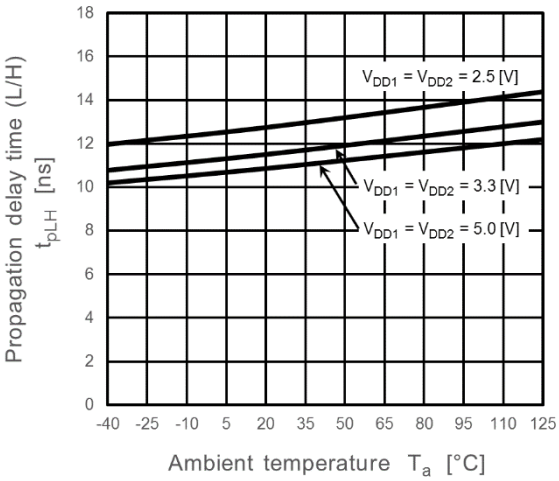


Fig.13.8 Propagation Delay Time t_{PLH} -Ta

14. Application Note

14-1. Eye diagram

The following figure shows typical eye diagrams of DCL521xx00 at the maximum data rate of 150 Mbps with pseudorandom bit sequences (PRBS), supply voltage 3.0V for reference only.

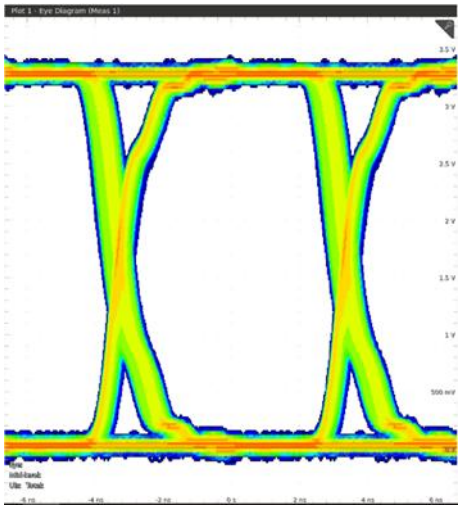


Fig.14.1 DCL521x00 Eye diagram at 150Mbps

14-2. PCB layout

A ceramic capacitor (0.1 μF) should be connected between pin 1 (V_{DD1}) and pin 2 (GND_1) for V_{DD1} and between pin 16 (V_{DD2}) and pin 15 (GND_2) for V_{DD2}, and it should be the layout on the IC as close as possible (less than 10mm). Otherwise, the IC may not operate properly.

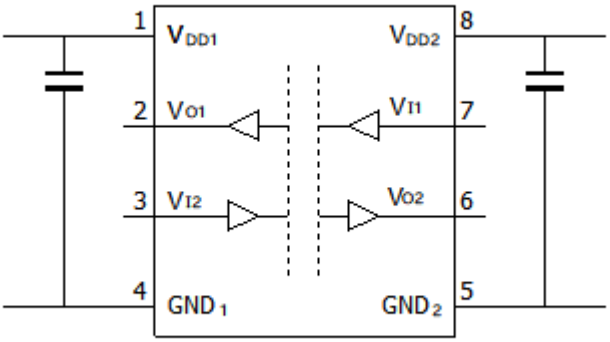
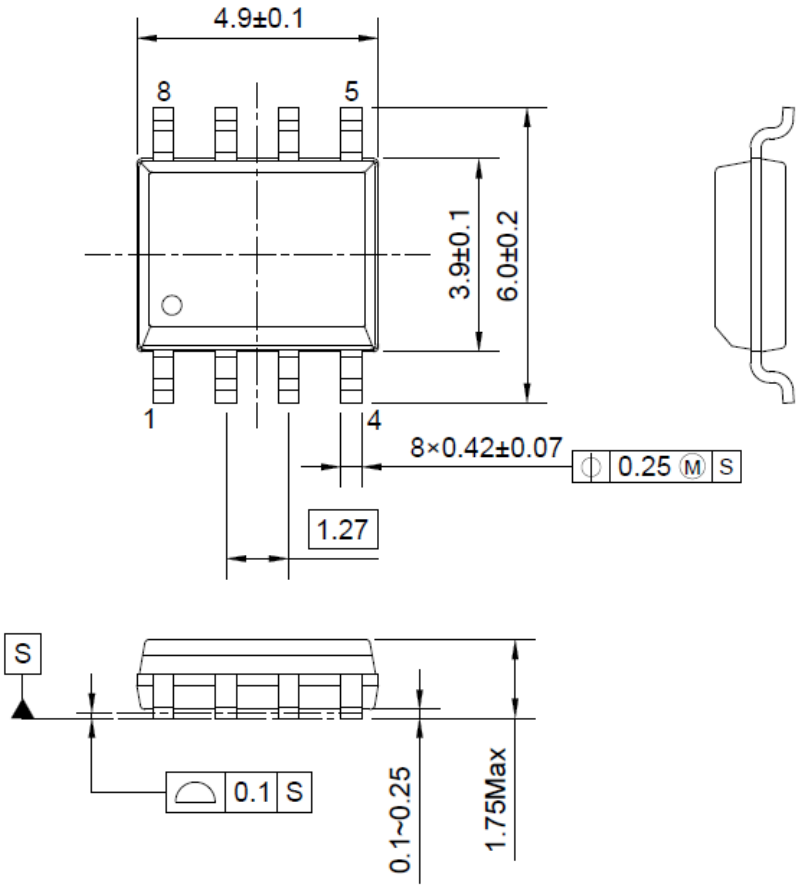
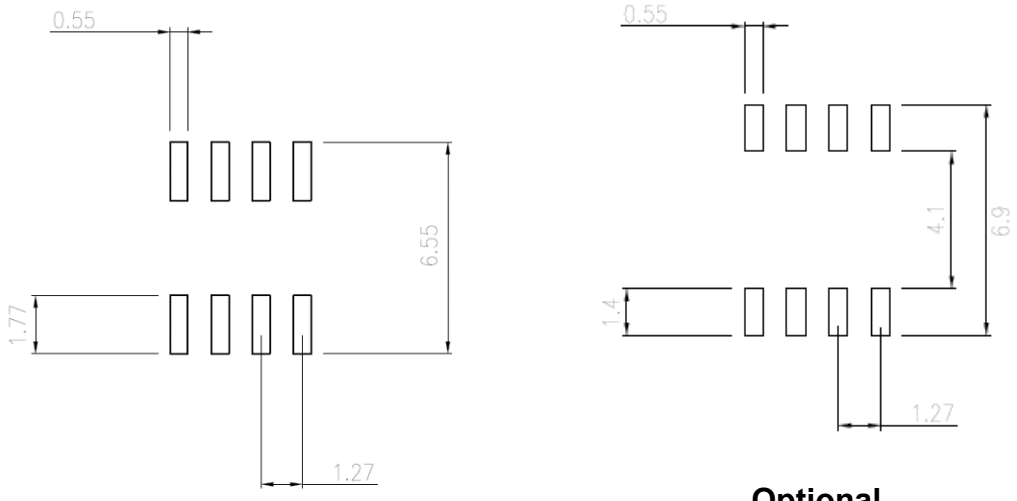


Fig.14.2 Recommended Printed Circuit Board Layout

15. Package Information

Implementation category	Surface Mount
Pin Number	8
Weight (g)	0.07 (Typical)
Package Dimension (mm) Width × Length × Height	4.9 ×6.0×1.75 (Max)
Package Dimension (mm)	
Land Pattern Example (mm) [for reference only]	 **Nominal** **Optional** Large interval between primary-secondary side

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