

MOSFETs Silicon P-Channel MOS (U-MOSVII)

# SSM6P78FU

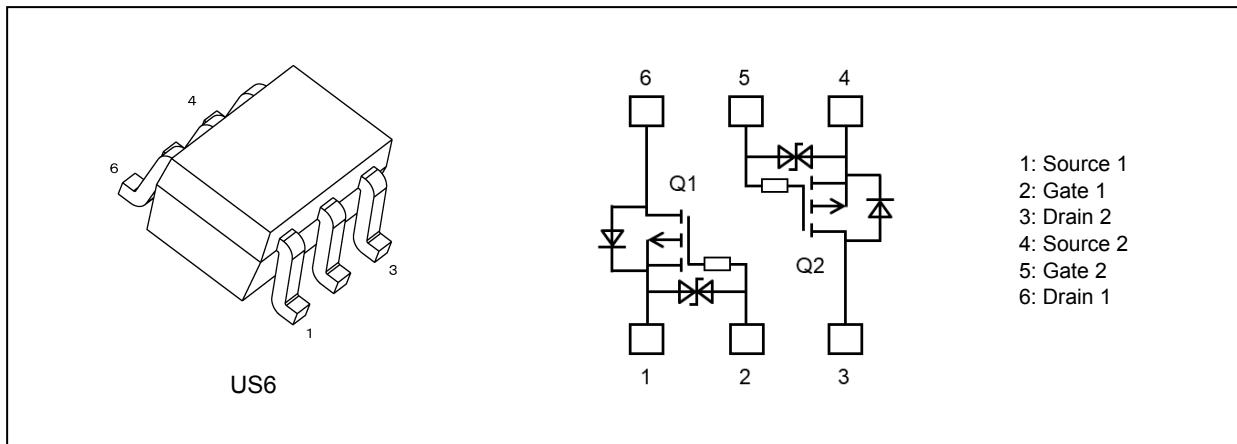
### 1. Applications

- Analog Switches

### 2. Features

- (1) 1.2 V drive
- (2) Low drain-source on-resistance
  - :  $R_{DS(ON)} = 3.2 \Omega$  (typ.) (@ $V_{GS} = -1.2$  V)
  - $R_{DS(ON)} = 2.3 \Omega$  (typ.) (@ $V_{GS} = -1.5$  V)
  - $R_{DS(ON)} = 2.0 \Omega$  (typ.) (@ $V_{GS} = -1.8$  V)
  - $R_{DS(ON)} = 1.5 \Omega$  (typ.) (@ $V_{GS} = -2.5$  V)
  - $R_{DS(ON)} = 1.1 \Omega$  (typ.) (@ $V_{GS} = -4.5$  V)
- (3) Low leakage current
- (4) P-ch 2-in-1

### 3. Packaging and Internal Circuit



Start of commercial production  
2024-04

### 4. Absolute Maximum Ratings (Note) (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$ )(Q1, Q2 Common)

Characteristics	Symbol	Rating	Unit
Drain-source voltage	$V_{DSS}$	-20	V
Gate-source voltage	$V_{GSS}$	$\pm 10$	
Drain current (DC) (Note 1)	$I_D$	-250	mA
Drain current (pulsed) (Note 1)	$I_{DP}$	-600	
Power dissipation (Note 2)	$P_D$	285	mW
Channel temperature	$T_{ch}$	150	$^\circ\text{C}$
Storage temperature	$T_{stg}$	-55 to 150	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Ensure that the channel temperature does not exceed  $150\text{ }^\circ\text{C}$ .

Note 2: Mounted on an FR4 board ( $25.4\text{ mm} \times 25.4\text{ mm} \times 1.6\text{ mm}$ , Cu pad:  $645\text{ mm}^2$ )(Total rating)

Note: This transistor is sensitive to electrostatic discharge and should be handled with care.

Note: The MOSFETs in this device are sensitive to electrostatic discharge. When handling this device, the worktables, operators, soldering irons and other objects should be protected against anti-static discharge.

Note: The channel-to-ambient thermal resistance,  $R_{th(ch-a)}$ , and the drain power dissipation,  $P_D$ , vary according to the board material, board area, board thickness and pad area. When using this device, be sure to take heat dissipation fully into account.

### 5. Electrostatic Discharge Test ( $T_a=25\text{ }^\circ\text{C}$ )

Apply voltage	Failure	Test conditions
$\pm 2000\text{ V}$	0/10 pcs	$C = 100\text{ pF}$ , $R = 1.5\text{ k}\Omega$ (JEITA ED-4701)

Note: Conducted Electrostatic Discharge Test based on JEITA ED-4701 standard, and confirmed above result.

### 6. Electrical Characteristics

#### 6.1. Static Characteristics (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$ )(Q1, Q2 Common)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 5\text{ V}$	—	—	$\pm 0.08$	$\mu\text{A}$
		$V_{DS} = 0\text{ V}, V_{GS} = \pm 10\text{ V}$	—	—	$\pm 1$	
Drain cut-off current	$I_{DSS}$	$V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V}$	—	—	-0.08	V
Drain-source breakdown voltage	$V_{(BR)DSS}$	$I_D = -1\text{ mA}, V_{GS} = 0\text{ V}$	-20	—	—	
Drain-source breakdown voltage (Note 1)	$V_{(BR)DSX}$	$I_D = -1\text{ mA}, V_{GS} = 10\text{ V}$	-10	—	—	
Gate threshold voltage (Note 2)	$V_{th}$	$V_{DS} = -10\text{ V}, I_D = -100\text{ }\mu\text{A}$	-0.3	—	-1	
Drain-source on-resistance (Note 3)	$R_{DS(ON)}$	$I_D = -10\text{ mA}, V_{GS} = -1.2\text{ V}$	—	3.2	20	$\Omega$
		$I_D = -20\text{ mA}, V_{GS} = -1.5\text{ V}$	—	2.3	4.0	
		$I_D = -50\text{ mA}, V_{GS} = -1.8\text{ V}$	—	2.0	2.9	
		$I_D = -150\text{ mA}, V_{GS} = -2.5\text{ V}$	—	1.5	2.1	
		$I_D = -150\text{ mA}, V_{GS} = -4.5\text{ V}$	—	1.1	1.4	
Forward transfer admittance (Note 3)	$ Y_{fs} $	$V_{DS} = -10\text{ V}, I_D = -100\text{ mA}$	—	430	—	mS

Note 1: If a reverse bias is applied between gate and source, this device enters  $V_{(BR)DSX}$  mode. Note that the drain-source breakdown voltage is lowered in this mode.

Note 2: Let  $V_{th}$  be the voltage applied between gate and source that causes the drain current ( $I_D$ ) to be below (-100  $\mu\text{A}$  for this device). Then, for normal switching operation,  $V_{GS(ON)}$  must be higher than  $V_{th}$ , and  $V_{GS(OFF)}$  must be lower than  $V_{th}$ . This relationship can be expressed as:  $V_{GS(OFF)} < V_{th} < V_{GS(ON)}$ .

Take this into consideration when using the device.

Note 3: Pulse measurement.

#### 6.2. Dynamic Characteristics (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$ )(Q1, Q2 Common)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Input capacitance	$C_{iss}$	$V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V},$ $f = 1\text{ MHz}$	—	21	42	$\mu\text{F}$
Reverse transfer capacitance	$C_{rss}$		—	2	—	
Output capacitance	$C_{oss}$		—	6	—	
Switching time (rise time)	$t_r$	$V_{DD} = -10\text{ V}, I_D = -50\text{ mA},$ $V_{GS} = 0\text{ to }-4.5\text{ V}, R_{GS} = 10\text{ }\Omega$ Duty $\leq 1\%$ , $V_{IN}: t_r, t_f < 5\text{ ns},$ Common source, See Chapter 6.3.	—	42	—	ns
Switching time (turn-on delay time)	$t_{d(on)}$		—	17	—	
Switching time (fall time)	$t_f$		—	145	—	
Switching time (turn-off delay time)	$t_{d(off)}$		—	420	—	

#### 6.3. Switching Time Test Circuit

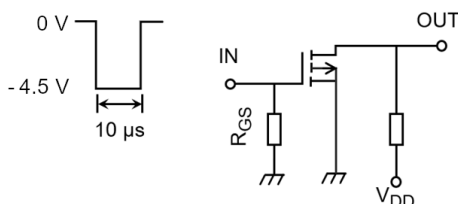


Fig. 6.3.1 Switching Time Test Circuit

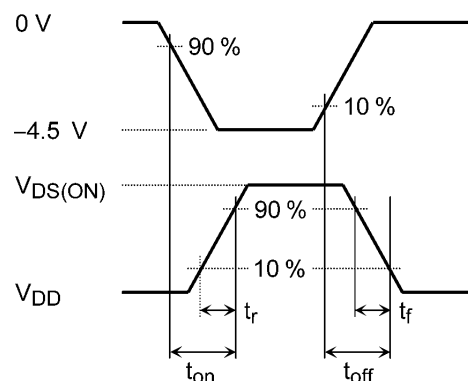


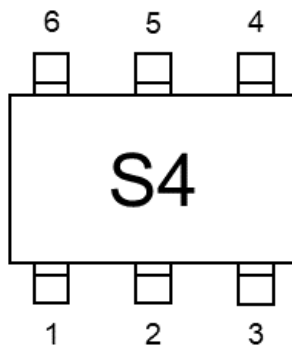
Fig. 6.3.2 Input Waveform/Output Waveform

## 6.4. Source-Drain Characteristics (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$ )(Q1, Q2 Common)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Diode forward voltage (Note 1)	$V_{DSF}$	$I_D = 100\text{ mA}$ , $V_{GS} = 0\text{ V}$	—	0.83	1.2	V

Note 1: Pulse measurement.

## 7. Marking



### 8. Characteristics Curves (Q1, Q2 Common) (Note)

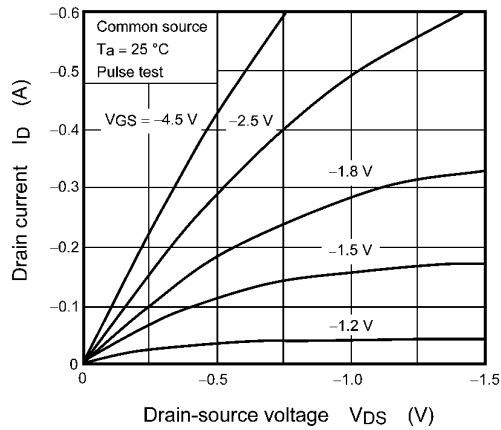


Fig. 8.1  $I_D - V_{DS}$

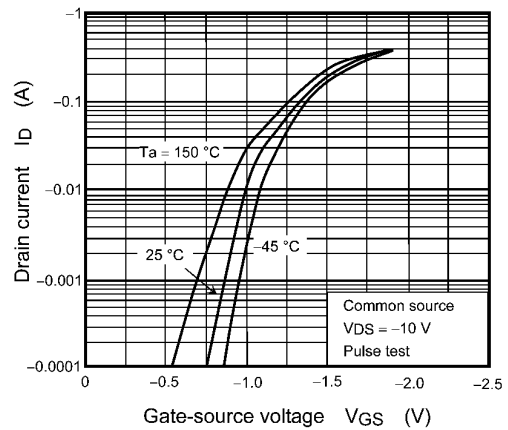


Fig. 8.2  $I_D - V_{GS}$

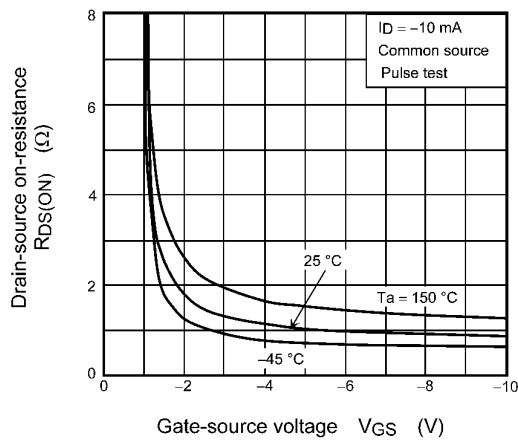


Fig. 8.3  $R_{DS(ON)} - V_{GS}$

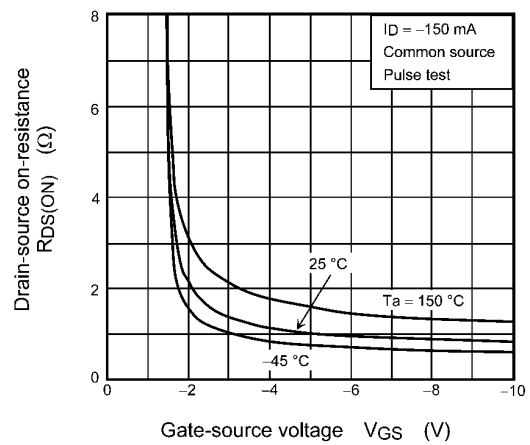


Fig. 8.4  $R_{DS(ON)} - V_{GS}$

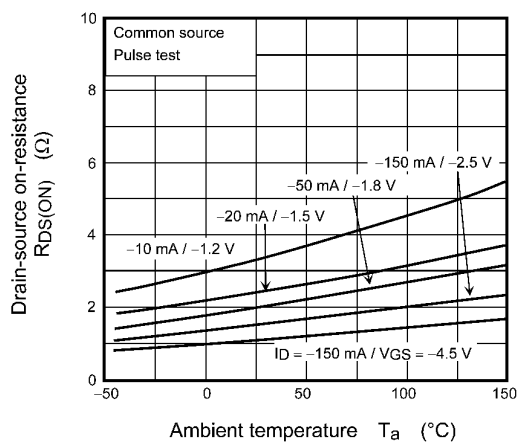


Fig. 8.5  $R_{DS(ON)} - T_a$

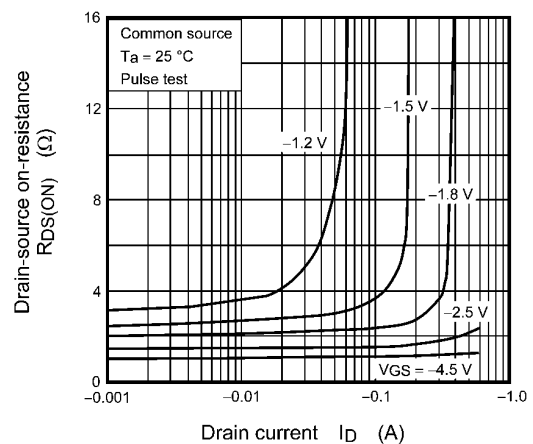
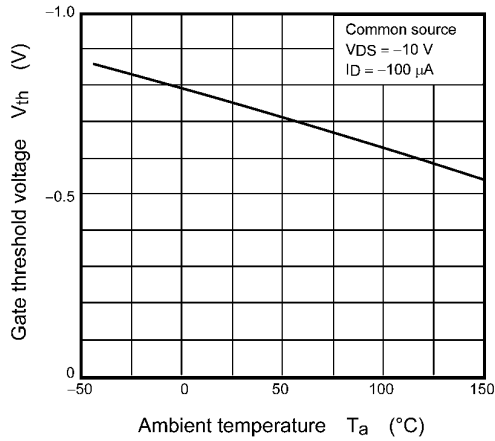
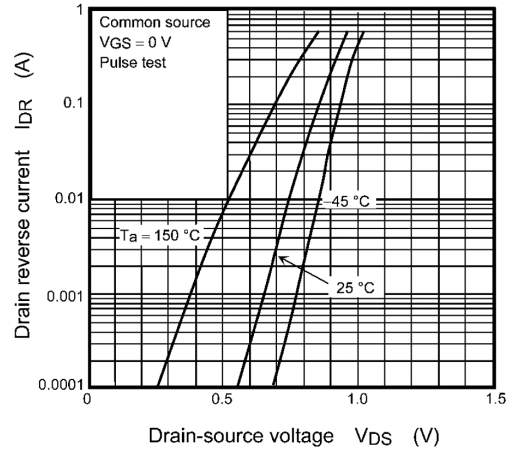


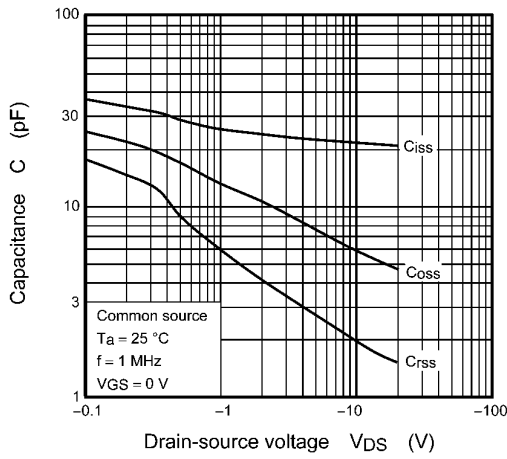
Fig. 8.6  $R_{DS(ON)} - I_D$



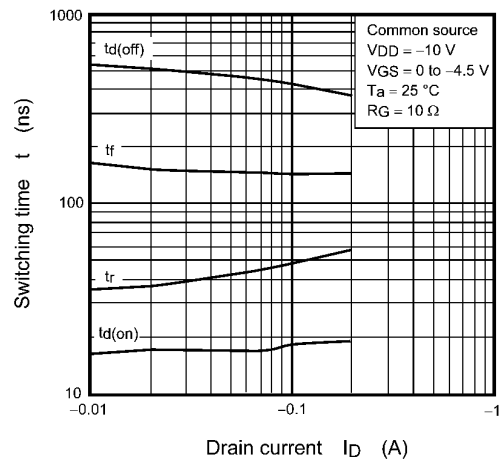
**Fig. 8.7  $V_{th} - T_a$**



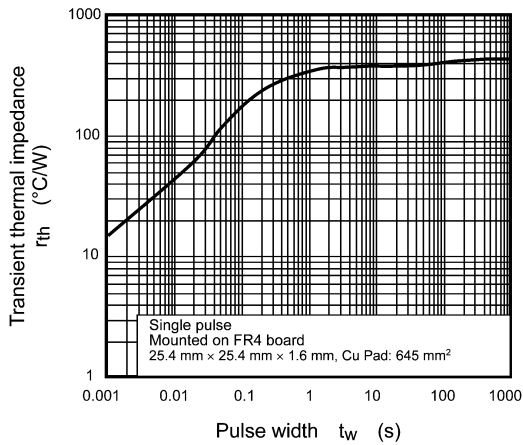
**Fig. 8.8  $I_{DR} - V_{DS}$**



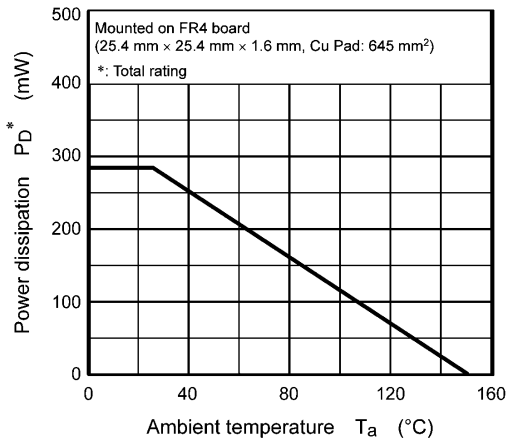
**Fig. 8.9  $C - V_{DS}$**



**Fig. 8.10  $t - I_D$**



**Fig. 8.11  $r_{th} - t_w$**



**Fig. 8.12  $P_D - T_a$**

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.



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