32-bit RISC Microcontroller
TXZ+ Family
TMPM4K Group(1)

Reference Manual
Product Information
(PINFO-M4K(1))

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Toshiba Electronic Devices & Storage Corporation

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Conventions

- Numeric formats follow the rules as shown below:
  Hexadecimal: 0xABC
  Decimal: 123 or 0d123 - Only when it needs to be explicitly shown that they are decimal numbers.
  Binary: 0b111 - It is possible to omit the "0b" when the number of bits can be distinctly understood from a sentence.
- "_N" is added to the end of signal names to indicate low active signals.
- It is called "assert" that a signal moves to its active level, "deassert" to its inactive level.
- When two or more signal names are referred, they are described like as [m:n].
  Example: S[3:0] shows four signal names S3, S2, S1 and S0 together.
- The characters surrounded by ***[ ]*** defines the register.
  Example: ***[ABCD]***
- "N" substitutes suffix number of two or more same kind of registers, fields, and bit names.
  Example: ***[XYZ1]***, ***[XYZ2]***, ***[XYZ3]*** → ***[XYZn]***
- "x" substitutes suffix number or character of units and channels in the register list.
- In case of unit, "x" means A, B, and C, ...
  Example: ***[ADACR0]***, ***[ADBCR0]***, ***[ADCCR0]*** → ***[ADxCR0]***
- In case of channel, "x" means 0, 1, and 2, ...
  Example: ***[T32A0RUNA]***, ***[T32A1RUNA]***, ***[T32A2RUNA]*** → ***[T32AxRUNA]***
- The bit range of a register is written like as [m: n].
  Example: Bit[3: 0] expresses the range of bit 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.
  Example: ***[ABCD]***<EFG> = 0x01 (hexadecimal), ***[XYZn]***<VW> = 1 (binary)
- Word and byte represent the following bit length.
  Byte: 8 bits
  Half word: 16 bits
  Word: 32 bits
  Double word: 64 bits
- Properties of each bit in a register are expressed as follows:
  R: Read only
  W: Write only
  R/W: Read and write are possible.
- Unless otherwise specified, register access supports only word access.
- The register defined as "Reserved" must not be rewritten. Moreover, do not use the read value.
- The value read from the bit having default value of "-" is unknown.
- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value, In the cases that default is "-", follow the definition of each register.
- Reserved bits of the write-only register should be written with their default value. In the cases that default is "-", follow the definition of each register.
- Do not use read-modified-write processing to the register of a definition which is different by writing and read out.

Terms and Abbreviations

Some of abbreviations used in this document are as follows:

ADC	Analog to Digital Converter
A-ENC32	Advanced Encoder input Circuit (32-bit)
A-PMD	Advanced Programmable Motor Control Circuit
CRC	Cyclic Redundancy Check
DMAC	Direct Memory Access Controller
DNF	Digital Noise Filter
EHOSC	External High-Speed Oscillator
EI2C	I^2C Interface Version A
IHOSC	Internal High-Speed Oscillator
INT	Interrupt
I2C	Inter-Integrated Circuit
LVD	Voltage Detection Circuit
NBDIF	Non Break Debug Interface
OFD	Oscillation Frequency Detector
OPAMP	Operational Amplifier
RAMP	RAM Parity
SIWDT	Clock Selective Watchdog Timer
TRGSEL	Trigger Selection Circuit
TRM	Trimming Circuit
TSPI	Serial Peripheral Interface
T32A	32-bit Timer Event Counter
UART	Asynchronous Serial Communication Circuit

1. Overview

This chapter describes peripheral function-related channels or number of units, information of pins and product-specific function information. Use this chapter in conjunction with Reference Manual for Peripheral Function.

2. Information of Peripheral Function

2.1. Register Base Address

The following table shows the type of base address of each peripheral.

Table 2.1 Type of Register Base Address

Product	Type of base address
TMPM4K Group(1)	TYPE1

To develop each peripheral function, please refer to the above type of base address.
In case of no information of Type1/2 of the base address in the Reference manual, it use as Type1.

Note: For the base address of the I^2C interface version A (EI2C), refer to "2.8.3 Base Address" in this document.

2.2. Trigger Selector (TRGSEL)

The trigger selector is the circuit which chooses the one trigger and outputs the trigger signal to the peripheral function from two or more triggers inputted from the peripheral function, the port, etc.

The trigger chosen from eight triggers by ***[TSEL0CRn]***<INSELm> is outputted to the peripheral function of a connection destination.

"Figure 2.1 Example of Trigger Selector Connection" is an example of connection DMA transmission end interrupts to DMAC via trigger selector. The setup of input trigger selection, edge detection condition selection, trigger output selection, and trigger output control is performed by ***[TSEL0CR3]***.

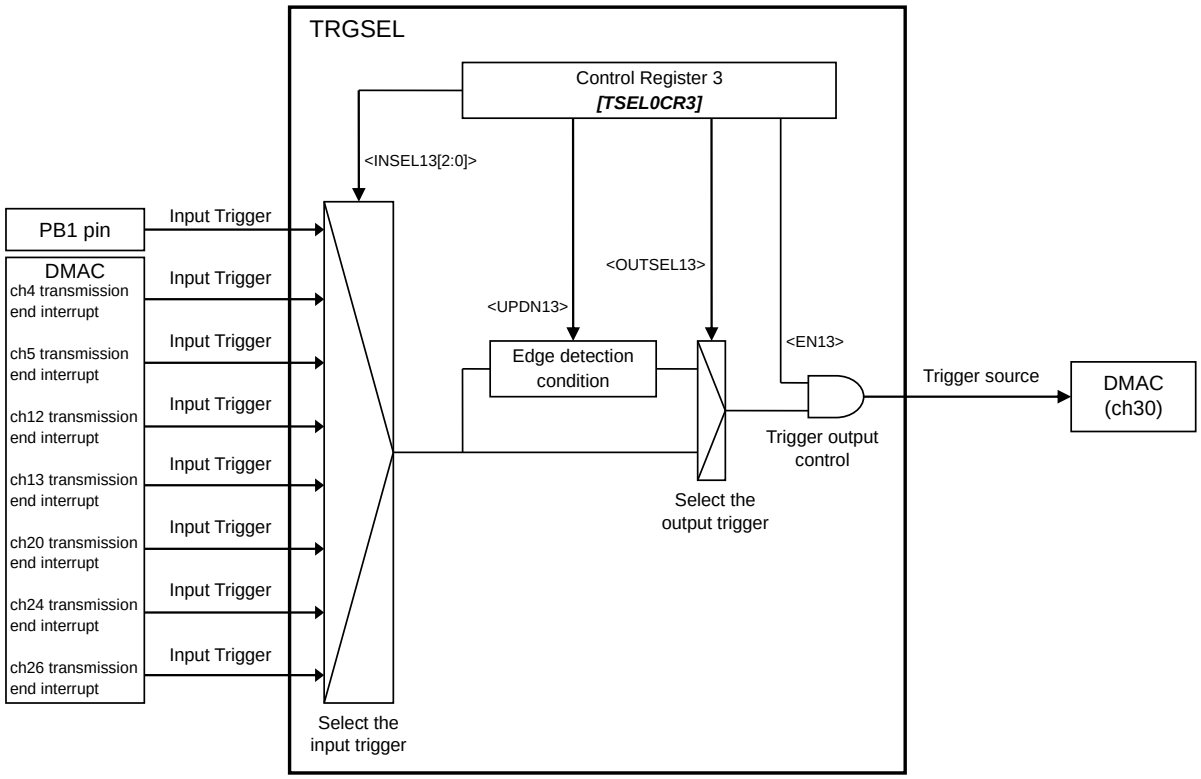

Figure 2.1 Example of Trigger Selector Connection

2.2.1. Trigger Selector List for Each Products

Trigger selector of TMPM4K Group(1) consist of 11 control registers (***[TSEL0CR0 to 10]***), and 43 triggers are controlled.

The following table shows "Trigger Selector List of each Product".

Table 2.2 Trigger Selector List for Each Product (1/6)

Register	Bit symbol	Destination	Trigger source	Product (✓:Available, -:N/A)		
				M4K4	M4K2	M4K1
[TSEL0CR0]	INSEL0	DMA ch7	TSPI ch3 transmit DMA request	✓	-	-
			ADC unit B general purpose trigger DMA request ADC unit B single conversion DMA request ADC unit B continuous conversion DMA request	✓	✓	✓
	INSEL1	DMA ch18	ADC unit A general purpose trigger DMA request ADC unit A single conversion DMA request ADC unit A continuous conversion DMA request	✓	✓	✓
	INSEL2	DMA ch19	T32A ch0 DMA request at match A1 register T32A ch0 DMA request at match C1 register T32A ch1 DMA request at match A1 register T32A ch1 DMA request at match C1 register A-PMD ch0 PWM interrupt	✓	✓	✓
	INSEL3	DMA ch20	T32A ch2 DMA request at match A1 register T32A ch2 DMA request at match C1 register T32A ch3 DMA request at match A1 register T32A ch3 DMA request at match C1 register	✓	✓	✓
			A-PMD ch1 PWM interrupt	✓	✓	-
[TSEL0CR1]	INSEL4	DMA ch21	T32A ch4 DMA request at match A1 register T32A ch4 DMA request at match C1 register T32A ch5 DMA request at match A1 register T32A ch5 DMA request at match C1 register	✓	✓	✓
	INSEL5	DMA ch22	T32A ch0 DMA request at match B1 register T32A ch1 DMA request at match B1 register T32A ch2 DMA request at match B1 register T32A ch3 DMA request at match B1 register T32A ch4 DMA request at match B1 register T32A ch5 DMA request at match B1 register	✓	✓	✓
	INSEL6	DMA ch23	T32A ch0 DMA request at capture A0 register T32A ch0 DMA request at capture A1 register T32A ch1 DMA request at capture A0 register T32A ch1 DMA request at capture A1 register T32A ch0 DMA request at capture C0 register T32A ch0 DMA request at capture C1 register T32A ch1 DMA request at capture C0 register T32A ch1 DMA request at capture C1 register	✓	✓	✓
	INSEL7	DMA ch24	T32A ch2 DMA request at capture A0 register T32A ch2 DMA request at capture A1 register T32A ch3 DMA request at capture A0 register T32A ch3 DMA request at capture A1 register T32A ch2 DMA request at capture C0 register T32A ch2 DMA request at capture C1 register T32A ch3 DMA request at capture C0 register T32A ch3 DMA request at capture C1 register	✓	✓	✓

Table 2.3 Trigger Selector List for Each Product (2/6)

Register	Bit symbol	Destination	Trigger source	Product (✓:Available, -:N/A)		
				M4K4	M4K2	M4K1
[TSEL0CR2]	INSEL8	DMA ch25	T32A ch4 DMA request at capture A0 register T32A ch4 DMA request at capture A1 register T32A ch5 DMA request at capture A0 register T32A ch5 DMA request at capture A1 register T32A ch4 DMA request at capture C0 register T32A ch4 DMA request at capture C1 register T32A ch5 DMA request at capture C0 register T32A ch5 DMA request at capture C1 register	✓	✓	✓
	INSEL9	DMA ch26	T32A ch0 DMA request at capture B0 register T32A ch0 DMA request at capture B1 register T32A ch1 DMA request at capture B0 register T32A ch1 DMA request at capture B1 register T32A ch2 DMA request at capture B0 register T32A ch2 DMA request at capture B1 register	✓	✓	✓
	INSEL10	DMA ch27	T32A ch3 DMA request at capture B0 register T32A ch3 DMA request at capture B1 register T32A ch4 DMA request at capture B0 register T32A ch4 DMA request at capture B1 register T32A ch5 DMA request at capture B0 register T32A ch5 DMA request at capture B1 register	✓	✓	✓
	INSEL11	DMA ch28	DMAC ch0 transfer completion DMAC ch1 transfer completion DMAC ch8 transfer completion DMAC ch9 transfer completion DMAC ch16 transfer completion DMAC ch17 transfer completion DMAC ch22 transfer completion	✓	✓	✓
[TSEL0CR3]	INSEL12	DMA ch29	DMAC ch2 transfer completion DMAC ch3 transfer completion	✓	-	-
			DMAC ch10 transfer completion DMAC ch11 transfer completion DMAC ch18 transfer completion DMAC ch19 transfer completion DMAC ch23 transfer completion	✓	✓	✓
			PF0 (TRGIN0)	✓	✓	✓
	INSEL13	DMA ch30	DMAC ch4 transfer completion DMAC ch5 transfer completion DMAC ch12 transfer completion DMAC ch13 transfer completion DMAC ch20 transfer completion DMAC ch24 transfer completion DMAC ch26 transfer completion	✓	✓	✓
			PB1 (TRGIN1)	✓	✓	✓
	INSEL14	DMA ch31	DMAC ch6 transfer completion DMAC ch14 transfer completion DMAC ch15 transfer completion	✓	-	-
			DMAC ch7 transfer completion DMAC ch21 transfer completion DMAC ch25 transfer completion DMAC ch27 transfer completion	✓	✓	✓
			PF2 (TRGIN2)	✓	-	-
	INSEL15	ADC unit A	PF0 (TRGIN0)	✓	✓	✓
			PB1 (TRGIN1)	✓	✓	✓
			PF2 (TRGIN2)	✓	-	-
			T32A ch5 Timer register A1 match trigger T32A ch5 Timer register B1 match trigger T32A ch5 Timer register C1 match trigger Trigger generation circuit output (TRGGEN)	✓	✓	✓

Table 2.4 Trigger Selector List for Each Product (3/6)

Register	Bit symbol	Destination	Trigger source	Product (✓:Available, -:N/A)		
				M4K4	M4K2	M4K1
[TSEL0CR4]	INSEL16	ADC unit B	PF0 (TRGIN0)	✓	✓	✓
			PB1 (TRGIN1)	✓	✓	✓
			PF2 (TRGIN2)	✓	-	-
			T32A ch3 Timer register A1 match trigger T32A ch3 Timer register B1 match trigger T32A ch3 Timer register C1 match trigger Trigger selector INSEL15 output	✓	✓	✓
	INSEL17	TSPI ch0	PF0 (TRGIN0)	✓	✓	✓
			PB1 (TRGIN1)	✓	✓	✓
			PF2 (TRGIN2)	✓	-	-
			T32A ch5 Timer register A1 match trigger T32A ch5 Timer register B1 match trigger T32A ch5 Timer register C1 match trigger	✓	✓	✓
	INSEL18	TSPI ch1	PF0 (TRGIN0)	✓	-	-
			PB1 (TRGIN1)	✓	-	-
			PF2 (TRGIN2)	✓	-	-
			T32A ch5 Timer register A1 match trigger T32A ch5 Timer register B1 match trigger T32A ch5 Timer register C1 match trigger	✓	-	-
	INSEL19	TSPI ch2	PF0 (TRGIN0)	✓	✓	✓
			PB1 (TRGIN1)	✓	✓	✓
			PF2 (TRGIN2)	✓	-	-
			T32A ch5 Timer register A1 match trigger T32A ch5 Timer register B1 match trigger T32A ch5 Timer register C1 match trigger	✓	✓	✓
[TSEL0CR5]	INSEL20	TSPI ch3	PF0 (TRGIN0)	✓	-	-
			PB1 (TRGIN1)	✓	-	-
			PF2 (TRGIN2)	✓	-	-
			T32A ch5 Timer register A1 match trigger T32A ch5 Timer register B1 match trigger T32A ch5 Timer register C1 match trigger	✓	-	-
	INSEL21	UART ch0	PF0 (TRGIN0)	✓	✓	✓
			PB1 (TRGIN1)	✓	✓	✓
			PF2 (TRGIN2)	✓	-	-
			T32A ch5 Timer register A1 match trigger T32A ch5 Timer register B1 match trigger T32A ch5 Timer register C1 match trigger	✓	✓	✓
	INSEL22	UART ch1	PF0 (TRGIN0)	✓	✓	✓
			PB1 (TRGIN1)	✓	✓	✓
			PF2 (TRGIN2)	✓	-	-
			T32A ch5 Timer register A1 match trigger T32A ch5 Timer register B1 match trigger T32A ch5 Timer register C1 match trigger	✓	✓	✓
	INSEL23	UART ch2	PF0 (TRGIN0)	✓	✓	✓
			PB1 (TRGIN1)	✓	✓	✓
			PF2 (TRGIN2)	✓	-	-
			T32A ch5 Timer register A1 match trigger T32A ch5 Timer register B1 match trigger T32A ch5 Timer register C1 match trigger	✓	✓	✓

Table 2.5 Trigger Selector List for Each Product (4/6)

Register	Bit symbol	Destination	Trigger source	Product (✓:Available, -:N/A)		
				M4K4	M4K2	M4K1
[TSEL0CR6]	INSEL24	UART ch3	PF0 (TRGIN0)	✓	-	-
			PB1 (TRGIN1)	✓	-	-
			PF2 (TRGIN2)	✓	-	-
			T32A ch5 Timer register A1 match trigger T32A ch5 Timer register B1 match trigger T32A ch5 Timer register C1 match trigger	✓	-	-
	INSEL25	T32A ch0 Timer A	PF0 (TRGIN0)	✓	✓	✓
			PB1 (TRGIN1)	✓	✓	✓
			PF2 (TRGIN2)	✓	-	-
			UART ch0 transmission completion trigger UART ch0 reception completion trigger TSPI ch0 transmit completion TSPI ch0 receive completion	✓	✓	✓
	INSEL26	T32A ch0 Timer B	T32A ch0 Timer register A0 match trigger T32A ch0 Timer register A1 match trigger T32A ch0 Timer A overflow trigger T32A ch0 Timer A underflow trigger	✓	✓	✓
	INSEL27	T32A ch0 Timer C	T32A ch5 Timer register C0 match trigger T32A ch5 Timer register C1 match trigger T32A ch5 Timer C overflow trigger T32A ch5 Timer C underflow trigger	✓	✓	✓
[TSEL0CR7]	INSEL28	T32A ch1 Timer A	PF0 (TRGIN0)	✓	✓	✓
			PB1 (TRGIN1)	✓	✓	✓
			PF2 (TRGIN2)	✓	-	-
			UART ch1 transmission completion trigger UART ch1 reception completion trigger	✓	✓	✓
			TSPI ch1 transmit completion TSPI ch1 receive completion	✓	-	-
			A-ENC32 ch1 divided pulse	✓	✓	✓
	INSEL29	T32A ch1 Timer B	T32A ch1 Timer register A0 match trigger T32A ch1 Timer register A1 match trigger T32A ch1 Timer A overflow trigger T32A ch1 Timer A underflow trigger	✓	✓	✓
	INSEL30	T32A ch1 Timer C	T32A ch0 Timer register C0 match trigger T32A ch0 Timer register C1 match trigger T32A ch0 Timer C overflow trigger T32A ch0 Timer C underflow trigger	✓	✓	✓
	INSEL31	T32A ch2 Timer A	PF0 (TRGIN0)	✓	✓	✓
			PB1 (TRGIN1)	✓	✓	✓
			PF2 (TRGIN2)	✓	-	-
			UART ch2 transmission completion trigger UART ch2 reception completion trigger TSPI ch2 transmit completion TSPI ch2 receive completion	✓	✓	✓

Table 2.6 Trigger Selector List for Each Product (5/6)

Register	Bit symbol	Destination	Trigger source	Product (✓:Available, -:N/A)		
				M4K4	M4K2	M4K1
[TSEL0CR8]	INSEL32	T32A ch2 Timer B	T32A ch2 Timer register A0 match trigger T32A ch2 Timer register A1 match trigger T32A ch2 Timer A overflow trigger T32A ch2 Timer A underflow trigger	✓	✓	✓
	INSEL33	T32A ch2 Timer C	T32A ch1 Timer register C0 match trigger T32A ch1 Timer register C1 match trigger T32A ch1 Timer C overflow trigger T32A ch1 Timer C underflow trigger	✓	✓	✓
	INSEL34	T32A ch3 Timer A	PF0 (TRGIN0)	✓	✓	✓
			PB1 (TRGIN1)	✓	✓	✓
			PF2 (TRGIN2)	✓	-	-
			UART ch3 transmission completion trigger UART ch3 reception completion trigger TSPI ch3 transmit completion TSPI ch3 receive completion	✓	-	-
			I2C ch0 interrupt EI2C ch0 status interrupt	✓	✓	✓
	INSEL35	T32A ch3 Timer B	T32A ch3 Timer register A0 match trigger T32A ch3 Timer register A1 match trigger T32A ch3 Timer A overflow trigger T32A ch3 Timer A underflow trigger	✓	✓	✓
[TSEL0CR9]	INSEL36	T32A ch3 Timer C	T32A ch2 Timer register C0 match trigger T32A ch2 Timer register C1 match trigger T32A ch2 Timer C overflow trigger T32A ch2 Timer C underflow trigger	✓	✓	✓
	INSEL37	T32A ch4 Timer A	PF0 (TRGIN0)	✓	✓	✓
			PB1 (TRGIN1)	✓	✓	✓
			PF2 (TRGIN2)	✓	-	-
			A-ENC32 ch0 divided pulse ADC unit B general purpose trigger interrupt ADC unit B single conversion interrupt ADC unit B continuous conversion interrupt ADC unit B monitor function 0 Interrupt	✓	✓	✓
	INSEL38	T32A ch4 Timer B	T32A ch4 Timer register A0 match trigger T32A ch4 Timer register A1 match trigger T32A ch4 Timer A overflow trigger T32A ch4 Timer A underflow trigger	✓	✓	✓
	INSEL39	T32A ch4 Timer C	T32A ch3 Timer register C0 match trigger T32A ch3 Timer register C1 match trigger T32A ch3 Timer C overflow trigger T32A ch3 Timer C underflow trigger	✓	✓	✓

Table 2.7 Trigger Selector List for Each Product (6/6)

Register	Bit symbol	Destination	Trigger source	Product (✓:Available, -:N/A)		
				M4K4	M4K2	M4K1
[TSEL0CR10]	INSEL40	T32A ch5 Timer A	PF0 (TRGIN0)	✓	✓	✓
			PB1 (TRGIN1)	✓	✓	✓
			PF2 (TRGIN2)	✓	-	-
			ADC unit A general purpose trigger interrupt ADC unit A single conversion interrupt ADC unit A continuous conversion interrupt ADC unit A monitor function 0 Interrupt ADC unit A monitor function 1 Interrupt	✓	✓	✓
	INSEL41	T32A ch5 Timer B	T32A ch5 Timer register A0 match trigger T32A ch5 Timer register A1 match trigger T32A ch5 Timer A overflow trigger T32A ch5 Timer A underflow trigger	✓	✓	✓
	INSEL42	T32A ch5 Timer C	T32A ch4 Timer register C0 match trigger T32A ch4 Timer register C1 match trigger T32A ch4 Timer C overflow trigger T32A ch4 Timer C underflow trigger	✓	✓	✓

2.2.2. Operation and Setting

When using TRGSEL, please set an applicable clock enable bit to "1" (clock supply) in fsys supply stop register A (***[CGFSYSENA]***), fsys supply stop register B (***[CGFSYSENB]***), and fc supply stop registers (***[CGFCEN]***).
An applicable register and the bit position vary according to a product. Therefore, the register may not exist with the product. Please refer to "Clock Control and Operation Mode" of the reference manual for the details.

Setting procedure of Trigger selector is as following.

(1) Selection of an input trigger (***[TSEL0CRn]*** <INSELm>)

Selection of the input trigger used for the trigger source is performed.

Please set up selection of the input trigger by the input trigger subdevice bit (***[TSEL0CRn]*** <INSELm>) of the control register. (n: register number, m: trigger number)

(2) Selection of edge detection conditions (***[TSEL0CRn]*** <UPDNm>)

For the input trigger signal which needs edge detection, selection of rising edge or falling edge detection is performed.

Please set up selection of edge detection conditions in the selection bit (***[TSEL0CRn]***<UPDNm>) of a control register.

The following shows the trigger signal which needs edge detection.

- External trigger input (TRGIN0, TRGIN1, and TRGIN2)

(3) Selection of a trigger output (***[TSEL0CRn]***<OUTSELm>)

Selection of an output without or with edge detection is performed.

Please set up selection of a trigger output in the selection bit (***[TSEL0CRn]***<OUTSELm>) of a control register.

(4) Output enable (***[TSEL0CRn]***<ENm>)

The output (enable/disable) of the selected trigger signal is chosen.

Please set up selection of output (enable/disable) in the setting bit (***[TSEL0CRn]***<ENm>) of a control register. A trigger output will be enabled if ***[TSEL0CRn]***<ENm> is set as "1".

2.2.3. List of Registers

The table below shows control registers and their addresses.

Peripheral function		Channel/Unit	Base address
Trigger selector	TRGSEL	ch0	0x400BB800

Register name		Address (Base+)
Control Register 0	***[TSELxCR0]***	0x0000
Control Register 1	***[TSELxCR1]***	0x0004
Control Register 2	***[TSELxCR2]***	0x0008
Control Register 3	***[TSELxCR3]***	0x000C
Control Register 4	***[TSELxCR4]***	0x0010
Control Register 5	***[TSELxCR5]***	0x0014
Control Register 6	***[TSELxCR6]***	0x0018
Control Register 7	***[TSELxCR7]***	0x001C
Control Register 8	***[TSELxCR8]***	0x0020
Control Register 9	***[TSELxCR9]***	0x0024
Control Register 10	***[TSELxCR10]***	0x0028

2.2.4. Details of Registers

The following chapters show the detail of registers. The sign in the functional column parenthesis of each table expresses each function signal name.

2.2.4.1. *[TSELxCR0]* (Control Register 0)

Bit	Bit symbol	After reset	Type	Function
31	-	0	R	Read as 0
30:28	INSEL3[2:0]	000	R/W	Select the input trigger (DMA ch20) 000: T32A ch2 DMA request at match A1 register (T32A02DMAREQCMPA1) 001: T32A ch2 DMA request at match C1 register (T32A02DMAREQCMPC1) 010: T32A ch3 DMA request at match A1 register (T32A03DMAREQCMPA1) 011: T32A ch3 DMA request at match C1 register (T32A03DMAREQCMPC1) 100: A-PMD ch1 PWM interrupt (INTPWM1) 101: Reserved 110: Reserved 111: Reserved
27	-	0	R	Read as 0
26	UPDN3	0	R/W	Edge detection 0: Rising edge detection 1: falling edge detection
25	OUTSEL3	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
24	EN3	0	R/W	Trigger output control 0: Disable 1: Enable
23	-	0	R	Read as 0
22:20	INSEL2[2:0]	000	R/W	Select the input trigger (DMA ch19) 000: T32A ch0 DMA request at match A1 register (T32A00DMAREQCMPA1) 001: T32A ch0 DMA request at match C1 register (T32A00DMAREQCMPC1) 010: T32A ch1 DMA request at match A1 register (T32A01DMAREQCMPA1) 011: T32A ch1 DMA request at match C1 register (T32A01DMAREQCMPC1) 100: A-PMD ch0 PWM interrupt (INTPWM0) 101: Reserved 110: Reserved 111: Reserved
19	-	0	R	Read as 0
18	UPDN2	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
17	OUTSEL2	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
16	EN2	0	R/W	Trigger output control 0: Disable 1: Enable
15	-	0	R	Read as 0

Bit	Bit symbol	After reset	Type	Function
14:12	INSEL1[2:0]	000	R/W	Select the input trigger (DMA ch18) 000: ADC unit A general purpose trigger DMA request (ADATRG_DMAREQ) 001: ADC unit A single conversion DMA request (ADASGL_DMAREQ) 010: ADC unit A continuous conversion DMA request (ADACNT_DMAREQ) 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved
11	-	0	R	Read as 0
10	UPDN1	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
9	OUTSEL1	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
8	EN1	0	R/W	Trigger output control 0: Disable 1: Enable
7	-	0	R	Read as 0
6:4	INSEL0[2:0]	000	R/W	Select the input trigger (DMA ch7) 000: TSPI ch3 transmit DMA request (TSPI3TX_DMA) 001: ADC unit B general purpose trigger DMA request (ADATRG_DMAREQ) 010: ADC unit B single conversion DMA request (ADASGL_DMAREQ) 011: ADC unit B continuous conversion DMA request (ADACNT_DMAREQ) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
3	-	0	R	Read as 0
2	UPDN0	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
1	OUTSEL0	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
0	EN0	0	R/W	Trigger output control 0: Disable 1: Enable

2.2.4.2. *[TSELxCR1]* (Control Register1)

Bit	Bit symbol	After reset	Type	Function
31	-	0	R	Read as 0
30:28	INSEL7[2:0]	000	R/W	Select the input trigger (DMA ch24) 000: T32A ch2 DMA request capture A0 (T32A02DMAREQCAPA0) 001: T32A ch2 DMA request capture A1 (T32A02DMAREQCAPA1) 010: T32A ch3 DMA request capture A0 (T32A03DMAREQCAPA0) 011: T32A ch3 DMA request capture A1 (T32A03DMAREQCAPA1) 100: T32A ch2 DMA request capture C0 (T32A02DMAREQCAPC0) 101: T32A ch2 DMA request capture C1 (T32A02DMAREQCAPC1) 110: T32A ch3 DMA request capture C0 (T32A03DMAREQCAPC0) 111: T32A ch3 DMA request capture C1 (T32A03DMAREQCAPC1)
27	-	0	R	Read as 0
26	UPDN7	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
25	OUTSEL7	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
24	EN7	0	R/W	Trigger output control 0: Disable 1: Enable
23	-	0	R	Read as 0
22:20	INSEL6[2:0]	000	R/W	Select the input trigger (DMA ch23) 000: T32A ch0 DMA request capture A0 (T32A00DMAREQCAPA0) 001: T32A ch0 DMA request capture A1 (T32A00DMAREQCAPA1) 010: T32A ch1 DMA request capture A0 (T32A01DMAREQCAPA0) 011: T32A ch1 DMA request capture A1 (T32A01DMAREQCAPA1) 100: T32A ch0 DMA request capture C0 (T32A00DMAREQCAPC0) 101: T32A ch0 DMA request capture C1 (T32A00DMAREQCAPC1) 110: T32A ch1 DMA request capture C0 (T32A01DMAREQCAPC0) 111: T32A ch1 DMA request capture C1 (T32A01DMAREQCAPC1)
19	-	0	R	Read as 0
18	UPDN6	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
17	OUTSEL6	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
16	EN6	0	R/W	Trigger output control 0: Disable 1: Enable
15	-	0	R	Read as 0
14:12	INSEL5[2:0]	000	R/W	Select the input trigger (DMA ch22) 000: T32A ch0 DMA request at match B1 register (T32A00DMAREQCMPB1) 001: T32A ch1 DMA request at match B1 register (T32A01DMAREQCMPB1) 010: T32A ch2 DMA request at match B1 register (T32A02DMAREQCMPB1) 011: T32A ch3 DMA request at match B1 register (T32A03DMAREQCMPB1) 100: T32A ch4 DMA request at match B1 register (T32A04DMAREQCMPB1) 101: T32A ch5 DMA request at match B1 register (T32A05DMAREQCMPB1) 110: Reserved 111: Reserved
11	-	0	R	Read as 0

Bit	Bit symbol	After reset	Type	Function
10	UPDN5	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
9	OUTSEL5	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
8	EN5	0	R/W	Trigger output control 0: Disable 1: Enable
7	-	0	R	Read as 0
6:4	INSEL4[2:0]	000	R/W	Select the input trigger (DMA ch21) 000: T32A ch4 DMA request at match A1 register (T32A04DMAREQCMPA1) 001: T32A ch4 DMA request at match C1 register (T32A04DMAREQCMPC1) 010: T32A ch5 DMA request at match A1 register (T32A05DMAREQCMPA1) 011: T32A ch5 DMA request at match C1 register (T32A05DMAREQCMPC1) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
3	-	0	R	Read as 0
2	UPDN4	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
1	OUTSEL4	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
0	EN4	0	R/W	Trigger output control 0: Disable 1: Enable

2.2.4.3. *[TSELxCR2]* (Control Register 2)

Bit	Bit symbol	After reset	Type	Function
31	-	0	R	Read as 0
30:28	INSEL11[2:0]	000	R/W	Select the input trigger (DMA ch28) 000: DMAC ch0 transfer completion (INTDMAATC0) 001: DMAC ch1 transfer completion (INTDMAATC1) 010: DMAC ch8 transfer completion (INTDMAATC8) 011: DMAC ch9 transfer completion (INTDMAATC9) 100: DMAC ch16 transfer completion (INTDMAATC16) 101: DMAC ch17 transfer completion (INTDMAATC17) 110: DMAC ch22 transfer completion (INTDMAATC22) 111: Reserved
27	-	0	R	Read as 0
26	UPDN11	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
25	OUTSEL11	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
24	EN11	0	R/W	Trigger output control 0: Disable 1: Enable
23	-	0	R	Read as 0
22:20	INSEL10[2:0]	000	R/W	Select the input trigger (DMA ch27) 000: T32A ch3 DMA request capture B0 (T32A03DMAREQCAPB0) 001: T32A ch3 DMA request capture B1 (T32A03DMAREQCAPB1) 010: T32A ch4 DMA request capture B0 (T32A04DMAREQCAPB0) 011: T32A ch4 DMA request capture B1 (T32A04DMAREQCAPB1) 100: T32A ch5 DMA request capture B0 (T32A05DMAREQCAPB0) 101: T32A ch5 DMA request capture B1 (T32A05DMAREQCAPB1) 110: Reserved 111: Reserved
19	-	0	R	Read as 0
18	UPDN10	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
17	OUTSEL1	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
16	EN10	0	R/W	Trigger output control 0: Disable 1: Enable
15	-	0	R	Read as 0
14:12	INSEL9[2:0]	000	R/W	Select the input trigger (DMA ch26) 000: T32A ch0 DMA request capture B0 (T32A00DMAREQCAPB0) 001: T32A ch0 DMA request capture B1 (T32A00DMAREQCAPB1) 010: T32A ch1 DMA request capture B0 (T32A01DMAREQCAPB0) 011: T32A ch1 DMA request capture B1 (T32A01DMAREQCAPB1) 100: T32A ch2 DMA request capture B0 (T32A00DMAREQCAPB0) 101: T32A ch2 DMA request capture B1 (T32A01DMAREQCAPB1) 110: Reserved 111: Reserved
11	-	0	R	Read as 0

Bit	Bit symbol	After reset	Type	Function
10	UPDN9	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
9	OUTSEL9	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
8	EN9	0	R/W	Trigger output control 0: Disable 1: Enable
7	-	0	R	Read as 0
6:4	INSEL8[2:0]	000	R/W	Select the input trigger (DMA ch25) 000: T32A ch4 DMA request capture A0 (T32A04DMAREQCAPA0) 001: T32A ch4 DMA request capture A1 (T32A04DMAREQCAPA1) 010: T32A ch5 DMA request capture A0 (T32A05DMAREQCAPA0) 011: T32A ch5 DMA request capture A1 (T32A05DMAREQCAPA1) 100: T32A ch4 DMA request capture C0 (T32A04DMAREQCAPC0) 101: T32A ch4 DMA request capture C1 (T32A04DMAREQCAPC1) 110: T32A ch5 DMA request capture C0 (T32A05DMAREQCAPC0) 111: T32A ch5 DMA request capture C1 (T32A05DMAREQCAPC1)
3	-	0	R	Read as 0
2	UPDN8	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
1	OUTSEL8	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
0	EN8	0	R/W	Trigger output control 0: Disable 1: Enable

2.2.4.4. *[TSELxCR3]* (Control Register 3)

Bit	Bit symbol	After reset	Type	Function
31	-	0	R	Read as 0
30:28	INSEL15[2:0]	000	R/W	Select the input trigger (ADC unit A general purpose trigger) 000: PF0 (TRGIN0) 001: PB1 (TRGIN1) 010: PF2 (TRGIN2) 011: T32A ch5 Timer register A1 match trigger (T32A05TRGOUTCMPA1) 100: T32A ch5 Timer register B1 match trigger (T32A05TRGOUTCMPB1) 101: T32A ch5 Timer register C1 match trigger (T32A05TRGOUTCMPC1) 110: Trigger generation circuit output (TRGGEN) 111: Reserved
27	-	0	R	Read as 0
26	UPDN15	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
25	OUTSEL15	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
24	EN15	0	R/W	Trigger output control 0: Disable 1: Enable
23	-	0	R	Read as 0
22:20	INSEL14[2:0]	000	R/W	Select the input trigger (DMA ch31) 000: DMAC ch6 transfer completion (INTDMAATC6) 001: DMAC ch7 transfer completion (INTDMAATC7) 010: DMAC ch14 transfer completion (INTDMAATC14) 011: DMAC ch15 transfer completion (INTDMAATC15) 100: DMAC ch21 transfer completion (INTDMAATC21) 101: DMAC ch25 transfer completion (INTDMAATC25) 110: DMAC ch27 transfer completion (INTDMAATC27) 111: PF2 (TRGIN2)
19	-	0	R	Read as 0
18	UPDN14	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
17	OUTSEL14	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
16	EN14	0	R/W	Trigger output control 0: Disable 1: Enable
15	-	0	R	Read as 0
14:12	INSEL13[2:0]	000	R/W	Select the input trigger (DMA ch30) 000: DMAC ch4 transfer completion (INTDMAATC4) 001: DMAC ch5 transfer completion (INTDMAATC5) 010: DMAC ch12 transfer completion (INTDMAATC12) 011: DMAC ch13 transfer completion (INTDMAATC13) 100: DMAC ch20 transfer completion (INTDMAATC20) 101: DMAC ch24 transfer completion (INTDMAATC24) 110: DMAC ch26 transfer completion (INTDMAATC26) 111: PB1 (TRGIN1)
11	-	0	R	Read as 0

Bit	Bit symbol	After reset	Type	Function
10	UPDN13	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
9	OUTSEL13	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
8	EN13	0	R/W	Trigger output control 0: Disable 1: Enable
7	-	0	R	Read as 0
6:4	INSEL12[2:0]	000	R/W	Select the input trigger (DMA ch29) 000: DMAC ch2 transfer completion (INTDMAATC2) 001: DMAC ch3 transfer completion (INTDMAATC3) 010: DMAC ch10 transfer completion (INTDMAATC10) 011: DMAC ch11 transfer completion (INTDMAATC11) 100: DMAC ch18 transfer completion (INTDMAATC18) 101: DMAC ch19 transfer completion (INTDMAATC19) 110: DMAC ch23 transfer completion (INTDMAATC23) 111: PF0 (TRGIN0)
3	-	0	R	Read as 0
2	UPDN12	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
1	OUTSEL12	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
0	EN12	0	R/W	Trigger output control 0: Disable 1: Enable

2.2.4.5. *[TSELxCR4]* (Control Register 4)

Bit	Bit symbol	After reset	Type	Function
31	-	0	R	Read as 0
30:28	INSEL19[2:0]	000	R/W	Select the input trigger (TSPI ch2 trigger input) 000: PF0 (TRGIN0) 001: PB1 (TRGIN1) 010: PF2 (TRGIN2) 011: T32A ch5 Timer register A1 match trigger (T32A05TRGOUTCMPA1) 100: T32A ch5 Timer register B1 match trigger (T32A05TRGOUTCMPB1) 101: T32A ch5 Timer register C1 match trigger (T32A05TRGOUTCMPC1) 110: Reserved 111: Reserved
27	-	0	R	Read as 0
26	UPDN19	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
25	OUTSEL19	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
24	EN19	0	R/W	Trigger output control 0: Disable 1: Enable
23	-	0	R	Read as 0
22:20	INSEL18[2:0]	000	R/W	Select the input trigger (TSPI ch1 trigger input) 000: PF0 (TRGIN0) 001: PB1 (TRGIN1) 010: PF2 (TRGIN2) 011: T32A ch5 Timer register A1 match trigger (T32A05TRGOUTCMPA1) 100: T32A ch5 Timer register B1 match trigger (T32A05TRGOUTCMPB1) 101: T32A ch5 Timer register C1 match trigger (T32A05TRGOUTCMPC1) 110: Reserved 111: Reserved
19	-	0	R	Read as 0
18	UPDN18	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
17	OUTSEL18	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
16	EN18	0	R/W	Trigger output control 0: Disable 1: Enable
15	-	0	R	Read as 0
14:12	INSEL17[2:0]	000	R/W	Select the input trigger (TSPI ch0 trigger input) 000: PF0 (TRGIN0) 001: PB1 (TRGIN1) 010: PF2 (TRGIN2) 011: T32A ch5 Timer register A1 match trigger (T32A05TRGOUTCMPA1) 100: T32A ch5 Timer register B1 match trigger (T32A05TRGOUTCMPB1) 101: T32A ch5 Timer register C1 match trigger (T32A05TRGOUTCMPC1) 110: Reserved 111: Reserved
11	-	0	R	Read as 0

Bit	Bit symbol	After reset	Type	Function
10	UPDN17	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
9	OUTSEL17	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
8	EN17	0	R/W	Trigger output control 0: Disable 1: Enable
7	-	0	R	Read as 0
6:4	INSEL16[2:0]	000	R/W	Select the input trigger (ADC unit B general purpose trigger) 000: PF0 (TRGIN0) 001: PB1 (TRGIN1) 010: PF2 (TRGIN2) 011: T32A ch3 Timer register A1 match trigger (T32A03TRGOUTCMPA1) 100: T32A ch3 Timer register B1 match trigger (T32A03TRGOUTCMPB1) 101: T32A ch3 Timer register C1 match trigger (T32A03TRGOUTCMPC1) 110: Trigger selector INSEL15 output 111: Reserved
3	-	0	R	Read as 0
2	UPDN16	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
1	OUTSEL16	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
0	EN16	0	R/W	Trigger output control 0: Disable 1: Enable

2.2.4.6. *[TSELxCR5]* (Control Register 5)

Bit	Bit symbol	After reset	Type	Function
31	-	0	R	Read as 0
30:28	INSEL23[2:0]	000	R/W	Select the input trigger (UART ch2 trigger input) 000: PF0 (TRGIN0) 001: PB1 (TRGIN1) 010: PF2 (TRGIN2) 011: T32A ch5 Timer register A1 match trigger (T32A05TRGOUTCMPA1) 100: T32A ch5 Timer register B1 match trigger (T32A05TRGOUTCMPB1) 101: T32A ch5 Timer register C1 match trigger (T32A05TRGOUTCMPC1) 110: Reserved 111: Reserved
27	-	0	R	Read as 0
26	UPDN23	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
25	OUTSEL23	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
24	EN23	0	R/W	Trigger output control 0: Disable 1: Enable
23	-	0	R	Read as 0
22:20	INSEL22[2:0]	000	R/W	Select the input trigger (UART ch1 trigger input) 000: PF0 (TRGIN0) 001: PB1 (TRGIN1) 010: PF2 (TRGIN2) 011: T32A ch5 Timer register A1 match trigger (T32A05TRGOUTCMPA1) 100: T32A ch5 Timer register B1 match trigger (T32A05TRGOUTCMPB1) 101: T32A ch5 Timer register C1 match trigger (T32A05TRGOUTCMPC1) 110: Reserved 111: Reserved
19	-	0	R	Read as 0
18	UPDN22	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
17	OUTSEL22	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
16	EN22	0	R/W	Trigger output control 0: Disable 1: Enable
15	-	0	R	Read as 0
14:12	INSEL21[2:0]	000	R/W	Select the input trigger (UART ch0 trigger input) 000: PF0 (TRGIN0) 001: PB1 (TRGIN1) 010: PF2 (TRGIN2) 011: T32A ch5 Timer register A1 match trigger (T32A05TRGOUTCMPA1) 100: T32A ch5 Timer register B1 match trigger (T32A05TRGOUTCMPB1) 101: T32A ch5 Timer register C1 match trigger (T32A05TRGOUTCMPC1) 110: Reserved 111: Reserved
11	-	0	R	Read as 0

Bit	Bit symbol	After reset	Type	Function
10	UPDN21	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
9	OUTSEL21	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
8	EN21	0	R/W	Trigger output control 0: Disable 1: Enable
7	-	0	R	Read as 0
6:4	INSEL20[2:0]	000	R/W	Select the input trigger (TSPI ch3 trigger input) 000: PF0 (TRGIN0) 001: PB1 (TRGIN1) 010: PF2 (TRGIN2) 011: T32A ch5 Timer register A1 match trigger (T32A05TRGOUTCMPA1) 100: T32A ch5 Timer register B1 match trigger (T32A05TRGOUTCMPB1) 101: T32A ch5 Timer register C1 match trigger (T32A05TRGOUTCMPC1) 110: Reserved 111: Reserved
3	-	0	R	Read as 0
2	UPDN20	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
1	OUTSEL20	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
0	EN20	0	R/W	Trigger output control 0: Disable 1: Enable

2.2.4.7. *[TSELxCR6]* (Control Register 6)

Bit	Bit symbol	After reset	Type	Function
31	-	0	R	Read as 0
30:28	INSEL27[2:0]	000	R/W	Select the input trigger (T32A ch0 Timer C internal trigger input) 000: T32A ch5 Timer register C0 match trigger (T32A05TRGOUTCMPC0) 001: T32A ch5 Timer register C1 match trigger (T32A05TRGOUTCMPC1) 010: T32A ch5 Timer C overflow trigger (T32A05TRGOUTOFC) 011: T32A ch5 Timer C underflow trigger (T32A05TRGOUTUFC) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
27	-	0	R	Read as 0
26	UPDN27	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
25	OUTSEL27	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
24	EN27	0	R/W	Trigger output control 0: Disable 1: Enable
23	-	0	R	Read as 0
22:20	INSEL26[2:0]	000	R/W	Select the input trigger (T32A ch0 Timer B internal trigger input) 000: T32A ch0 Timer register A0 match trigger (T32A00TRGOUTCMPA0) 001: T32A ch0 Timer register A1 match trigger (T32A00TRGOUTCMPA1) 010: T32A ch0 Timer A overflow trigger (T32A00TRGOUTOFA) 011: T32A ch0 Timer A underflow trigger (T32A00TRGOUTUFA) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
19	-	0	R	Read as 0
18	UPDN26	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
17	OUTSEL26	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
16	EN26	0	R/W	Trigger output control 0: Disable 1: Enable
15	-	0	R	Read as 0
14:12	INSEL25[2:0]	000	R/W	Select the input trigger (T32A ch0 Timer A internal trigger input) 000: PF0 (TRGIN0) 001: PB1 (TRGIN1) 010: PF2 (TRGIN2) 011: UART ch0 transmission completion trigger (UART0TXTRG) 100: UART ch0 reception completion trigger (UART0RXTRG) 101: TSPI ch0 transmit completion (TSPI0TXEND) 110: TSPI ch0 receive completion (TSPI0RXEND) 111: Reserved
11	-	0	R	Read as 0

Bit	Bit symbol	After reset	Type	Function
10	UPDN25	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
9	OUTSEL25	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
8	EN25	0	R/W	Trigger output control 0: Disable 1: Enable
7	-	0	R	Read as 0
6:4	INSEL24[2:0]	000	R/W	Select the input trigger (UART ch3 trigger input) 000: PF0 (TRGIN0) 001: PB1 (TRGIN1) 010: PF2 (TRGIN2) 011: T32A ch5 Timer register A1 match trigger (T32A05TRGOUTCMPA1) 100: T32A ch5 Timer register B1 match trigger (T32A05TRGOUTCMPB1) 101: T32A ch5 Timer register C1 match trigger (T32A05TRGOUTCMPC1) 110: Reserved 111: Reserved
3	-	0	R	Read as 0
2	UPDN24	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
1	OUTSEL24	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
0	EN24	0	R/W	Trigger output control 0: Disable 1: Enable

2.2.4.8. *[TSELxCR7]* (Control Register 7)

Bit	Bit symbol	After reset	Type	Function
31	-	0	R	Read as 0
30:28	INSEL31[2:0]	000	R/W	Select the input trigger (T32A ch2 Timer A internal trigger input) 000: PF0 (TRGIN0) 001: PB1 (TRGIN1) 010: PF2 (TRGIN2) 011: UART ch2 transmission completion trigger (UART2TXTRG) 100: UART ch2 reception completion trigger (UART2RXTRG) 101: TSPI ch2 transmit completion (TSPI2TXEND) 110: TSPI ch2 receive completion (TSPI2RXEND) 111: Reserved
27	-	0	R	Read as 0
26	UPDN31	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
25	OUTSEL31	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
24	EN31	0	R/W	Trigger output control 0: Disable 1: Enable
23	-	0	R	Read as 0
22:20	INSEL30[2:0]	000	R/W	Select the input trigger (T32A ch1 Timer C internal trigger input) 000: T32A ch0 Timer register C0 match trigger (T32A00TRGOUTCMPC0) 001: T32A ch0 Timer register C1 match trigger (T32A00TRGOUTCMPC1) 010: T32A ch0 Timer C overflow trigger (T32A00TRGOUTOFC) 011: T32A ch0 Timer C underflow trigger (T32A00TRGOUTUFC) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
19	-	0	R	Read as 0
18	UPDN30	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
17	OUTSEL30	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
16	EN30	0	R/W	Trigger output control 0: Disable 1: Enable
15	-	0	R	Read as 0
14:12	INSEL29[2:0]	000	R/W	Select the input trigger (T32A ch1 Timer B internal trigger input) 000: T32A ch1 Timer register A0 match trigger (T32A01TRGOUTCMPA0) 001: T32A ch1 Timer register A1 match trigger (T32A01TRGOUTCMPA1) 010: T32A ch1 Timer A overflow trigger (T32A01TRGOUTOFA) 011: T32A ch1 Timer A underflow trigger (T32A01TRGOUTUFA) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
11	-	0	R	Read as 0

Bit	Bit symbol	After reset	Type	Function
10	UPDN29	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
9	OUTSEL29	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
8	EN29	0	R/W	Trigger output control 0: Disable 1: Enable
7	-	0	R	Read as 0
6:4	INSEL28[2:0]	000	R/W	Select the input trigger (T32A ch1 Timer A internal trigger input) 000: PF0 (TRGIN0) 001: PB1 (TRGIN1) 010: PF2 (TRGIN2) 011: UART ch1 transmission completion trigger (UART1TXTRG) 100: UART ch1 reception completion trigger (UART1RXTRG) 101: TSPI ch1 transmit completion (TSPI1TXEND) 110: TSPI ch1 receive completion (TSPI1RXEND) 111: A-ENC32 ch1 divided pulse signal (ENC1TIMPLS)
3	-	0	R	Read as 0
2	UPDN28	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
1	OUTSEL28	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
0	EN28	0	R/W	Trigger output control 0: Disable 1: Enable

2.2.4.9. *[TSELxCR8]* (Control Register 8)

Bit	Bit symbol	After reset	Type	Function
31	-	0	R	Read as 0
30:28	INSEL35[2:0]	000	R/W	Select the input trigger (T32A ch3 Timer B internal trigger input) 000: T32A ch3 Timer register A0 match trigger (T32A03TRGOUTCMPA0) 001: T32A ch3 Timer register A1 match trigger (T32A03TRGOUTCMPA1) 010: T32A ch3 Timer A overflow trigger (T32A03TRGOUTOFA) 011: T32A ch3 Timer A underflow trigger (T32A03TRGOUTUFA) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
27	-	0	R	Read as 0
26	UPDN35	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
25	OUTSEL35	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
24	EN35	0	R/W	Trigger output control 0: Disable 1: Enable
23	-	0	R	Read as 0
22:20	INSEL34[2:0]	000	R/W	Select the input trigger (T32A ch3 Timer A internal trigger input) 000: PF0 (TRGIN0) 001: PB1 (TRGIN1) 010: PF2 (TRGIN2) 011: UART ch3 transmission completion trigger (UART3TXTRG) 100: UART ch3 reception completion trigger (UART3RXTRG) 101: TSPI ch3 transmit completion (TSPI3TXEND) 110: TSPI ch3 receive completion (TSPI3RXEND) 111: I2C ch0 interrupt (INTI2C0)/EI2C ch0 status interrupt (INTI2C0ST)
19	-	0	R	Read as 0
18	UPDN34	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
17	OUTSEL34	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
16	EN34	0	R/W	Trigger output control 0: Disable 1: Enable
15	-	0	R	Read as 0
14:12	INSEL33[2:0]	000	R/W	Select the input trigger (T32A ch2 Timer C internal trigger input) 000: T32A ch1 Timer register C0 match trigger (T32A01TRGOUTCMPC0) 001: T32A ch1 Timer register C1 match trigger (T32A01TRGOUTCMPC1) 010: T32A ch1 Timer C overflow trigger (T32A01TRGOUTOFC) 011: T32A ch1 Timer C underflow trigger (T32A01TRGOUTUFC) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
11	-	0	R	Read as 0

Bit	Bit symbol	After reset	Type	Function
10	UPDN33	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
9	OUTSEL33	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
8	EN33	0	R/W	Trigger output control 0: Disable 1: Enable
7	-	0	R	Read as 0
6:4	INSEL32[2:0]	000	R/W	Select the input trigger (T32A ch2 Timer B internal trigger input) 000: T32A ch2 Timer register A0 match trigger (T32A02TRGOUTCMPA0) 001: T32A ch2 Timer register A1 match trigger (T32A02TRGOUTCMPA1) 010: T32A ch2 Timer A overflow trigger (T32A02TRGOUTOFA) 011: T32A ch2 Timer A underflow trigger (T32A02TRGOUTUFA) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
3	-	0	R	Read as 0
2	UPDN32	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
1	OUTSEL32	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
0	EN32	0	R/W	Trigger output control 0: Disable 1: Enable

2.2.4.10. *[TSELxCR9]* (Control Register 9)

Bit	Bit symbol	After reset	Type	Function
31	-	0	R	Read as 0
30:28	INSEL39[2:0]	000	R/W	Select the input trigger (T32A ch4 Timer C internal trigger input) 000: T32A ch3 Timer register C0 match trigger (T32A03TRGOUTCMPC0) 001: T32A ch3 Timer register C1 match trigger (T32A03TRGOUTCMPC1) 010: T32A ch3 Timer C overflow trigger (T32A03TRGOUTOFC) 011: T32A ch3 Timer C underflow trigger (T32A03TRGOUTUFC) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
27	-	0	R	Read as 0
26	UPDN39	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
25	OUTSEL39	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
24	EN39	0	R/W	Trigger output control 0: Disable 1: Enable
23	-	0	R	Read as 0
22:20	INSEL38[2:0]	000	R/W	Select the input trigger (T32A ch4 Timer B internal trigger input) 000: T32A ch4 Timer register A0 match trigger (T32A04TRGOUTCMPA0) 001: T32A ch4 Timer register A1 match trigger (T32A04TRGOUTCMPA1) 010: T32A ch4 Timer A overflow trigger (T32A04TRGOUTOFA) 011: T32A ch4 Timer A underflow trigger (T32A04TRGOUTUFA) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
19	-	0	R	Read as 0
18	UPDN38	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
17	OUTSEL38	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
16	EN38	0	R/W	Trigger output control 0: Disable 1: Enable
15	-	0	R	Read as 0
14:12	INSEL37[2:0]	000	R/W	Select the input trigger (T32A ch4 Timer A internal trigger input) 000: PF0 (TRGIN0) 001: PB1 (TRGIN1) 010: PF2 (TRGIN2) 011: A-ENC32 ch0 divided pulse signal (ENC0TIMPLS) 100: ADC unit B general purpose trigger interrupt (INTADBTRG) 101: ADC unit B single conversion interrupt (INTADBSGL) 110: ADC unit B continuous conversion interrupt (INTADBCNT) 111: ADC unit B monitor function 0 Interrupt (INTADBCP0)
11	-	0	R	Read as 0

Bit	Bit symbol	After reset	Type	Function
10	UPDN37	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
9	OUTSEL37	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
8	EN37	0	R/W	Trigger output control 0: Disable 1: Enable
7	-	0	R	Read as 0
6:4	INSEL36[2:0]	000	R/W	Select the input trigger (T32A ch3 Timer C internal trigger input) 000: T32A ch2 Timer register C0 match trigger (T32A02TRGOUTCMPC0) 001: T32A ch2 Timer register C1 match trigger (T32A02TRGOUTCMPC1) 010: T32A ch2 Timer C overflow trigger (T32A02TRGOUTOFC) 011: T32A ch2 Timer C underflow trigger (T32A02TRGOUTUFC) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
3	-	0	R	Read as 0
2	UPDN36	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
1	OUTSEL36	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
0	EN36	0	R/W	Trigger output control 0: Disable 1: Enable

2.2.4.11. *[TSELxCR10]* (Control Register 10)

Bit	Bit symbol	After reset	Type	Function
31:23	-	0	R	Read as 0
22:20	INSEL42[2:0]	000	R/W	Select the input trigger (T32A ch5 Timer C internal trigger input) 000: T32A ch4 Timer register C0 match trigger (T32A04TRGOUTCMPC0) 001: T32A ch4 Timer register C1 match trigger (T32A04TRGOUTCMPC1) 010: T32A ch4 Timer C overflow trigger (T32A04TRGOUTOFC) 011: T32A ch4 Timer C underflow trigger (T32A04TRGOUTUFC) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
19	-	0	R	Read as 0
18	UPDN42	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
17	OUTSEL42	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
16	EN42	0	R/W	Trigger output control 0: Disable 1: Enable
15	-	0	R	Read as 0
14:12	INSEL41[2:0]	000	R/W	Select the input trigger (T32A ch5 Timer B internal trigger input) 000: T32A ch5 Timer register A0 match trigger (T32A05TRGOUTCMPA0) 001: T32A ch5 Timer register A1 match trigger (T32A05TRGOUTCMPA1) 010: T32A ch5 Timer A overflow trigger (T32A05TRGOUTOFA) 011: T32A ch5 Timer A underflow trigger (T32A05TRGOUTUFA) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
11	-	0	R	Read as 0
10	UPDN41	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
9	OUTSEL41	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
8	EN41	0	R/W	Trigger output control 0: Disable 1: Enable
7	-	0	R	Read as 0
6:4	INSEL40[2:0]	000	R/W	Select the input trigger (T32A ch5 Timer A internal trigger input) 000: PF0 (TRGIN0) 001: PB1 (TRGIN1) 010: PF2 (TRGIN2) 011: ADC unit A general purpose trigger interrupt (INTADATRG) 100: ADC unit A single conversion interrupt (INTADASGL) 101: ADC unit A continuous conversion interrupt (INTADACNT) 110: ADC unit A monitor function 0 Interrupt (INTADACP0) 111: ADC unit A monitor function 1 Interrupt (INTADACP1)
3	-	0	R	Read as 0

Bit	Bit symbol	After reset	Type	Function
2	UPDN40	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
1	OUTSEL40	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
0	EN40	0	R/W	Trigger output control 0: Disable 1: Enable

2.3. Direct Memory Access Controller (DMAC)

2.3.1. Built-in Unit

Following table shows the built-in unit of each product.

Table 2.8 DMAC Built-in Unit

Product name	DMAC unit (✓: Available, - : N/A)
	Unit A
M4K4	✓
M4K2	✓
M4K1	✓

2.3.2. DMA Request Table

Following table shows the DMA request List.

The channel which has a register name in the trigger selector column of a table should choose the request used by a trigger selector.

"-" in the table does not have an applicable function.

Table 2.9 DMA Request Table (1/4)

ch No	Single transfer		Burst transfer		
		Signal name	Trigger selector		Signal name
0	TSPI ch0 reception	TSPI0RX_DMA	-	TSPI ch0 reception	TSPI0RX_DMA
1	TSPI ch0 transmission	TSPI0TX_DMA	-	TSPI ch0 transmission	TSPI0TX_DMA
2	TSPI ch1 reception	TSPI1RX_DMA	-	TSPI ch1 reception	TSPI1RX_DMA
3	TSPI ch1 transmission	TSPI1TX_DMA	-	TSPI ch1 transmission	TSPI1TX_DMA
4	TSPI ch2 reception	TSPI2RX_DMA	-	TSPI ch2 reception	TSPI2RX_DMA
5	TSPI ch2 transmission	TSPI2TX_DMA	-	TSPI ch2 transmission	TSPI2TX_DMA
6	TSPI ch3 reception	TSPI3RX_DMA	-	TSPI ch3 reception	TSPI3RX_DMA
7	TSPI ch3 transmission	TSPI3TX_DMA	***[TSEL0CR0]*** <INSEL0>	TSPI ch3 transmission	TSPI3TX_DMA
				ADC unit B general purpose trigger	ADBTRG_DMAREQ
				ADC unit B single conversion	ADBSGL_DMAREQ
				ADC unit B continue conversion	ADBCNT_DMAREQ
8	UART ch0 reception	UART0RX_DMAREQ	-	UART ch0 reception	UART0RX_DMAREQ
9	UART ch0 transmission	UART0TX_DMAREQ	-	UART ch0 transmission	UART0TX_DMAREQ
10	UART ch1 reception	UART1RX_DMAREQ	-	UART ch1 reception	UART1RX_DMAREQ
11	UART ch1 transmission	UART1TX_DMAREQ	-	UART ch1 transmission	UART1TX_DMAREQ
12	UART ch2 reception	UART2RX_DMAREQ	-	UART ch2 reception	UART2RX_DMAREQ
13	UART ch2 transmission	UART2TX_DMAREQ	-	UART ch2 transmission	UART2TX_DMAREQ
14	UART ch3 reception	UART3RX_DMAREQ	-	UART ch3 reception	UART3RX_DMAREQ
15	UART ch3 transmission	UART3TX_DMAREQ	-	UART ch3 transmission	UART3TX_DMAREQ
16	-	-		I2C/EI2C ch0 reception	I2C0ARXDMAREQ/ I2C0RXDMAREQ

Note: The ch7 is set by trigger source of DMA request. For the detail of connection, refer to the "2.2. Trigger Selector (TRGSEL)".

Table 2.10 DMA Request Table (2/4)

ch No	Single transfer		Burst transfer		
		Signal name	Trigger selector		Signal name
17	-	-		I2C/EI2C ch0 transmission	I2C0ATXDMAREQ/ I2C0TXDMAREQ
18	-	-	***[TSEL0CR0]*** <INSEL1>	ADC unit A general purpose trigger	ADATRG_DMAREQ
				ADC unit A single conversion	ADASGL_DMAREQ
				ADC unit A continue conversion	ADACNT_DMAREQ
19	-	-	***[TSEL0CR0]*** <INSEL2>	T32A ch0 compare A1 matched	T32A00DMAREQCMPA1
				T32A ch0 compare C1 matched	T32A00DMAREQCMPC1
				T32A ch1 compare A1 matched	T32A01DMAREQCMPA1
				T32A ch1 compare C1 matched	T32A01DMAREQCMPC1
				A-PMD ch0 PWM interrupt	INTPWM0
20	-	-	***[TSEL0CR0]*** <INSEL3>	T32A ch2 compare A1 matched	T32A02DMAREQCMPA1
				T32A ch2 compare C1 matched	T32A02DMAREQCMPC1
				T32A ch3 compare A1 matched	T32A03DMAREQCMPA1
				T32A ch3 compare C1 matched	T32A03DMAREQCMPC1
				A-PMD ch1 PWM interrupt	INTPWM1
21	-	-	***[TSEL0CR1]*** <INSEL4>	T32A ch4 compare A1 matched	T32A04DMAREQCMPA1
				T32A ch4 compare C1 matched	T32A04DMAREQCMPC1
				T32A ch5 compare A1 matched	T32A05DMAREQCMPA1
				T32A ch5 compare C1 matched	T32A05DMAREQCMPC1
22	-	-	***[TSEL0CR1]*** <INSEL5>	T32A ch0 compare B1 matched	T32A00DMAREQCMPB1
				T32A ch1 compare B1 matched	T32A01DMAREQCMPB1
				T32A ch2 compare B1 matched	T32A02DMAREQCMPB1
				T32A ch3 compare B1 matched	T32A03DMAREQCMPB1
				T32A ch4 compare B1 matched	T32A04DMAREQCMPB1
				T32A ch5 compare B1 matched	T32A05DMAREQCMPB1
23	-	-	***[TSEL0CR1]*** <INSEL6>	T32A ch0 capture A0	T32A00DMAREQCAPA0
				T32A ch0 capture A1	T32A00DMAREQCAPA1
				T32A ch1 capture A0	T32A01DMAREQCAPA0
				T32A ch1 capture A1	T32A01DMAREQCAPA1
				T32A ch0 capture C0	T32A00DMAREQCAPC0
				T32A ch0 capture C1	T32A00DMAREQCAPC1
				T32A ch1 capture C0	T32A01DMAREQCAPC0
				T32A ch1 capture C1	T32A01DMAREQCAPC1
24	-	-	***[TSEL0CR1]*** <INSEL7>	T32A ch2 capture A0	T32A02DMAREQCAPA0
				T32A ch2 capture A1	T32A02DMAREQCAPA1
				T32A ch3 capture A0	T32A03DMAREQCAPA0
				T32A ch3 capture A1	T32A03DMAREQCAPA1
				T32A ch2 capture C0	T32A02DMAREQCAPC0
				T32A ch2 capture C1	T32A02DMAREQCAPC1
				T32A ch3 capture C0	T32A03DMAREQCAPC0
				T32A ch3 capture C1	T32A03DMAREQCAPC1

Note: The ch18 to 24 are set by trigger source of DMA request. For the detail of connection, refer to the "2.2. Trigger Selector (TRGSEL)"

Table 2.11 DMA Request Table (3/4)

ch No	Single transfer		Burst transfer		
		Signal name	Trigger selector		Signal name
25	-	-	***[TSEL0CR2]*** <INSEL8>	T32A ch4 capture A0	T32A04DMAREQCAPA0
				T32A ch4 capture A1	T32A04DMAREQCAPA1
				T32A ch5 capture A0	T32A05DMAREQCAPA0
				T32A ch5 capture A1	T32A05DMAREQCAPA1
				T32A ch4 capture C0	T32A04DMAREQCAPC0
				T32A ch4 capture C1	T32A04DMAREQCAPC1
				T32A ch5 capture C0	T32A05DMAREQCAPC0
				T32A ch5 capture C1	T32A05DMAREQCAPC1
26	-	-	***[TSEL0CR2]*** <INSEL9>	T32A ch0 capture B0	T32A00DMAREQCAPB0
				T32A ch0 capture B1	T32A00DMAREQCAPB1
				T32A ch1 capture B0	T32A01DMAREQCAPB0
				T32A ch1 capture B1	T32A01DMAREQCAPB1
				T32A ch2 capture B0	T32A02DMAREQCAPB0
				T32A ch2 capture B1	T32A02DMAREQCAPB1
27	-	-	***[TSEL0CR2]*** <INSEL10>	T32A ch3 capture B0	T32A03DMAREQCAPB0
				T32A ch3 capture B1	T32A03DMAREQCAPB1
				T32A ch4 capture B0	T32A04DMAREQCAPB0
				T32A ch4 capture B1	T32A04DMAREQCAPB1
				T32A ch5 capture B0	T32A05DMAREQCAPB0
				T32A ch5 capture B1	T32A05DMAREQCAPB1
28	-	-	***[TSEL0CR2]*** <INSEL11>	DMAC ch0 transfer completion	INTDMAATC0
				DMAC ch1 transfer completion	INTDMAATC1
				DMAC ch8 transfer completion	INTDMAATC8
				DMAC ch9 transfer completion	INTDMAATC9
				DMAC ch16 transfer completion	INTDMAATC16
				DMAC ch17 transfer completion	INTDMAATC17
				DMAC ch22 transfer completion	INTDMAATC22
29	-	-	***[TSEL0CR3]*** <INSEL12>	DMAC ch2 transfer completion	INTDMAATC2
				DMAC ch3 transfer completion	INTDMAATC3
				DMAC ch10 transfer completion	INTDMAATC10
				DMAC ch11 transfer completion	INTDMAATC11
				DMAC ch18 transfer completion	INTDMAATC18
				DMAC ch19 transfer completion	INTDMAATC19
				DMAC ch23 transfer completion	INTDMAATC23
				TRGIN0 (PF0)	TRGIN0

Note: The ch25 to 29 are set by trigger source of DMA request. For the detail of connection, refer to the "2.2. Trigger Selector (TRGSEL)

Table 2.12 DMA Request Table (4/4)

ch no.	Single transfer		Burst transfer		
		Signal name	TRG selector		Signal name
30	-	-	***[TSEL0CR3]*** <INSEL13>	DMAC ch4 transfer completion	INTDMAATC4
				DMAC ch5 transfer completion	INTDMAATC5
				DMAC ch12 transfer completion	INTDMAATC12
				DMAC ch13 transfer completion	INTDMAATC13
				DMAC ch20 transfer completion	INTDMAATC20
				DMAC ch24 transfer completion	INTDMAATC24
				DMAC ch26 transfer completion	INTDMAATC26
				TRGIN1 (PB1)	TRGIN1
31	-	-	***[TSEL0CR3]*** <INSEL14>	DMAC ch6 transfer completion	INTDMAATC6
				DMAC ch7 transfer completion	INTDMAATC7
				DMAC ch14 transfer completion	INTDMAATC14
				DMAC ch15 transfer completion	INTDMAATC15
				DMAC ch21 transfer completion	INTDMAATC21
				DMAC ch25 transfer completion	INTDMAATC25
				DMAC ch27 transfer completion	INTDMAATC27
				TRGIN2 (PF2)	TRGIN2

Note: The ch30 and ch31 are set by trigger source of DMA request. For the detail of connection, refer to the "2.2. Trigger Selector (TRGSEL)"

2.4. 32-bit Timer Event Counter (T32A)

2.4.1. Built-in Channel

Following table shows the T32A built-in channel of each product.

Table 2.13 T32A Built-in Channel

Product	T32A channel (✓: Available, - : N/A)					
	ch0	ch1	ch2	ch3	ch4	ch5
M4K4	✓	✓	✓	✓	✓	✓
M4K2	✓	✓	✓	✓	✓	✓
M4K1	✓	✓	✓	✓	✓	✓

2.4.2. Functional Pins

The functional pins are assigned to the port of the following tables.
Please do not use simultaneously the same function currently assigned to two or more pins.
There is also a channel which does not have functional pins depending on a product.

Table 2.14 T32A Functional Pin and Port (1/2)

Channel	Functional pin (Signal name)		Port	Ports for products (✓: Available, - : N/A)		
				M4K4	M4K2	M4K1
ch0	T32A00INA0	Input	PK1	✓	✓	✓
	T32A00INA1	Input	-	-	-	-
	T32A00OUTA	Output	PK0	✓	✓	✓
	T32A00INB0	Input	-	-	-	-
	T32A00INB1	Input	-	-	-	-
	T32A00OUTB	Output	-	-	-	-
	T32A00INC0	Input	PK1	✓	✓	✓
	T32A00INC1	Input	-	-	-	-
	T32A00OUTC	Output	PK0	✓	✓	✓
ch1	T32A01INA0	Input	PA1	✓	✓	-
	T32A01INA1	Input	PA2	✓	-	-
	T32A01OUTA	Output	PA2	✓	-	-
	T32A01INB0	Input	PA0	✓	✓	✓
	T32A01INB1	Input	-	-	-	-
	T32A01OUTB	Output	PA0	✓	✓	✓
	T32A01INC0	Input	PA1	✓	✓	-
	T32A01INC1	Input	PA2	✓	-	-
	T32A01OUTC	Output	PA2	✓	-	-
ch2	T32A02INA0	Input	PG1	✓	✓	✓
	T32A02INA1	Input	PG2	✓	✓	✓
	T32A02OUTA	Output	PG0	✓	✓	✓
	T32A02INB0	Input	-	-	-	-
	T32A02INB1	Input	-	-	-	-
	T32A02OUTB	Output	-	-	-	-
	T32A02INC0	Input	PG1	✓	✓	✓
	T32A02INC1	Input	PG2	✓	✓	✓
	T32A02OUTC	Output	PG0	✓	✓	✓

Table 2.15 T32A Functional Pins and Port (2/2)

Channel	Functional pin (Signal name)		Port	Ports for products (✓: Available, - : N/A)		
				M4K4	M4K2	M4K1
ch3	T32A03INA0	Input	PC1	✓	-	-
	T32A03INA1	Input	PC2	✓	-	-
	T32A03OUTA	Output	PC0	✓	✓	✓
	T32A03INB0	Input	-	-	-	-
	T32A03INB1	Input	-	-	-	-
	T32A03OUTB	Output	-	-	-	-
	T32A03INC0	Input	PC1	✓	-	-
	T32A03INC1	Input	PC2	✓	-	-
	T32A03OUTC	Output	PC0	✓	✓	✓
ch4	T32A04INA0	Input	PF1	✓	-	-
	T32A04INA1	Input	PF2	✓	-	-
	T32A04OUTA	Output	PF0	✓	✓	✓
	T32A04INB0	Input	-	-	-	-
	T32A04INB1	Input	-	-	-	-
	T32A04OUTB	Output	-	-	-	-
	T32A04INC0	Input	PF1	✓	-	-
	T32A04INC1	Input	PF2	✓	-	-
	T32A04OUTC	Output	PF0	✓	✓	✓
ch5	T32A05INA0	Input	PB1	✓	✓	✓
	T32A05INA1	Input	-	-	-	-
	T32A05OUTA	Output	PB0	✓	✓	✓
	T32A05INB0	Input	-	-	-	-
	T32A05INB1	Input	-	-	-	-
	T32A05OUTB	Output	PB1	✓	✓	✓
	T32A05INC0	Input	PB1	✓	✓	✓
	T32A05INC1	Input	-	-	-	-
	T32A05OUTC	Output	PB0	✓	✓	✓

2.4.3. Clock for Prescaler

The 32-bit timer event counter uses the clock of the following table as a prescaler clock.

Table 2.16 T32A Clock for Prescaler

Clock
ΦT0

2.4.4. Internal Signal Connection Specification

2.4.4.1. Capture Trigger Signal Connection

In the 32-bit timer event counter, capture trigger signal is connected to signals of the following table.

The input trigger signal which has a register name in the trigger selector column of the following table should choose the input trigger used by a trigger selector.

Table 2.17 T32A Capture Trigger Connection (1/3)

Channel	Timer	Input signal name of capture trigger	Trigger source		
			Trigger selector	Input trigger signal	Signal name
ch0	Timer A	T32A00TRGINAPHCK (Other timer output)	-	-	-
		T32A00TRGINAPCK (Internal trigger input)	***[TSEL0CR6]*** <INSEL25>	PF0 (TRGIN0)	TRGIN0
				PB1 (TRGIN1)	TRGIN1
				PF2 (TRGIN2)	TRGIN2
				UART ch0 transmission completion trigger	UART0TXTRG
				UART ch0 reception completion trigger	UART0RXTRG
				TSPI ch0 transmit completion	TSPI0TXEND
				TSPI ch0 receive completion	TSPI0RXEND
	Timer B	T32A00TRGINBPHCK (Other timer output)	T32A ch0 timer A output		T32A00OUTA
		T32A00TRGINBPCK (other timer input)	***[TSEL0CR6]*** <INSEL26>	T32A ch0 timer register A0 match trigger	T32A00TRGOUTCMPA0
				T32A ch0 timer register A1 match trigger	T32A00TRGOUTCMPA1
				T32A ch0 timer A overflow trigger	T32A00TRGOUTOFA
				T32A ch0 timer A underflow trigger	T32A00TRGOUTUFA
	Timer C	T32A00TRGINCPHCK (Other timer output)	-	-	-
		T32A00TRGINCPCK (Internal trigger input)	***[TSEL0CR6]*** <INSEL27>	T32A ch5 timer register C0 match trigger	T32A05TRGOUTCMPC0
				T32A ch5 timer register C1 match trigger	T32A05TRGOUTCMPC1
				T32A ch5 timer C overflow trigger	T32A05TRGOUTOFC
				T32A ch5 timer C underflow trigger	T32A05TRGOUTUFC
ch1	Timer A	T32A01TRGINAPHCK (Other timer output)	-	-	-
		T32A01TRGINAPCK (Internal trigger input)	***[TSEL0CR7]*** <INSEL28>	PF0 (TRGIN0)	TRGIN0
				PB1 (TRGIN1)	TRGIN1
				PF2 (TRGIN2)	TRGIN2
				UART ch1 transmission completion trigger	UART1TXTRG
				UART ch1 reception completion trigger	UART1RXTRG
				TSPI ch1 transmit completion	TSPI1TXEND
				TSPI ch1 receive completion	TSPI1RXEND
	Timer B	T32A01TRGINBPHCK (Other timer output)	T32A ch1 timer A output		T32A01OUTA
		T32A01TRGINBPCK (Internal trigger input)	***[TSEL0CR7]*** <INSEL29>	T32A ch1 timer register A0 match trigger	T32A01TRGOUTCMPA0
				T32A ch1 timer register A1 match trigger	T32A01TRGOUTCMPA1
				T32A ch1 timer A overflow trigger	T32A01TRGOUTOFA
				T32A ch1 timer A underflow trigger	T32A01TRGOUTUFA
	Timer C	T32A01TRGINCPHCK (Other timer output)	-	-	-
		T32A00TRGINCPCK (Internal trigger input)	***[TSEL0CR7]*** <INSEL30>	T32A ch0 timer register C0 match trigger	T32A00TRGOUTCMPC0
				T32A ch0 timer register C1 match trigger	T32A00TRGOUTCMPC1
				T32A ch0 timer C overflow trigger	T32A00TRGOUTOFC
				T32A ch0 timer C underflow trigger	T32A00TRGOUTUFC

Note: ***[TSEL0CRn]***<INSELm> is set the internal trigger of trigger source by trigger selector. For the detail of connection, refer to the "2.2. Trigger Selector (TRGSEL)".

Table 2.18 T32A Capture Trigger Connection (2/3)

Channel	Timer	Input signal name of capture trigger	Trigger source		
			Trigger selector	Input trigger signal	Signal name
ch2	Timer A	T32A02TRGINAPHCK (Other timer output)	-	-	-
		T32A02TRGINAPCK (Internal trigger input)	***[TSEL0CR7]*** <INSEL31>	PF0 (TRGIN0)	TRGIN0
				PB1 (TRGIN1)	TRGIN1
				PF2 (TRGIN2)	TRGIN2
				UART ch2 transmission completion trigger	UART2TXTRG
				UART ch2 reception completion trigger	UART2RXTRG
				TSPI ch2 transmit completion	TSPI2TXEND
				TSPI ch2 receive completion	TSPI2RXEND
	Timer B	T32A02TRGINBPHCK (Other timer output)	T32A ch2 timer A output		T32A02OUTA
		T32A02TRGINBPCK (Internal trigger input)	***[TSEL0CR8]*** <INSEL32>	T32A ch2 timer register A0 match trigger	T32A02TRGOUTCMPA0
				T32A ch2 timer register A1 match trigger	T32A02TRGOUTCMPA1
				T32A ch2 timer A overflow trigger	T32A02TRGOUTOFA
				T32A ch2 timer A underflow trigger	T32A02TRGOUTUFA
	Timer C	T32A02TRGINCPHCK (Other timer output)	-	-	-
		T32A02TRGINCPCK (Internal trigger input)	***[TSEL0CR8]*** <INSEL33>	T32A ch1 timer register C0 match trigger	T32A01TRGOUTCMPC0
				T32A ch1 timer register C1 match trigger	T32A01TRGOUTCMPC1
				T32A ch1 timer C overflow trigger	T32A01TRGOUTOFC
				T32A ch1 timer C underflow trigger	T32A01TRGOUTUFC
ch3	Timer A	T32A03TRGINAPHCK (Other timer output)	-	-	-
		T32A03TRGINAPCK (Internal trigger input)	***[TSEL0CR8]*** <INSEL34>	PF0 (TRGIN0)	TRGIN0
				PB1 (TRGIN1)	TRGIN1
				PF2 (TRGIN2)	TRGIN2
				UART ch3 transmission completion trigger	UART3TXTRG
				UART ch3 reception completion trigger	UART3RXTRG
				TSPI ch3 transmit completion	TSPI3TXEND
				TSPI ch3 receive completion	TSPI3RXEND
				I2C ch0 interrupt/ EI2C ch0 status interrupt	INTI2C0/INTI2C0ST
	Timer B	T32A03TRGINBPHCK (Other timer output)	T32A ch3 timer A output		T32A03OUTA
		T32A03TRGINBPCK (Internal trigger input)	***[TSEL0CR8]*** <INSEL35>	T32A ch3 timer register A0 match trigger	T32A03TRGOUTCMPA0
				T32A ch3 timer register A1 match trigger	T32A03TRGOUTCMPA1
				T32A ch3 timer A overflow trigger	T32A03TRGOUTOFA
				T32A ch3 timer A underflow trigger	T32A03TRGOUTUFA
	Timer C	T32A03TRGINCPHCK (Other timer output)	-	-	-
		T32A03TRGINCPCK (Internal trigger input)	***[TSEL0CR9]*** <INSEL36>	T32A ch2 timer register C0 match trigger	T32A02TRGOUTCMPC0
				T32A ch2 timer register C1 match trigger	T32A02TRGOUTCMPC1
				T32A ch2 timer C overflow trigger	T32A02TRGOUTOFC
				T32A ch2 timer C underflow trigger	T32A02TRGOUTUFC

Note: ***[TSEL0CRn]***<INSELm> is set the internal trigger of trigger source by trigger selector. For the detail of connection, refer to the "2.2. Trigger Selector (TRGSEL)".

Table 2.19 T32A Capture Trigger Connection (3/3)

Channel	Timer	Input signal name of capture trigger	Trigger source		
			Trigger selector	Input trigger signal	Signal name
ch4	Timer A	T32A04TRGINAPHCK (Other timer output)	-	-	-
		T32A04TRGINAPCK (Internal trigger input)	***[TSEL0CR9]*** <INSEL37>	PF0 (TRGIN0)	TRGIN0
				PB1 (TRGIN1)	TRGIN1
				PF2 (TRGIN2)	TRGIN2
				A-ENC32 divided plus signal	ENC0TIMPLS
				ADC unit B general purpose trigger interrupt	INTADBTRG
				ADC unit B single conversion interrupt	INTADBSGL
				ADC unit B continuous conversion interrupt	INTADBCNT
				ADC unit B monitor function 0 interrupt	INTADBCP0
	Timer B	T32A04TRGINBPHCK (Other timer output)	T32A ch4 timer A output		T32A04OUTA
		T32A04TRGINBPCK (Internal trigger input)	***[TSEL0CR9]*** <INSEL38>	T32A ch4 timer register A0 match trigger	T32A04TRGOUTCMPA0
				T32A ch4 timer register A1 match trigger	T32A04TRGOUTCMPA1
				T32A ch4 timer A overflow trigger	T32A04TRGOUTOFA
				T32A ch4 timer A underflow trigger	T32A04TRGOUTUFA
	Timer C	T32A04TRGINCPHCK (Other timer output)	-	-	-
		T32A04TRGINCPCK (Internal trigger input)	***[TSEL0CR9]*** <INSEL39>	T32A ch3 timer register C0 match trigger	T32A03TRGOUTCMPC0
				T32A ch3 timer register C1 match trigger	T32A03TRGOUTCMPC1
				T32A ch3 timer C overflow trigger	T32A03TRGOUTOFC
				T32A ch3 timer C underflow trigger	T32A03TRGOUTUFC
ch5	Timer A	T32A05TRGINAPHCK (Other timer output)	-	-	-
		T32A05TRGINAPCK (Internal trigger input)	***[TSEL0CR10]*** <INSEL40>	PF0 (TRGIN0)	TRGIN0
				PB1 (TRGIN1)	TRGIN1
				PF2 (TRGIN2)	TRGIN2
				ADC unit A general purpose trigger interrupt	INTADATRG
				ADC unit A single conversion interrupt	INTADASGL
				ADC unit A continuous conversion interrupt	INTADACNT
				ADC unit A monitor function 0 interrupt	INTADACP0
				ADC unit A monitor function 1 interrupt	INTADACP1
	Timer B	T32A05TRGINBPHCK (Other timer output)	T32A ch5 timer A output		T32A05OUTA
		T32A05TRGINBPCK (Internal trigger input)	***[TSEL0CR10]*** <INSEL41>	T32A ch5 timer register A0 match trigger	T32A05TRGOUTCMPA0
				T32A ch5 timer register A1 match trigger	T32A05TRGOUTCMPA1
				T32A ch5 timer A overflow trigger	T32A05TRGOUTOFA
				T32A ch5 timer A underflow trigger	T32A05TRGOUTUFA
	Timer C	T32A05TRGINCPHCK (Other timer output)	-	-	-
		T32A05TRGINCPCK (Internal trigger input)	***[TSEL0CR10]*** <INSEL42>	T32A ch4 timer register C0 match trigger	T32A04TRGOUTCMPC0
				T32A ch4 timer register C1 match trigger	T32A04TRGOUTCMPC1
				T32A ch4 timer C overflow trigger	T32A04TRGOUTOFC
				T32A ch4 timer C underflow trigger	T32A04TRGOUTUFC

Note: ***[TSEL0CRn]***<INSELm> is set the internal trigger of trigger source by trigger selector. For the detail of connection, refer to the "2.2. Trigger Selector (TRGSEL)".

2.4.4.2. Synchronous Control Connection

In the 32-bit timer event counter, as shown in the following tables, synchronous connection of the timer is carried out within the same channel.

Table 2.20 T32A Synchronous Control Connection Specifications

Channel	Timer	Master		Timer	Slave	
		Function (output)	Signal name		Function (input)	Signal name
ch0	Timer A	Synchronous start output A	T32A00SYNCSTARTOUTA	Timer B	Synchronous start B	T32A00SYNCSTARTB
		Synchronous stop output A	T32A00SYNCSTOPOUTA		Synchronous stop B	T32A00SYNCSTOPB
		Synchronous Reload output A	T32A00SYNCRELOADOUTA		Synchronous Reload B	T32A00SYNCRELOADB
ch1	Timer A	Synchronous start output A	T32A01SYNCSTARTOUTA	Timer B	Synchronous start B	T32A01SYNCSTARTB
		Synchronous stop output A	T32A01SYNCSTOPOUTA		Synchronous stop B	T32A01SYNCSTOPB
		Synchronous Reload output A	T32A01SYNCRELOADOUTA		Synchronous Reload B	T32A01SYNCRELOADB
ch2	Timer A	Synchronous start output A	T32A02SYNCSTARTOUTA	Timer B	Synchronous start B	T32A02SYNCSTARTB
		Synchronous stop output A	T32A02SYNCSTOPOUTA		Synchronous stop B	T32A02SYNCSTOPB
		Synchronous Reload output A	T32A02SYNCRELOADOUTA		Synchronous Reload B	T32A02SYNCRELOADB
ch3	Timer A	Synchronous start output A	T32A03SYNCSTARTOUTA	Timer B	Synchronous start B	T32A03SYNCSTARTB
		Synchronous stop output A	T32A03SYNCSTOPOUTA		Synchronous stop B	T32A03SYNCSTOPB
		Synchronous Reload output A	T32A03SYNCRELOADOUTA		Synchronous Reload B	T32A03SYNCRELOADB
ch4	Timer A	Synchronous start output A	T32A04SYNCSTARTOUTA	Timer B	Synchronous start B	T32A04SYNCSTARTB
		Synchronous stop output A	T32A04SYNCSTOPOUTA		Synchronous stop B	T32A04SYNCSTOPB
		Synchronous Reload output A	T32A04SYNCRELOADOUTA		Synchronous Reload B	T32A04SYNCRELOADB
ch5	Timer A	Synchronous start output A	T32A05SYNCSTARTOUTA	Timer B	Synchronous start B	T32A05SYNCSTARTB
		Synchronous stop output A	T32A05SYNCSTOPOUTA		Synchronous stop B	T32A05SYNCSTOPB
		Synchronous Reload output A	T32A05SYNCRELOADOUTA		Synchronous Reload B	T32A05SYNCRELOADB

2.4.5. Pulse Counter List for Each Product

In the 32-bit timer event counter, as shown in the following tables, correspondence of a pulse counter changes with products.

Table 2.21 T32A Pulse Counter List for Each Product

Channel	M4K4	M4K2	M4K1
ch0	1-phase pulse count		
ch1	2-phase pulse count 1-phase pulse count	1-phase pulse count	-
ch2	2-phase pulse count 1-phase pulse count		
ch3	2-phase pulse count 1-phase pulse count	-	
ch4	2-phase pulse count 1-phase pulse count	-	
ch5	1-phase pulse count		

2.4.6. DMA Request

In the 32-bit timer event counter, DMA request are shown in the following table.

What has the statement of a register name in the trigger selector column of a table should choose the request used by a trigger selector.

Table 2.22 T32A DMA Request (1/2)

Channel	Request	Signal name	Trigger selector	DMA request channel		
					Single transfer	Burst transfer
ch0	DMA request at match A1 register	T32A00DMAREQCMPA1	***[TSEL0CR0]*** <INSEL2>	19	-	✓
	DMA request at match C1 register	T32A00DMAREQCMPC1				
	DMA request at match B1 register	T32A00DMAREQCMPB1	***[TSEL0CR1]*** <INSEL5>	22	-	✓
	DMA request at capture A0 register	T32A00DMAREQCAPA0	***[TSEL0CR1]*** <INSEL6>	23	-	✓
	DMA request at capture A1 register	T32A00DMAREQCAPA1				
	DMA request at capture C0 register	T32A00DMAREQCAPC0				
	DMA request at capture C1 register	T32A00DMAREQCAPC1				
	DMA request at capture B0 register	T32A00DMAREQCAPB0	***[TSEL0CR2]*** <INSEL9>	26	-	✓
	DMA request at capture B1 register	T32A00DMAREQCAPB1				
ch1	DMA request at match A1 register	T32A01DMAREQCMPA1	***[TSEL0CR0]*** <INSEL2>	19	-	✓
	DMA request at match C1 register	T32A01DMAREQCMPC1				
	DMA request at match B1 register	T32A01DMAREQCMPB1	***[TSEL0CR1]*** <INSEL5>	22	-	✓
	DMA request at capture A0 register	T32A01DMAREQCAPA0	***[TSEL0CR1]*** <INSEL6>	23	-	✓
	DMA request at capture A1 register	T32A01DMAREQCAPA1				
	DMA request at capture C0 register	T32A01DMAREQCAPC0				
	DMA request at capture C1 register	T32A01DMAREQCAPC1				
	DMA request at capture B0 register	T32A01DMAREQCAPB0	***[TSEL0CR2]*** <INSEL9>	26	-	✓
	DMA request at capture B1 register	T32A01DMAREQCAPB1				

Note: ✓: Available, - : N/A

Table 2.23 T32A DMA Request (2/2)

Channel	Request	Signal name	Trigger selector	DMA request channel		
					Single transfer	Burst transfer
ch2	DMA request at match A1 register	T32A02DMAREQCMPA1	***[TSEL0CR0]*** <INSEL3>	20	-	✓
	DMA request at match C1 register	T32A02DMAREQCMPC1				
	DMA request at match B1 register	T32A02DMAREQCMPB1	***[TSEL0CR1]*** <INSEL5>	22	-	✓
	DMA request at capture A0 register	T32A02DMAREQCAPA0	***[TSEL0CR1]*** <INSEL7>	24	-	✓
	DMA request at capture A1 register	T32A02DMAREQCAPA1				
	DMA request at capture C0 register	T32A02DMAREQCAPC0				
	DMA request at capture C1 register	T32A02DMAREQCAPC1				
	DMA request at capture B0 register	T32A02DMAREQCAPB0	***[TSEL0CR2]*** <INSEL9>	26	-	✓
	DMA request at capture B1 register	T32A02DMAREQCAPB1				
ch3	DMA request at match A1 register	T32A03DMAREQCMPA1	***[TSEL0CR0]*** <INSEL3>	20	-	✓
	DMA request at match C1 register	T32A03DMAREQCMPC1				
	DMA request at match B1 register	T32A03DMAREQCMPB1	***[TSEL0CR1]*** <INSEL5>	22	-	✓
	DMA request at capture A0 register	T32A03DMAREQCAPA0	***[TSEL0CR1]*** <INSEL7>	24	-	✓
	DMA request at capture A1 register	T32A03DMAREQCAPA1				
	DMA request at capture C0 register	T32A03DMAREQCAPC0				
	DMA request at capture C1 register	T32A03DMAREQCAPC1				
	DMA request at capture B0 register	T32A03DMAREQCAPB0	***[TSEL0CR2]*** <INSEL10>	27	-	✓
	DMA request at capture B1 register	T32A03DMAREQCAPB1				
ch4	DMA request at match A1 register	T32A04DMAREQCMPA1	***[TSEL0CR1]*** <INSEL4>	21	-	✓
	DMA request at match C1 register	T32A04DMAREQCMPC1				
	DMA request at match B1 register	T32A04DMAREQCMPB1	***[TSEL0CR1]*** <INSEL5>	22	-	✓
	DMA request at capture A0 register	T32A04DMAREQCAPA0	***[TSEL0CR2]*** <INSEL8>	25	-	✓
	DMA request at capture A1 register	T32A04DMAREQCAPA1				
	DMA request at capture C0 register	T32A04DMAREQCAPC0				
	DMA request at capture C1 register	T32A04DMAREQCAPC1				
	DMA request at capture B0 register	T32A04DMAREQCAPB0	***[TSEL0CR2]*** <INSEL10>	27	-	✓
	DMA request at capture B1 register	T32A04DMAREQCAPB1				
ch5	DMA request at match A1 register	T32A05DMAREQCMPA1	***[TSEL0CR1]*** <INSEL4>	21	-	✓
	DMA request at match C1 register	T32A05DMAREQCMPC1				
	DMA request at match B1 register	T32A05DMAREQCMPB1	***[TSEL0CR1]*** <INSEL5>	22	-	✓
	DMA request at capture A0 register	T32A05DMAREQCAPA0	***[TSEL0CR2]*** <INSEL8>	25	-	✓
	DMA request at capture A1 register	T32A05DMAREQCAPA1				
	DMA request at capture C0 register	T32A05DMAREQCAPC0				
	DMA request at capture C1 register	T32A05DMAREQCAPC1				
	DMA request at capture B0 register	T32A05DMAREQCAPB0	***[TSEL0CR2]*** <INSEL10>	27	-	✓
	DMA request at capture B1 register	T32A05DMAREQCAPB1				

Note: ✓: Available, - : N/A

2.4.7. Internal Signal Connection Specification

Every count interrupt (INTT32AxEVRYC) does not correspond in the TMPM4K Group(1).

2.5. Universal Asynchronous Receiver Transmitter Circuit (UART)

2.5.1. Built-in Channel

Following table show the UART built-in channel of each product.
In TMPM4K Group(1), Maximum Communication speed of UART is 5 Mbps.

Table 2.24 UART Built-in Channel

Product	UART channel (✓: Available, - : N/A)			
	ch0	ch1	ch2	ch3
M4K4	✓	✓	✓	✓
M4K2	✓	✓	✓	-
M4K1	✓	✓	✓	-

2.5.2. Function Pin and Port

The functional pins are assigned to the port of the following tables.
Please do not use simultaneously the same function currently assigned to two or more pins.
There is also a channel which does not have functional pins depending on a product.

Table 2.25 UART Functional Pin and Port

Channel	Function Pin (signal name)		Port	Products list (✓: Available, - : N/A)		
				M4K4	M4K2	M4K1
ch0	UT0TXDA	Output	PK1	✓	✓	✓
			PK3	✓	✓	✓
			PK0	✓	✓	✓
			PK2	✓	✓	✓
	UT0RXD	Input	PK0	✓	✓	✓
			PK2	✓	✓	✓
			PK1	✓	✓	✓
			PK3	✓	✓	✓
ch1	UT1TXDA	Output	PA0	✓	✓	-
			PA1	✓	✓	-
			PB1	✓	✓	✓
			PB0	✓	✓	✓
	UT1RXD	Input	PA1	✓	✓	-
			PA0	✓	✓	-
			PB0	✓	✓	✓
			PB1	✓	✓	✓
ch2	UT2TXDA	Output	PG0	✓	✓	✓
	UT2RXD	Input	PG1	✓	✓	✓
ch3	UT3TXDA	Output	PC0	✓	-	-
			PC1	✓	-	-
	UT3RXD	Input	PC1	✓	-	-
			PC0	✓	-	-

2.5.3. Half Clock Mode Support

Half clock mode of the UART corresponds to 1-pin mode only.

2.5.4. Clock for Prescaler

The UART use the clock of the following table as a prescaler clock.

Table 2.26 UART Clock for Prescaler

Clock
ΦT0

2.5.5. DMA Request

The following table shows the DMA request in the UART.
"-" in the table does not have an applicable function.

Table 2.27 UART DMA Request

Channel	Request	Signal name	Trigger selector	DMA request channel		
					Single transfer	Burst transfer
ch0	UART ch0 reception	UART0RX_DMAREQ	-	8	✓	✓
	UART ch0 transmission	UART0TX_DMAREQ		9	✓	✓
ch1	UART ch1 reception	UART1RX_DMAREQ	-	10	✓	✓
	UART ch1 transmission	UART1TX_DMAREQ		11	✓	✓
ch2	UART ch2 reception	UART2RX_DMAREQ	-	12	✓	✓
	UART ch2 transfer	UART2TX_DMAREQ		13	✓	✓
ch3	UART ch3 reception	UART3RX_DMAREQ	-	14	✓	✓
	UART ch3 transmission	UART3TX_DMAREQ	-	15	✓	✓

Note: ✓: Available, - : N/A

2.5.6. Internal Signal Connection Specification

2.5.6.1. Trigger Transfer Signal Connection

Transfer function of the UART has a trigger signal control.
A trigger control signal is selected with the trigger source and use it as the following table.

Table 2.28 UART Trigger Transfer Signal Connection

Channel		Trigger source		
	Signal	Trigger selector	Input trigger signal	Signal name
ch0	UART0TRGIN	***[TSEL0CR5]*** <INSEL21>	PF0 (TRGIN0)	TRGIN0
			PB1 (TRGIN1)	TRGIN1
			PF2 (TRGIN2)	TRGIN2
			T32A ch5 timer register A1 match trigger	T32A05TRGOUTCMPA1
			T32A ch5 timer register B1 match trigger	T32A05TRGOUTCMPB1
			T32A ch5 timer register C1 match trigger	T32A05TRGOUTCMPC1
ch1	UART1TRGIN	***[TSEL0CR5]*** <INSEL22>	PF0 (TRGIN0)	TRGIN0
			PB1 (TRGIN1)	TRGIN1
			PF2 (TRGIN2)	TRGIN2
			T32A ch5 timer register A1 match trigger	T32A05TRGOUTCMPA1
			T32A ch5 timer register B1 match trigger	T32A05TRGOUTCMPB1
			T32A ch5 timer register C1 match trigger	T32A05TRGOUTCMPC1
ch2	UART2TRGIN	***[TSEL0CR5]*** <INSEL23>	PF0 (TRGIN0)	TRGIN0
			PB1 (TRGIN1)	TRGIN1
			PF2 (TRGIN2)	TRGIN2
			T32A ch5 timer register A1 match trigger	T32A05TRGOUTCMPA1
			T32A ch5 timer register B1 match trigger	T32A05TRGOUTCMPB1
			T32A ch5 timer register C1 match trigger	T32A05TRGOUTCMPC1
ch3	UART3TRGIN	***[TSEL0CR6]*** <INSEL24>	PF0 (TRGIN0)	TRGIN0
			PB1 (TRGIN1)	TRGIN1
			PF2 (TRGIN2)	TRGIN2
			T32A ch5 timer register A1 match trigger	T32A05TRGOUTCMPA1
			T32A ch5 timer register B1 match trigger	T32A05TRGOUTCMPB1
			T32A ch5 timer register C1 match trigger	T32A05TRGOUTCMPC1

Note: ***[TSEL0CRn]***<INSELm> is set the internal trigger of trigger source by trigger selector. For the detail of connection, refer to the "2.2. Trigger Selector (TRGSEL)".

2.5.6.2. T32A Connection

In the UART, there is a signal connected with the peripheral function inside in addition to this as shown in the following table.

Table 2.29 UART Inside Connection List: Output

Channel	Function output		Trigger selector	Output destination	
		Signal name			Signal name
ch0	UART ch0 transmission completion trigger output	UART0TXTRG	***[TSEL0CR6]*** <INSEL25>	T32A ch0 Timer A	T32A00TRGINAPCK
	UART ch0 reception completion trigger output	UART0RXTRG			
ch1	UART ch1 transmission completion trigger output	UART1TXTRG	***[TSEL0CR7]*** <INSEL28>	T32A ch1 Timer A	T32A01TRGINAPCK
	UART ch1 reception completion trigger output	UART1RXTRG			
ch2	UART ch2 transmission completion trigger output	UART2TXTRG	***[TSEL0CR7]*** <INSEL31>	T32A ch2 Timer A	T32A02TRGINAPCK
	UART ch2 reception completion trigger output	UART2RXTRG			
ch3	UART ch3 transmission completion trigger output	UART3TXTRG	***[TSEL0CR8]*** <INSEL34>	T32A ch3 Timer A	T32A03TRGINAPCK
	UART ch3 reception completion trigger output	UART3RXTRG			

2.6. Serial Peripheral Interface (TSPI)

2.6.1. Built-in Channel

The following table shows the TSPI built-in channel of each product.
In TMPM4K Group(1), Maximum Communication speed of TSPI is 20 Mbps.

Table 2.30 TSPI Built-in Channel

Product	TSPI channel (✓: Available, - : N/A)			
	ch0	ch1	ch2	ch3
M4K4	✓	✓	✓	✓
M4K2	✓	-	✓	-
M4K1	✓	-	✓	-

2.6.2. Function Pin and Port

The function pins are assigned to the port of the following tables.
Please do not use simultaneously the same function currently assigned to two or more pins.
There is also a channel which does not have functional pins depending on a product.

Table 2.31 TSPI Function Pin and Port

Channel	function pin (signal name)		Port	Products list (✓: Available, - : N/A)		
				M4K4	M4K2	M4K1
ch0	TSPI0SCK	I/O	PK4	✓	✓	✓
	TSPI0TXD	Output	PK3	✓	✓	✓
	TSPI0RXD	Input	PK2	✓	✓	✓
ch1	TSPI1SCK	I/O	PA2	✓	-	-
	TSPI1TXD	Output	PA0	✓	-	-
	TSPI1RXD	Input	PA1	✓	-	-
ch2	TSPI2SCK	I/O	PG2	✓	✓	✓
	TSPI2TXD	Output	PG0	✓	✓	✓
	TSPI2RXD	Input	PG1	✓	✓	✓
ch3	TSPI3SCK	I/O	PC2	✓	-	-
	TSPI3TXD	Output	PC0	✓	-	-
	TSPI3RXD	Input	PC1	✓	-	-

Note: In TMPM4K Group(1), there is no TSPIxCSIN pin, TSPIxCS0 pin, TSPIxCS1 pin, TSPIxCS2 pin and TSPIxCS3 pin.

2.6.3. Transfer Mode of Each Product

The transfer modes which can be used with the product as TSPI is shown in the following tables differ.

Table 2.32 TSPI Mode List

Channel	Support Mode		
	M4K4	M4K2	M4K1
ch0	SIO mode		
ch1	SIO mode	-	-
ch2	SIO mode		
ch3	SIO mode	-	-

2.6.4. *[TSPIxCR2]*<RXDLY> Set Value

TMPM4K Group(1) products setting value of TSPI control register 2 (***[TSPIxCR2]***<RXDLY[2:0]>) is as follows:

Table 2.33 *[TSPIxCR2]*<RXDLY[2:0]> Set Value

Bit	Bit symbol	After reset	Function
18:16	<RXDLY[2:0]>	001	000: fsys ≤ 40MHz 001: fsys > 40MHz

2.6.5. Clock for Prescaler

The TSPI use the clock of the following table as a prescaler clock.

Table 2.34 TSPI Clock for Prescaler

Clock
ΦT0

2.6.6. DMA Request

The following table shows the DMA request in the TSPI.
"-" in the table does not have an applicable function.

Table 2.35 TSPI DMA Request

Channel	Request	Signal name	Trigger selector	DMA request channel		
					Single transfer	Burst transfer
ch0	TSPI ch0 reception	TSPI0RX_DMA	-	0	✓	✓
	TSPI ch0 transmission	TSPI0TX_DMA		1	✓	✓
ch1	TSPI ch1 reception	TSPI1RX_DMA	-	2	✓	✓
	TSPI ch1 transmission	TSPI1TX_DMA		3	✓	✓
ch2	TSPI ch2 reception	TSPI2RX_DMA	-	4	✓	✓
	TSPI ch2 transmission	TSPI2TX_DMA	-	5	✓	✓
ch3	TSPI ch3 reception	TSPI3RX_DMA	-	6	✓	✓
	TSPI ch3 transmission	TSPI3TX_DMA	***[TSEL0CR0]*** <INSEL0>	7	✓	✓

Note: ✓: Available, - : N/A

2.6.7. Internal Signal Connection Specification

2.6.7.1. Trigger Transfer Signal Connection

Transfer function of the TSPI has a trigger signal control.
A trigger control signal is selected with the trigger source and use it as the following table.

Table 2.36 TSPI Trigger Transfer

Channel		Trigger source		
	Signal name	Trigger selector	Input trigger signal	Signal name
ch0	TSPI0TRG (input)	***[TSEL0CR4]*** <INSEL17>	PF0 (TRGIN0)	TRGIN0
			PB1 (TRGIN1)	TRGIN1
			PF2 (TRGIN2)	TRGIN2
			T32A ch5 timer register A1 match trigger	T32A05TRGOUTCMPA1
			T32A ch5 timer register B1 match trigger	T32A05TRGOUTCMPB1
			T32A ch5 timer register C1 match trigger	T32A05TRGOUTCMPC1
ch1	TSPI1TRG (input)	***[TSEL0CR4]*** <INSEL18>	PF0 (TRGIN0)	TRGIN0
			PB1 (TRGIN1)	TRGIN1
			PF2 (TRGIN2)	TRGIN2
			T32A ch5 timer register A1 match trigger	T32A05TRGOUTCMPA1
			T32A ch5 timer register B1 match trigger	T32A05TRGOUTCMPB1
			T32A ch5 timer register C1 match trigger	T32A05TRGOUTCMPC1
ch2	TSPI2TRG (input)	***[TSEL0CR4]*** <INSEL19>	PF0 (TRGIN0)	TRGIN0
			PB1 (TRGIN1)	TRGIN1
			PF2 (TRGIN2)	TRGIN2
			T32A ch5 timer register A1 match trigger	T32A05TRGOUTCMPA1
			T32A ch5 timer register B1 match trigger	T32A05TRGOUTCMPB1
			T32A ch5 timer register C1 match trigger	T32A05TRGOUTCMPC1
ch3	TSPI3TRG (input)	***[TSEL0CR5]*** <INSEL20>	PF0 (TRGIN0)	TRGIN0
			PB1 (TRGIN1)	TRGIN1
			PF2 (TRGIN2)	TRGIN2
			T32A ch5 timer register A1 match trigger	T32A05TRGOUTCMPA1
			T32A ch5 timer register B1 match trigger	T32A05TRGOUTCMPB1
			T32A ch5 timer register C1 match trigger	T32A05TRGOUTCMPC1

Note: ***[TSEL0CR4]***<INSELm>, ***[TSEL0CR5]***<INSELm> is set the trigger source by trigger selector. For the detail of connection, refer to the "2.2. Trigger Selector (TRGSEL)".

2.6.7.2. T32A Connection

In the TSPI, there is a signal connected with the peripheral function inside in addition to this as shown in the following table.

Table 2.37 TSPI Inside Connection (Output)

Channel	Function output		Trigger selector	Output destination	
		Signal name			Signal name
ch0	TSPI ch0 transmission completion	TSPI0TXEND	***[TSEL0CR6]*** <INSEL25>	T32A ch0 Timer A	T32A00TRGINAPCK
	TSPI ch0 reception completion	TSPI0RXEND			
ch1	TSPI ch1 transmission completion	TSPI1TXEND	***[TSEL0CR7]*** <INSEL28>	T32A ch1 Timer A	T32A01TRGINAPCK
	TSPI ch1 reception completion	TSPI1RXEND			
ch2	TSPI ch2 transmission completion	TSPI2TXEND	***[TSEL0CR7]*** <INSEL31>	T32A ch2 Timer A	T32A02TRGINAPCK
	TSPI ch2 reception completion	TSPI2RXEND			
ch3	TSPI ch3 transmission completion	TSPI3TXEND	***[TSEL0CR8]*** <INSEL34>	T32A ch3 Timer A	T32A03TRGINAPCK
	TSPI ch3 reception completion	TSPI3RXEND			

2.7. I²C Interface (I2C)

The I2C and EI2C must be used exclusively.

2.7.1. Built-in Channel

The following table show the I2C built-in channel of each product.
The I²C interface of TMPM4K Group(1) products supports "Standard Mode" and "Fast Mode".

Table 2.38 I2C Built-in Channel

Product	I2C channel (✓: Available, - : N/A)
	ch0
M4K4	✓
M4K2	✓
M4K1	✓

2.7.2. Function Pin and Port

The functional pins are assigned to the port of the following tables.

Table 2.39 I2C Function Pin and Port

Channel	Function pin (signal name)		Port	Product list (✓: Available, - : N/A)		
				M4K4	M4K2	M4K1
ch0	I2C0SCL	I/O	PB1	✓	✓	✓
	I2C0SDA	I/O	PB0	✓	✓	✓

2.7.3. Clock for Prescaler

The I2C use the clock of the following table as a prescaler clock.

Table 2.40 I2C Clock for Prescaler

Clock
fsys

2.7.4. DMA Request

The following table shows the DMA request in the I^2C interface.
"-" in the table does not have an applicable function.

Table 2.41 I2C DMA Request

Channel	Request	Signal name	Trigger selector	DMA request channel		
					Single transfer	Burst transfer
ch0	I2C ch0 reception	I2C0RXDMAREQ	-	16	-	✓
	I2C ch0 transmission	I2C0TXDMAREQ	-	17	-	✓

Note: ✓: Available, - : N/A

2.8. I²C Interface Version A (EI2C)

Use I2C and EI2C exclusively.

2.8.1. Built-in Channel

The following table shows the I²C interface version A built-in channel of each product.
In the TMPM4K Group(1), the I²C interface version A supports Standard mode, Fast mode, and Fast mode plus.

Table 2.42 EI2C Built-in Channel

Product	EI2C channel (✓: Available, - : N/A)
	ch0
M4K4	✓
M4K2	✓
M4K1	✓

2.8.2. Function Pin and Port

The function pins are assigned to the port of the following table.

Table 2.43 EI2C Function Pin and Port

Channel	Function pin		Port	Product list (✓: Available, -: N/A)		
				M4K4	M4K2	M4K1
ch0	EI2C0SCL	I/O	PB1	✓	✓	✓
	EI2C0SDA	I/O	PB0	✓	✓	✓

2.8.3. Base Address

Table 2.44 shows the EI2C base addresses for TMPM4K Group(1).

Note: The EI2C base address is different from that described in the reference manual.

Table 2.44 EI2C Base Address

Function name		Channel / unit	Base address
I²C Interface	EI2C	ch0	0x400A0100

2.8.4. Clock for Prescaler

The I²C interface version A uses the clock of the following table as a prescaler clock.

Table 2.45 EI2C Clock for Prescaler

Clock
fsys

2.8.5. DMA Request

The following table shows the DMA request in the I²C interface version A.

Table 2.46 EI2C DMA Request

Channel	Request	Signal name	Trigger selector	DMA request channel		
					Single transfer	Burst transfer
ch0	EI2C ch0 reception	I2C0ARXDMAREQ	-	16	-	✓
	EI2C ch0 transmission	I2C0ATXDMAREQ	-	17	-	✓

Note: ✓: Available, -: N/A

2.9. 12-bit Analog to Digital Converter (ADC)

2.9.1. Built-in Unit

The following table shows the ADC built-in unit of each product.

Table 2.47 ADC Built-in Unit

Product	ADC unit (✓: Available, - : N/A)	
	Unit A	Unit B
M4K4	✓	✓
M4K2	✓	✓
M4K1	✓	✓

2.9.2. Corresponding Registers

The following table shows the correspondence registers for each unit of TMPM4K Group(1).

Table 2.48 ADC Corresponding Registers for Each Unit

Unit	General purpose start-up factor program register	Conversion result storage register
A	*[ADATSET0] to [ADATSET23]*	*[ADAREG0] to [ADAREG23]*
B	*[ADBTSET0 to [ADBTSET23]*	*[ADBREG0] to [ADBREG23]*

2.9.3. Function Pin and Port

The functional pins are assigned to the port of the following tables.
There is also a channel which does not have functional pins depending on a product.

Table 2.49 ADC Function Pin and Port

Input channel	Function pin (signal name)	Port	Product list (✓: Available, - : N/A)		
			M4K4	M4K2	M4K1
ch0	-	-	-	-	-
ch1	AINA01/AINB01	PE4	✓	-	-
ch2	AINA02/AINB02	PE3	✓	-	-
ch3	AINA03/AINB03	PE2	✓	✓	-
ch4	AINA04/AINB04	PE1	✓	✓	✓
ch5	AINA05/AINB05	PE0	✓	✓	✓
ch6	AINA06/AINB06	PD6	✓	✓	✓
ch7	AINA07/AINB07	PD5	✓	✓	✓
ch8	AINA08/AINB08	PD4	✓	✓	✓
ch9	AINA09/AINB09	PD3	✓	✓	✓
ch10	AINA10/AINB10	PD2	✓	✓	✓
ch11	AINA11/AINB11	PD0	✓	✓	✓
ch12	AINA12/AINB12	PD1	✓	✓	✓
ch13	-	-	-	-	-
ch14	-	-	-	-	-
ch15	-	-	-	-	-
ch16	VREFH	-	✓	✓	✓
ch17	VREFL (Note2)	-	✓	✓	✓
ch18	Reference power (Note3)	-	✓	✓	✓

Note1: For both units A and B, ch16 to ch18 are connected internally for self-check function support.

Note2: The VREFL is connected to AVSS.

Note3: For reference power supply, refer to the electrical characteristics of "TMPM4K Group(1) Data Sheet".

2.9.4. Conversion Clock of ADC

The 12-bit ADC uses the clock of the following table as a conversion clock.

Table 2.50 Conversion Clock of ADC

Clock
ADCLK

2.9.5. Setting Value of Mode Setting Register 2

For the setting value of mode setting register 2 (***[ADxMOD2]***), set the values in the table below.

Table 2.51 Setting Value of ADC Mode Setting Register 2

Register name	Value
[ADxMOD2]<MOD2[31:0]>	0x00000000

2.9.6. Trimming Setting Register Setting Value

For the trimming setting register (***[ADxTRM]***), set the values in the table below.

Table 2.52 Setting Value of Trimming Setting Register

Register name	Conditions	Value
[ADxTRM]<TRM[31:0]>	4.5V ≤ AVDD5 ≤ 5.5V	0x0000E000
	2.7V ≤ AVDD5 < 4.5V	0x00000000

2.9.7. DMA Request

The following table shows the DMA request in the 12-bit ADC.

Table 2.53 ADC DMA Request

Unit	Request	Signal name	Trigger selector	DMA request channel		
					Single transfer	Burst transfer
A	General purpose trigger DMA request	ADATRG_DMAREQ	***[TSEL0CR0]*** <INSEL1>	18	-	✓
	Single conversion DMA request	ADASGL_DMAREQ			-	✓
	Continuous conversion DMA request	ADACNT_DMAREQ			-	✓
B	General purpose trigger DMA request	ADBTRG_DMAREQ	***[TSEL0CR0]*** <INSEL0>	7	-	✓
	Single conversion DMA request	ADBSGL_DMAREQ			-	✓
	Continuous conversion DMA request	ADBCNT_DMAREQ			-	✓

Note: ✓: Available, - : N/A

2.9.8. Internal Signal Connection Specification

Figure 2.2 shows the connections between the 12-bit analog to digital converter and peripheral functions.

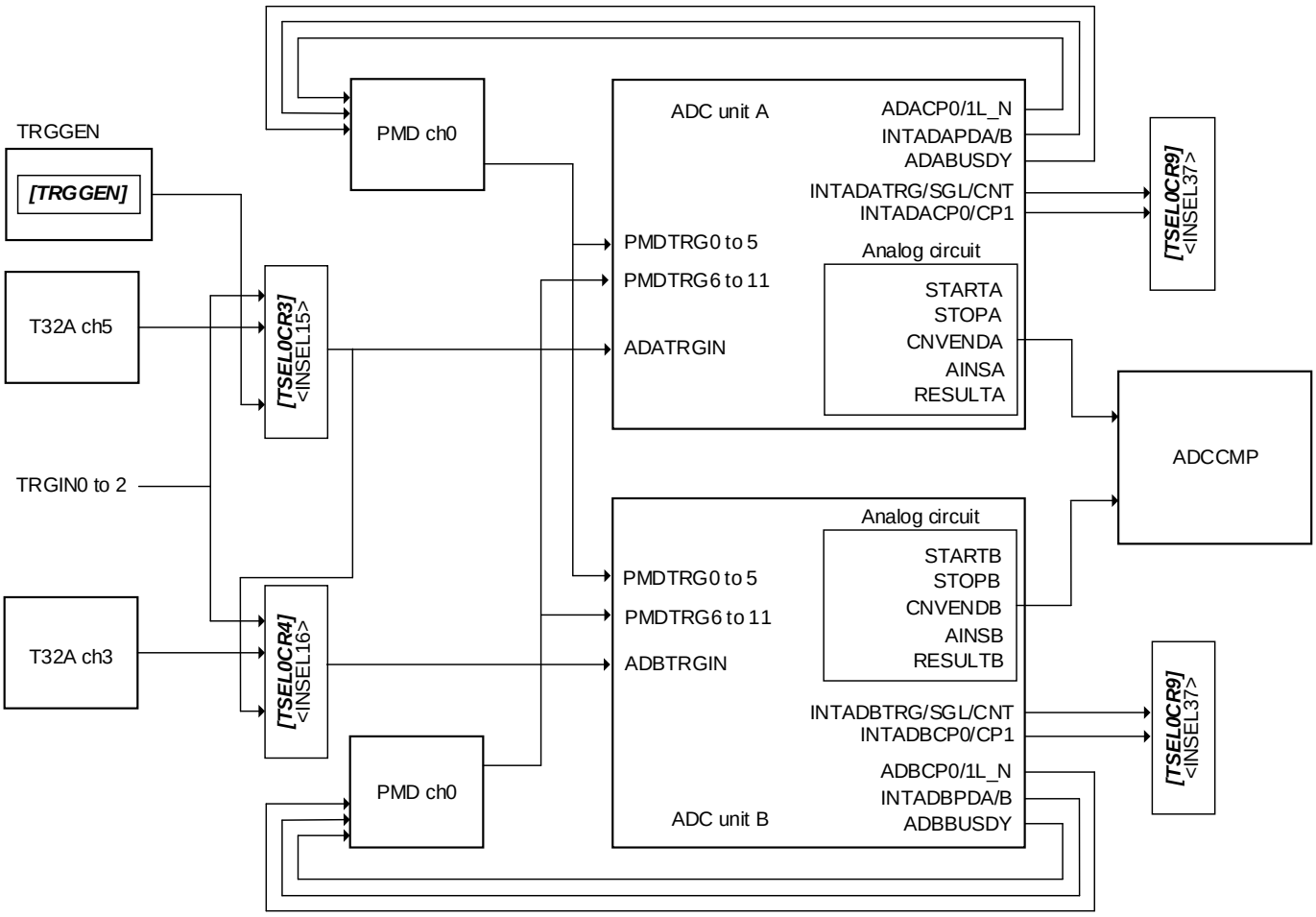

Figure 2.2 Connecting of ADC and Peripheral Functions

2.9.8.1. Startup Trigger Connection Specifications

The 12-bit analog to digital converter can start AD conversion by trigger signals. The trigger signal connections are shown in Table 2.54.

If a register is listed in the Trigger selector column, select the trigger in the listed register. "-" in the table does not have an applicable function.

There are two types of triggers: A-PMD output triggers and general purpose triggers.

General-purpose trigger sources include terminal inputs, timer outputs, and the output of the trigger generation circuit (TRGGEN). TRGGEN is a circuit that controls the trigger signal by register setting. See "2.9.9 Trigger Generation Circuit (TRGGEN)" for details.

When simultaneously startup Unit A and Unit B of the 12-bit analog-to-digital converter with a general-purpose trigger, the general-purpose trigger selection (***[TRGSEL]***<INSEL16>) for Unit B should select the output of the general-purpose trigger selection (***[TRGSEL]***<INSEL15>) for Unit A.

Table 2.54 ADC Startup Trigger Connection Specifications

Unit	Function input		Trigger selector	Input source	
		Signal name			Signal name
A	PMD0 PMD trigger 0	PMDTRG0	-	A-PMD ch0	PMD0TRG0
	PMD0 PMD trigger 1	PMDTRG1	-		PMD0TRG1
	PMD0 PMD trigger 2	PMDTRG2	-		PMD0TRG2
	PMD0 PMD trigger 3	PMDTRG3	-		PMD0TRG3
	PMD0 PMD trigger 4	PMDTRG4	-		PMD0TRG4
	PMD0 PMD trigger 5	PMDTRG5	-		PMD0TRG5
	PMD1 PMD trigger 0	PMDTRG6		A-PMD ch1	PMD1TRG0
	PMD1 PMD trigger 1	PMDTRG7	-		PMD1TRG1
	PMD1 PMD trigger 2	PMDTRG8	-		PMD1TRG2
	PMD1 PMD trigger 3	PMDTRG9	-		PMD1TRG3
	PMD1 PMD trigger 4	PMDTRG10	-		PMD1TRG4
	PMD1 PMD trigger 5	PMDTRG11	-		PMD1TRG5
	General purpose trigger	ADATRGIN	***[TSEL0CR3]*** <INSEL15>	PF0 (TRGIN0)	TRGIN0
				PB1 (TRGIN1)	TRGIN1
				PF2 (TRGIN2)	TRGIN2
				T32A ch5	T32A05TRGOUTCMPA1
					T32A05TRGOUTCMPB1
					T32A05TRGOUTCMPC1
				TRGGEN	TRGGEN
B	PMD0 PMD trigger 0	PMDTRG0	-	A-PMD ch0	PMD0TRG0
	PMD0 PMD trigger 1	PMDTRG1	-		PMD0TRG1
	PMD0 PMD trigger 2	PMDTRG2	-		PMD0TRG2
	PMD0 PMD trigger 3	PMDTRG3	-		PMD0TRG3
	PMD0 PMD trigger 4	PMDTRG4	-		PMD0TRG4
	PMD0 PMD trigger 5	PMDTRG5	-		PMD0TRG5
	PMD1 PMD trigger 0	PMDTRG6		A-PMD ch1	PMD1TRG0
	PMD1 PMD trigger 1	PMDTRG7	-		PMD1TRG1
	PMD1 PMD trigger 2	PMDTRG8	-		PMD1TRG2
	PMD1 PMD trigger 3	PMDTRG9	-		PMD1TRG3
	PMD1 PMD trigger 4	PMDTRG10	-		PMD1TRG4
	PMD1 PMD trigger 5	PMDTRG11	-		PMD1TRG5
	General purpose trigger	ADBTRGIN	***[TSEL0CR4]*** <INSEL16>	PF0 (TRGIN0)	TRGIN0
				PB1 (TRGIN1)	TRGIN1
				PF2 (TRGIN2)	TRGIN2
				T32A ch3	T32A03TRGOUTCMPA1
					T32A03TRGOUTCMPB1
					T32A03TRGOUTCMPC1
				TRGSEL	***[TSEL0CR3]***<INSEL15> output

Note: ***[TSEL0CR3]***<INSEL15> and ***[TSEL0CR4]***<INSEL16> are set the trigger source by trigger selector. For the detail of connection, refer to the "2.2 Trigger Selector (TRGSEL)".

2.9.8.2. Other Connection

The output of the 12-bit analog to digital converter is connected to peripheral functions as shown in Table 2.55.
"-" in the table does not have an applicable function.
For T32A and A-PMD, refer to respective reference manuals.
For ADCCMP, refer to "2.9.10 AD Conversion Result Comparison Circuit (ADCCMP)".

Table 2.55 ADC Inside Connection: Output

Unit	Function output		Trigger selector	Output destination	
		Signal name			Signal name
A	General purpose trigger interrupt	INTADATRG	***[TSEL0CR10]*** <INSEL40>	T32A ch5 Timer A	T32A05TRGINAPCK
	Single conversion interrupt	INTADASGL			
	Continuous conversion interrupt	INTADACNT			
	Monitor function 0 interrupt	INTADACP0			
	Monitor function 1 interrupt	INTADACP1			
	Monitor function 0 output for PMD protect function	ADACP0L_N	-	A-PMD ch0	ADACMP0L_N
	Monitor function 1 output for PMD protect function	ADACP1L_N	-		ADACMP1L_N
	PMD conversion end interrupt A	INTADAPDA	-		INTADAPDA
	PMD conversion end interrupt B	INTADAPDB	-		INTADAPDB
	AD conversion flag	ADABUSY	-		ADABUSY
	Conversion start	STARTA	-	ADCCMP	STARTA
	Forced end	STOPA	-		STOPA
	Conversion end	CNVENDA	-		CNVENDA
	Conversion channel	AINSA	-		AINSA
	Conversion result	RESULTA	-		RESULTA
B	General purpose trigger interrupt	INTADBTRG	***[TSEL0CR9]*** <INSEL37>	T32A ch4 Timer A	T32A04TRGINAPCK
	Single conversion interrupt	INTADBSGL			
	Continuous conversion interrupt	INTADBCNT			
	Monitor function 0 interrupt	INTADBCP0			
	Monitor function 0 output for PMD protect function	ADBCP0L_N	-	A-PMD ch1	ADBCMP0L_N
	Monitor function 1 output for PMD protect function	ADBCP1L_N	-		ADBCMP1L_N
	PMD conversion end interrupt A	INTADBPDA	-		INTADBPDA
	PMD conversion end interrupt B	INTADBPDB	-		INTADBPDB
	AD conversion flag	ADBBUSY	-		ADBBUSY
	Conversion start	STARTB	-	ADCCMP	STARTB
	Forced end	STOPB	-		STOPB
	Conversion end	CNVENDB	-		CNVENDB
	Conversion channel	AINSB	-		AINSB
	Conversion result	RESULTB	-		RESULTB

2.9.9. Trigger Generation Circuit (TRGGEN)

2.9.9.1. Function and Operation

TRGGEN is a circuit that generates a general purpose trigger for 12-bit analog to digital converters.

To generate a general purpose trigger, set ***[TRGGEN]***<GEN> to "1". After the generation of a general purpose trigger, clear ***[TRGGEN]***<GEN> to "0" to enable the next general purpose trigger generation.

2.9.9.2. Registers

The control registers and their addresses are shown as follows:

Peripheral function		Channel/unit	Base address
Trigger generation circuit	TRG	-	0x400FF000

Register name		Address (Base+)
Trigger generation register	***[TRGGEN]***	0x0000

2.9.9.3. *[TRGGEN]* (Trigger generation register)

Bit	Bit symbol	After reset	Type	Function
31:1	-	0	R	Read as “0”.
0	GEN	0	R/W	Generate general purpose trigger for ADC 0: Preparation for generating general purpose trigger 1: Generate general purpose trigger

2.9.10. AD Conversion Result Comparison Circuit (ADCCMP)

2.9.10.1. Outlines

ADCCMP detects that the difference in conversion results is greater than the setting when the same AIN channel is converted simultaneously in ADC unit A and unit B.

2.9.10.2. Configuration

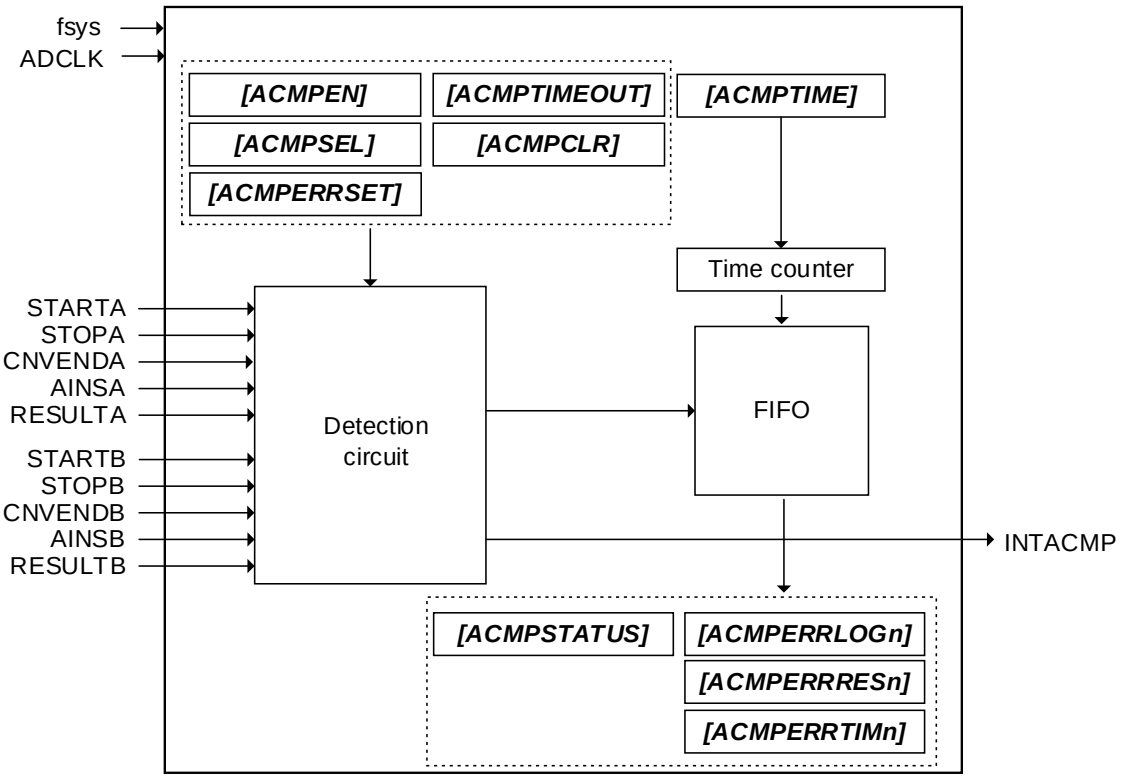

Figure 2.3 ADCCMP Block Diagram

Table 2.56 Signal List

No	Signal name		I/O	Refer to reference manual
1	fsys	System clock	Input	Clock Control and Operation Mode
1	ADCLK	Conversion clock for ADC	Input	Clock Control and Operation Mode
3	STARTA	ADC unit A conversion start	Input	2.9.8. Internal signal connection specification
4	STOPA	ADC unit A conversion stop	Input	2.9.8. Internal signal connection specification
5	CNVENDA	ADC unit A conversion end	Input	2.9.8. Internal signal connection specification
6	AINSA	ADC unit A conversion AIN selection	Input	2.9.8. Internal signal connection specification
7	RESULTA	ADC unit A conversion result	Input	2.9.8. Internal signal connection specification
8	STARTB	ADC unit B conversion start	Input	2.9.8. Internal signal connection specification
9	STOPB	ADC unit B conversion stop	Input	2.9.8. Internal signal connection specification
10	CNVENDB	ADC unit B conversion end	Input	2.9.8. Internal signal connection specification
11	AINSB	ADC unit B conversion AIN selection	Input	2.9.8. Internal signal connection specification
12	RESULTB	ADC unit B conversion result	Input	2.9.8. Internal signal connection specification
13	INTADCCMP	ADCCMP interrupt	output	Exception

2.9.10.3. Function and Operation

2.9.10.3.1. Clock Supply

When using ADCCMP, set an applicable clock enable bit to "1" (clock supply) in Clock supply and stop register B for fsys (***[CGFSYSENB]***). Also, set the conversion clock enable (***[CGSPCLKEN]***<ADCKEN0><ADCKEN1>) of ADC unit A and unit B to "1" (clock supply) simultaneously.

2.9.10.3.2. Detection

ADCCMP detects the following events.

[Group A]
A-1: Different conversion start timings for the two units

[Group B]
B-1: Stop conversion of either unit
B-2: Different conversion end timings for the two units
B-3: No conversion completion for both units within the timeout setting time
B-4: Differences in conversion results that exceed the settings

If the start of conversion differs by more than 2 clocks in ADCLK, A-1 is detected twice.
B-1, B-2, and B-3 in Group B may be detected simultaneously.
Group A and Group B events may be detected simultaneously.

For all events, information on detection is stored in the FIFO.
Any event other than B-1 is an interrupt factor, and the interrupt signal INTADCCMP is output when detected.
Use as described in "2.9.10.3.4 Operation Setting" can prevent A-1, B-2, and B-3 events from occurring.

2.9.10.3.3. Information at Time of Detection

Information at the time of detection is stored in the 8 stage FIFO in order from 0 stage to 7 stage. Each stage of the FIFO is assigned an address, and the data can be read from the registers. There are three registers for reading data from the FIFO: error log register n (***[ACMPERRLOGn]***(n=0 to 7)), error result register n (***[ACMPERRRESn]***(n=0 to 7)), and error time register n (***[ACMPERRTIMn]***(n=0 to 7)).

The FIFO and their corresponding registers are listed in Table 2.57.

Table 2.57 FIFO and their Corresponding Registers

FIFO stage	Register		
0	***[ACMPERRLOG0]***	***[ACMPERRRES0]***	***[ACMPERRTIM0]***
1	***[ACMPERRLOG1]***	***[ACMPERRRES1]***	***[ACMPERRTIM1]***
2	***[ACMPERRLOG2]***	***[ACMPERRRES2]***	***[ACMPERRTIM2]***
:	:	:	:
7	***[ACMPERRLOG7]***	***[ACMPERRRES7]***	***[ACMPERRTIM7]***

The information stored in ***[ACMPERLOGn] [ACMPERRRESn]*** is shown in Table 2.58.

The value of the time counter at the time of detection is stored in ***[ACMPERRTIMn]***. The time counter is a free-running counter that counts in ADCLK.

If the A-1 event is detected twice, the information for the two events is stored in the FIFO.

When multiple events occur simultaneously, the information stored in the FIFO is as follows:

- Simultaneous occurrence of Group B events
  The information of the event with the lowest number among B-1 to B-4 is stored in the FIFO.
- Simultaneous occurrence of Group A and Group B events
  Group B events, followed by Group A events, are stored in the FIFO.
  If the FIFO has one free stage, only the information of Group B is stored.

Table 2.58 Information Stored in FIFO

Event		*[ACMPERRLOGn]*							*[ACMPERRRESn]*	
		<AINA>	<AINB>	<ETYPE>	<ENDA>	<ENDB>	<STARTA>	<STARTB>	<RESULTA>	<RESULTB>
A	1	AINA	AINB	01	0	0	STARTA	STARTB	0x000	0x000
B	1	AINA	AINB	00	0	0	0	0	0x000	0x000
	2	AINA	AINB	10	CONVENDA	CONVENDB	1	1	0x000	0x000
	3	AINA	AINB	11	0	0	1	1	0x000	0x000
	4	AINA	AINB	00	1	1	1	1	RESULTA	RESULTB

The number of information held in the FIFO can be checked in the status register ***[ACMPSTATUS]***<LOGNUM>.
Data in the FIFO can be read by following the steps below; after steps 1-3, the next data can be read.

1. Reads ***[ACMPERRLOGn]*** corresponding to the target FIFO stage.
   At this time, ***[ACMPERRLOGn]***<READFLG> is "0".
2. Wait until ***[ACMPERRLOGn]***<READFLG> becomes "1".
3. When ***[ACMPERRLOGn]***<READFLG> is set to "1", data other than <READFLG> of ***[ACMPERRLOGn]*** read at this time is also valid. Continue reading ***[ACMPERRRESn]*** and ***[ACMPERRTIMn]***.

FIFO is not cleared when read. See "2.9.10.3.6 Clearing FIFO" for details on clearing FIFO.

2.9.10.3.4. Operation Setting

For the AIN channels to be compared, set the conversion clocks, conversion times, and start-up factors of ADC units A and B to the same settings.
Use the PMD trigger or general purpose trigger as the start-up factor so that ADC unit A and unit B start conversion at the same time. When using a general purpose trigger, Unit B should set ***[TSEL0CR4]***<INSEL16> to "110" (trigger selector INSEL15 output) to start conversion with the same general purpose trigger factor as Unit A. Setting ADCCMP is shown as bellows;

1. Set the upper and lower limits of the difference allowed as a result of the conversion of unit B compared to the result of the conversion of unit A in the tolerance setting register (***[ACMPERRSET]***).
2. Set the timeout period to the timeout period setting register (***[ACMPTIMEOUT]***). Set a value larger than the conversion time. The timeout period is counted by ADCLK.
3. Set the AIN channel to be compared to the comparison channel selection register (***[ACMPSEL])***.
4. The time counter register (***[ACMPTIME]***) can be set to any value. Writing to ***[ACMPTIME]*** causes ***[ACMPSTATUS]***<TWRITE> to be set to "1". After <TWRITE> has become "0" indicating that writing is complete, perform the following operations.
5. Setting "1" to the enable register ***[ACMPEN]***<EN> starts the operation.

2.9.10.3.5. Clearing Interrupt

To clear the interrupt, write "1" to ***[ACMPCLR]***<ICLR>**.**
If multiple factors are detected at the same time or if a new interrupt factor is detected during the interrupt clear process, the interrupt is not cleared in a single write. To completely clear the interrupt, repeatedly write "1" until a "0" is read from <ICLR>.

2.9.10.3.6. Clearing FIFO

Clearing of the FIFO is done for data in the 0-stage. Writing "1" to ***[ACMPCLR]***<LCLR> erases the data in the 0-stage and moves the data in stages 1 to 7 to one smaller number. Read <LCR> to confirms the completion of the clearing operation.
To clear all data in the FIFO, repeat the above operation until ***[ACMPSTATUS]***<LOGNUM> is "0".

If a new event is detected during a FIFO clearing operation, the added data may remain in the FIFO. Stopping AD conversion and then performing the operation ensures that all data in the FIFO is cleared.

2.9.10.4. Registers

The control registers and their addresses are shown as follows:

Peripheral function		Channel/unit	Base address
AD Conversion Result Comparison Circuit	ADCCMP	-	0x400BE000

Register name		Address (Base+)
Enable Register	***[ACMPEN]***	0x0000
Tolerance Setting Register	***[ACMPERRSET]***	0x0004
Timeout Period Setting Register	***[ACMPTIMEOUT]***	0x0008
Comparison Channel Selection Register	***[ACMPSEL]***	0x000C
Time Counter Register	***[ACMPTIME]***	0x0010
Clear Register	***[ACMPCLR]***	0x0020
Status Register	***[ACMPSTATUS]***	0x0024
Error Log Register 0	***[ACMPERRLOG0]***	0x0200
Error Results Register 0	***[ACMPERRRES0]***	0x0204
Error Time Register 0	***[ACMPERRTIM0]***	0x0208
Error Log Register 1	***[ACMPERRLOG1]***	0x0210
Error Results Register 1	***[ACMPERRRES1]***	0x0214
Error Time Register 1	***[ACMPERRTIM1]***	0x0218
Error Log Register 2	***[ACMPERRLOG2]***	0x0220
Error Results Register 2	***[ACMPERRRES2]***	0x0224
Error Time Register 2	***[ACMPERRTIM2]***	0x0228
Error Log Register 3	***[ACMPERRLOG3]***	0x0230
Error Results Register 3	***[ACMPERRRES3]***	0x0234
Error Time Register 3	***[ACMPERRTIM3]***	0x0238
Error Log Register 4	***[ACMPERRLOG4]***	0x0240
Error Results Register 4	***[ACMPERRRES4]***	0x0244
Error Time Register 4	***[ACMPERRTIM4]***	0x0248
Error Log Register 5	***[ACMPERRLOG5]***	0x0250
Error Results Register 5	***[ACMPERRRES5]***	0x0254
Error Time Register 5	***[ACMPERRTIM5]***	0x0258
Error Log Register 6	***[ACMPERRLOG6]***	0x0260
Error Results Register 6	***[ACMPERRRES6]***	0x0264
Error Time Register 6	***[ACMPERRTIM6]***	0x0268
Error Log Register 7	***[ACMPERRLOG7]***	0x0270
Error Results Register 7	***[ACMPERRRES7]***	0x0274
Error Time Register 7	***[ACMPERRTIM7]***	0x0278

[ACMPERRSET], ***[ACMPTIMEOUT]*** and ***[ACMPSEL]*** must not be rewritten during operation (***[ACMPEN]*** <EN>="1").

2.9.10.5. *[ACMPEN]* (Enable Register)

Bit	Bit symbol	After reset	Type	Function
31:1	-	0	R	Read as “0”.
0	EN	0	R/W	ADCCMP operation control 0: Disable operation 1: Enable operation

2.9.10.6. *[ACMPERRSET]* (Tolerance Setting Register)

Bit	Bit symbol	After reset	Type	Function
31:28	-	0	R	Read as “0”.
27:16	UERR[11:0]	0x000	R/W	Upper limit of error Sets the maximum error value when the conversion result of ADC unit B is greater than the conversion result of ADC unit A.
15:12	-	0	R	Read as “0”.
11:0	DERR[11:0]	0x000	R/W	Lower limit of error Sets the maximum value of error when the conversion result of ADC unit B is smaller than the conversion result of ADC unit A.

2.9.10.7. *[ACMPTIMEOUT]* (Timeout Period Setting Register)

Bit	Bit symbol	After reset	Type	Function
31:16	-	0	R	Read as “0”.
15:0	TIMEOUT	0x0000	R/W	Timeout period Sets the timeout period time.

2.9.10.8. *[ACMPSEL]* (Comparison Channel Selection Register)

Bit	Bit symbol	After reset	Type	Function
31:19	-	0	R/W	Write as “0”.
18	SEL18	0	R/W	Comparison channel selection 0: No comparison 1: Comparison The bit number corresponds to the input channel number.
17	SEL17	0	R/W	
16	SEL16	0	R/W	
15	SEL15	0	R/W	Write as “0”.
14	SEL14	0	R/W	
13	SEL13	0	R/W	
12	SEL12	0	R/W	Comparison channel selection 0: No comparison 1: Comparison The bit number corresponds to the input channel number.
11	SEL11	0	R/W	
10	SEL10	0	R/W	
9	SEL9	0	R/W	
8	SEL8	0	R/W	
7	SEL7	0	R/W	
6	SEL6	0	R/W	
5	SEL5	0	R/W	
4	SEL4	0	R/W	
3	SEL3	0	R/W	
2	SEL2	0	R/W	
1	SEL1	0	R/W	
0	SEL0	0	R/W	Write as “0”.

2.9.10.9. *[ACMPTIME]* (Time Counter Register)

Bit	Bit symbol	After reset	Type	Function
31:0	TIME	0	R/W	Time counter [Write] Set a value to the counter. [Read] The counter value can be read.

2.9.10.10. *[ACMPCLR]* (Clear Register)

Bit	Bit symbol	After reset	Type	Function
31:9	-	0	R	Read as “0”.
8	ICLR	0	R/W	Clearing Interrupt [Write] 1: Clear interrupt Writing "0" has no meaning. [Read] 0: No interrupt is occurring 1: Interrupt is occurring
7:1	-	0	R	Read as “0”.
0	LCLR	0	R/W	Clearing the 0-stage of the FIFO [Write] 1: Clear the 0-stage of the FIFO Writing "0" has no meaning. [Read] 0: The FIFO clear operation not in progress 1: The FIFO clear operation in progress

2.9.10.11. *[ACMPSTATUS]* (Status Register)

Bit	Bit symbol	After reset	Type	Function
31:9	-	0	R	Read as “0”.
8	TWRITE	0	R	Writing status of the time counter 0: Time counter is not in writing operation 1: Time counter is in writing operation
7:6	-	0	R	Read as “0”.
5:0	LOGNUM	0	R	Number of data in FIFO Indicates the number of data stored in the FIFO.

2.9.10.12. *[ACMPERRLOG0]* (Error Log Register 0)

Example for ***[ACMPERRRLOG0]***. The same configuration applies to ***[ACMPERRLOG1]*** to ***[ACMPERRLOG7]***.

Bit	Bit symbol	After reset	Type	Function
31:29	-	0	R	Read as “0”.
28:24	AINA	00000	R	Indicates the AIN channel of ADC unit A on detection in all events
23:21	-	0	R	Read as “0”.
20:16	AINB	00000	R	Indicates the AIN channel of ADC unit B on detection in all events
15:10	-	0	R	Read as “0”.
9:8	ETYPE	00	R	Detected event 00: Conversion stopped (B-1) or conversion results bigger than setting error (B-4) 01: Different conversion start timings (A-1) 10: Different conversion stop timings (B-2) 11: Timeout (B-3)
7	ENDB	0	R	Conversion end signal status of ADC unit B Indicates the state of the CONVENDB signal on ADC unit B when event B-2 is detected.
6	ENDA	0	R	Conversion end signal status of ADC unit A Indicates the state of the CONVENDA signal on ADC unit A when event B-2 is detected.
5	STARTB	0	R	Conversion start signal status of ADC unit B Indicates the state of the STARTB signal on ADC unit B when event A-1 is detected.
4	STARTA	0	R	Conversion start signal status of ADC unit A Indicates the state of the STARTA signal on ADC unit A when event A-1 is detected.
3:1	-	0	R	Read as “0”.
0	READFLG	0	R	FIFO read flag Reading "1" means that the values in ***[ACMPERRLOG0]***, ***[ACMPERRRES0], [ACMPERRTIM0]*** are valid.

2.9.10.13. *[ACMPERRRES0]* (Error Results Register 0)

Example for ***[ACMPERRRES0]***. The same configuration applies to ***[ACMPERRRES1]*** to ***[ACMPERRRES7]***.

Bit	Bit symbol	After reset	Type	Function
31:28	-	0	R	Read as “0”.
27:16	RESULTA	0x000	R	Conversion result of ADC unit A The conversion result of ADC unit A when event B-4 is detected.
15:12	-	0	R	Read as “0”.
11:0	RESULTB	0x000	R	Conversion result of ADC unit B The conversion result of ADC unit B when event B-4 is detected.

2.9.10.14. *[ACMPERRTIM0]* (Error Time Register 0)

Example for ***[ACMPERRTIM0]***. The same configuration applies to ***[ACMPERRTIM1]*** to ***[ACMPERRTIM7]***.

Bit	Bit symbol	After reset	Type	Function
31:0	ERRTIME	0x00000000	R	Error time Indicates the value of the time counter at the time of all event detections.

2.10. Advanced Programmable Motor Control Circuit (A-PMD)

2.10.1. Built-in Channel

The following table shows the A-PMD built-in channel of each product.

Table 2.59 A-PMD Built-in Channel

Product	A-PMD channel (✓: Available, - : N/A)	
	ch0	ch1
M4K4	✓	✓
M4K2	✓	✓
M4K1	✓	-

2.10.2. Function Pin and Port

The functional pins are assigned to the port of the following tables.

Table 2.60 A-PMD Function Pin

Channel	Function pin		Signal name	Port	Product list (✓: Available, - : N/A)		
					M4K4	M4K2	M4K1
ch0	XO0	Output	XO0	PJ1	✓	✓	✓
	YO0	Output	YO0	PJ3	✓	✓	✓
	ZO0	Output	ZO0	PJ5	✓	✓	✓
	UO0	Output	UO0	PJ0	✓	✓	✓
	VO0	Output	VO0	PJ2	✓	✓	✓
	WO0	Output	WO0	PJ4	✓	✓	✓
	EMG0	Input	EMG0	PD6	✓	✓	✓
				PH2	✓	✓	✓
				PJ6	✓	✓	✓
	OVV0	Input	OVV0	PJ7	✓	-	-
	Debug output	Output	PMD0DBG	PB0	✓	✓	✓
				PG0	✓	✓	✓
				PJ0	✓	✓	✓
ch1	XO1	Output	XO1	PG3	✓	✓	-
	YO1	Output	YO1	PG4	✓	✓	-
	ZO1	Output	ZO1	PG5	✓	✓	-
	UO1	Output	UO1	PG0	✓	✓	-
	VO1	Output	VO1	PG1	✓	✓	-
	WO1	Output	WO1	PG2	✓	✓	-
	EMG1	Input	EMG1	PF0	✓	✓	-
	OVV1	Input	OVV1	-	-	-	-
	Debug output	Output	PMD1DBG	PB1	✓	✓	-
				PG1	✓	✓	-
				PJ1	✓	✓	-

2.10.3. DMA Request

The following table shows the DMA request in the A-PMD.

Table 2.61 A-PMD DMA Request

Channel	Request	Signal name	Trigger selector	DMA request channel		
					Single transfer	Burst transfer
ch0	A-PMD ch0 PWM interrupt	INTPWM0	***[TSEL0CR0]*** <INSEL2>	19	-	✓
ch1	A-PMD ch1 PWM interrupt	INTPWM1	***[TSEL0CR0]*** <INSEL3>	20	-	✓

Note: ✓: Available, - : N/A

2.10.4. Internal Signal Connection Specification

2.10.4.1. Other Connection

In the A-PMD, there is a signal connected with the peripheral function inside in addition to this as shown in the following table.

Table 2.62 A-PMD Inside Connection List: Input (1/2)

Channel	Function input		Input source	
		Signal name		Signal name
ch0	ADC conversion completion interrupt A	INTADAPDA	ADC unit A	INTADAPDA
	ADC conversion completion interrupt B	INTADAPDB		INTADAPDB
	ADC conversion signal	ADABUSY		ADABUSY
	ADC monitor function 0 (OVV detection)	ADACMP0L_N		ADACP0L_N
	ADC monitor function 1 (OVV detection)	ADACMP1L_N		ADACP1L_N
	ADC conversion completion interrupt C	INTADxPDC	-	-
	ADC conversion completion interrupt D	INTADxPDD		
	ADC conversion priority interrupt	INTADxPFLG		
	Commutation trigger (A-ENC32 position detect synchronous)	INTENC00	A-ENC32 ch0	INTENC00
	Commutation trigger (General purpose timer synchronous)	PMD0TMR	T32A ch0	T32A00TRGOUTCMPA0
	Commutation trigger (A-ENC MCMP completion synchronous)	ENC0CTRGO	A-ENC32 ch0	ENC0CTRG0
	VE U-phase PWM duty	VExCMPU	-	-
	VE V-phase PWM duty	VExCMPV		
	VE W-phase PWM duty	VExCMPW		
	VE Trigger comparison 0	VExTRGCMP0		
	VE Trigger comparison 1	VExTRGCMP1		
	VE Trigger output selection	VExTRGSEL		
	VE Conduction control / Output control	VExOUTCR		
	VE EMG release	VExEMGRS		
	VE Task transition signal	VExTASKP		
	VE interrupt	INTVCNx		

Table 2.63 A-PMD Inside Connection List: Input (2/2)

Channel	Function input		Input source	
		Signal name		Signal name
ch1	ADC conversion completion interrupt A	INTADBPDA	ADC unit B	INTADBPDA
	ADC conversion completion interrupt B	INTADBPDB		INTADBPDB
	ADC conversion signal	ADBBUSY		ADBBUSY
	ADC monitor function 0 (OVV detection)	ADBCMP0L_N		ADBCP0L_N
	ADC monitor function 1 (OVV detection)	ADBCMP1L_N		ADBCP1L_N
	ADC conversion completion interrupt C	INTADxPDC	-	-
	ADC conversion completion interrupt D	INTADxPDD		
	ADC conversion priority interrupt	INTADxPFLG		
	Commutation trigger (A-ENC32 position detect synchronous)	INTENC10	A-ENC32 ch1	INTENC10
	Commutation trigger (General purpose timer synchronous)	PMD1TMR	T32A ch2	T32A02TRGOUTCMPA0
	Commutation trigger (A-ENC MCMP completion synchronous)	ENC1CTRGO	A-ENC32 ch1	ENC1CTRG0
	VE U-phase PWM duty	VExCMPU	-	-
	VE V-phase PWM duty	VExCMPV		
	VE W-phase PWM duty	VExCMPW		
	VE Trigger comparison 0	VExTRGCMP0		
	VE Trigger comparison 1	VExTRGCMP1		
	VE Trigger output selection	VExTRGSEL		
	VE Conduction control / Output control	VExOUTCR		
	VE EMG release	VExEMGRS		
	VE Task transition signal	VE0TASKP		
	VE interrupt	INTVCN1		

Table 2.64 A-PMD Inside Connection List: Output

Channel	Function output		Output destination	Signal name
		Signal name		
ch0	ADC synchronous trigger output 0	PMD0TRG0	ADC unit A	PMD0TRG0
			ADC unit B	PMD0TRG0
	ADC synchronous trigger output 1	PMD0TRG1	ADC unit A	PMD0TRG1
			ADC unit B	PMD0TRG1
	ADC synchronous trigger output 2	PMD0TRG2	ADC unit A	PMD0TRG2
			ADC unit B	PMD0TRG2
	ADC synchronous trigger output 3	PMD0TRG3	ADC unit A	PMD0TRG3
			ADC unit B	PMD0TRG3
	ADC synchronous trigger output 4	PMD0TRG4	ADC unit A	PMD0TRG4
			ADC unit B	PMD0TRG4
	ADC synchronous trigger output 5	PMD0TRG5	ADC unit A	PMD0TRG5
			ADC unit B	PMD0TRG5
	PWM signal for the encoder input	PMD0PWMON	A-ENC32 ch0	ENC0PWMON
	PWM interrupt	INTPWM0	-	-
ch1	ADC synchronous trigger output 0	PMD1TRG0	ADC unit A	PMD1TRG0
			ADC unit B	PMD1TRG0
	ADC synchronous trigger output 1	PMD1TRG1	ADC unit A	PMD1TRG1
			ADC unit B	PMD1TRG1
	ADC synchronous trigger output 2	PMD1TRG2	ADC unit A	PMD1TRG2
			ADC unit B	PMD1TRG2
	ADC synchronous trigger output 3	PMD1TRG3	ADC unit A	PMD1TRG3
			ADC unit B	PMD1TRG3
	ADC synchronous trigger output 4	PMD1TRG4	ADC unit A	PMD1TRG4
			ADC unit B	PMD1TRG4
	ADC synchronous trigger output 5	PMD1TRG5	ADC unit A	PMD1TRG5
			ADC unit B	PMD1TRG5
	PWM signal for the encoder input	PMD1PWMON	A-ENC32 ch1	ENC1PWMON
	PWM interrupt	INTPWM1	-	-

2.10.4.2. Inter-channel Synchronous Control Connection

The PMD is synchronously connected between the channels as shown in the table below.

Table 2.65 PMD Inter-channel Synchronous Control Connection

Master			Slave		
Channel	Function (output)	Signal name	Channel	Function (input)	Signal name
ch0	Synchronization output for PWM enable	PMD0SYNCMDENO	ch1	Synchronization input for PWM enable	PMD1SYNCMDENI
	Synchronization output for EMG protection	PMD0SYNCEMGO		Synchronization input for EMG protection	PMD1SYNCEMGI
	Synchronization output for OVV protection	PMD0SYNCOVVO		Synchronization input for OVV protection	PMD1SYNCOVVI

2.11. Advanced Encoder Input Circuit (32-bit) (A-ENC32)

2.11.1. Built-in Channel

The following table shows the A-ENC32 built-in channel of each product.

Table 2.66 A-ENC32 Built-in Channel

Product	A-ENC32 channel (✓: Available, - : N/A)	
	ch0	ch1
M4K4	✓	✓
M4K2	✓	✓
M4K1	✓	✓

2.11.2. Function Pin and Port

The functional pins are assigned to the port of the following tables.

Table 2.67 A-ENC32 Function Pin

Channel	Function		(Signal name)	Port	Product list (✓: Available, - : N/A)		
					M4K4	M4K2	M4K1
ch0	ENC0A	Input	ENC0A	PG0	✓	✓	✓
	ENC0B	Input	ENC0B	PG1	✓	✓	✓
	ENC0Z	Input	ENC0Z	PG2	✓	✓	✓
ch1	ENC1A	Input	ENC1A	PJ5	✓	✓	✓
	ENC1B	Input	ENC1B	PJ4	✓	✓	✓
	ENC1Z	Input	ENC1Z	PJ3	✓	✓	✓

2.11.3. Internal Signal Connection Specification

2.11.3.1. T32A/A-ENC32 Connection

In the A-ENC32, there is a signal connected with the peripheral function inside in addition to this as shown in the following table.

"-" in the table does not have an applicable function.

Table 2.68 A-ENC32 Internal Connection Specification: Input

Channel	Function Input		Input source	
		Signal		Signal name
ch0	General purpose timer output signal	ENC0PSGI	T32A ch0 timer output A	T32A00OUTA
	PWM signal for sampling	ENC0PWMON	A-PMD ch0 PWM signal	PMD0PWMON
Ch1	General purpose timer output signal	ENC1PSGI	T32A ch2 timer output A	T32A02OUTA
	PWM signal for sampling	ENC1PWMON	A-PMD ch1 PWM signal	PMD1PWMON

Table 2.69 A-ENC32 Internal Connection Specification: Output

Channel	Function output		Trigger selector	Output destination	
		Signal			Signal name
ch0	Divided pulse signal	ENC0TIMPLS	***[TSEL0CR8]*** <INSEL37>	T32A ch4 Timer A Capture trigger input	T32A04TRGINAPHCK
	Commutation trigger	ENC0CTRGO	-	A-PMD ch0 commutation trigger (Electrical angle synchronous)	ENC0CTRGO
	Encoder input interrupt 0	INTENC00	-	A-PMD ch0 commutation trigger (ENC position detection synchronous)	INTENC00
ch1	Divided pulse signal	ENC1TIMPLS	***[TSEL0CR7]*** <INSEL28>	T32A ch1 Timer A Capture trigger input	T32A01TRGINAPHCK
	Commutation trigger	ENC1CTRGO	-	A-PMD ch1 commutation trigger (Electrical angle synchronous)	ENC1CTRGO
	Encoder input interrupt 0	INTENC10	-	A-PMD ch1 commutation trigger (ENC position detection synchronous)	INTENC10

2.12. Operational Amplifier (OPAMP)

2.12.1. Built-in Unit

The following table shows the OPAMP built-in unit of each product.

Table 2.70 OPAMP Built-in Unit

Product	OPAMP unit (✓: Available, - : N/A)
	Unit A
M4K4	✓
M4K2	✓
M4K1	✓

2.12.2. Connected Pin

The terminal of the AD converter which can connect OPAMP is as follows.

Table 2.71 OPAMP Connected Pin

OPAMP	ADC pin	Products (✓: Available, - : N/A)		
		M4K4	M4K2	M4K1
AMPA	AINA11/AINB11 AINA12/AINB12	✓	✓	✓

2.12.3. Internal Connection

The internal connection of OPAMP and an AD converter is as follows.

Table 2.72 OPAMP Internal Connection

ADC input pin	OPAMP input pin	OPAMP output pin	OPAMP output to ADC
AINA11/AINB11	AINAM	AMPOUTA	AINA12/AINB12
AINA12/AINB12	AINAP		

2.13. Clock Selective Watchdog Timer (SIWDT)

2.13.1. Built-in Channel

The following table shows the SIWDT built-in channel of each product.

Table 2.73 SIWDT Built-in Channel

Product	SIWDT channel (✓: Available, - : N/A)
M4K4	✓
M4K2	✓
M4K1	✓

2.13.2. Count Clock

The Clock Selective Watchdog Timer can select the clock to count.
The following table shows the selectable clock.

Table 2.74 SIWDT Count Clock

Clock	Signal	Selection
System clock	fsys	Selected by ***[SIWD0MOD]***<WDCLS>
Internal High speed oscillator1 clock	f_{IHOSC1}	
Internal High speed oscillator2 clock	f_{IHOSC2}	

2.13.3. Output Control

To select the Internal High speed oscillator 2 (f_{IHOSC2}), Rewriting of the internal High speed oscillator2 can be forbidden.

Table 2.75 SIWDT Output Control

Output control	Signal name	Remark
Protect signal of Internal High speed oscillator 2 control bit (***[CGOSCCR]***<IHOSC2EN>)	OSCPRO	Setting by ***[SIWD0OSCCR]***<OSCPRO>

2.14. CRC Calculation Circuit (CRC)

The following table shows the CRC built-in channel of each product.

Table 2.76 CRC Built-in Channel

Product	CRC built-in (✓: Available, - : N/A)
M4K4	✓
M4K2	✓
M4K1	✓

2.15. RAM Parity (RAMP)

2.15.1. Built-in Channel

The following table shows the RAMP built-in channel of each product.

Table 2.77 RAMP Built-in Channel

Product	RAMP built-in (✓: Available, - : N/A)
M4K4	✓
M4K2	✓
M4K1	✓

2.15.2. Error Detection Block Area

The following table shows the detection RAM block area of each product.

Table 2.78 RAM Area and Address of RAMP

Register name	RAM area address	Products (✓: Available, - : N/A)		
		M4K4	M4K2	M4K1
[RPARST]<RPARFG2>	0x20002000-0x200047FF	✓	✓	✓
[RPARST]<RPARFG1>	0x20001000-0x20001FFF	✓	✓	✓
[RPARST]<RPARFG0>	0x20000000-0x20000FFF	✓	✓	✓

2.16. Oscillation Frequency Detection Circuit (OFD)

2.16.1. Built-in Channel

The following table shows the OFD built-in channel of each product.

Table 2.79 OFD Built-in Channel

Product	OFD built-in (✓: Available, - : N/A)
M4K4	✓
M4K2	✓
M4K1	✓

2.16.2. Reference Clock

The Oscillation frequency detection circuit operates considering the clock of the following tables as a reference clock.

Table 2.80 OFD Reference Clock

Reference clock	Signal name	Divide value
Internal High speed oscillator 2	f_{IHOSC2}	256

2.16.3. Clock for Detection

The Oscillation frequency detection circuit chooses the clock to monitor from the detection object clock of the following tables.

Table 2.81 OFD Clock for Detection

Clock for detection		Signal name
Input signal	External High speed oscillator clock	f_{EHOSC}
	Selected clock by the ***[CGOSCCR]***<OSCSEL> and ***[CGPLL0SEL]***<PLL0SEL> in CG (Clock control block)	fc

2.17. Debug Interface

2.17.1. Debug Interface List for Each Product

Table 2.82 Debug Interface List

Debug function	Debug pin (Signal name)	Port	support pin list (✓: Available, - : N/A)		
			M4K4	M4K2	M4K1
Serial wire	SWDIO	PK2	✓	✓	✓
	SWCLK	PK3	✓	✓	✓
	SWV	PK1	✓	✓	✓
JTAG	TMS	PK2	✓	✓	✓
	TCK	PK3	✓	✓	✓
	TDO	PK1	✓	✓	✓
	TDI	PK0	✓	✓	✓
	TRST_N	PK4	✓	✓	✓
ETM trace	TRACECLK	PL4	✓	-	-
	TRACEDATA0	PL0	✓	-	-
	TRACEDATA1	PL1	✓	-	-
	TRACEDATA2	PL2	✓	-	-
	TRACEDATA3	PL3	✓	-	-

2.18. Non Break Debug Interface (NBDIF)

2.18.1. Built-in Channel

The following table shows the NBDIF built-in channel of each product.

Table 2.83 NBDIF Built-in Channel

Product	NBDIF built-in (✓: Available, - : N/A)
M4K4	✓
M4K2	-
M4K1	-

2.18.2. NBDIF List for Each Product

Table 2.84 NBDIF Interface List

Debug pin (Signal name)	Port	Pin (✓: Available, - : N/A)		
		M4K4	M4K2	M4K1
NBDSYNC	PK4	✓	-	-
NBDCLK	PL4	✓	-	-
NBDDATA0	PL0	✓	-	-
NBDDATA1	PL1	✓	-	-
NBDDATA2	PL2	✓	-	-
NBDDATA3	PL3	✓	-	-

2.19. Digital Noise Filter (DNF)

2.19.1. Built-in Unit

The following table shows the DNF built-in unit of each product.

Table 2.85 DNF Built-in Unit

Product	DNF built-in (✓: Available, - : N/A)
	Unit A
M4K4	✓
M4K2	✓
M4K1	✓

2.19.2. External Interrupt List for Each Product

The digital noise filter circuit corresponds to the following external interrupt pins.

Table 2.86 External Interrupt and DNF

External interrupt pin (Signal name)	Port	Setting register name	DNF (✓: Available, - : N/A)		
			M4K4	M4K2	M4K1
INT00a	PK0	***[DNFAENCR]***<NFEN0>	✓	✓	✓
INT00b	PF1	***[DNFAENCR]***<NFEN11>	✓	-	-
INT01a	PK1	***[DNFAENCR]***<NFEN1>	✓	✓	✓
INT01b	PF2	***[DNFAENCR***]<NFEN12>	✓	-	-
INT02a	PK2	***[DNFAENCR]***<NFEN2>	✓	✓	✓
INT02b	PB0	***[DNFAENCR]***<NFEN13>	✓	✓	✓
INT03a	PK3	***[DNFAENCR]***<NFEN3>	✓	✓	✓
INT03b	PB1	***[DNFAENCR]***<NFEN14>	✓	✓	✓
INT04	PG0	***[DNFAENCR]***<NFEN4>	✓	✓	✓
INT05	PG1	***[DNFAENCR]***<NFEN5>	✓	✓	✓
INT06	PK4	***[DNFAENCR]***<NFEN6>	✓	✓	✓
INT07a	PA0	***[DNFAENCR***]<NFEN7>	✓	✓	✓
INT07b	PC2	***[DNFAENCR]***<NFEN15>	✓	-	-
INT08	PC0	***[DNFAENCR]***<NFEN8>	✓	✓	✓
INT09	PA1	***[DNFAENCR]***<NFEN9>	✓	✓	-
INT10	PC1	***[DNFAENCR]***<NFEN10>	✓	-	-

2.19.3. Sampling Source Clock

The clock which shows a digital noise filter circuit in the following tables as a sauce clock of a sampling is used.

Table 2.87 DNF Sampling Source Clock

Clock
fc

2.20. Trimming Circuit (TRM)

2.20.1. Built-in Channel

The following table shows the TRM built-in channel of each product.

Table 2.88 TRM Built-in Channel

Product	TRM built-in (✓: Available, - : N/A)
M4K4	✓
M4K2	✓
M4K1	✓

2.20.2. Target Oscillator

The target oscillator of the trimming circuit is the oscillator shown in the following tables.

Table 2.89 TRM Trimming Target Oscillator

Target oscillator	Oscillator
Internal High-speed oscillator 1	IHOSC1

2.21. Voltage Detection Circuit (LVD)

2.21.1. Built-in Channel

The following table shows the LVD built-in channel of each product.

Table 2.90 LVD Built-in Channel

Product	LVD built-in (✓: Available, - : N/A)
M4K4	✓
M4K2	✓
M4K1	✓

2.21.2. Detection Power Supply

A voltage detecting circuit monitors the power supply of the following tables.

Table 2.91 LVD Detection Power Supply

Detection power supply	Power supply name
Digital power source	DVDD5A/DVDD5B/DVDD5C

2.22. Flash Memory

2.22.1. Clock for Programming/Erasing

As for flash memory, the clock of the following tables is used for programming/erasing of the code flash.

Table 2.92 Clock for Programming/Erasing

Clock for programming/erasing
f_{IHOSC1}

2.22.2. Code Flash Block Configuration of Each Product

The code flash memory differs in the block configuration of the memory with the product, as shown in the following table.

Table 2.93 Code Flash of Each Product

Block name		M4K4FYBUG M4K2FYBDUG M4K1FYBUG	M4K4FWBUG M4K2FWBDUG M4K1FWBUG	Block size (KB)
Block0	PG0	✓	✓	4
	PG1	✓	✓	4
	PG2	✓	✓	4
	PG3	✓	✓	4
	PG4	✓	✓	4
	PG5	✓	✓	4
	PG6	✓	✓	4
	PG7	✓	✓	4
Block1		✓	✓	32
Block2		✓	✓	32
Block3		✓	✓	32
Block4		✓	-	32
Block5		✓	-	32
Block6		✓	-	32
Block7		✓	-	32

Note: ✓: Available, -: N/A

2.22.3. Access Control Register *[FCACCR]*<FCLC[2:0]> Setting

The settings of access control register ***[FCACCR]***<FCLC[2:0]> is as follows:
In TMPM4K Group(1), use <FCLC[2:0]> with the value after reset.

Table 2.94 Access Control Register *[FCACCR]*<FCLC[2:0]> Setting

Bit	Bit symbol	After reset	Function
2:0	<FCLC[2:0]>	011	Code flash read clock control

2.22.4. Macro Code at ID-Read

The macro code values for this product are as follows:

Table 2.95 Macro Code at ID-Read

Code	ID[15:0]
Macro code (Code Flash)	0x0421

2.22.5. Single Boot Resource

The peripheral function of the following table is used in single boot.

Table 2.96 Single Boot Resource

Peripheral function	Channel	Function	Pin name
BOOT	-	-	PJ6 (BOOT_N)
UART	ch0	RXD	PK0 (UT0RXD)
		TXD	PK1 (UT0TXDA)
T32A	ch0	-	-

3. Revision History

Table 3.1 Revision History

Revision	Date	Description
1.0	2024-07-22	- First release

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