

TC74HC390AP, TC74HC390AF

Dual Decade Counter

The TC74HC390A is a high speed CMOS DUAL DECADE COUNTER fabricated with silicon gate C²MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

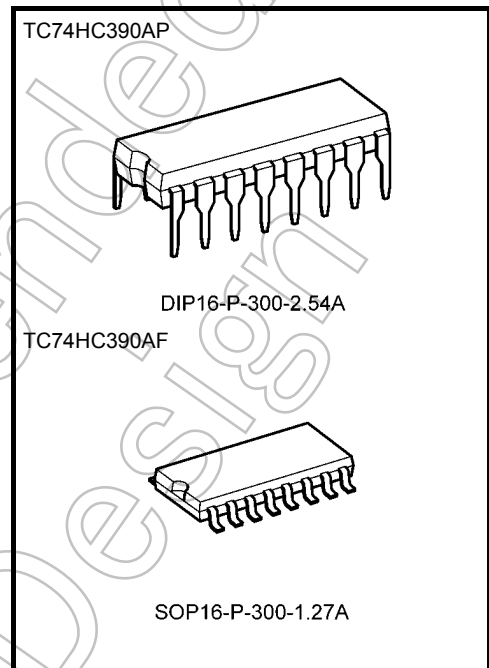
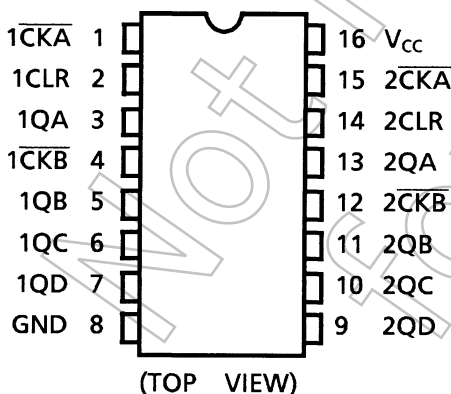
It consists of two independent 4-bit counters, each composed of a divide-by-two and a divide-by-five counter. The divide-by-two counter is incremented on the negative going transition of clock A (\overline{CKA}). The divided-by-five counter is incremented on the negative going transition of clock B (\overline{CKB}). The counter can be cascaded to form decade, bi-quinary, or various combinations up to a divide-by-100 counter. When the CLR input is set high, the Q outputs are set to low independent of the clock inputs.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

Features

- High speed: $f_{max} = 84$ MHz (typ.) at $V_{CC} = 5$ V
- Low power dissipation: $I_{CC} = 4$ μ A (max) at $T_a = 25^\circ$ C
- High noise immunity: $V_{NIH} = V_{NIL} = 28\%$ V_{CC} (min)
- Output drive capability: 10 LSTTL loads
- Symmetrical output impedance: $|I_{OH}| = I_{OL} \cong 4$ mA (min)
- Balanced propagation delays: $t_{pLH} \cong t_{pHL}$
- Wide operating voltage range: $V_{CC} (opr) = 2$ to 6 V
- Pin and function compatible with 74LS390

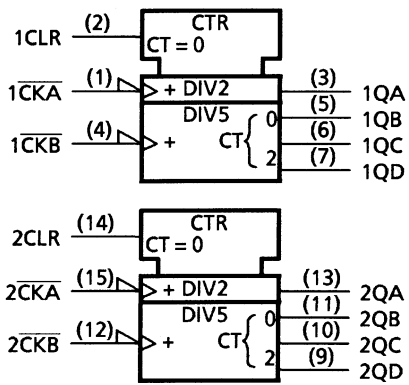
Pin Assignment



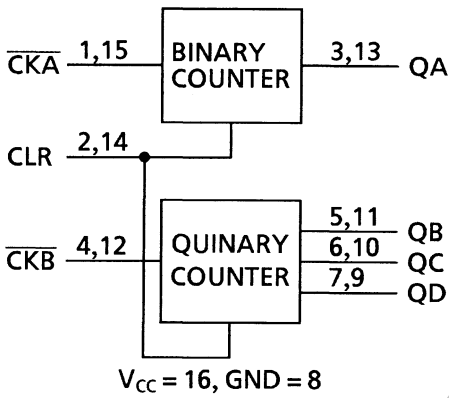
Weight	
DIP16-P-300-2.54A	: 1.00 g (typ.)
SOP16-P-300-1.27A	: 0.18 g (typ.)

Start of commercial production
1986-11

IEC Logic Symbol



Block Diagram

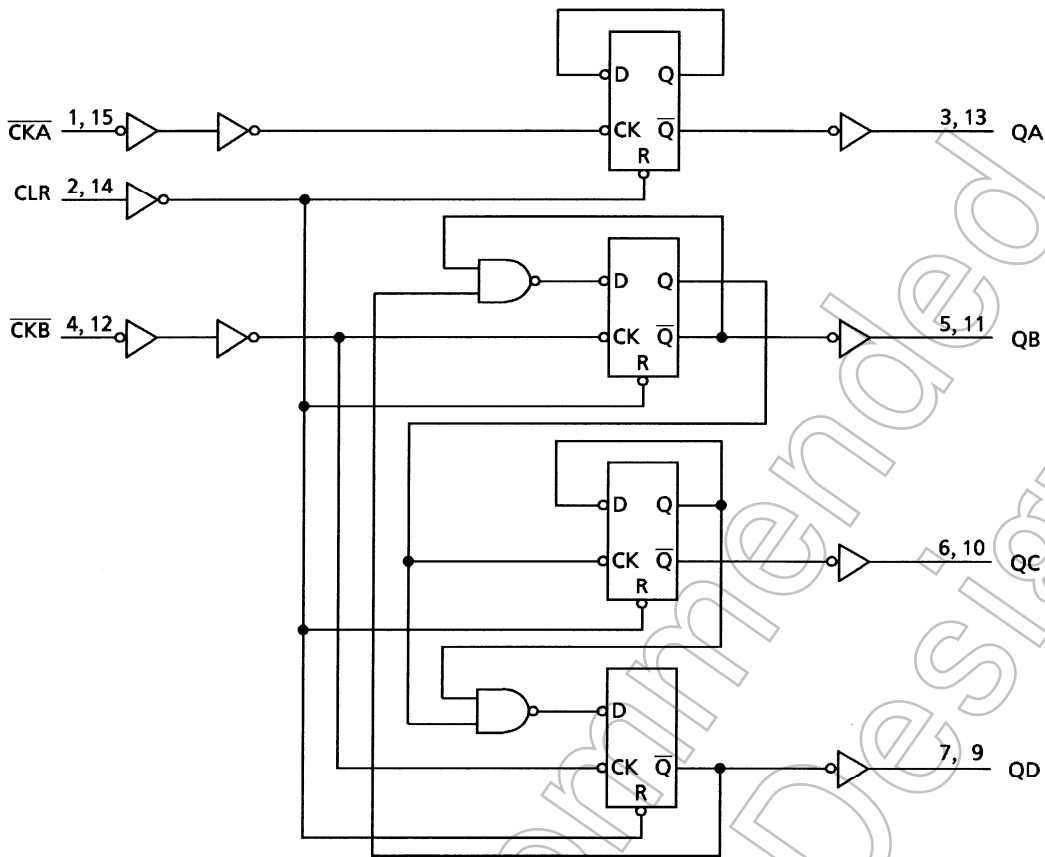


Truth Table

Inputs			Outputs			
\overline{CKA}	\overline{CKB}	CLR	QA	QB	QC	QD
X	X	H	L	L	L	L
\downarrow	X	L	Binary Count Up			
X	\downarrow	L	Quinary Count Up			

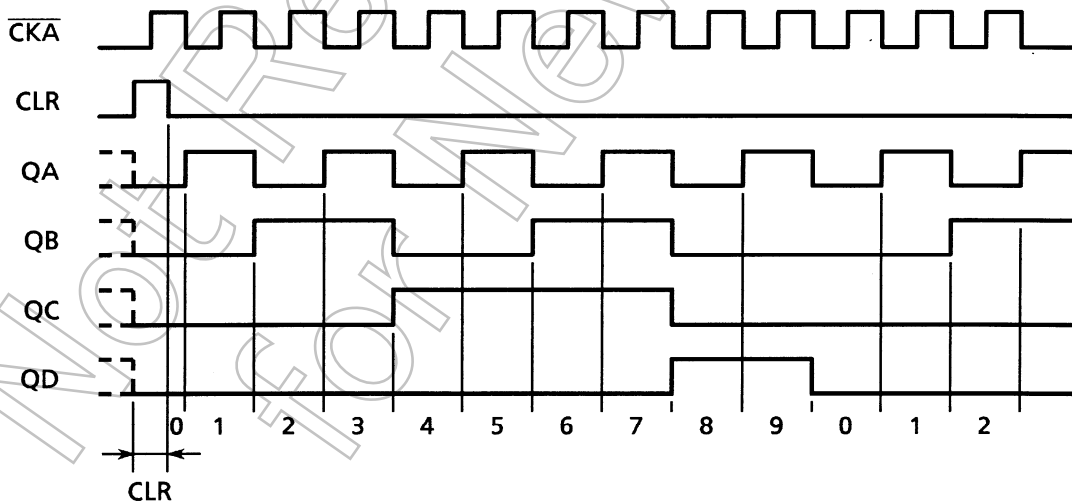
X: Don't care

System Diagram (1/2 package)



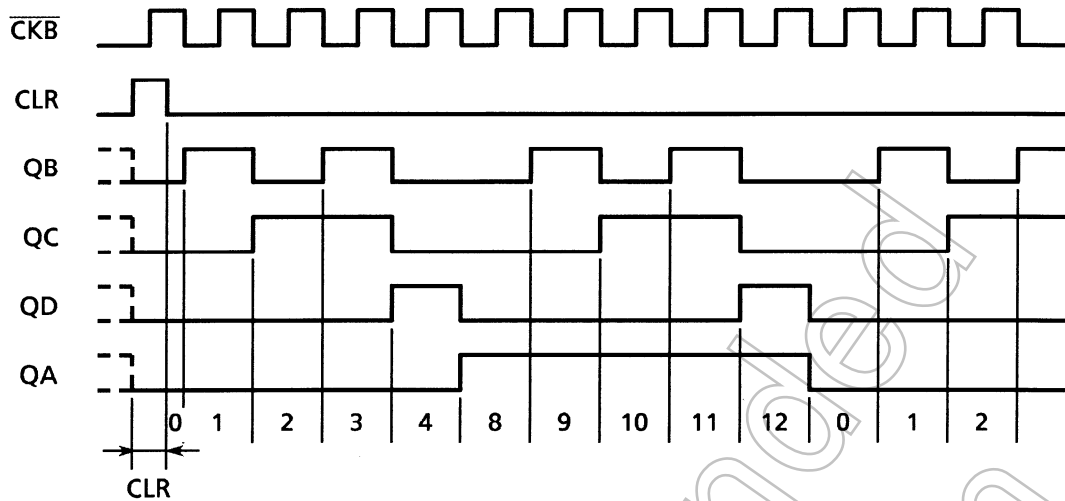
Timing Chart

(1) BCD count sequence (Note)



Note: QA connected to \overline{CKB}

(2) BI-quinary count sequence (Note)



Note: QD connected to \overline{CKA}

Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	-0.5 to 7	V
DC input voltage	V_{IN}	-0.5 to $V_{CC} + 0.5$	V
DC output voltage	V_{OUT}	-0.5 to $V_{CC} + 0.5$	V
Input diode current	I_{IK}	± 20	mA
Output diode current	I_{OK}	± 20	mA
DC output current	I_{OUT}	± 25	mA
DC V_{CC} /ground current	I_{CC}	± 50	mA
Power dissipation	P_D	500 (DIP) (Note 2)/180 (SOP)	mW
Storage temperature	T_{stg}	-65 to 150	$^{\circ}C$

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction. Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: 500 mW in the range of $T_a = -40$ to $65^{\circ}C$. From $T_a = 65$ to $85^{\circ}C$ a derating factor of -10 mW/ $^{\circ}C$ shall be applied until 300 mW.

Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	2 to 6	V
Input voltage	V_{IN}	0 to V_{CC}	V
Output voltage	V_{OUT}	0 to V_{CC}	V
Operating temperature	T_{opr}	-40 to 85	$^{\circ}C$
Input rise and fall time	t_r, t_f	0 to 1000 ($V_{CC} = 2.0$ V) 0 to 500 ($V_{CC} = 4.5$ V) 0 to 400 ($V_{CC} = 6.0$ V)	ns

Note: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either V_{CC} or GND.

Electrical Characteristics

DC Characteristics

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = -40 to 85°C		Unit	
				V _{CC} (V)	Min	Typ.	Max	Min		Max
High-level input voltage	V _{IH}	—		2.0	1.50	—	—	1.50	—	V
				4.5	3.15	—	—	3.15	—	
				6.0	4.20	—	—	4.20	—	
Low-level input voltage	V _{IL}	—		2.0	—	—	0.50	—	0.50	V
				4.5	—	—	1.35	—	1.35	
				6.0	—	—	1.80	—	1.80	
High-level output voltage	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -20 μA	2.0	1.9	2.0	—	1.9	—	V
				4.5	4.4	4.5	—	4.4	—	
			I _{OH} = -4 mA I _{OH} = -5.2 mA	4.5	4.18	4.31	—	4.13	—	
				6.0	5.68	5.80	—	5.63	—	
Low-level output voltage	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 20 μA	2.0	—	0.0	0.1	—	0.1	V
				4.5	—	0.0	0.1	—	0.1	
			I _{OL} = 4 mA I _{OL} = 5.2 mA	4.5	—	0.17	0.26	—	0.33	
				6.0	—	0.18	0.26	—	0.33	
Input leakage current	I _{IN}	V _{IN} = V _{CC} or GND		6.0	—	—	±0.1	—	±1.0	μA
Quiescent supply current	I _{CC}	V _{IN} = V _{CC} or GND		6.0	—	—	4.0	—	40.0	μA

Timing Requirements (input: t_r = t_f = 6 ns)

Characteristics	Symbol	Test Condition		Ta = 25°C		Ta = -40 to 85°C	Unit	
				V _{CC} (V)	Typ.	Limit		Limit
Minimum pulse width (\overline{CK})	t _W (H) t _W (L)	—		2.0	—	75	95	ns
				4.5	—	15	19	
				6.0	—	13	16	
Minimum pulse width (CLR)	t _W (H)	—		2.0	—	75	95	ns
				4.5	—	15	19	
				6.0	—	13	16	
Minimum removal time	t _{rem}	—		2.0	—	25	30	ns
				4.5	—	5	6	
				6.0	—	5	5	
Clock frequency (\overline{CKA})	f	—		2.0	—	6	5	MHz
				4.5	—	32	26	
				6.0	—	38	31	
Clock frequency (\overline{CKB})	f	—		2.0	—	6	5	MHz
				4.5	—	31	25	
				6.0	—	36	29	

AC Characteristics ($C_L = 15\text{ pF}$, $V_{CC} = 5\text{ V}$, $T_a = 25^\circ\text{C}$ input: $t_r = t_f = 6\text{ ns}$)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Output transition time	t_{TLH} t_{THL}	—	—	4	8	ns
Propagation delay time (\overline{CKA} -QA)	t_{pLH} t_{pHL}	—	—	10	20	ns
Propagation delay time (\overline{CKA} -QC)	t_{pLH} t_{pHL}	QA connected to \overline{CKB}	—	29	51	ns
Propagation delay time (\overline{CKB} -QB, QD)	t_{pLH} t_{pHL}	—	—	12	22	ns
Propagation delay time (\overline{CKB} -QC)	t_{pLH} t_{pHL}	—	—	17	32	ns
Propagation delay time (CLR-Qn)	t_{pHL}	—	—	12	26	ns
Maximum clock frequency (\overline{CKA})	f_{max}	—	35	84	—	MHz
Maximum clock frequency (\overline{CKB})	f_{max}	—	33	65	—	MHz

Not Recommended for New Designs

AC Characteristics (C_L = 50 pF, input: t_r = t_f = 6 ns)

Characteristics	Symbol	Test Condition	V _{CC} (V)	Ta = 25°C			Ta = -40 to 85°C		Unit
				Min	Typ.	Max	Min	Max	
Output transition time	t _{TLH} t _{THL}	—	2.0	—	30	75	—	95	ns
			4.5	—	8	15	—	19	
			6.0	—	7	13	—	16	
Propagation delay time (\overline{CKA} -QA)	t _{pLH} t _{pHL}	—	2.0	—	39	120	—	150	ns
			4.5	—	13	24	—	30	
			6.0	—	11	20	—	26	
Propagation delay time (\overline{CKA} -QC)	t _{pLH} t _{pHL}	QA connected to \overline{CKB}	2.0	—	102	290	—	365	ns
			4.5	—	34	58	—	73	
			6.0	—	29	49	—	62	
Propagation delay time (\overline{CKB} -QB, QD)	t _{pLH} t _{pHL}	—	2.0	—	45	130	—	165	ns
			4.5	—	15	26	—	33	
			6.0	—	13	22	—	28	
Propagation delay time (\overline{CKB} -QC)	t _{pLH} t _{pHL}	—	2.0	—	63	185	—	230	ns
			4.5	—	21	37	—	46	
			6.0	—	18	31	—	39	
Propagation delay time (CLR-Qn)	t _{pHL}	—	2.0	—	45	150	—	190	ns
			4.5	—	15	30	—	38	
			6.0	—	13	26	—	32	
Maximum clock frequency (\overline{CKA})	f _{max}	—	2.0	6	20	—	5	—	MHz
			4.5	32	77	—	26	—	
			6.0	38	90	—	31	—	
Maximum clock frequency (\overline{CKB})	f _{max}	—	2.0	6	15	—	5	—	MHz
			4.5	32	60	—	25	—	
			6.0	36	70	—	29	—	
Input capacitance	C _{IN}	—	—	5	10	—	10	pF	
Power dissipation capacitance	C _{PD} (Note)	—	—	44	—	—	—	pF	

Note: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

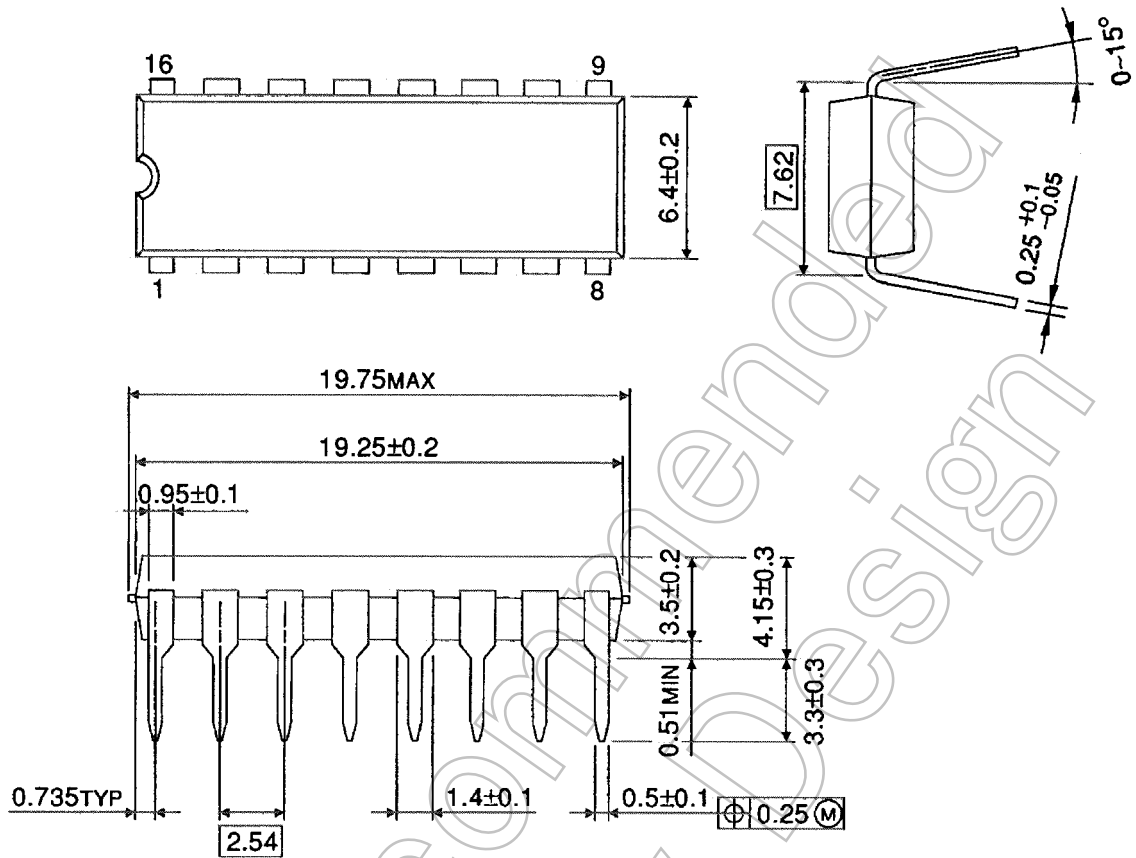
Average operating current can be obtained by the equation:

$$I_{CC}(\text{opr}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2 \text{ (per counter)}$$

Package Dimensions

DIP16-P-300-2.54A

Unit : mm



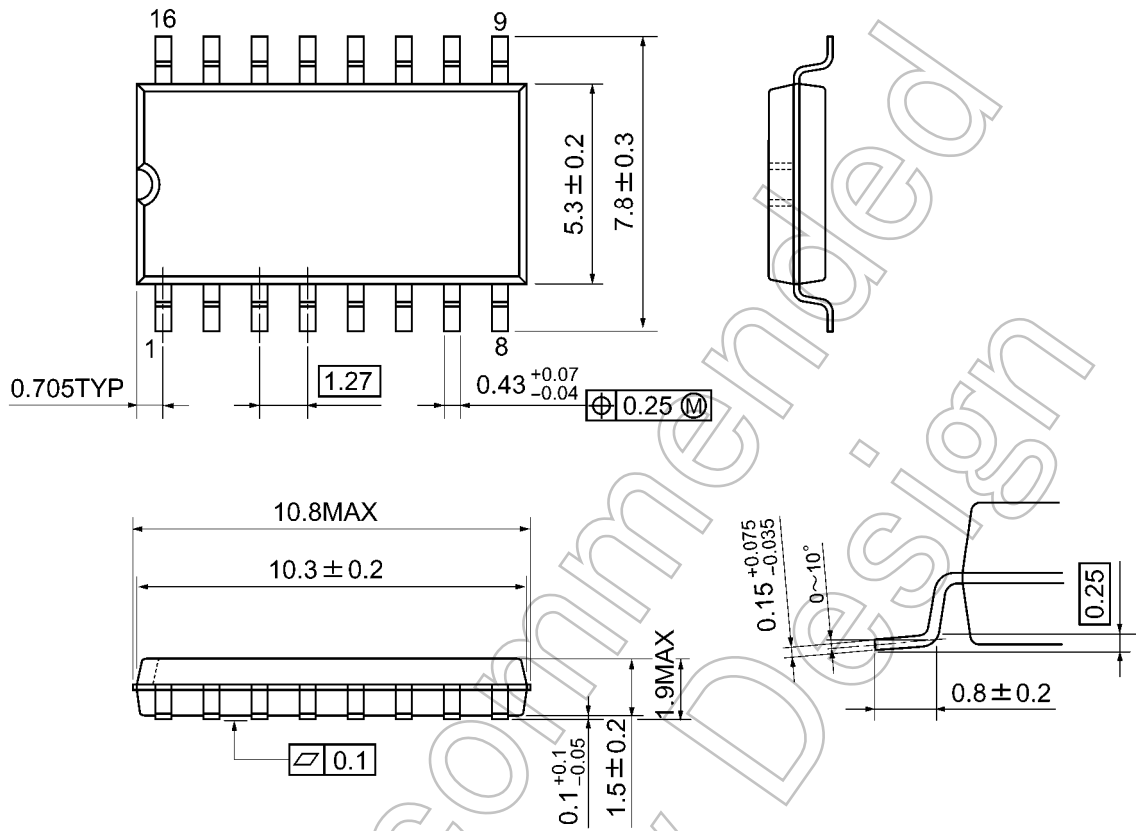
Weight: 1.00 g (typ.)

Not Recommended for New Design

Package Dimensions

SOP16-P-300-1.27A

Unit: mm



Weight: 0.18 g (typ.)

Not Recommended for New Design

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