CMOS Digital Integrated Circuit Silicon Monolithic

TMPM471F10FG

LQFP100 14x14mm, 0.5mm pitch

General Description

- Arm® Cortex®-M4 processor with FPU
  Operating frequency: 1 to 160 MHz, Operating voltage: 4.5 to 5.5 V
- Code flash: 1MB
- Package: 100 pin

Applications

Motors, major appliances using motors, and industrial equipment.

Features

- Arm Cortex-M4 processor with FPU
  - Operating frequency: 1 to 160 MHz
  - Memory Protection Unit (MPU)
- Low-power consumption mode
  - Operating voltage: 4.5 to 5.5 V
  - Low-power consumption operation: IDLE, STOP1
- Operating temperature: -40 to + 85°C
- Internal memory
  - Code flash: 1MB, rewritable up to 100,000 times
  - A code flash area is rewritable in parallel with instruction execution on another code area
  - RAM: 64KB, with parity
- Clock
  - External high-speed oscillator: 6 to 24 MHz(Ceramic, Crystal)
  - External high-speed clock input: 6 to 10 MHz
  - Internal high-speed oscillator (IHOSC1): 10 MHz, user trimming function
  - PLL: 160 MHz output(System clock)
- Oscillation frequency detection (OFD): Abnormal system clock detection
- Voltage Detection (LVD): 4 level, Generate interrupts and reset outputs
- Interruption
  - External factors: 16
    (External pinsfactors: 16 pins, with DNF)
  - Internal factors: 80
- I/O ports: 81 (Input: 2)
  - open-drain, pull-up/-down
- On-chip debug (JTAG/SW)
- Trigger Selector (TRGSEL)
  - Expand Trigger request for DMAC, Timer, others
- DMA controller (DMAC): 1 unit
  - Channel: 30 channels, internal/external triggers
- CRC Calculation Circuit (CRC): CRC32, CRC16
- Asynchronous Serial Interface (UART): 5 channels
  - 5Mbps (Max), FIFO (Transmission 8-stage, Reception 8-stage)
- Serial Peripheral Interface (TSPI): 4 channels
  - SIO/SPI mode, 20MHz (MAX), FIFO (Transmitter: 16bitx8, Receive: 16bitx8)
- I^2C Interface Version A (EI2C): 2 channels
  - Multi master, support 10bit slave addressing
- 12-bit Analog to Digital Converter (ADC): 23 inputs in 2 units
  - Conversion time: 0.6 μs (Fastest)
  - Self-diagnosis support function
- Advanced programmable motor control circuit (A-PMD): 2 channels
  - 3-phase complementary PWM output, Synchronized with ADC
  - PFC control: support 3-phase interleaved PFC
  - Emergency stop function by external inputs (EMG pin, OVV pin)
- Advanced Encoder input circuit (32-bit) (A-ENC32): 2 channels
  - Encoder/sensor (3 types)/Timer /Phase counter mode

Start of commercial production
2024-09

- 32-bit Timer Event Counter (T32A)
  - 5 channels as 32-bit Timers, 10 channels as 16-bit Timers
  - Interval Timer, event counter, input capture, phase difference input, PPG output, Sync Start, Trigger start
- Watchdog timer (SIWDT): 1 channel
  - Clock system other than the system clock can be selected
  - Clear window, interrupts and reset output

Products Lists Categorized by Functions

Table.1.1 Products Lists

Built-in Functions		TMPM471F10FG
Memory	Code Flash (KB)	1024
	RAM (KB)	64
I/O port	PORT (pin)	81
External interrupt	Factor	16
	Pin	16
DMA	DMAC (ch)	30
Timer function	T32A (ch)	5
Serial communication function	UART (ch)	5
	EI2C (ch)	2
	TSPI (ch)	4
Analog function	12-bit ADC Unit A/B (AIN ch)	12/11
Motor control peripherals	A-PMD (ch)	2
	A-ENC32 (ch)	2
Other peripherals	CRC	1
	RAMP (ch)	2
System function	LVD	1
	WDT (ch)	1
	OFD	1
	POR	1
Debug interface	Debug	JTAG/SW TRACE (4bit)
Package	Package type	LQFP100 (14 mm x 14 mm, 0.5 mm pitch)

Contents

List of Figures

List of Tables

Preface

Conventions

- Numeric formats follow the rules as shown below:
  Hexadecimal: 0xABC
  Decimal: 123 or 0d123 - Only when it needs to be explicitly shown that they are decimal numbers.
  Binary: 0b111 - It is possible to omit the "0b" when the number of bits can be distinctly understood from a sentence.
- "_N" is added to the end of signal names to indicate low active signals.
- It is called "assert" that a signal moves to its active level, "deassert" to its inactive level.
- When two or more signal names are referred, they are described like as [m:n].
  Example: S[3:0] shows four signal names S3, S2, S1 and S0 together.
- The characters surrounded by ***[ ]*** defines the register.
  Example: ***[ABCD]***
- "N" substitutes suffix number of two or more same kind of registers, fields, and bit names.
  Example: ***[XYZ1]***, ***[XYZ2]***, ***[XYZ3]*** → ***[XYZn]***
- "x" substitutes suffix number or character of units and channels in the register list.
- In case of unit, "x" means A, B, and C, ...
  Example: ***[ADACR0]***, ***[ADBCR0]***, ***[ADCCR0]*** → ***[ADxCR0]***
- In case of channel, "x" means 0, 1, and 2, ...
  Example: ***[T32A0RUNA]***, ***[T32A1RUNA]***, ***[T32A2RUNA]*** → ***[T32AxRUNA]***
- The bit range of a register is written like as [m: n].
  Example: Bit[3: 0] expresses the range of bit 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.
  Example: ***[ABCD]***<EFG> = 0x01 (hexadecimal), ***[XYZn]***<VW> = 1 (binary)
- Word and byte represent the following bit length.
  Byte: 8 bits
  Half word: 16 bits
  Word: 32 bits
  Double word: 64 bits
- Properties of each bit in a register are expressed as follows:
  R: Read only
  W: Write only
  R/W: Read and write are possible.
- Unless otherwise specified, register access supports only word access.
- The register defined as "Reserved" must not be rewritten. Moreover, do not use the read value.
- The value read from the bit having default value of "-" is unknown.
- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value, In the cases that default is "-", follow the definition of each register.
- Reserved bits of the write-only register should be written with their default value. In the cases that default is "-", follow the definition of each register.
- Do not use read-modified-write processing to the register of a definition which is different by writing and read out.

Terms and Abbreviations

Some of abbreviations used in this document are as follows:

ADC	Analog to Digital Converter
A-ENC32	Advanced Encoder Input Circuit (32-bit)
A-PMD	Advanced Programmable Motor Control Circuit
CRC	Cyclic Redundancy Check
DMAC	Direct Memory Access Controller
DNF	Digital Noise Filter
EHOSC	External High-speed Oscillator
EI2C	I^2C Interface Version A
IHOSC	Internal High-speed Oscillator
INT	Interrupt
I^2C	Inter-Integrated Circuit
LVD	Voltage Detection Circuit
NMI	Non-Maskable Interrupt
OFD	Oscillation Frequency Detector
POR	Power On Reset Circuit
RAMP	RAM Parity
SIWDT	Clock Selective Watchdog Timer
TRGSEL	Trigger Selection Circuit
TRM	Trimming Circuit
TSPI	Serial Peripheral Interface
T32A	32-bit Timer Event Counter
UART	Asynchronous Serial Communication Circuit

1. Block Diagram

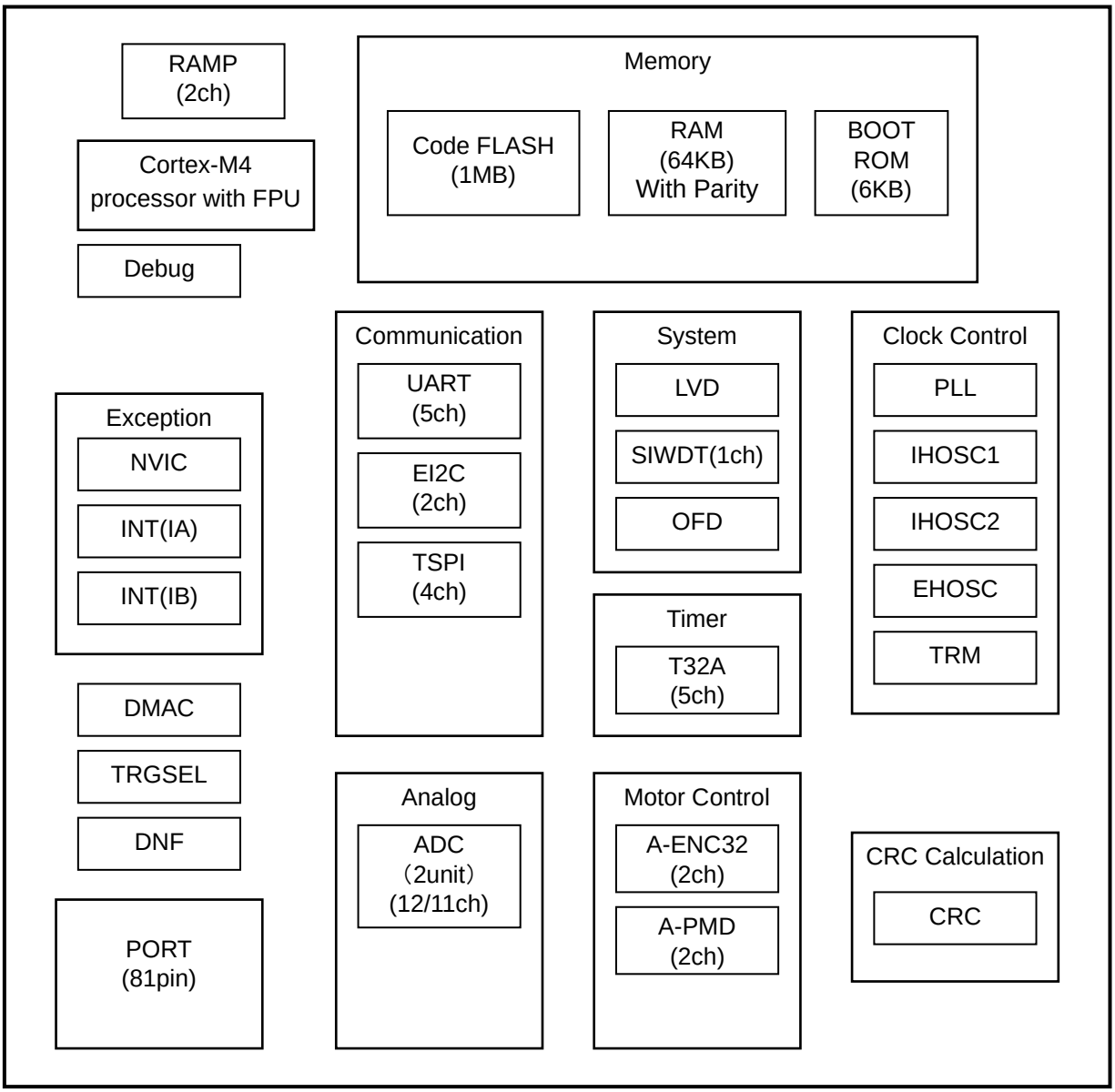
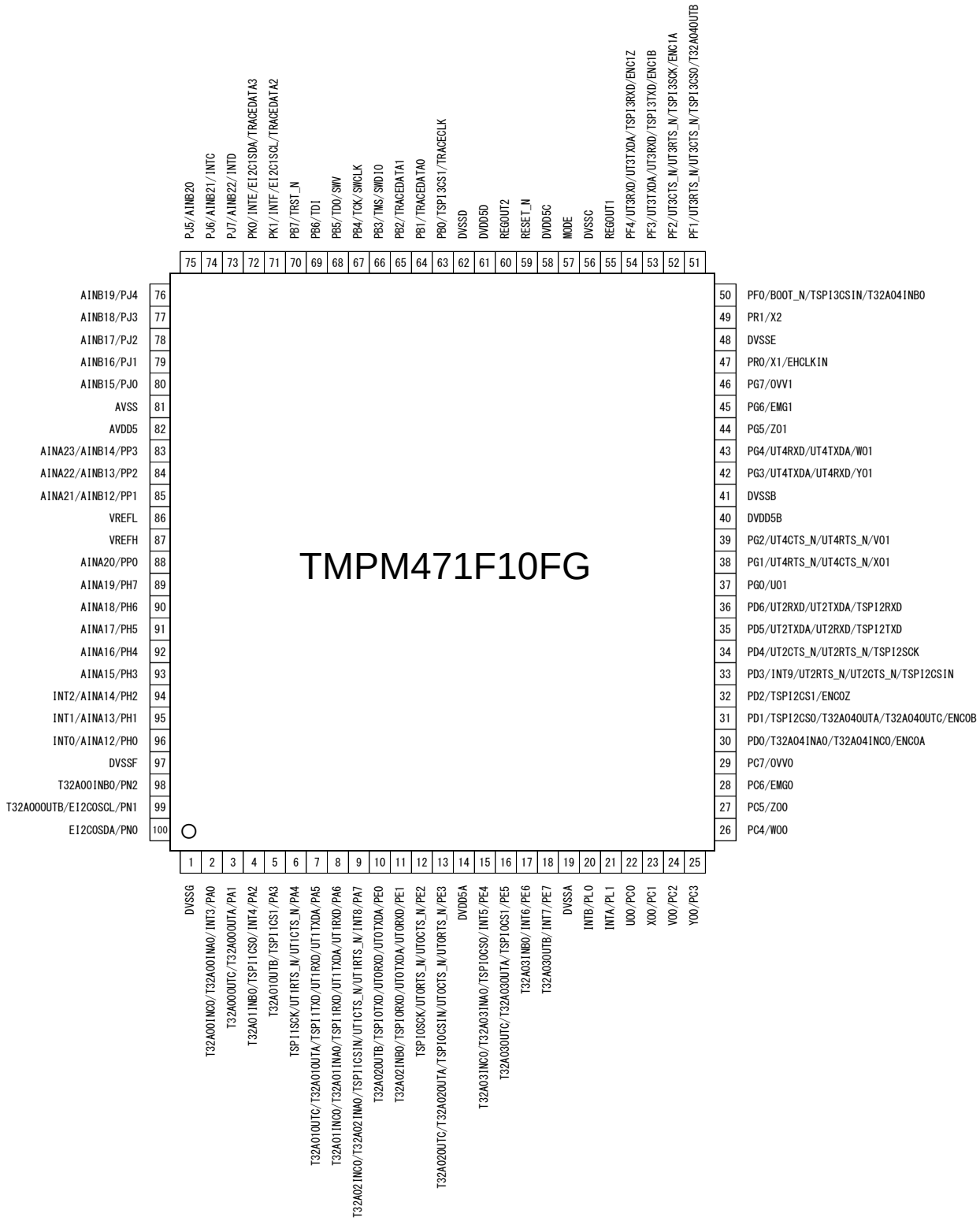


Figure 1.1 Block Diagram of TMPM471F10FG

2. Pin Assignment

2.1. LQFP100



3. Memory Map

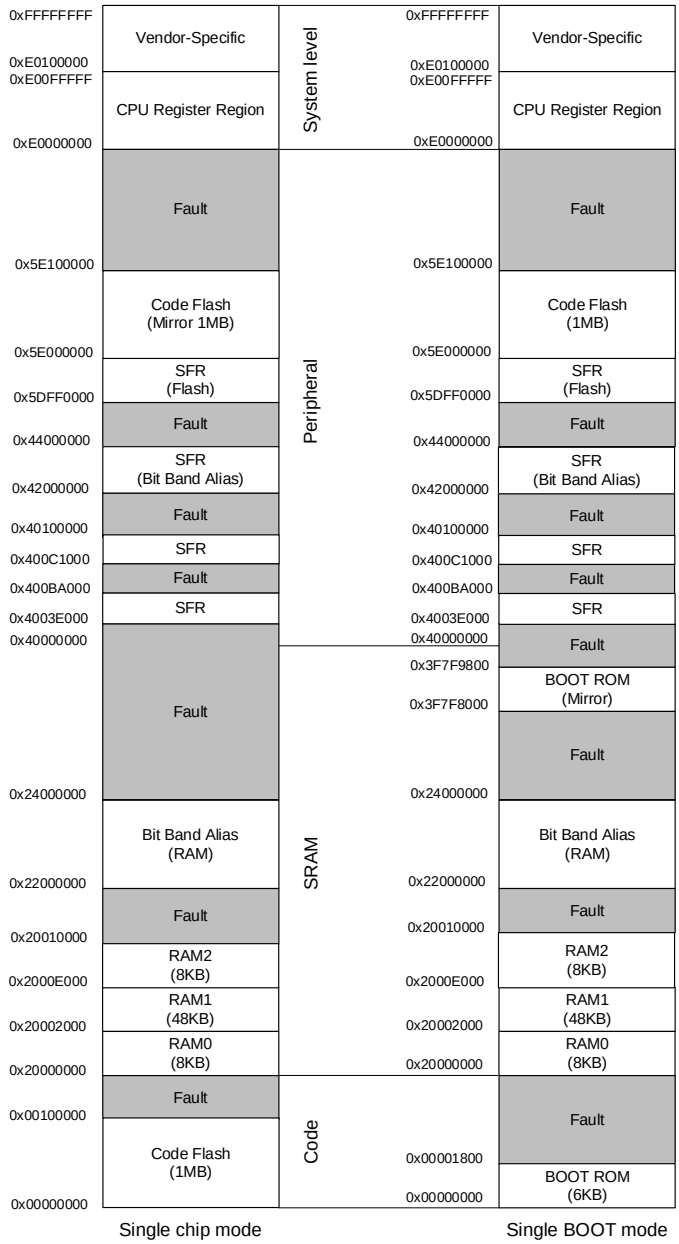


Figure 3.1 Memory Map of TMPM471F10FG

Note1: Fault: Please do not access their region.

Note2: For details of Single Chip Mode and Single Boot Mode, refer to "Flash Memory" in the Reference Manual.

4. Pin Description

4.1. Functional Pin Name and Functions

4.1.1. Function Pins of Peripheral

Table 4.1 Pin Names and Functions of Peripheral Pins

Peripheral function	Pin name	Input or Output	Function
Interrupt Control (IA/IB)	INTx	Input	External interrupt input pin External input pin provides the noise filter (filter width: Typ. 30 ns).
32-bit Timer Event Counter (T32A)	T32AxINA0	Input	16-bit timer A input capture input pin 0
	T32AxOUTA	Output	16-bit timer A output pin
	T32AxINB0	Input	16-bit timer B input capture input pin 0
	T32AxOUTB	Output	16-bit timer B output pin
	T32AxINC0	Input	32-bit timer input capture input pin 0
	T32AxOUTC	Output	32-bit timer output pin
Serial Peripheral Interface (TSPI)	TSPIxCSIN	Input	Chip select input pin
	TSPIxCS0	Output	Chip select output pin 0
	TSPIxCS1	Output	Chip select output pin 1
	TSPIxRXD	Input	Data input pin
	TSPIxTXD	Output	Data output pin
	TSPIxSCK	I/O	Clock input/output pin
Asynchronous Serial Communication Circuit (UART)	UTxRXD	Input	Data input pin
	UTxTXDA	Output	Data output pin A
	UTxCTS_N	Input	Clear to send signal pin
	UTxRTS_N	Output	Request to send signal pin
I^2C Interface Version A (EI2C)	EI2CxSDA	I/O	Data input/output pin
	EI2CxSCL	I/O	Clock input/output pin
Advanced Programmable Motor Control Circuit (A-PMD)	EMGx	Input	Emergency state detection input pin
	OVVx	Input	Overvoltage detection input pin
	UOx	Output	U-phase output pin
	VOx	Output	V-phase output pin
	WOx	Output	W-phase output pin
	XOx	Output	X-phase output pin
	YOx	Output	Y-phase output pin
	ZOx	Output	Z-phase output pin
Advanced Encoder Input Circuit (32-bit) (A-ENC32)	ENCxA	Input	Encoder input pin A
	ENCxB	Input	Encoder input pin B
	ENCxZ	Input	Encoder input pin Z
Analog to Digital Converter (ADC)	AINAx, AINBx	Input	Analog input pin

Note: "x" means channel number, unit number or interrupt number.

4.1.2. Debug Pins

Table 4.2 Debug Pin Names and Function

Debug PORT	Pin name	Input or Output	Function
JTAG	TMS	Input	JTAG test mode selection input pin
	TCK	Input	JTAG serial clock input pin
	TDO	Output	JTAG serial data output pin
	TDI	Input	JTAG serial data input pin
	TRST_N	Input	JTAG test reset input pin
SW	SWDIO	I/O	Serial wire data input/output pin
	SWCLK	Input	Serial wire clock input pin
	SWV	Output	Serial wire viewer output pin
TRACE	TRACECLK	Output	Trace clock output pin
	TRACEDATA0	Output	Trace data output pin 0
	TRACEDATA1	Output	Trace data output pin 1
	TRACEDATA2	Output	Trace data output pin 2
	TRACEDATA3	Output	Trace data output pin 3

4.1.3. Control Pins

Table 4.3 Control Pin Names and Function

	Pin name	Input or Output	Function
Control Pin	X1	Input	High-speed oscillator connection pin
	X2	Output	High-speed oscillator connection pin
	EHCLKIN	Input	External Clock signal input pin
	BOOT_N	Input	BOOT mode control pin The BOOT mode control pin is sampled on the rising edge of the RESET_N input. It's not sampled by internal Reset factor. If the BOOT mode control pin is "Low" level, the MCU enters single boot mode. If it is "High", the MCU enters single chip mode. For details, refer to "Flash Memory" of Reference Manual.
	RESET_N	Input	Reset signal input pin
	MODE	Input	Mode Pin This pin must be fixed to "Low" level.

4.1.4. Power Supply Pins

Table 4.4 Power Supply Pin Names and Function

	Pin name	Function
Power Supply	DVDD5A (Note1) DVDD5B (Note1) DVDD5C (Note1) DVDD5D (Note1)	Power supply pin for digital DVDD5A/B/C/D supplies the power to the following pins: PA to PG, PK, PL, PN, PR, MODE, RESET_N
	DVSSA (Note2) DVSSB (Note2) DVSSC (Note2) DVSSD (Note2) DVSSE (Note2) DVSSF (Note2) DVSSG (Note2)	GND pin for digital
	REGOUT1 (Note3)	Capacitor for a regulator connection pin (Note4)
	REGOUT2 (Note3)	Capacitor for a regulator connection pin (Note4)
	AVDD5 VREFH	Power supply pin for analog and reference power pin for analog (VREFH). AVDD5 supplies the power to the following pins: PH, PJ, PP
	AVSS VREFL	GND pin for analog and reference GND pin for analog (VREFL)

Note1: Apply the voltage to DVDD5A, DVDD5B, DVDD5C and DVDD5D, at the same potential except the case that the pins are not provided.

Note2: Apply the external voltage to DVSSA, DVSSB, DVSSC, DVSSD, DVSSE, DVSSF and DVSSG at the same potential except the case that the pins are not provided.

Note3: For REGOUT1 and REGOUT2, do not cause a short circuit with DVDD5A, DVDD5B, DVDD5C, DVDD5D, DVSSA, DVSSB, DVSSC, DVSSD, DVSSE, DVSSF or DVSSG.

Note4: For the capacitor value, refer to the "7.12. Regulator"

4.1.5. Capacitors between Power Supply Pins

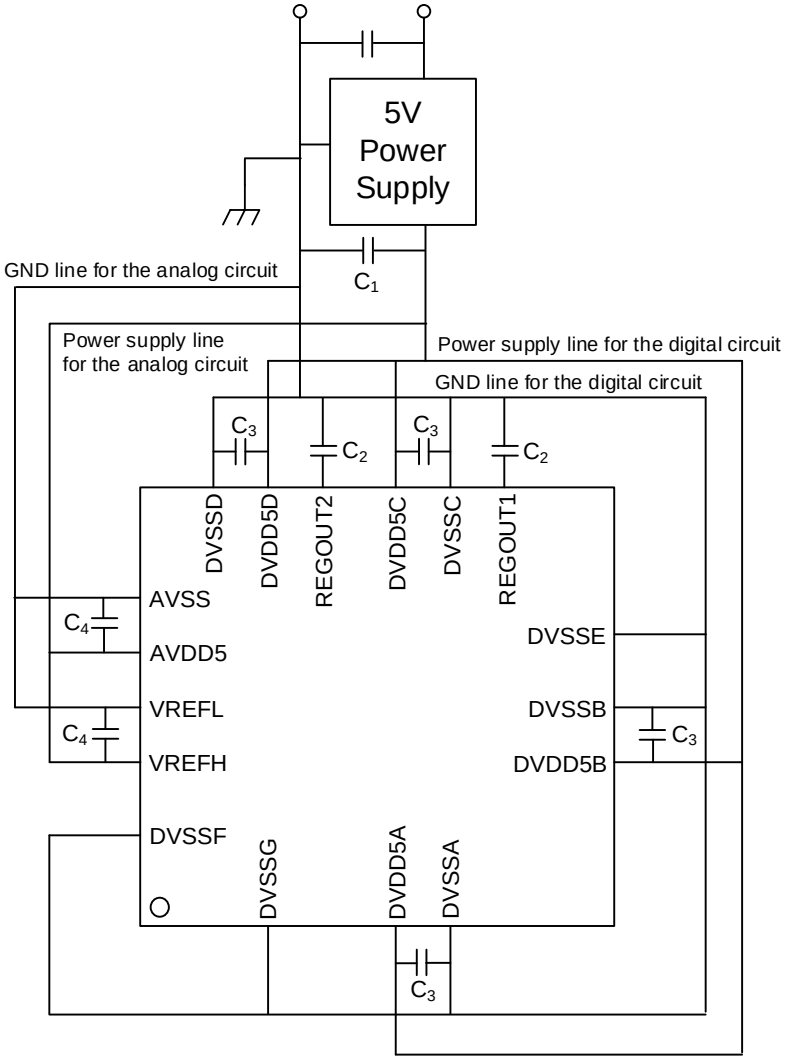


Figure 4.1 Capacitors for Power Supply Pins Connection Circuit

Note1: Insert a ceramic capacitor (C_1) near the output terminal of the 5V power supply. The power gradient with C_1 must be satisfied V_{PON} and V_{POFF} in "7.6. Characteristics of Internal Processing at RESET".

Note2: Insert the bypass capacitor ((C_3, C_4:0.01 µF to 0.1 µF) between the power supply and GND near each MCU power supply pin.

Note3: Insert the power supply stabilizing ceramic capacitor (C_2) of the same capacity into the capacitor connection pin for the internal regulator (REGOUT1, REGOUT2). These capacitors should be placed near DVSSC for REGOUT1 and DVSSD for REGOUT2. Regarding value of capacitor, refer to "7.12. Regulator".

Note4: In order to suppress noise mixing from the digital power supply to the analog circuit, separate the analog power supply line and the digital power supply line near the 5V power supply output.

Note5: In order to suppress noise mixing from the peripheral circuit to the analog circuit, when inserting a filter circuit or pull-up / down resistor to the input / output terminal of the analog power supply system, connect the components that make up these circuits to the analog power supply line.

Note6: In order to suppress high frequency noise received from the loop circuit by the power supply line, the GND line and the capacitor, do not separate the power supply line and the GND line from each other.

4.2. Functional Pin and Ports Assignment (Pin Number)

Following table shows a pin number of the port assignment and each product which were seen from the functional pin.

Table 4.5 Signal Connection List: UART

Function	Combination functional pin name	Port name	TMPM471F10FG (LQFP100)
UART ch0	UT0RXD	PE0	10
		PE1	11
	UT0TXDA	PE1	11
		PE0	10
	UT0CTS_N	PE2	12
		PE3	13
	UT0RTS_N	PE3	13
		PE2	12
UART ch1	UT1RXD	PA5	7
		PA6	8
	UT1TXDA	PA6	8
		PA5	7
	UT1CTS_N	PA4	6
		PA7	9
	UT1RTS_N	PA7	9
		PA4	6
UART ch2	UT2RXD	PD5	35
		PD6	36
	UT2TXDA	PD6	36
		PD5	35
	UT2CTS_N	PD3	33
		PD4	34
	UT2RTS_N	PD4	34
		PD3	33
UART ch3	UT3RXD	PF3	53
		PF4	54
	UT3TXDA	PF4	54
		PF3	53
	UT3CTS_N	PF1	51
		PF2	52
	UT3RTS_N	PF2	52
		PF1	51
UART ch4	UT4RXD	PG3	42
		PG4	43
	UT4TXDA	PG4	43
		PG3	42
	UT4CTS_N	PG1	38
		PG2	39
	UT4RTS_N	PG2	39
		PG1	38

Table 4.6 Signal Connection List: EI2C/TSPI

Function	Combination functional pin name	Port name	TMPM471F10FG (LQFP100)
EI2C ch0	EI2C0SDA	PN0	100
	EI2C0SCL	PN1	99
EI2C ch1	EI2C1SDA	PK0	72
	EI2C1SCL	PK1	71
TSPI ch0	TSPI0RXD	PE1	11
	TSPI0TXD	PE0	10
	TSPI0SCK	PE2	12
	TSPI0CSIN	PE3	13
	TSPI0CS0	PE4	15
	TSPI0CS1	PE5	16
TSPI ch1	TSPI1RXD	PA6	8
	TSPI1TXD	PA5	7
	TSPI1SCK	PA4	6
	TSPI1CSIN	PA7	9
	TSPI1CS0	PA2	4
	TSPI1CS1	PA3	5
TSPI ch2	TSPI2RXD	PD6	36
	TSPI2TXD	PD5	35
	TSPI2SCK	PD4	34
	TSPI2CSIN	PD3	33
	TSPI2CS0	PD1	31
	TSPI2CS1	PD2	32
TSPI ch3	TSPI3RXD	PF4	54
	TSPI3TXD	PF3	53
	TSPI3SCK	PF2	52
	TSPI3CSIN	PF0	50
	TSPI3CS0	PF1	51
	TSPI3CS1	PB0	63

Table 4.7 Signal Connection List: T32A

Function	Combination functional pin name	Port name	TMPM471F10FG (LQFP100)
T32A ch0	T32A00INA0	PA0	2
	T32A00OUTA	PA1	3
	T32A00INB0	PN2	98
	T32A00OUTB	PN1	99
	T32A00INC0	PA0	2
	T32A00OUTC	PA1	3
T32A ch1	T32A01INA0	PA6	8
	T32A01OUTA	PA5	7
	T32A01INB0	PA2	4
	T32A01OUTB	PA3	5
	T32A01INC0	PA6	8
	T32A01OUTC	PA5	7
T32A ch2	T32A02INA0	PA7	9
	T32A02OUTA	PE3	13
	T32A02INB0	PE1	11
	T32A02OUTB	PE0	10
	T32A02INC0	PA7	9
	T32A02OUTC	PE3	13
T32A ch3	T32A03INA0	PE4	15
	T32A03OUTA	PE5	16
	T32A03INB0	PE6	17
	T32A03OUTB	PE7	18
	T32A03INC0	PE4	15
	T32A03OUTC	PE5	16
T32A ch4	T32A04INA0	PD0	30
	T32A04OUTA	PD1	31
	T32A04INB0	PF0	50
	T32A04OUTB	PF1	51
	T32A04INC0	PD0	30
	T32A04OUTC	PD1	31

Table 4.8 Signal Connection List: ADC/INT

Function	Combination functional pin name	Port name	TMPM471F10FG (LQFP100)
ADC unit A	AINA12	PH0	96
	AINA13	PH1	95
	AINA14	PH2	94
	AINA15	PH3	93
	AINA16	PH4	92
	AINA17	PH5	91
	AINA18	PH6	90
	AINA19	PH7	89
	AINA20	PP0	88
	AINA21	PP1	85
	AINA22	PP2	84
	AINA23	PP3	83
ADC unit B	AINB12	PP1	85
	AINB13	PP2	84
	AINB14	PP3	83
	AINB15	PJ0	80
	AINB16	PJ1	79
	AINB17	PJ2	78
	AINB18	PJ3	77
	AINB19	PJ4	76
	AINB20	PJ5	75
	AINB21	PJ6	74
	AINB22	PJ7	73
INT	INT0	PH0	96
	INT1	PH1	95
	INT2	PH2	94
	INT3	PA0	2
	INT4	PA2	4
	INT5	PE4	15
	INT6	PE6	17
	INT7	PE7	18
	INT8	PA7	9
	INT9	PD3	33
	INTA	PL1	21
	INTB	PL0	20
	INTC	PJ6	74
	INTD	PJ7	73
	INTE	PK0	72
	INTF	PK1	71

Table 4.9 Signal Connection List: A-PMD/A-ENC32

Function	Combination functional pin name	Port name	TMPM471F10FG (LQFP100)
A-PMD ch0	EMG0	PC6	28
	OVV0	PC7	29
	UO0	PC0	22
	VO0	PC2	24
	WO0	PC4	26
	XO0	PC1	23
	YO0	PC3	25
	ZO0	PC5	27
A-PMD ch1	EMG1	PG6	45
	OVV1	PG7	46
	UO1	PG0	37
	VO1	PG2	39
	WO1	PG4	43
	XO1	PG1	38
	YO1	PG3	42
	ZO1	PG5	44
A-ENC32 ch0	ENC0A	PD0	30
	ENC0B	PD1	31
	ENC0Z	PD2	32
A-ENC32 ch1	ENC1A	PF2	52
	ENC1B	PF3	53
	ENC1Z	PF4	54

Table 4.10 Signal Connection List: JTAG/SW/TRACE/Control pin

Function	Combination functional pin name	Port name	TMPM471F10FG (LQFP100)
JTAG	TMS	PB3	66
	TCK	PB4	67
	TDO	PB5	68
	TDI	PB6	69
	TRST_N	PB7	70
SW	SWDIO	PB3	66
	SWCLK	PB4	67
	SWV	PB5	68
TRACE	TRACECLK	PB0	63
	TRACEDATA0	PB1	64
	TRACEDATA1	PB2	65
	TRACEDATA2	PK1	71
	TRACEDATA3	PK0	72
Control pin	X1	PR0	47
	X2	PR1	49
	EHCLKIN	PR0	47
	BOOT_N	PF0	50
	RESET_N		59
	MODE		57

4.3. Ports

The symbols of each table of the port have the following meanings.

- Input/Output: Input and/or Output of Port
  Input: Input port
  Output: Output port
  I/O: Input/Output port

- PU/PD: Programmable pull-up/pull-down
  PU: Programmable pull-up is selectable
  PD: Programmable pull-down is selectable

- OD: Programmable open-drain output
  Yes: Support
  No: Non support

- SMT/CMOS: Input gate
  SMT: Schmitt trigger input
  CMOS: CMOS input

- State under Reset: Port state under Reset
  Hi-Z: High impedance
  PU: Pull-up
  PD: Pull-down

- State after Reset: Port state after Reset
  Hi-Z: High impedance
  PU: Pull-up
  PD: Pull-down

4.3.1. Port Specification Table

Table 4.11 Pin Numbers, and Specifications of Port A, B, C, D

Port name	Input/Output	PU/PD	OD	SMT/ CMOS	Under reset	After reset
PA0	I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
PA1	I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
PA2	I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
PA3	I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
PA4	I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
PA5	I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
PA6	I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
PA7	I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
PB0	I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
PB1	I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
PB2	I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
PB3	I/O	PU/PD	YES	SMT	PU (Note)	PU (Note)
PB4	I/O	PU/PD	YES	SMT	PD (Note)	PD (Note)
PB5	I/O	PU/PD	YES	SMT	Hi-Z(Note)	Hi-Z (Note)
PB6	I/O	PU/PD	YES	SMT	PU (Note)	PU (Note)
PB7	I/O	PU/PD	YES	SMT	PU (Note)	PU (Note)
PC0	I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
PC1	I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
PC2	I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
PC3	I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
PC4	I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
PC5	I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
PC6	I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
PC7	I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
PD0	I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
PD1	I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
PD2	I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
PD3	I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
PD4	I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
PD5	I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
PD6	I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z

Note: It is assigned to a debugging pin in the state of the initial stage. (PB6: TDI, PB5: TDO/SWV, PB3: TMS/SWDIO, PB2: TCK/SWCLK, PB7: TRST_N)
When receiving the command from TOOL, PB5: TDO/SWV becomes output.

Table 4.12 Pin Numbers, and Specifications of Port E, F, G, H

Port name	Input/Output	PU/PD	OD	SMT/ CMOS	Under reset	After reset
PE0	I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
PE1	I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
PE2	I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
PE3	I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
PE4	I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
PE5	I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
PE6	I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
PE7	I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
PF0	I/O	PU/PD (Note)	YES	SMT	Hi-Z (Note)	Hi-Z
PF1	I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
PF2	I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
PF3	I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
PF4	I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
PG0	I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
PG1	I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
PG2	I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
PG3	I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
PG4	I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
PG5	I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
PG6	I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
PG7	I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
PH0	I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
PH1	I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
PH2	I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
PH3	I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
PH4	I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
PH5	I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
PH6	I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
PH7	I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z

Note: Combination with BOOT_N. When RESET_N=0, Pull-up resistor is enabled. When RESET_N=1, the pin state is Hi-Z with internal reset.

Table 4.13 Pin Numbers, and Specifications of Port J, K, L, N, P, R

Port name	Input/Output	PU/PD	OD	SMT/ CMOS	Under reset	After reset
PJ0	I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
PJ1	I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
PJ2	I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
PJ3	I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
PJ4	I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
PJ5	I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
PJ6	I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
PJ7	I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
PK0	I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
PK1	I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
PL0	I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
PL1	I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
PN0	I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
PN1	I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
PN2	I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
PP0	I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
PP1	I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
PP2	I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
PP3	I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
PR0	Input	PD	NO	SMT	Hi-Z	Hi-Z
PR1	Input	PD	NO	SMT	Hi-Z	Hi-Z

5. Functional Description and Operation Description

5.1. Reference Manuals

For more information on TMPM471F10FG, please refer to Reference Manuals below;

Table 5.1 Reference Manuals for TMPM471F10FG

Reference manual	IP symbol	Category
Input/Output Ports (TMPM471F10FG)	PORT-TMPM471F10FG	System
Exception (TMPM471F10FG)	EXCEPT-TMPM471F10FG	System
Clock Control and Operation Mode (TMPM471F10FG)	CG-TMPM471F10FG	System
Product Information (TMPM471F10FG)	PINFO-TMPM471F10FG	System
Flash Memory	FLASH10MUD32-A	Peripheral
Trimming Circuit	TRM-B	Peripheral
Oscillation Frequency Detector	OFD-A	Peripheral
Voltage Detection Circuit	LVD-D2	Peripheral
Digital Noise Filter Circuit	DNF-A	Peripheral
Debug Interface	DEBUG-A	Peripheral
DMA Controller	DMAC-B	Peripheral
Asynchronous Serial Communication Circuit	UART-C	Peripheral
Serial Peripheral Interface	TSPI-E	Peripheral
I^2C Interface Version A	EI2C-A	Peripheral
12-bit Analog to Digital Converter	ADC-G2	Peripheral
Advanced Programmable Motor Control Circuit	A-PMD-A	Peripheral
Advanced Encoder Input Circuit (32-bit)	A-ENC32-A	Peripheral
32-bit Timer Event Counter	T32A-C	Peripheral
Clock Selective Watchdog Timer	SIWDT-A	Peripheral
CRC Calculation Circuit	CRC-A	Peripheral
RAM Parity	RAMP-B	Peripheral

5.2. Processor Core

The TMPM471F10FG incorporates a high-performance 32-bit processor core (Arm Cortex-M4 processor with FPU).

For the operation of the processor core, refer to the "Arm Cortex-M4 Processor Technical Reference Manual". This section explains the product-specific information.

5.2.1. Core Information

The revision of Cortex-M4 processor with FPU used in the TMPM471F10FG is shown as below:

Table 5.2 Core Revision

Core revision
r0p1

5.2.2. Configurable Options

In the Cortex-M4 processor with FPU, some blocks can be selected to implement. The following table shows the configurations of the TMPM471F10FG.

Table 5.3 Configurable Options and Implementations

Configurable option	Implementation
FWB	Literal comparator: 2 Instruction comparator: 6
DWT	Comparator: 4
ITM	Available
MPU	Available
ETM	Available
AHB-AP	Available
AHB trace macro cell interface	Not available
TPIU	Available
WIC	Not available
Debug port	JTAG/Serial wire
Bit band	Available
Sequential control of AHB	Not available

5.3. Clock Control and Operation Mode (CG)

The CG selects a clock gear ratio and the prescaler clock, or warm up time of the oscillator.

There are NORMAL mode and low-power consumption mode as operation modes. Power consumption can be decreased by mode transition.

The system clock consists of "High-speed system clock" and "Middle-speed system clock". The former is a high-speed oscillation clock and the latter is generated by dividing High-speed system clock.

The outline of the clock/mode control circuit is as follows:

- Internal high-speed oscillator: 10MHz
- Selectable from the external high-speed oscillator or internal high-speed oscillator.
- PLL (Clock Multiplication Circuit)

  For System clock, Capable of 160 MHz output by changing the multiplication ratio according to the frequency of the high-speed oscillation circuit.
- Clock gear:

  The high-speed clock can be divided by 1, 2, 4, 8, or 16 and the clock is used as the system clock (fsys).
- Low-power consumption mode:

  IDLE: Only the CPU is stopped in this mode. Each peripheral circuit can enable or disable operation in the IDLE mode.

  STOP1: The system clock is stopped in this mode.

5.4. Flash Memory (Code FLASH)

TMPM471F10FG has 1MB of Code flash.

The code flash stores instruction code, and CPU reads instruction code and executes.

TMPM4KxF10A has a dual mode that possible to rewrite another area while executing instructions in one area.

It has protection function which prohibits write or erase by the block unit and it has the security function which prohibits the reading of the program code by the 3rd person.

5.5. Oscillator

External High-Speed Oscillator (EHOSC):

Connect crystal resonator or ceramic resonator to terminals. Use clock source for System clock.

Internal High-Speed Oscillator 1 (IHOSC1):

The oscillation frequency is 10MHz. Use clock source for System clock.

Internal High-Speed Oscillator 2 (IHOSC2):

The oscillation frequency is 10MHz. Use clock source for OFD and SIWDT.

Table 5.4 Built-in Oscillator

	TMPM471F10FG
EHOSC	✓
IHOSC1	✓
IHOSC2	✓

5.6. Trimming Circuit (TRM)

The TRM can adjust oscillation frequency of the internal high-speed oscillator (IHOSC1).

Table 5.5 Built-in TRM

	TMPM471F10FG
TRM	✓

5.7. Oscillation Frequency Detection Circuit (OFD)

The OFD is a function that detects an abnormal state of the clock. It measures the external high-speed oscillation (f_{EHOSC}) or high-speed clock (fc) based on the internal reference clock (f_{IHOSC2}). If an oscillation or clock frequency is out of the specified range, a reset signal occurs.

The upper limit and the lower limit of detection frequency ranges can be specified.

Table 5.6 Built-in OFD

	TMPM471F10FG
OFD	✓

5.8. Voltage Detection Circuit (LVD)

The LVD is a peripheral function that detects whether a power supply voltage is lower or higher than the preset voltage. When a low voltage or higher voltage than the preset voltage is detected, the LVD generates an interrupt request or reset the MCU.

Setting voltage can be chosen from eight kinds. LVD is set to enable from the Reset state at the Power on.

Table 5.7 Built-in LVD

	TMPM471F10FG
LVD	✓

5.9. Digital Noise Filter Circuit (DNF)

The DNF can eliminate the noise of input signals from external interrupt pins at the certain range. The noise of the High level / Low level input of the external interrupt signal INTx is removed.

Table 5.8 Number of DNF

	TMPM471F10FG
Number of DNF	16

5.10. Debug Interface (DEBUG)

TMPM471F10FG contains interface for connecting debug tool, which is the Serial Wire Debug Port (SWCLK, SWDIO) and the JTAG Debug Port (TDI, TDO, TMS, TCK, TRST_N). These are connected with the Debug tool and used for program development. And also it contains the trace clock (TRACECLK) and data output (TRACEDATA0 to 3) to reduce the debug process.

TMPM471F10FG supports serial wire debug ports, JTAG debug ports, and trace outputs.

5.11. DMA Controller (DMAC)

The DMAC is the peripheral function to move the data between peripheral functions and the memory, or between memories. These operations are performed separately from the CPU control; thus, the CPU load can greatly be reduced by using the DMA.

TMPM471F10FG has one DMA controller (DMAC) unit, and there are up to 32 channels of activation factors per unit.

Table 5.9 Built-in DMAC

Unit	TMPM471F10FG
Unit A	✓

5.12. Asynchronous Serial Communication Circuit (UART)

The UART is asynchronous serial communication function. It can choose the data length of 7, 8 or 9bits, parity existence, and a STOP bit length function. Moreover, selection of the MSB first / LSB first and reversal of data polarity can be performed and Terminal exchanged of TXD/RXD can be performed in a Port setting.

The FIFO buffer supports data communication on 8-stage at transmission; and on 8-stage at reception. The telecommunication control by CTS/RTS is supported.

Table 5.10 Built-in UART

Channel	TMPM471F10FG
Channel 0	✓
Channel 1	✓
Channel 2	✓
Channel 3	✓
Channel 4	✓

5.13. Serial Peripheral Interface (TSPI)

The TSPI supports two communication methods and enables serial communication to perform between other devices at high speed. The SPI bus type, which uses a CS (Chip Select) signal at communications, and SIO bus type, which does not use a CS signal at communications can be selected.

The data length can be changed from 7 bits (with a parity bit) to 32 bits (without a parity bit) in the unit of one bit. There is an 8-stage 16-bit FIFO for reception and transmission, each. The TSPI supports the master and slave communications.

It can support frame mode (frame length (8 to 32 bit)) or sector mode (8 to 128 bit of frame length is configured in 2 to 4 sectors).

Table 5.11 Built-in TSPI

Channel	TMPM471F10FG
Channel 0	✓
Channel 1	✓
Channel 2	✓
Channel 3	✓

5.14. I²C Interface Version A (EI2C)

EI2C is two-wire bi-directional serial communications between master and slave device. The mode in which two or more masters can exist on the same bus called a multi-master is supported. It supports Standard-mode (Max 100kHz), Fast-mode (Max 400kHz), Fast-mode Plus (Max 1MHz), and 7-bit addressing and more 10-bit addressing.

Table 5.12 Built-in EI2C

Channel	TMPM471F10FG
Channel 0	✓
Channel 1	✓

5.15. 12-bit Analog to Digital Converter (ADC)

The ADC is a 12-bit successive-approximation analog-to-digital converter. The combination of a conversion result register and analog input can be programmed in each startup trigger of AD conversion. A startup trigger for analog to digital conversion can be selected from software or peripheral functions (A-PMD trigger outputs, timer/event counter outputs, port inputs). A motor is easily controllable by cooperating especially with A-PMD.

The monitor function of conversion result is also available and it can generate an interrupt when the compare conditions are matched.

This ADC incorporates a selector to connect VREFH/VREFL with reference power supply. Controlling by software can support self-diagnosis function.

Table 5.13 Built-in ADC Channel List

ADC	TMPM471F10FG
Unit A Analog Inputs Pin count	12
Unit B Analog Inputs Pin count	11

5.16. Advanced Programmable Motor Control Circuit (A-PMD)

The A-PMD enables users to control brushless DC motors easily. It incorporates the pulse modulation circuit and dead-time circuit, and easily generates signals for motor control that makes 3-phase complementary PWM output and ADC cooperate.

It also provides the over-voltage detection input and abnormal detection input to support safety measures.

Furthermore, 3-phase interleaved PFC control for power-factor improvement can be provided.

Table 5.14 Built-in A-PMD

Channel	TMPM471F10FG
Channel 0	✓
Channel 1	✓

5.17. Advanced Encoder Input Circuit (32-bit) (A-ENC32)

The A-ENC32 supports an incremental encoder to acquire the motor position easily. The noise canceller is installed in the input pins, so that the signals from an incremental encoder or Hall sensor can be input directly.

The A-ENC32 provides six operation modes: encoder mode, sensor modes (3 kinds), timer mode, and phase counter mode.

Table 5.15 Built-in A-ENC

Channel	TMPM471F10FG
Channel 0	✓
Channel 1	✓

5.18. 32-bit Timer Event Counter (T32A)

The T32A is a timer event counter that can operate as a 32-bit timer or two 16-bit timers. 16-bit Timer or 32-bit Timer can be selected. In 16-bit Timer, the T32A is comprised of Timer A and Timer B incorporating a 16-bit counter. In 32-bit Timer, the T32A operates as Timer C incorporating a 32-bit counter.

The T32A have an interval timer, event counter, input capture, 2-phase counter input, PPG output, Synchronous Start, and Trigger start/stop functions.

Table 5.16 Built-in T32A

Channel	TMPM471F10FG
Channel 0	✓
Channel 1	✓
Channel 2	✓
Channel 3	✓
Channel 4	✓

5.19. Clock Selective Watchdog Timer (SIWDT)

The SIWDT is a peripheral function that detects an overflow of the binary counter and generates an interrupt request or resets the MCU. This state occurs when a binary counter cannot be cleared within the preset detection time.

The count clock can be selected from three clocks: system clock (fsys/4), internal oscillator1 (f_{IHOSC1}), or internal oscillator2 (f_{IHOSC2}).

It also provides the count-clear window function that can clear the count only for the specified period.

Moreover, change of a register can be forbidden by setting to protected mode.(the count-clear function is possible)

Table 5.17 Built-in SIWDT

Channel	TMPM471F10FG
Channel 0	✓

5.20. CRC Calculation Circuit (CRC)

The CRC Calculation Circuit has the hardware calculation circuit for CRC32 and CRC16.
It can be used for detecting a memory and communication data error.

Table 5.18 Built-in CRC

	TMPM471F10FG
CRC	✓

5.21. RAM Parity (RAMP)

The RAM parity function generates and (8-bit unit) stores even parity data when writing to RAM, and performs a parity judging when reading from RAM.
An interrupt is generated when it becomes an error by judgment. The Status and Address which the error generated are known.

Table 5.19 Built-in RAMP

Channel	TMPM471F10FG
Channel 0	✓
Channel 1	✓

5.22. Measures for Security Risk

5.22.1. Outline

TMPM471F10FG contains two measures for security risk to prevent unauthorized access. Table 5.20, Table 5.21 and Figure 5.1 show the assumed access paths and protection targets for each operation mode.
For more information, refer to the reference manual “Flash Memory”.

(1) Security Function
The security function prohibits communication with debugging tools. It also prohibits flash writers from reading and writing to flash memory.

Table 5.20 Access Paths and Protection Targets (1)

Operation mode	Access path	Protected object
Single chip mode Single Boot mode	JTAG/SW	CPU FLASH/ROM/RAM
Flash writer mode	Flash writer	FLASH

(2) Password in RAM Transfer Command
Single boot mode is operated by sending a command via UART communication.
The RAM transfer command is authenticated by the password.

Table 5.21 Access Paths and Protection Targets (2)

Operation mode	Access path	Protected object
Single Boot mode	UART	CPU FLASH/ROM/RAM

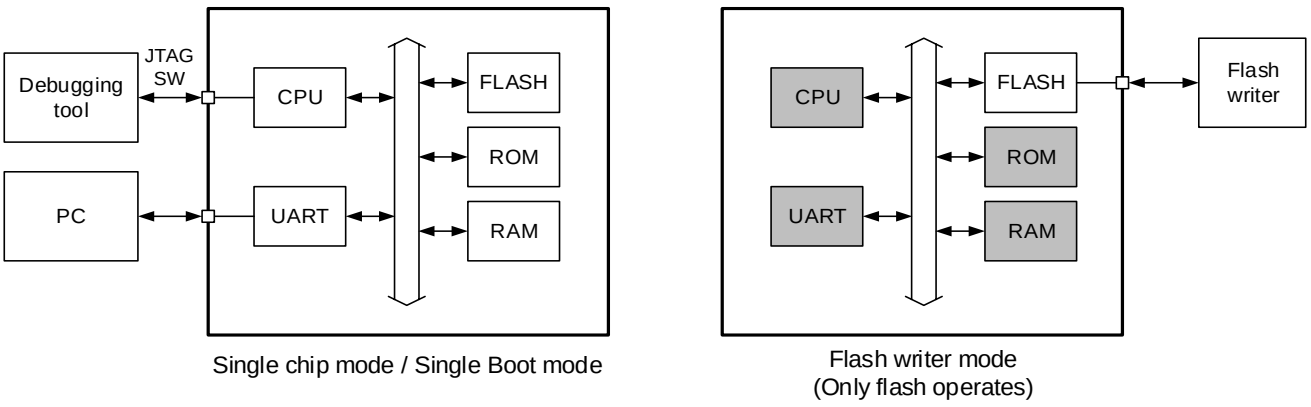


Figure 5.1 Measures for Security Risk

Note: The security function does not prohibit Non Break Debug Interface (NBDIF) communication. Prohibit it with ***[NBDCR0]***<NBDEN>.
(It’s applicable to the products with NBDIF.)

5.22.2. Disclaimer

Refer to "RESTRICTIONS ON PRODUCT USE" at the end of this manual.

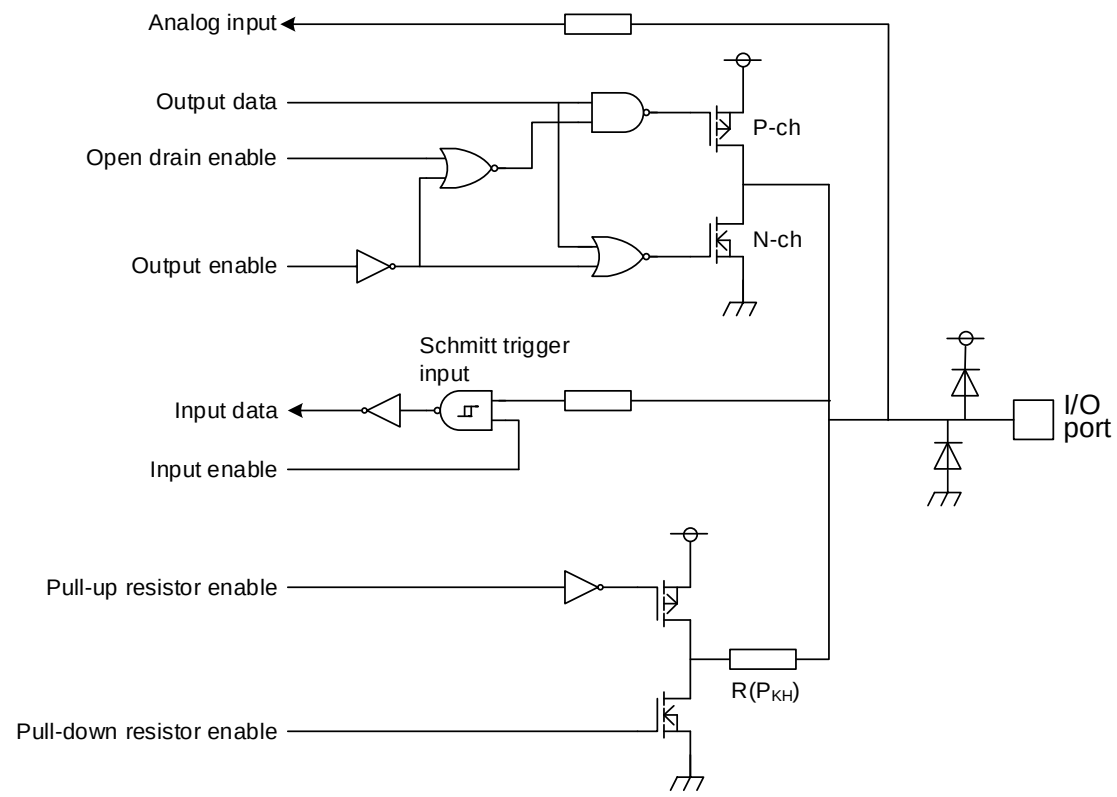
6. Equivalent Circuit

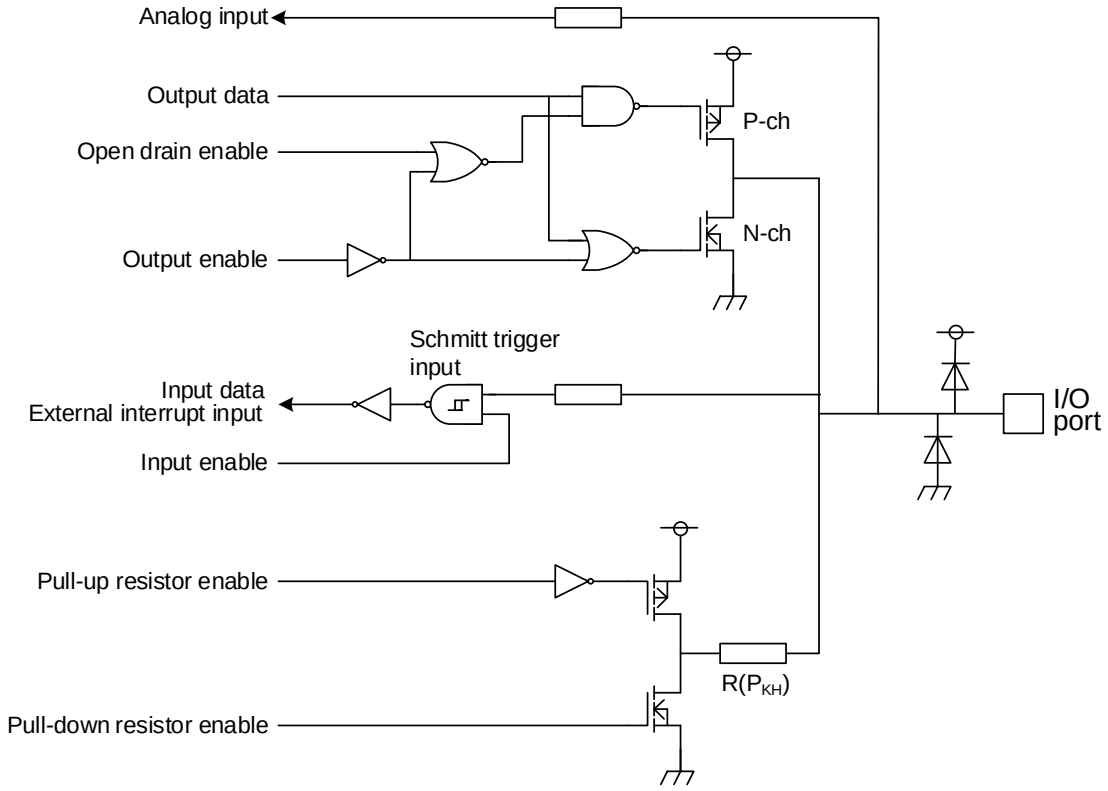
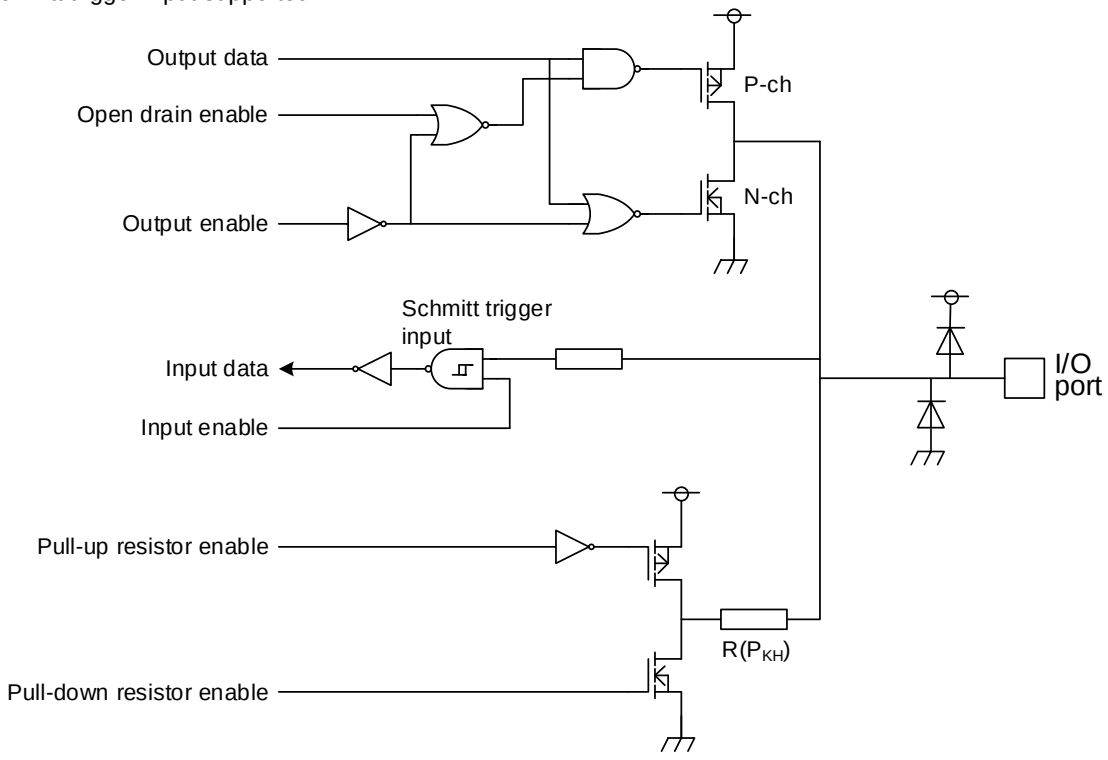
Basically, the gate symbols written are the same as those used for the standard CMOS logic IC [74HCxx] series.
The input protection resistance ranges from several tens of Ω to several hundred Ω. Feedback resistor and Damping resistor are shown with a typical value.

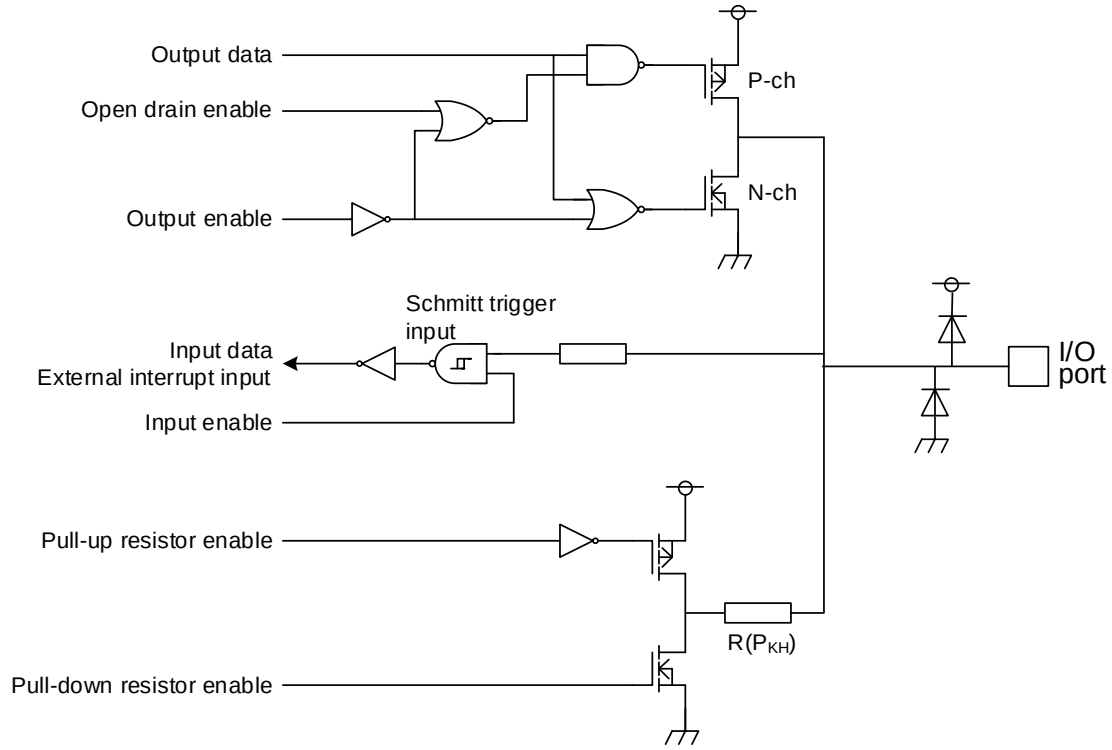
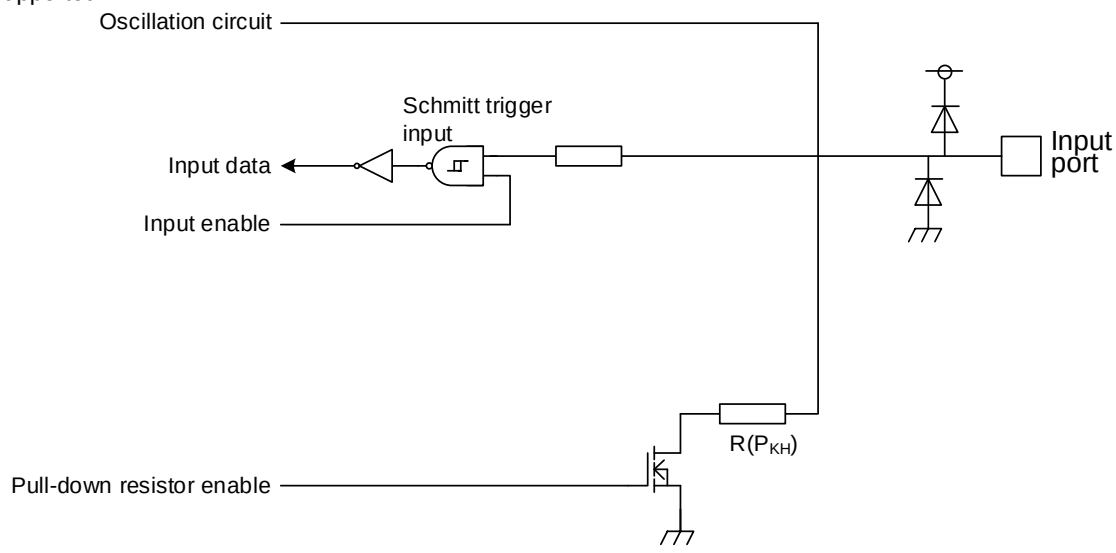
Note: The resistance without the statement of the numerical value in the figure shows input protection resistance.

6.1. Port

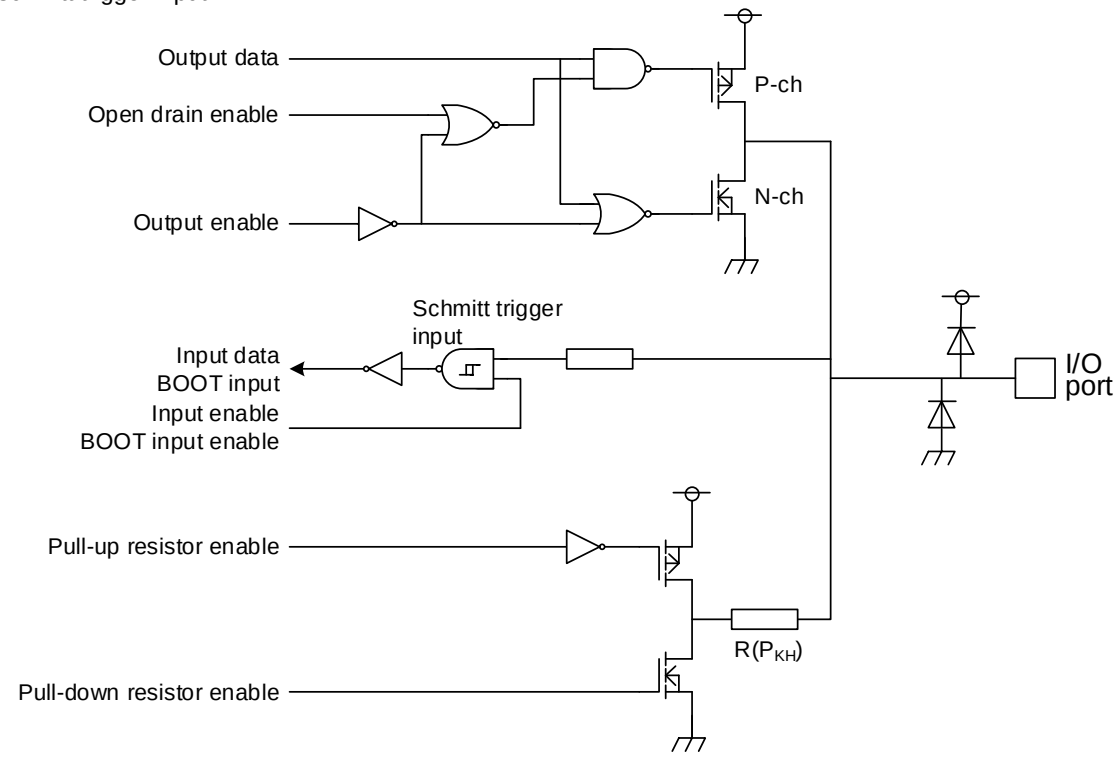
PH3 to PH7, PJ0 to PJ5, PP0 to PP3	Programmable pull-up and pull-down resistor supported, programable open-drain output supported, schmitt trigger input supported, and analog input supported



PH0 to PH2, PJ6, PJ7	Programmable pull-up and pull-down resistor supported, programable open-drain output supported, schmitt trigger input supported, analog input supported, and external interrupt input supported 
PA1, PA3 to PA6, PB0 to PB7, PC0 to PC7, PD0 to PD2, PD4 to PD6, PE0 to PE3, PE5, PF1 to PF4, PG0 to PG7, PN0 to PN2	Programmable pull-up and pull-down resistor supported, programable open-drain output supported, and schmitt trigger input supported 

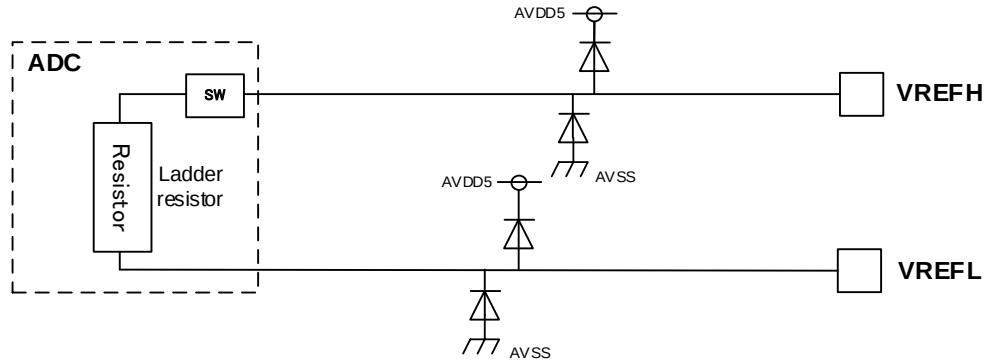
PA0, PA2, PA7, PD3, PE4, PE6、PE7, PK0, PK1, PL0, PL1	Programmable pull-up and pull-down resistor supported, programable open-drain output supported, schmitt trigger input supported, and external interrupt input supported 
PR0, PR1	Programmable pull-down resistor supported, schmitt trigger input supported, and oscillation circuit supported 

PF0/BOOT_N	Programmable pull-up and pull-down resistor supported, programable open-drain output supported, and schmitt trigger input



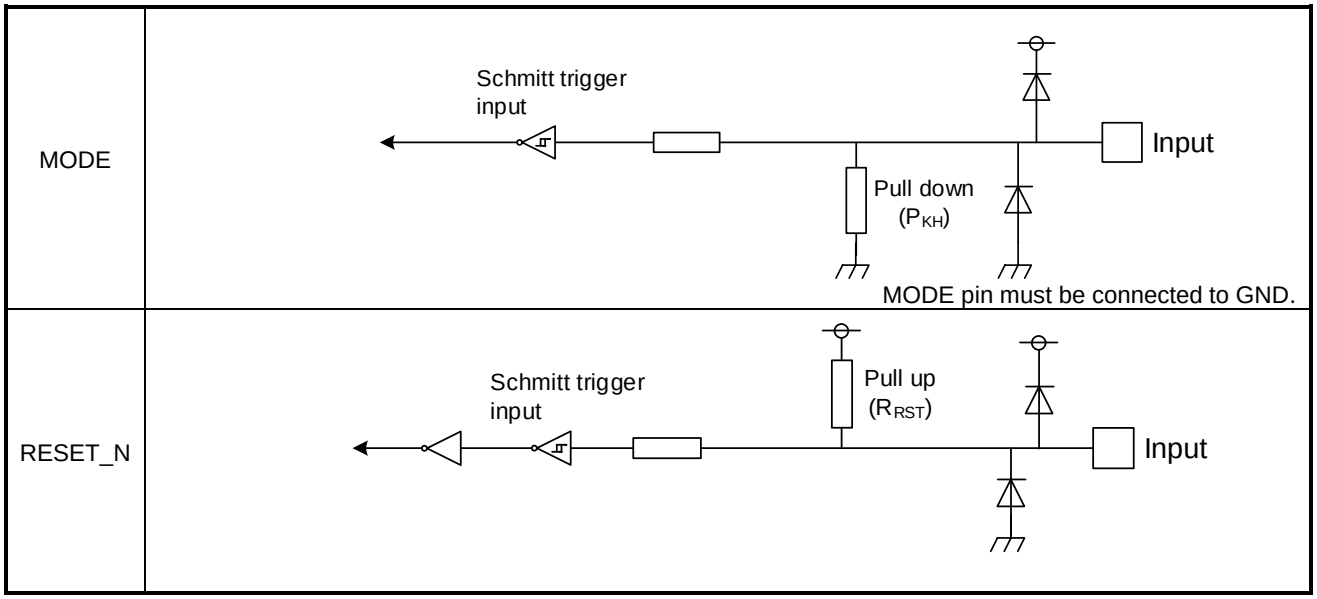
6.2. Analog Reference pin

VREFH VREFL	

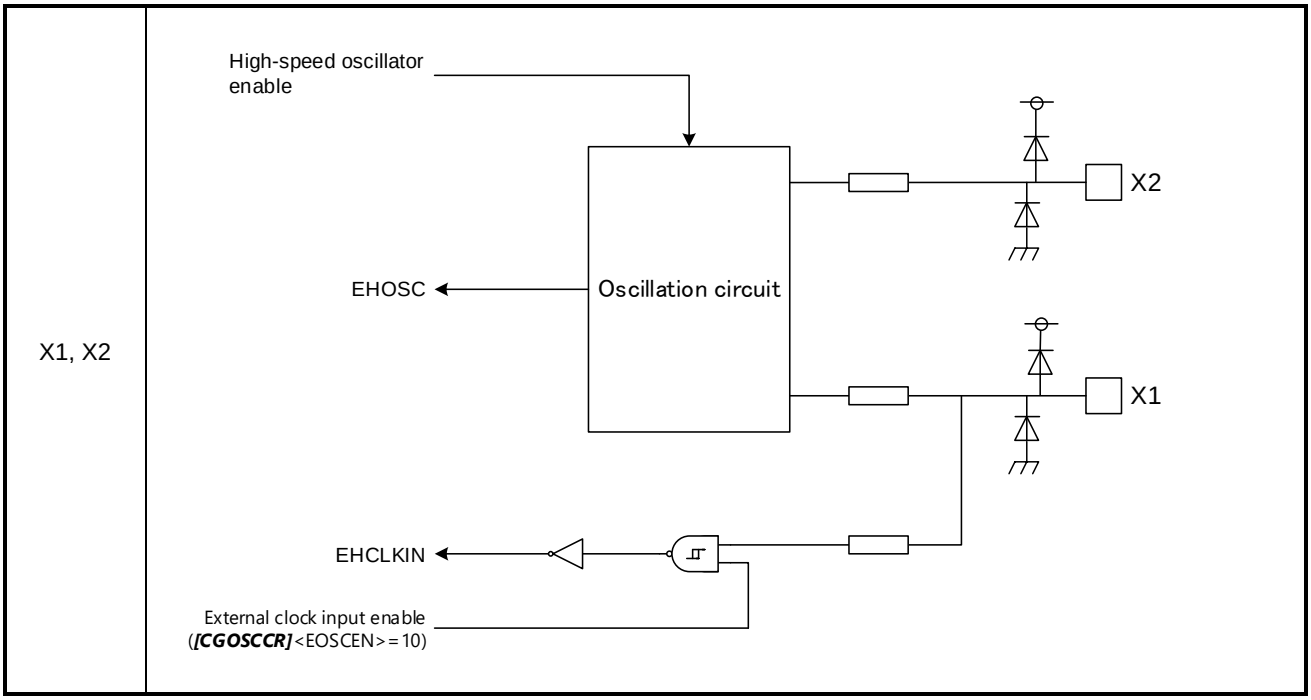


Note: SW: ON/OFF Switch Circuit

6.3. Control Pin



6.4. Clock Control



7. Electrical Characteristics

DVDD5 is a generic name for DVDD5A, DVDD5B, DVDD5C and DVDD5D. DVSS is a generic name for DVSSA, DVSSB, DVSSC, DVSSD, DVSSE, DVSSF and DVSSG.

7.1. Absolute Maximum Ratings

Table 7.1 Absolute Maximum Ratings

Parameter		Symbol	Rating	Unit
Power supply voltage		DVDD5	-0.3 to 6.0	V
		AVDD5	-0.3 to DVDD5 (Note2)	
Input voltage	PA0 to PA7, PB0 to PB7, PC0 to PC7, PD0 to PD6, PE0 to PE7, PF0 to PF4, PG0 to PG7, PK0, PK1, PL0, PL1, PN0 to PN2, PR0, PR1, MODE, RESET_N	V_{IN1}	-0.3 to DVDD5+0.3(≤6.0V) (Note2)	V
	PH0 to PH7, PJ0 to PJ7, PP0 to PP3	V_{IN2}	-0.3 to AVDD5+0.3(≤6.0V) (Note2)	
Low level output current	Per pin PA0 to PA7, PB0 to PB7, PC0 to PC7, PD0 to PD6, PE0 to PE7, PF0 to PF4, PG0 to PG7, PH0 to PH7, PJ0 to PJ7, PK0, PK1, PL0, PL1, PN0 to PN2, PP0 to PP3	I_{OL}	5	mA
	Total of all pins	ΣI_{OL}	50	
High level output current	Per pin PA0 to PA7, PB0 to PB7, PC0 to PC7, PD0 to PD6, PE0 to PE7, PF0 to PF4, PG0 to PG7, PH0 to PH7, PJ0 to PJ7, PK0, PK1, PL0, PL1, PN0 to PN2, PP0 to PP3	I_{OH}	-5	
	Total of all pins	ΣI_{OH}	-50	
Soldering temperature		T_{SOLDER}	260	°C
Storage temperature		T_{STG}	-55 to 125	°C
Operational temperature		T_{OPR}	-40 to 85	°C
Junction temperature (Note3)		Tj	-40 to 125	

Note1: Absolute maximum ratings are limiting values of operating and environmental conditions which should not be exceeded under the worst possible conditions. The equipment manufacturer should design so that no Absolute maximum rating value is exceeded with respect to current, voltage, power consumption, temperature, etc. Exposure to conditions beyond those listed above may cause permanent damage to the device or affect device reliability, which could increase potential risks of personal injury due to IC blow up and/or burning.

Note2: Apply the same voltage to DVDD5 and AVDD5 from power-on to power-off.

Note3: The calculation formula for the maximum junction temperature (Tj) is shown below.

$Tj\ (Max) = TOPR\ (Max) + PD\ (Max) \times \theta ja$

Refer to Table 7.2 for θja (thermal resistance of the package (°C/W)).
The calculation formula for maximum power dissipation (PD (Max)) is shown below.

$$PD\ (Max) = V_{DD} \times I_{DD}\ (Max) + \Sigma\ (I_{OL} \times V_{OL}) + \Sigma\ ((V_{DD} - V_{OH}) \times I_{OH})$$

I_{OL}: "Low" level output current
I_{OH}: "High" level output current
V_{OL}: "Low" level output voltage
V_{OH}: "High" level output voltage
I_{DD}(Max): Consumption current of the MCU excluding I/O.
Please refer to "7.3.DC Electrical Characteristics (2/2)".

Table 7.2 Thermal Resistance of Package

Parameter	Symbol	Package	Board condition	Value (Note)	Unit
Thermal resistance of package	θja	P-LQFP100-1414-0.50-002	JESD51-2, JESD51-3 compliant (1s)	65.9	°C/W
			JESD51-2, JESD51-7 compliant (2s-2p)	53.3	

Note: Values are for reference. Refer to JEDEC standards for details on board conditions.

7.2. DC Electrical Characteristics (1/2)

4.5V ≤ DVDD5=AVDD5 ≤ 5.5V
DVSS = AVSS=0V
Ta=-40 to 85 °C

Parameter		Symbol	Conditions	Min	Typ.	Max	Unit
Power supply voltage	DVDD5, AVDD5	VDD	fosc = 6 to 24MHz fsys = 1 to 160MHz fsysm=1 to 80MHz	4.5	-	5.5	V
Power supply voltage (When power supply is turned on and turned off) (Note 3)	DVDD5, AVDD5	VDD	fosc = 6 to 24MHz fsys = 1 to 160MHz fsysm=1 to 80MHz	3.91	-	4.5	
Low-level Input voltage	PA0 to PA7, PB0 to PB7, PC0 to PC7, PD0 to PD6, PE0 to PE7, PF0 to PF4, PG0 to PG7, PK0, PK1, PL0, PL1, PN0 to PN2, PR0, PR1, MODE, RESET_N	V_{IL1}	-	-0.3	-	DVDD5×0.25	V
	PH0 to PH7, PJ0 to PJ7, PP0 to PP3	V_{IL2}	-			AVDD5×0.25	
High-level Input voltage	PA0 to PA7, PB0 to PB7, PC0 to PC7, PD0 to PD6, PE0 to PE7, PF0 to PF4, PG0 to PG7, PK0, PK1, PL0, PL1, PN0 to PN2, PR0, PR1, MODE, RESET_N	V_{IH1}	-	DVDD5×0.75	-	DVDD5+0.3	V
	PH0 to PH7, PJ0 to PJ7, PP0 to PP3	V_{IH2}		AVDD5×0.75		AVDD5+0.3	
Low-level output voltage	PA0 to PA7, PB0 to PB7, PC0 to PC7, PD0 to PD6, PE0 to PE7, PF0 to PF4, PG0 to PG7, PK0, PK1, PL0, PL1, PN0 to PN2	V_{OL1}	DVDD5≥4.5V I_{OL}=1.6mA	-	-	0.4	V
	PH0 to PH7, PJ0 to PJ7, PP0 to PP3	V_{OL2}	AVDD5≥4.5V I_{OL}=1.6mA	-	-	0.4	
High-level output voltage	PA0 to PA7, PB0 to PB7, PC0 to PC7, PD0 to PD6, PE0 to PE7, PF0 to PF4, PG0 to PG7, PK0, PK1, PL0, PL1, PN0 to PN2	V_{OH1}	DVDD5≥4.5V I_{OH} = -1.6mA	DVDD5-0.4	-	-	V
	PH0 to PH7, PJ0 to PJ7, PP0 to PP3	V_{OH2}	AVDD5≥4.5V I_{OH} = -1.6mA	AVDD5-0.4	-	-	

Note1: Typ. value is in Ta = 25 °C, DVDD5 = AVDD5 = 5.0V, unless otherwise noted.

Note2: Apply same voltage line to DVDD5 and AVDD5.

Note3: It is a voltage range in the case of power on or power off (when LVD disabled). In the range whose power supply is 3.9V ≤ VDD < 4.5V, does not guarantee a 12-bit A/D converter and AC electrical characteristics.

4.5V ≤ DVDD5=AVDD5 ≤ 5.5V
DVSS=AVSS=0V
Ta= -40 to 85°C

Parameter		Symbol	Conditions	Min	Typ.	Max	Unit
Leak current		I_L	0V ≤ VIN ≤ DVDD5 0V ≤ VIN ≤ AVDD5	-5	±0.05	5	μA
Schmitt trigger Input width		V_{TH}	DVDD5=AVDD5=5V	-	1.0	-	V
Reset pull-up resistor		R_{RST}		25	50	100	kΩ
Programmable pull-up/pull-down resistor		P_{KH}	Pull-up	25	50	100	
			Pull-down	25	50	100	
Pin capacity (except power supply pin)		C_{IO}	fc =1MHz	-	-	10	pF
Low-level output current	Per pin	I_{OL}	DVDD5=AVDD5=5V	-	-	2 (Note3)	mA
	Total of PA0 to PA7, PE0 to PE7, PN0 to PN3	ΣI_{OL1}	DVDD5=5V	-	-	35 (Note4)	
	Total of PC0 to PC7, PD0 to PD6, PG0 to PG7, PL0, PL1	ΣI_{OL2}	DVDD5=5V	-	-	35 (Note4)	
	Total of PB0 to PB7, PF0 to PF4, PK0, PK1	ΣI_{OL3}	AVDD5=5V	-	-	35 (Note4)	
	Total of PH0 to PH7, PJ0 to PJ7, PP0 to PP3	ΣI_{OH4}	AVDD5=5V	-	-	35 (Note4)	
High-level output current	Per pin	I_{OH}	DVDD5=AVDD5=5V	-2 (Note3)	-	-	mA
	Total of PA0 to PA7, PE0 to PE7, PN0 to PN3	ΣI_{OH1}	DVDD5=5V	-35 (Note4)	-	-	
	Total of PC0 to PC7, PD0 to PD6, PG0 to PG7, PL0, PL1	ΣI_{OH2}	DVDD5=5V	-35 (Note4)	-	-	
	Total of PB0 to PB7, PF0 to PF4, PK0, PK1	ΣI_{OH3}	DVDD5=5V	-35 (Note4)	-	-	
	Total of PH0 to PH7, PJ0 to PJ7, PP0 to PP3	ΣI_{OH4}	AVDD5=5V	-35 (Note4)	-	-	

Note1: Typ. value is in Ta = 25 °C, DVDD5 = AVDD5 = 5.0V, unless otherwise noted.

Note2: Apply same voltage line to DVDD5 and AVDD5.

Note3: The sum of the terminal currents in each group should not exceed the total current of each group.

Note4: The sum of each group current should not exceed the absolute maximum rating.

7.3. DC Electrical Characteristics (2/2)

Ta= -40 to 85°C

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
NORMAL	I_{DD}	Refer to Table 7.3 and Table 7.4 for detail.	-	30	75	mA
IDLE			-	5	50	
STOP1			-	1	25	

Note1: Typ. value is in Ta = 25 °C, DVDD5 = AVDD5 = 5.0V, unless otherwise noted.
Note2: Apply same voltage to DVDD5 and AVDD5.
Note3: Current consumption includes AVDD5 and VREF current.

Table 7.3 I_{DD} Measurement Condition (Pin setting, Oscillation Circuit)

		NORMAL	IDLE	STOP1
Pin setting	DVDD5 AVDD5 VREFH	5.0V(Typ.), 5.5V(Max)		
	X1, X2	Oscillator connected (10MHz)		
	Input pins	Fixed		
	Output pins	Open		
Operating condition (Oscillation circuit)	System clock (fsys/fsysm)	160MHz/80MHz		Stop
	External high-speed oscillator (EHOSC)	Oscillation		Stop
	Internal high-speed oscillator (IHOSC1)	Stop		
	PLL	Run		Stop

Table 7.4 I_{DD} Measurement Condition (CPU, Peripheral)

Peripheral	Unit number	NORMAL	IDLE	STOP1
CPU	1	Run (DhrystoneVer.2.1)	Stop	
DMAC	1	(Request from UARTch0, ch2: TX source: RAM)	Stop	
ADC	2	Run (0.6µs, continuous conversion)	Stop	
T32A	5	All ch: Run	Stop	
A-PMD	2	All ch: Run	Stop	
A-ENC32	2	Run	Stop	
SIWDT	1	Run	Stop	
UART	5	3ch: Transmission (1.25Mbps)	Stop	
EI2C	2	Stop		
TSPI	4	2ch: Transmission (10MHz)	Stop	
CRC	1	Stop		
RAMP	2	Run	Stop	
LVD	1	Stop		
OFD	1	Run	Stop	
Debug	1	Stop		
Input/Output Port	-	Run	Stop	

Ta= -40 to 85°C

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Power consumption (Includes VREF current)	I_{AVDD}	AVDD5=5.0V (Typ,), 5.5V (Max), AVSS=0V ADC 2 unit operation	-	10	13	mA

7.4. 12-bit AD Converter Characteristics

DVDD5=AVDD5=4.5V to 5.5V
DVSS=AVSS=0V
Ta= -40 to 85°C

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Analog reference voltage (+)	VREFH	-	4.5	-	AVDD5	V
Analog input voltage	V_{AIN}	-	VREFL	-	VREFH	
Difference between analog power supply and reference voltage	Δ VREF	VREFH ≤ AVDD5	0	-	0.5	
Integral nonlinear error (INL)	-	1 unit operation 4.5V ≤ AVDD5 ≤ 5.5V 4.5V ≤ VREFH ≤ 5.5V AVSS = VREFL = 0V AIN load resistor = 600 Ω AIN load capacity ≥ 0.1μF	-5	-	5	LSB
Differential nonlinear error (DNL)			-2	-	3	
Zero-scale error			-4	-	5	
Full-scale error			-5	-	4	
Total errors			-7	-	5	
SCLK frequency	f_{SCLK}	4.5V ≤ AVDD5 ≤ 5.5V	4	-	40	MHz
Sampling time	t_{smpl}	-	0.2	-	-	μs
Conversion time	t_{conv}	4.5V ≤ AVDD5 ≤ 5.5V SCLK = 40MHz	0.6	-	-	
Stable time	t_{sta}	After set ***[ADxMOD0]***<DACON> is "1".	3	-	-	

Note1: 1LSB = (VREFH - VREFL) / 4096 [V]

Note2: The characteristic when single AD converter operates.

DVDD5=AVDD5=4.5V to 5.5V
DVSS=AVSS=0V
Ta= -40 to 85°C

Parameter	Conditions	Min	Typ.	Max	Unit
Reference power supply voltage	Unit A: ch26 selected Unit B: ch25 selected	0.99	-	1.21	V

7.5. Power Supply Voltage Fluctuation

DVSS=AVSS=0V
Ta= -40 to 85°C

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Power gradient	V_{PON}	Rising slope at power-on	0.3	-	100	mV/µs
	V_{POFF}	Falling slope at power-off	-	-	10	
Power supply fluctuation rate	V_{fr}	4.5V ≤ DVDD5 = AVDD5 ≤ 5.5V	-50	-	50	

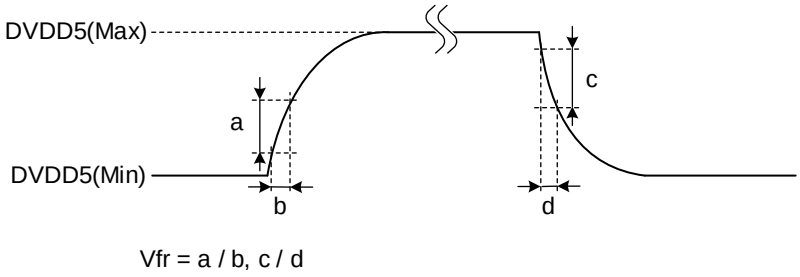


Figure 7.1 Power Supply Fluctuation Rate

7.6. Characteristics of Internal Processing at RESET

DVSS=AVSS=0V
Ta= -40 to 85°C

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Internal initialized time	t_{IINIT}	Power on	-	-	1.92	ms
Internal processing time for Reset	t_{IRST}	-	0.15	-	1.13	
Waiting time till CPU running (Note)	t_{CPUWT}	Power on Reset operation by LVD in STOP1 mode Reset operation by RESET_N pin in STOP1 mode	12	-	15	µs
		Reset operation by LVD in NORMAL or IDLE mode Reset operation by RESET_N pin in NORMAL or IDLE mode Reset operation by SIWDT, OFD, LOCKUP, or SYSRESET in NORMAL or IDLE mode	143	-	148	

Note: Except reset operation by SIWDT, OFD, LOCKUP, or SYSRESET, when reset factor repeats, t_{CPUWT} (Waiting time till CPU running) starts measuring elapse time after releasing this factor.

7.7. Characteristics of Power-on Reset

DVSS=AVSS=0V
Ta= -40 to 85°C

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Release voltage	V_{PREL}	Power increases	2.22	2.33	2.44	V
Detection voltage	V_{PDET}	Power decreases	2.17	2.28	2.39	
Detection pulse width 1	T_{PDET1}	-	200	-	-	μs

7.8. Characteristics of PORF

DVSS=AVSS=0V
Ta= -40 to 85°C

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Release voltage	V_{PORFL}	Power increases	2.57	2.64	2.71	V
Detection voltage	V_{PORFD}	Power decreases	2.52	2.59	2.66	
Detection pulse width 2	T_{PDET2}	-	200	-	-	μs

7.9. Characteristics of Voltage Detection Circuit

DVDD5=AVDD5=4.5V to 5.5V
DVSS=AVSS=0V
Ta= -40 to 85°C

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Detection/release voltage	V_{LVL0}	Power increases	3.96	4.05	4.14	V
		Power decreases	3.91	4.0	4.09	
	V_{LVL1}	Power increases	4.16	4.25	4.34	V
		Power decreases	4.11	4.2	4.29	
	V_{LVL2}	Power increases	4.36	4.45	4.54	V
		Power decreases	4.31	4.4	4.49	
	V_{LVL3}	Power increases	4.56	4.65	4.74	V
		Power decreases	4.51	4.6	4.69	
Detection response time	t_{VDDT1}	Power decreases	-	-	100	μs
Release delay time	t_{VDDT2}	Power increases	-	-	100	
Setup time	t_{LVDEN}	-	-	-	100	
Detection Minimum pulse width	t_{LVDPW}	-	200	-	-	

7.10. AC Electrical Characteristics

The values shown in the "AC Electrical Characteristics" of this chapter do not include clock errors.
In practice, the AC characteristics can be affected by both errors (a) and (b).

(a) Oscillation frequency error of the clock used as fosc
(b) PLL error (maximum ±3%)

7.10.1. Serial Peripheral Interface (TSPI)

7.10.1.1. Conditions

The AC characteristics are as follows:

- DVDD5=AVDD5= 4.5 to 5.5 V
- Ta = -40 to 85°C
- Input/output level: High = 0.5 × DVDD5, Low = 0.5 × DVDD5
- Load capacity: CL = 30pF

7.10.1.2. AC Electrical Characteristics

"T" indicates an operation clock cycle of the TSPI. This operation clock has the same cycle of the system clock (fsysm). This cycle depends on the clock gear setting.
The number of cycles can be 1 to 16. It is specified with TSPIxSCK. The value of "k1" is specified with ***[TSPIxFMTR0]***<CSSCKDL[3:0]>; the value of "k2" is specified with ***[TSPIxFMTR0]***<SCKCSDL[3:0]>. These values are 1 to 16. The value of k3 is the value specified with ***[TSPIxCR2]***<RXDLY[2:0]> plus 1. These values are 1 to 8.

(1) Master in SPI mode

Parameter	Symbol	Min	Max	Unit
TSPIxSCK output frequency	f_{CYC}	-	20	MHz
TSPIxSCK output cycle	t_{CYC}	50	-	ns
TSPIxSCK low level output pulse width	t_{WL}	(t_{CYC} / 2) - 13	-	
TSPIxSCK high level output pulse width	t_{WH}	(t_{CYC} / 2) - 13	-	
TSPIxCSn output ← TSPIxSCK rise/fall time	t_{CSU}	(t_{CYC} × k1) - 20	(t_{CYC} × k1) + 9	
TSPIxSCK rise/fall → TSPIxCSn hold time	t_{CHD}	(t_{CYC} × (k2 + 0.5)) - 20	-	
TSPIxRXD Input ← TSPIxSCK rise/fall time	t_{DSU}	35 - k3 × T	-	
TSPIxSCK rise/fall → TSPIxRXD hold time	t_{DHD}	k3 × T - 8.5	-	
TSPIxSCK rise/fall → TSPIxTXD hold time	t_{ODLY1}	-18	-	
TSPIxSCK rise/fall → TSPIxTXD delay time	t_{ODLY2}	-	16	
TSPIxCSn fall → TSPIxTXD delay time	t_{ODLY3}	(t_{CYC} × (k1 - 0.5)) - 25	(t_{CYC} × (k1 - 0.5)) + 6	

(2) Slave in SPI mode

Parameter	Symbol	Min	Max	Unit
TSPIxSCK Input frequency	f_{CYC}	-	15	MHz
TSPIxSCK Input cycle	t_{CYC}	66.6	-	ns
TSPIxSCK low level Input pulse width	t_{WL}	20.3	-	
TSPIxSCK high level Input pulse width	t_{WH}	20.3	-	
TSPIxCSIN Input (1st) ← TSPIxSCK rise/fall time	t_{CSU1}	170	-	
TSPIxCSIN Input (2nd) ← TSPIxSCK rise/fall time	t_{CSU2}	80	-	
TSPIxSCK rise/fall → TSPIxCSIN hold time (1st)	t_{CHD}	80	-	
TSPIxSCK rise/fall → TSPIxCSIN hold time (2nd)	t_{CHD}	7	-	
TSPIxRXD Input ← TSPIxSCK rise/fall time	t_{DSU}	7	-	
TSPIxSCK rise/fall → TSPIxRXD hold time	t_{DHD}	10	-	
TSPIxSCK rise/fall → TSPIxTXD hold time	t_{ODLY1}	0	-	
TSPIxSCK rise/fall → TSPIxTXD delay time	t_{ODLY2}	-	30	
TSPIxCSIN fall → TSPIxTXD delay time	t_{ODLY3}	-	55	
TSPIxCSIN high level input pulse width (1st)	t_{WDIS}	T × 5 + 20	-	
TSPIxCSIN high level input pulse width (2nd)	t_{WDIS}	T × 2 + 20	-	

(3) Master in SIO Mode

Parameter	Symbol	Min	Max	Unit
TSPIxSCK output frequency	f_{CYC}	-	20	MHz
TSPIxSCK output cycle	t_{CYC}	50	-	ns
TSPIxSCK low-level output pulse width	t_{WL}	(t_{CYC} / 2) - 13	-	
TSPIxSCK high-level output pulse width	t_{WH}	(t_{CYC} / 2) - 13	-	
TSPIxRXD input ← TSPIxSCK rise/fall time	t_{DSU}	35 - k3 × T	-	
TSPIxSCK rise/fall → TSPIxRXD hold time	t_{DHD}	k3 × T - 8.5	-	
TSPIxSCK rise/ fall → TSPIxTXD hold time	t_{ODLY1}	-18	-	
TSPIxSCK Rise/ fall → TSPIxTXD delay time	t_{ODLY2}	-	16	

(4) Slave in SIO mode

Parameter	Symbol	Min	Max	Unit
TSPIxSCK input frequency	f_{CYC}	-	15	MHz
TSPIxSCK input cycle	t_{CYC}	66.6	-	ns
TSPIxSCK low-level input pulse width	t_{WL}	20.3	-	
TSPIxSCK high-level input pulse width	t_{WH}	20.3	-	
TSPIxSCK rise/fall → TSPIxCSIN hold time	t_{CHD}	7	-	
TSPIxRXD Input ← TSPIxSCK rise/fall time	t_{DSU}	7	-	
TSPIxSCK rise/fall → TSPIxRXD hold time	t_{DHD}	10	-	
TSPIxSCK rise/fall → TSPIxTXD hold time	t_{ODLY1}	0	-	
TSPIxSCK rise/fall → TSPIxTXD delay time	t_{ODLY2}	-	38	

(1) 1st Clock Edge Sampling (Master)

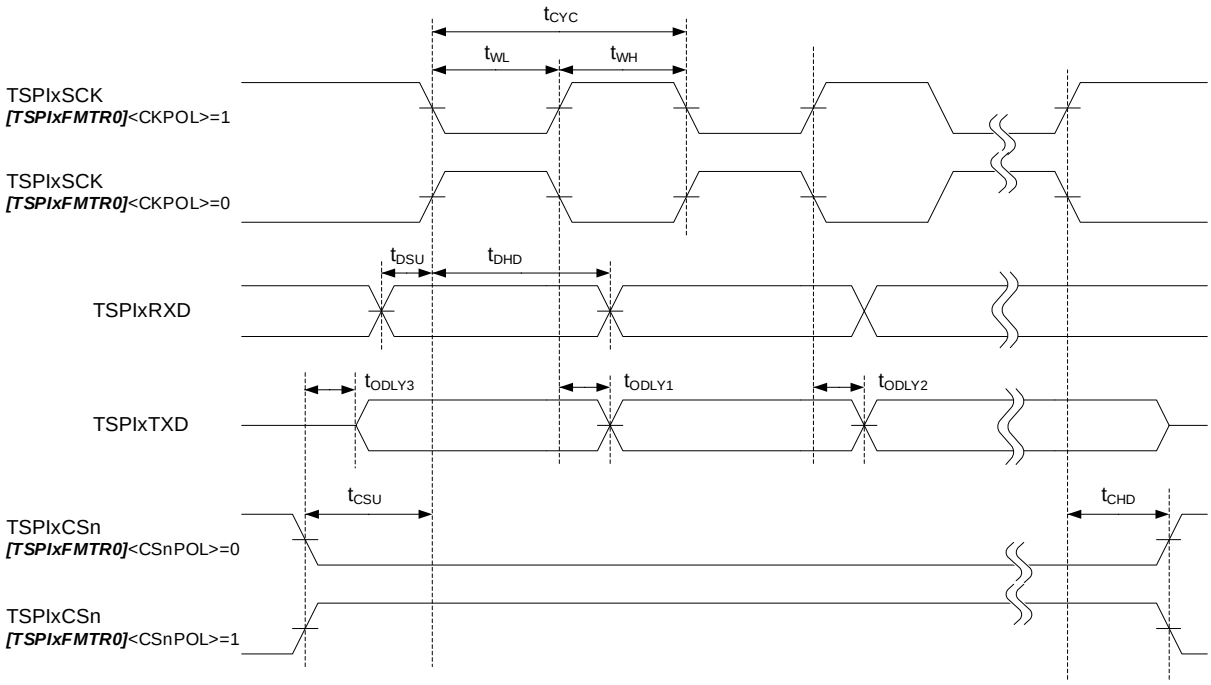


Figure 7.2 1st Clock Edge Sampling (Master)

(2) 2nd Clock Edge Sampling (Master)

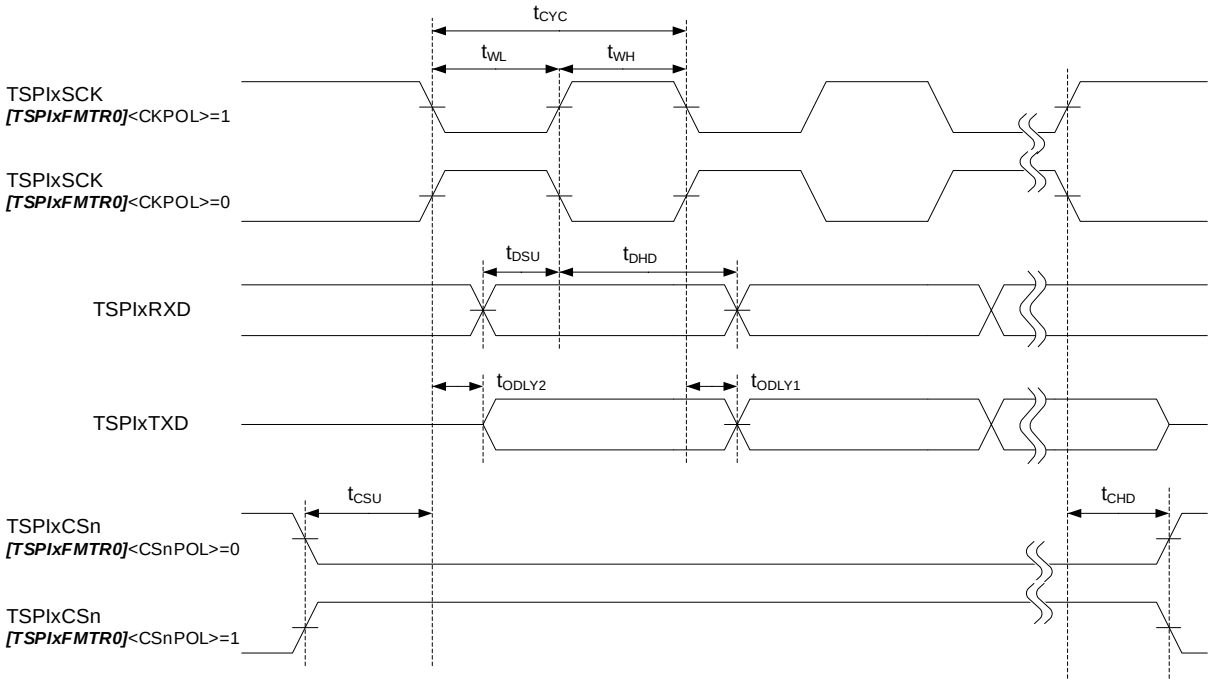


Figure 7.3 2nd Clock Edge Sampling (Master)

(3) 1st Clock Edge Sampling (slave)

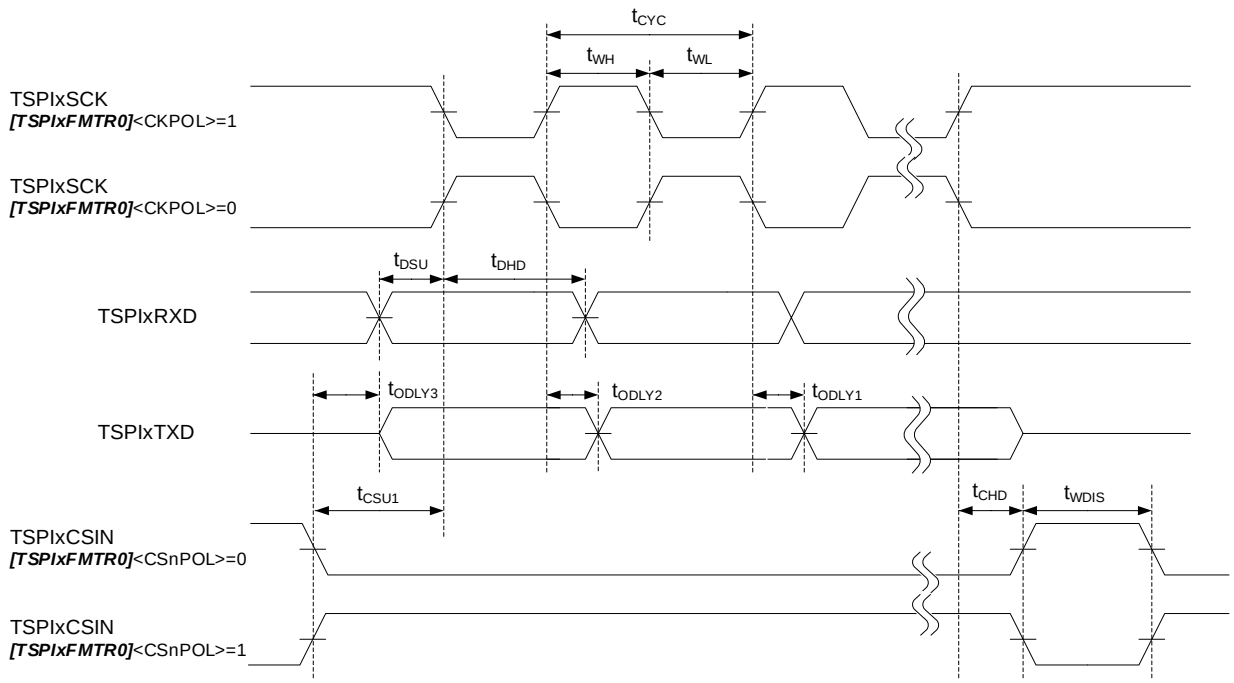


Figure 7.4 1st Clock Edge Sampling (Slave)

(4) 2nd Clock Edge Sampling (slave)

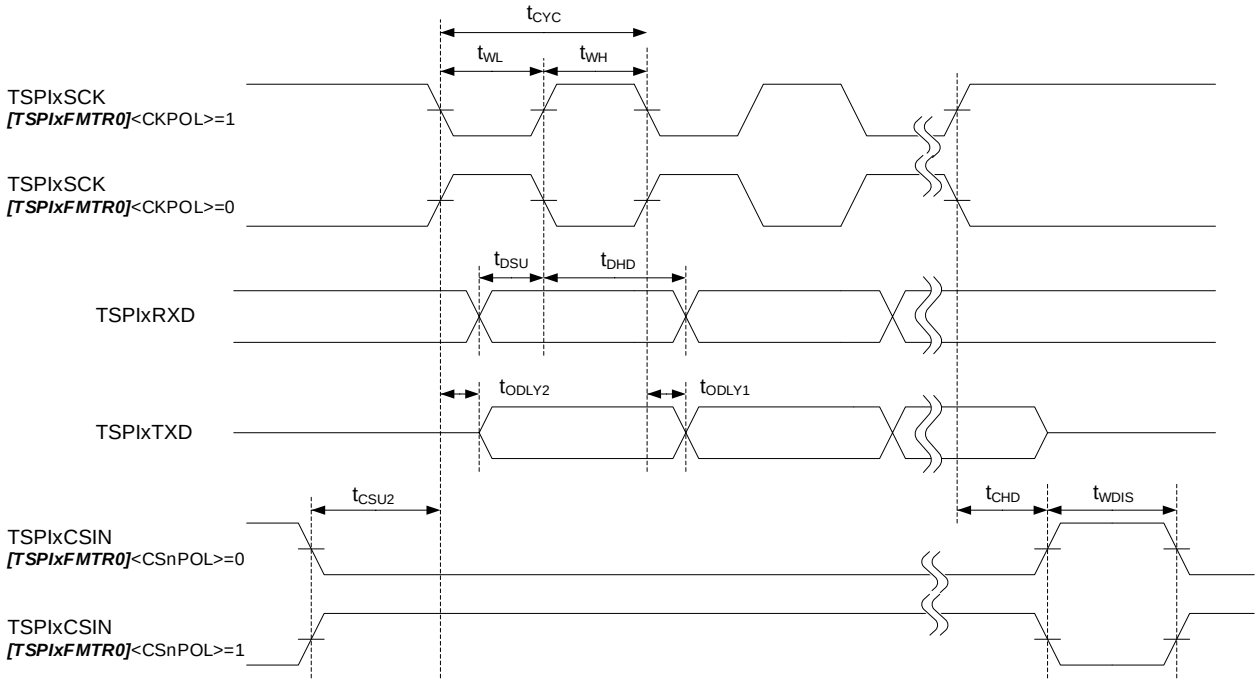


Figure 7.5 2nd Clock Edge Sampling (Slave)

7.10.2. I²C Interface Version A (EI2C)

7.10.2.1. Conditions

The AC characteristics are as follows:

- DVDD5=AVDD5= 4.5 to 5.5 V
- Ta = -40 to 85°C
- Output level: Low = 0.4V
- Input level: High = 0.7 × DVDD5, Low = 0.3 × DVDD5
- Load capacity: CL = 30pF
- External pull-up resistor: Rp = 2.2 kΩ

7.10.2.2. AC Electrical Characteristics

Parameter	Symbol	Standard-mode		Fast-mode		Fast-mode Plus		Unit
		Min	Max	Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	0	100	0	400	0	1000	kHz
Start condition hold time	$t_{HD;STA}$	4.0	-	0.6	-	0.26	-	μs
SCL clock Low width (Input) (Note1)	t_{LOW}	4.7	-	1.3	-	0.5	-	
SCL clock High width (Input) (Note1)	t_{HIGH}	4.0	-	0.6	-	0.26	-	
Re-start condition setup time	$t_{SU;STA}$	4.7	-	0.6	-	0.26	-	
Data hold time (Input) (Note2)	$t_{HD;DAT}$	0	-	0	-	0	-	
Data setup time	$t_{SU;DAT}$	250	-	100	-	50	-	ns
Stop condition setup time	$t_{SU;STO}$	4.0	-	0.6	-	0.26	-	μs
Bus free time between stop condition and start condition (Note3)	t_{BUF}	4.7	-	1.3	-	0.5	-	

Note1: On I²C bus standard, the maximum speed of Standard-mode/Fast-mode/Fast-mode Plus is 100kHz/400 kHz/1000kHz, respectively. For the frequency setting of the internal SCL clock, refer to the calculation formula in chapter 3.3.1 of "I²C Interface Version A" in reference manual .

Note2: On I²C bus standard, it is described that a data internal hold time should be set at least 300 ns to avoid unstable condition on the falling of the SCL when the SDA is input; however, this precaution is not supported in this MCU. Also, the edge slope control function for the SCL is not available. Therefore, when the customer designs the MCU, make sure to follow the data hold time (input) in the table above. Note that t_r/t_f on the SCL/SDA should be included in the data hold time.

Note3: To keep the time by software.

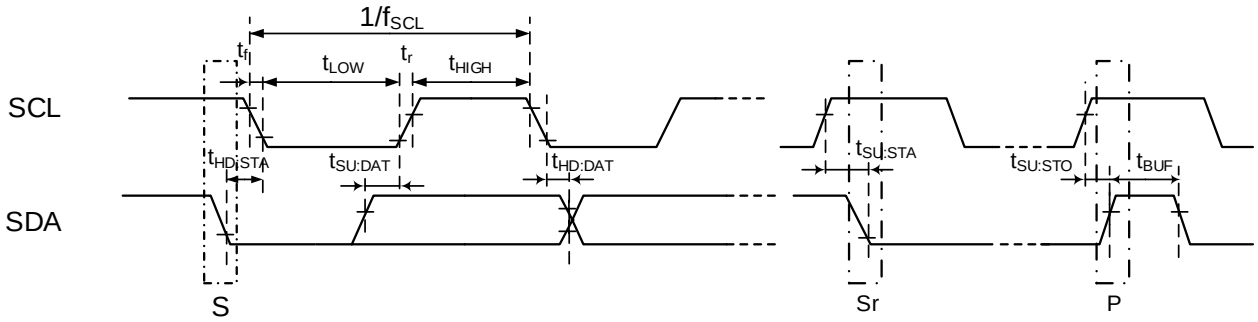


Figure 7.6 AC Timing of EI2C

7.10.3. 32-bit Timer Event Counter (T32A)

This section describes AC characteristics of T32AxINA0, T32AxINB0, and T32AxINC0.

7.10.3.1. Conditions

The AC characteristics are as follows:

- DVDD5=AVDD5= 4.5 to 5.5 V
- Ta = -40 to 85°C
- Input level: High = 0.5 × DVDD5, Low = 0.25 × DVDD5

7.10.3.2. AC Electrical Characteristics

"T" in the table below indicates the operation clock cycle of the T32A. The operation clock of the T32A is the same cycle as the ΦT0m clock. This cycle is depending on the prescaler clock setting.

(1) Operation other than the pulse count

Parameter	Symbol	Min	Max	Unit
Low-level pulse width	t_{VCKL}	2T + 20	-	ns
High-level pulse width	t_{VCKH}	2T + 20	-	

(2) At the pulse count

Parameter	Symbol	Min	Max	Unit
Pulse cycle	t_{DCYC}	1000	-	ns
Low-level pulse width	t_{PWL}	500	-	
High-level pulse width	t_{PWH}	500	-	

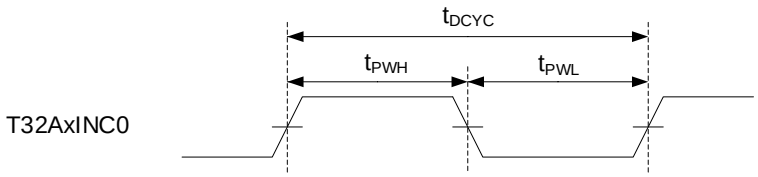


Figure 7.7 Count Pulse Input

7.10.4. External Interrupt

7.10.4.1. Conditions

The AC characteristics are as follows:

- DVDD5=AVDD5= 4.5V to 5.5V
- Ta = -40 to 85°C
- Input level: High = 0.5 × DVDD5, Low = 0.5 × DVDD5

7.10.4.2. AC Electrical Characteristics

"T" in the table below indicates the cycle of the system clock (fsys).

(1) NORMAL, IDLE mode

Parameter	Symbol	Min	Max	Unit
Low-level pulse width	t_{INTAL1}	T + 100	-	ns
High-level pulse width	t_{INTAH1}	T + 100	-	

(2) STOP1 mode

Parameter	Symbol	Min	Max	Unit
Low-level pulse width	t_{INTCL2}	125	-	ns
High-level pulse width	t_{INTCH2}	125	-	

7.10.5. Debug Communication

7.10.5.1. Conditions

The AC characteristics are as follows:

- DVDD5=AVDD5= 4.5V to 5.5V
- Ta = -40 to 85°C
- Input/output level: High = 0.5 × DVDD5, Low = 0.5 × DVDD5
- Load capacity: CL = 30pF

7.10.5.2. SWD Interface

Parameter	Symbol	Min	Max	Unit
High-level pulse width of CLK	t_{dckh}	50	-	ns
Low-level pulse width of CLK	t_{dckl}	50	-	
Output data hold from on the rising edge of CLK	t_{d1}	1	-	
Output data valid from on the rising edge of CLK	t_{d2}	-	35	
From input data valid to the rising edge of CLK	t_{ds}	20	-	
Input data hold from on the rising edge of CLK	t_{dh}	15	-	

7.10.5.3. JTAG Interface

Parameter	Symbol	Min	Max	Unit
High-level pulse width of CLK	t_{dckh}	50	-	ns
Low-level pulse width of CLK	t_{dckl}	50	-	
Output data hold from on the rising edge of CLK	t_{d3}	0	-	
Output data valid from on the rising edge of CLK	t_{d4}	-	35	
From input data valid to the rising edge of CLK	t_{ds}	20	-	
Input data hold from on the rising edge of CLK	t_{dh}	15	-	

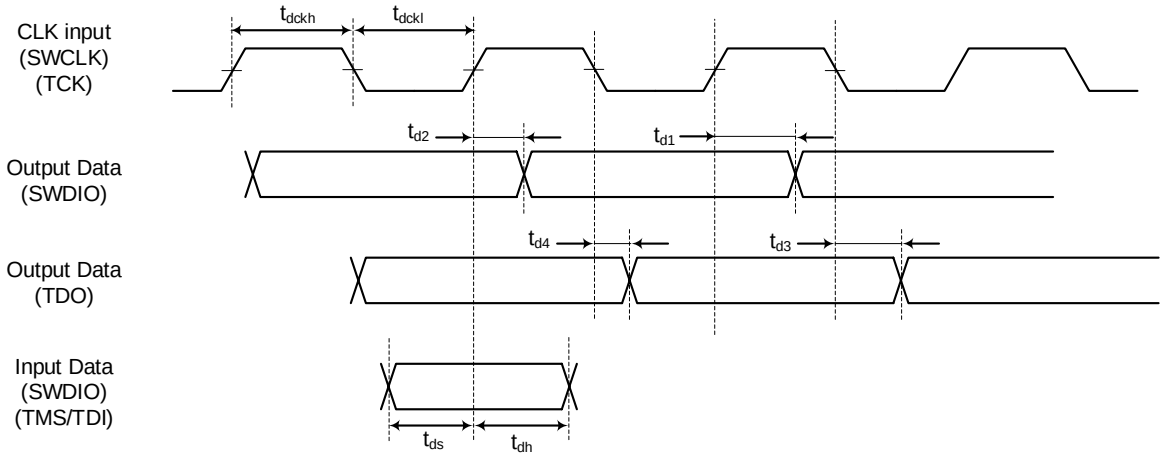


Figure 7.8 JTAG/SW Waveform

7.10.5.4. ETM Trace

Parameter	Symbol	Min	Max	Unit
TRACECLK cycle	t_{tclk}	25	-	ns
Data valid from rising on TRACECLK	t_{setupr}	2	-	
TRACEDATA hold from on the rising edge of TRACECLK	t_{holdr}	1	-	
TRACEDATA valid from on the falling edge of TRACECLK	t_{setupf}	2	-	
TRACEDATA hold from on the falling edge of TRACECLK	t_{holdf}	1	-	

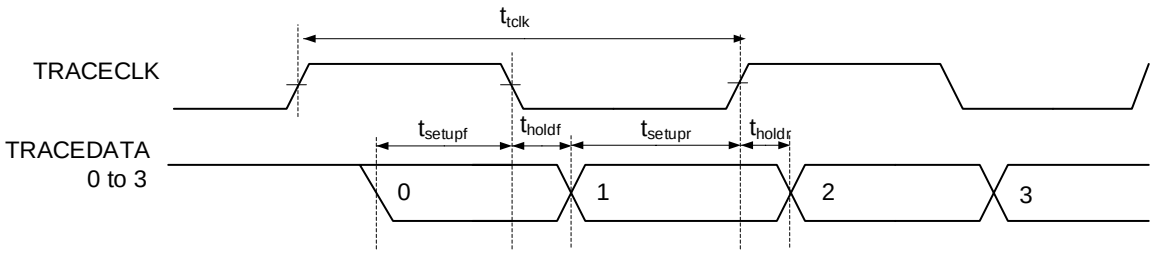


Figure 7.9 Trace Signal Waveform

7.10.6. Noise Filter Characteristics

Parameter	Condition	Min	Typ.	Max	Unit
Noise cancel width	DVDD5 = 4.5 to 5.5V Ta = -40 to 85°C	15	30	60	ns

7.10.7. External Clock Input

7.10.7.1. Conditions

The AC characteristics are as follows:

- DVDD5=AVDD5= 4.5V to 5.5V
- Ta = -40 to 85°C
- Input level: High = 0.75 × DVDD5, Low = 0.25 × DVDD5

7.10.7.2. AC Electrical Characteristics

Parameter	Symbol	Min	Typ.	Max	Unit
Clock frequency (1/$t_{EHCLKIN}$)	$f_{EHCLKIN}$	6	-	10	MHz
Clock duty	-	45	-	55	%
Clock rise time	t_r	-	-	10	ns
Clock fall time	t_f	-	-	10	ns

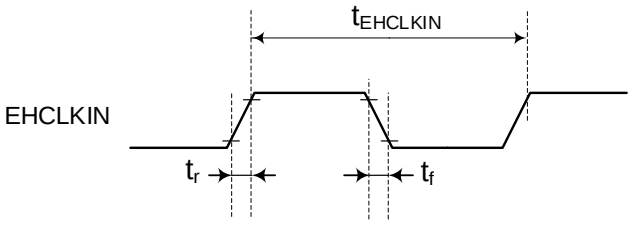


Figure 7.10 External Clock Input Waveform

7.11. Flash Memory Characteristics

7.11.1. Code Flash

DVDD5=4.5V to 5.5V
Ta= -40 to 85°C

Parameter	Condition	Min	Typ.	Max	Unit
Endurance	-	-	-	100,000	cycles
Programming time	Word program time	-	22.6	-	μs
Erase time	Page erase time	1.1	-	4.2	ms
	Block erase time	8.4	-	33.6	
	Area erase time (Note)	-	9.1	-	

Note: No block with effective protection

7.11.2. Chip Erase

DVDD5=4.5V to 5.5V
Ta= -40 to 85°C

Parameter	Condition	Min	Typ.	Max	Unit
Chip Erase time	Erasing of code flash, Protect bits (Code), and Security bits	20.3	-	26.5	ms

Note: Total execution time of automatic chip erasing, automatic protect bit erasing (code) and automatic security bit erasing. An execution time of automatic chip erasing is when no blocks are protected.

7.12. Regulator

DVDD5=4.5V to 5.5V
Ta= -40 to 85°C

Parameter	Condition	Min	Typ.	Max	Unit
Capacitance of REGOUT1 capacitor	-	0.8	4.7	5.64	μF
Capacitance of REGOUT2 capacitor		0.8	4.7	5.64	

7.13. Oscillation Circuit

7.13.1. Internal Oscillator

DVDD5=4.5V to 5.5V
Ta= -40 to 85°C

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Oscillation frequency	f_{IHOSC1}	-	9.9	10	10.1	MHz
	f_{IHOSC2}		9	10	11	

7.13.2. External Oscillator

DVDD5=4.5V to 5.5V
Ta= -40 to 85°C

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Oscillation frequency	f_{EHOSC}	-	6	-	24	MHz

Note1: Use in an environment where oscillation within 1% accuracy is always supplied.

Note2: Please contact the oscillator vendor, regarding the matching data of the device and the oscillator.

7.13.3. Oscillation Circuit

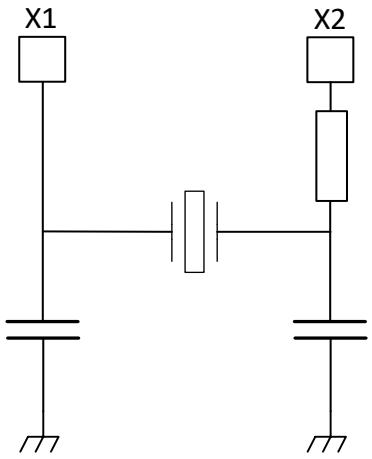


Figure 7.11 Oscillation Circuit Sample

To obtain a stable oscillation, load capacity and the position of the oscillator must be configured properly.

Since these factors are strongly affected by substrate patterns, please evaluate oscillation stability using the substrate you use.

This product has been evaluated by the oscillator vendor below. Please refer this information when selecting external parts.

7.13.4. Ceramic Resonator

This product has been evaluated by the ceramic resonator by Murata Manufacturing Co., Ltd.
Please refer to the company's website for details.

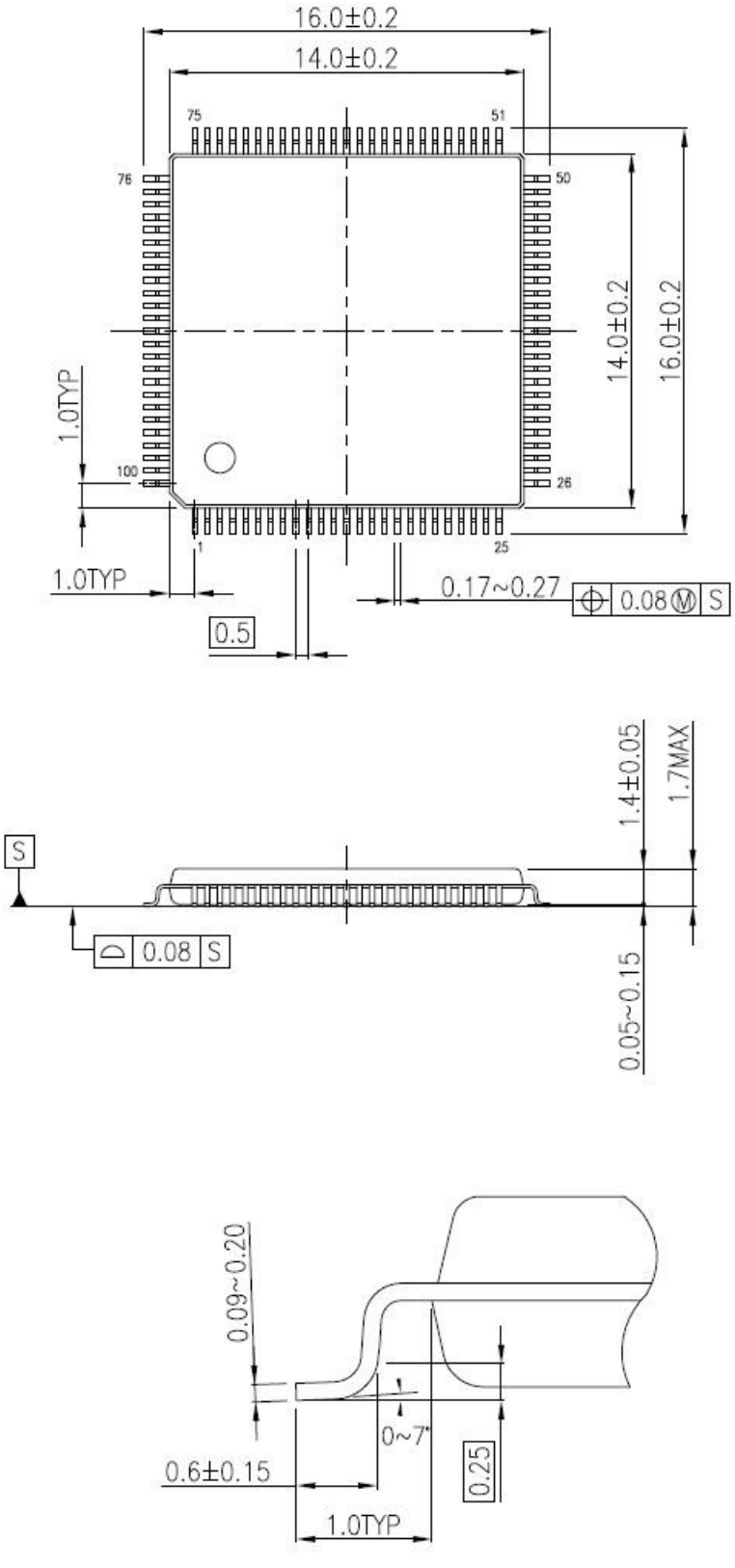
7.13.5. Precautions for Designing Printed Circuit Board

Be sure to design printed circuit board patterns that connect a resonator with other oscillation elements so that the length of such patterns become shortest possible to prevent deterioration of characteristics due to stray capacitances and wiring inductance. For multilayer circuit boards, it is important not to wire the ground and other signal patterns right beneath the oscillation circuit. For more information, please refer to the URL of the crystal unit vendor.

8. Package Dimensions

8.1. P-LQFP100-1414-0.50-002

Unit: mm



9. Precautions

This Page explains general precautions on the use of our MCUs.

Note that if there is a difference between the general precautions and the description in the body of the document, the description in the body of the document has higher priority.

(1) The MCUs' operation at power on

At power on, internal state of the MCUs is unstable. Therefore, state of the pins is undefined until reset operation is completed.

When a reset is performed by an external reset pin, pins of the MCUs that use the reset pin are undefined until reset operation by the external pin is completed.

Also, when a reset is performed by the internal power on reset, pins of the MCUs that use the internal power on reset are undefined until power supply voltage reaches the voltage at which power on reset is valid.

(2) Unused pins

Unused input/output ports of the MCUs are prohibited to use. The pins are high-impedance.

Generally, if MCUs operate while the high-impedance pins left open, electrostatic damage or latch-up may occur in the internal LSI due to induced voltage influenced from external noise.

We recommend that each unused pin should be connected to the power supply pins or GND pins via resistors.

(3) Clock oscillation stability

A reset state must be released after the clock oscillation becomes stable. If the clock is changed to another clock while the program is in progress, wait until the clock is stable.

10. Revision History

Table 10.1 Revision History

Revision	Date	Description
1.0	2024-08-30	- First release

Appendix
List of All Pins

Function A to C: These are the functions which become effective without setting up port function registers.
Function 1 to 7: These are the functions which become effective with setting up port function registers.

M471 QFP100	Pin Name	Function A	Function B	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Input/ Output	PU/PD	OD	SMT/ CMOS	Under reset	After reset
1	DVSSG										-	-	-	-	-	-
2	PA0		INT3				T32A00INA0	T32A00INC0			I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
3	PA1						T32A00OUTA	T32A00OUTC			I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
4	PA2		INT4			TSPI1CS0	T32A01INB0				I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
5	PA3					TSPI1CS1	T32A01OUTB				I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
6	PA4			UT1CTS_N	UT1RTS_N	TSPI1SCK					I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
7	PA5			UT1TXDA	UT1RXD	TSPI1TXD	T32A01OUTA	T32A01OUTC			I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
8	PA6			UT1RXD	UT1TXDA	TSPI1RXD	T32A01INA0	T32A01INC0			I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
9	PA7		INT8	UT1RTS_N	UT1CTS_N	TSPI1CSIN	T32A02INA0	T32A02INC0			I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
10	PE0			UT0TXDA	UT0RXD	TSPI0TXD	T32A02OUTB				I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
11	PE1			UT0RXD	UT0TXDA	TSPI0RXD	T32A02INB0				I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
12	PE2			UT0CTS_N	UT0RTS_N	TSPI0SCK					I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
13	PE3			UT0RTS_N	UT0CTS_N	TSPI0CSIN	T32A02OUTA	T32A02OUTC			I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
14	DVDD5A										-	-	-	-	-	-
15	PE4		INT5			TSPI0CS0	T32A03INA0	T32A03INC0			I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
16	PE5					TSPI0CS1	T32A03OUTA	T32A03OUTC			I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
17	PE6		INT6				T32A03INB0				I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
18	PE7		INT7				T32A03OUTB				I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
19	DVSSA										-	-	-	-	-	-
20	PL0		INTB								I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
21	PL1		INTA								I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
22	PC0								UO0		I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
23	PC1								XO0		I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
24	PC2								VO0		I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
25	PC3								YO0		I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
26	PC4								WO0		I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
27	PC5								ZO0		I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
28	PC6								EMG0		I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
29	PC7								OVV0		I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
30	PD0						T32A04INA0	T32A04INC0	ENC0A		I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
31	PD1					TSPI2CS0	T32A04OUTA	T32A04OUTC	ENC0B		I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
32	PD2					TSPI2CS1			ENC0Z		I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
33	PD3		INT9	UT2RTS_N	UT2CTS_N	TSPI2CSIN					I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
34	PD4			UT2CTS_N	UT2RTS_N	TSPI2SCK					I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
35	PD5			UT2TXDA	UT2RXD	TSPI2TXD					I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
36	PD6			UT2RXD	UT2TXDA	TSPI2RXD					I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
37	PG0								UO1		I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
38	PG1			UT4RTS_N	UT4CTS_N				XO1		I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
39	PG2			UT4CTS_N	UT4RTS_N				VO1		I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
40	DVDD5B										-	-	-	-	-	-
41	DVSSB										-	-	-	-	-	-
42	PG3			UT4TXDA	UT4RXD				YO1		I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
43	PG4			UT4RXD	UT4TXDA				WO1		I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
44	PG5								ZO1		I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
45	PG6								EMG1		I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
46	PG7								OVV1		I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
47	PR0	X1	EHCLKIN								Input	PD	-	SMT	Hi-Z	Hi-Z
48	DVSSE										-	-	-	-	-	-
49	PR1	X2									Input	PD	-	SMT	Hi-Z	Hi-Z
50	PF0	BOOT_N				TSPI3CSIN	T32A04INB0				I/O	PU/PD	YES	SMT	Hi-Z (Note1)	Hi-Z
51	PF1			UT3RTS_N	UT3CTS_N	TSPI3CS0	T32A04OUTB				I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
52	PF2			UT3CTS_N	UT3RTS_N	TSPI3SCK			ENC1A		I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
53	PF3			UT3TXDA	UT3RXD	TSPI3TXD			ENC1A		I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
54	PF4			UT3RXD	UT3TXDA	TSPI3RXD			ENC1A		I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
55	REGOUT1										-	-	-	-	-	-

M471 QFP100	Pin Name	Function A	Function B	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Input/ Output	PU/PD	OD	SMT/ CMOS	Under reset	After reset
56	DVSSC										-	-	-	-	-	-
57	MODE										Input	PD	-	SMT	-	-
58	DVDD5C										-	-	-	-	-	-
59	RESET_N										Input	PU	-	SMT	-	-
60	REGOUT2										-	-	-	-	-	-
61	DVDD5D										-	-	-	-	-	-
62	DVSSD										-	-	-	-	-	-
63	PB0					TSPI3CS1				TRACECLK	I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
64	PB1									TRACEDATA0	I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
65	PB2									TRACEDATA1	I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
66	PB3									TMS/SWDIO	I/O	PU/PD	YES	SMT	PU (Note2)	PU (Note2)
67	PB4									TCK/SWCLK	I/O	PU/PD	YES	SMT	PD (Note2)	PD (Note2)
68	PB5									TDO/SWV	I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
69	PB6									TDI	I/O	PU/PD	YES	SMT	PU (Note2)	PU (Note2)
70	PB7									TRST_N	I/O	PU/PD	YES	SMT	PU (Note2)	PU (Note2)
71	PK1		INTF			EI2C1SCL				TRACEDATA2	I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
72	PK0		INTE			EI2C1SDA				TRACEDATA3	I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
73	PJ7	AINB22	INTD								I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
74	PJ6	AINB21	INTC								I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
75	PJ5	AINB20									I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
76	PJ4	AINB19									I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
77	PJ3	AINB18									I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
78	PJ2	AINB17									I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
79	PJ1	AINB16									I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
80	PJ0	AINB15									I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
81	AVSS										-	-	-	-	-	-
82	AVDD5										-	-	-	-	-	-
83	PP3	AINA23/AINB14									I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
84	PP2	AINA22/AINB13									I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
85	PP1	AINA21/AINB12									I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
86	VREFL										-	-	-	-	-	-
87	VREFH										-	-	-	-	-	-
88	PP0	AINA20									I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
89	PH7	AINA19									I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
90	PH6	AINA18									I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
91	PH5	AINA17									I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
92	PH4	AINA16									I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
93	PH3	AINA15									I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
94	PH2	AINA14	INT2								I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
95	PH1	AINA13	INT1								I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
96	PH0	AINA12	INT0								I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
97	DVSSF										-	-	-	-	-	-
98	PN2						T32A00INB0				I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
99	PN1					EI2C0SCL	T32A00OUTB				I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z
100	PN0					EI2C0SDA					I/O	PU/PD	YES	SMT	Hi-Z	Hi-Z

Note1: When RESET_N pin is "Low", built-in pull-up resistor is enabled.

Note2: The initial value of built-in Pull-up/Pull-down resistor is effective.

RESTRICTIONS ON PRODUCT USE

Toshiba Corporation and its subsidiaries and affiliates are collectively referred to as “TOSHIBA”.
Hardware, software and systems described in this document are collectively referred to as “Product”.

- TOSHIBA reserves the right to make changes to the information in this document and related Product without notice.
- This document and any information herein may not be reproduced without prior written permission from TOSHIBA. Even with TOSHIBA's written permission, reproduction is permissible only if reproduction is without alteration/omission.
- Though TOSHIBA works continually to improve Product's quality and reliability, Product can malfunction or fail. Customers are responsible for complying with safety standards and for providing adequate designs and safeguards for their hardware, software and systems which minimize risk and avoid situations in which a malfunction or failure of Product could cause loss of human life, bodily injury or damage to property, including data loss or corruption. Before customers use the Product, create designs including the Product, or incorporate the Product into their own applications, customers must also refer to and comply with (a) the latest versions of all relevant TOSHIBA information, including without limitation, this document, the specifications, the data sheets and application notes for Product and the precautions and conditions set forth in the "TOSHIBA Semiconductor Reliability Handbook" and (b) the instructions for the application with which the Product will be used with or for. Customers are solely responsible for all aspects of their own product design or applications, including but not limited to (a) determining the appropriateness of the use of this Product in such design or applications; (b) evaluating and determining the applicability of any information contained in this document, or in charts, diagrams, programs, algorithms, sample application circuits, or any other referenced documents; and (c) validating all operating parameters for such designs and applications. **TOSHIBA ASSUMES NO LIABILITY FOR CUSTOMERS' PRODUCT DESIGN OR APPLICATIONS.**
- **PRODUCT IS NEITHER INTENDED NOR WARRANTED FOR USE IN EQUIPMENTS OR SYSTEMS THAT REQUIRE EXTRAORDINARILY HIGH LEVELS OF QUALITY AND/OR RELIABILITY, AND/OR A MALFUNCTION OR FAILURE OF WHICH MAY CAUSE LOSS OF HUMAN LIFE, BODILY INJURY, SERIOUS PROPERTY DAMAGE AND/OR SERIOUS PUBLIC IMPACT ("UNINTENDED USE").** Except for specific applications as expressly stated in this document, Unintended Use includes, without limitation, equipment used in nuclear facilities, equipment used in the aerospace industry, lifesaving and/or life supporting medical equipment, equipment used for automobiles, trains, ships and other transportation, traffic signaling equipment, equipment used to control combustions or explosions, safety devices, elevators and escalators, and devices related to power plant. **IF YOU USE PRODUCT FOR UNINTENDED USE, TOSHIBA ASSUMES NO LIABILITY FOR PRODUCT.** For details, please contact your TOSHIBA sales representative or contact us via our website.
- Do not disassemble, analyze, reverse-engineer, alter, modify, translate or copy Product, whether in whole or in part.
- Product shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable laws or regulations.
- The information contained herein is presented only as guidance for Product use. No responsibility is assumed by TOSHIBA for any infringement of patents or any other intellectual property rights of third parties that may result from the use of Product. No license to any intellectual property right is granted by this document, whether express or implied, by estoppel or otherwise.
- **ABSENT A WRITTEN SIGNED AGREEMENT, EXCEPT AS PROVIDED IN THE RELEVANT TERMS AND CONDITIONS OF SALE FOR PRODUCT, AND TO THE MAXIMUM EXTENT ALLOWABLE BY LAW, TOSHIBA (1) ASSUMES NO LIABILITY WHATSOEVER, INCLUDING WITHOUT LIMITATION, INDIRECT, CONSEQUENTIAL, SPECIAL, OR INCIDENTAL DAMAGES OR LOSS, INCLUDING WITHOUT LIMITATION, LOSS OF PROFITS, LOSS OF OPPORTUNITIES, BUSINESS INTERRUPTION AND LOSS OF DATA, AND (2) DISCLAIMS ANY AND ALL EXPRESS OR IMPLIED WARRANTIES AND CONDITIONS RELATED TO SALE, USE OF PRODUCT, OR INFORMATION, INCLUDING WARRANTIES OR CONDITIONS OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, ACCURACY OF INFORMATION, OR NONINFRINGEMENT.**
- Do not use or otherwise make available Product or related software or technology for any military purposes, including without limitation, for the design, development, use, stockpiling or manufacturing of nuclear, chemical, or biological weapons or missile technology products (mass destruction weapons). Product and related software and technology may be controlled under the applicable export laws and regulations including, without limitation, the Japanese Foreign Exchange and Foreign Trade Law and the U.S. Export Administration Regulations. Export and re-export of Product or related software or technology are strictly prohibited except in compliance with all applicable export laws and regulations.
- Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS compatibility of Product. Please use Product in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. **TOSHIBA ASSUMES NO LIABILITY FOR DAMAGES OR LOSSES OCCURRING AS A RESULT OF NONCOMPLIANCE WITH APPLICABLE LAWS AND REGULATIONS.**