32-bit RISC Microcontroller
TX Family
TMPM471F10FG

Reference Manual
Input/Output Ports
(PORT-TMPM471F10FG)

Revision 1.0

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Toshiba Electronic Devices & Storage Corporation

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Conventions

- Numeric formats follow the rules as shown below:
  Hexadecimal: 0xABC
  Decimal: 123 or 0d123 – Only when it needs to be explicitly shown that they are decimal numbers.
  Binary: 0b111 – It is possible to omit the "0b" when the number of bits can be distinctly understood from a sentence.
- "_N" is added to the end of signal names to indicate low active signals.
- It is called "assert" that a signal moves to its active level, "deassert" to its inactive level.
- When two or more signal names are referred, they are described like as [m: n].
  Example: S[3: 0] shows four signal names S3, S2, S1 and S0 together.
- The characters surrounded by ***[ ]*** defines the register.
  Example: ***[ABCD]***
- "n" substitutes suffix number of two or more same kind of registers, fields, and bit names.
  Example: ***[XYZ1], [XYZ2], [XYZ3] → [XYZn]***
- "x" substitutes suffix number or character of units and channels in the Register List.

  In case of unit, "x" means A, B, and C . . .
  Example: ***[ADACR0], [ADBCR0], [ADCCR0] → [ADxCR0]***
  In case of channel, "x" means 0, 1, and 2 . . .
  Example: ***[T32A0RUNA], [T32A1RUNA], [T32A2RUNA] → [T32AxRUNA]***
- The bit range of a register is written like as [m: n].
  Example: Bit[3: 0] expresses the range of bit 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.
  Example: ***[ABCD]***<EFG> = 0x01 (hexadecimal), ***[XYZn]***<VW> = 1 (binary)
- Word and Byte represent the following bit length.
  Byte: 8 bits
  Half word: 16 bits
  Word: 32 bits
  Double word: 64 bits
- Properties of each bit in a register are expressed as follows:
  R: Read only
  W: Write only
  R/W: Read and Write are possible
- Unless otherwise specified, register access supports only word access.
- The register defined as reserved must not be rewritten. Moreover, do not use the read value.
- The value read from the bit having default value of "-" is unknown.
- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value, In the cases that default is "-", follow the definition of each register.
- Reserved bits of the Write-only register should be written with their default value. In the cases that default is "-", follow the definition of each register.
- Do not use read-modified-write processing to the register of a definition which is different by writing and read out.

Terms and Abbreviations

Some of abbreviations used in this document are as follows:

I^2C	Inter-integrated circuit
JTAG	Joint test action group
SW	Serial wire

1. Outlines

It is described the register and setting of port. A list of the functions is indicated below.

Function classification	Function	Description
Port	-	Programmable pull-up/Programmable pull-down/Open-drain output are possible.
Peripheral function pins	External Interrupt	Interrupt pin has a noise filter (Filter width 30ns Typ.).
	32-bit timer event counter	Input capture input pin. Timer output pin.
	Serial peripheral interface	Chip select Input 1pin, chip select output 2pin, data input pin, data output pin, clock input/output pin
	Asynchronous serial communication circuit	Data input pin, data output pin, handshake function pins.
	I^2C interface version A	Data input/output pin, clock input/output pin
	Analog to digital converter	Analog input pin
	Advanced programmable motor control circuit	X/Y/Z phase output pins, U/V/W phase output pins, anomaly detection input pin, overvoltage detection input pin.
	Advanced encoder input circuit (32-bit)	Encoder input pin
Debug pins	JTAG	Test select input pin, serial clock input pin, serial data output pin, serial data input pin, test reset pin
	SW	Serial wire data input/output pin, serial wire clock input pin, serial wire viewer output pin
	Trace	Trace clock output pin, trace data output 4pins.
Control pins	Clock control	High-speed resonator connection pin, external high-speed clock input
	BOOT mode control	BOOT mode control pin

2. Function

2.1. Clock Supply

When PORT is used, the corresponding clock enable bits should be set to "1" (clock supply) in fsys supply stop register A (***[CGFSYSENA]*** and ***[CGFSYSMENA]***), fsys supply stop register B (***[CGFSYSMENB])***, and fc supply stop register (***[CGFCEN]***).

The corresponding registers and the bit locations depend on a product. Some products do not have all registers. For the details, refer to "Clock Control and Operation Mode" in Reference manual.

3. Signal Connection List

This table is sorted the function pins by the signal name of the block diagram which is described each reference manual. Register setting of the peripherals function is being explained in the port order, so please use for a reverse lookup of port name.

The numerical value shows the pin number.

Table 3.1 Signal Connection List: UART ch0, 1, 2, 3

Related reference manual	Function pin name	Port name	TMPM471F10FG (LQFP100)
Asynchronous serial communication circuit	UT0RXD	PE0	10
		PE1	11
	UT0TXDA	PE1	11
		PE0	10
	UT0CTS_N	PE2	12
		PE3	13
	UT0RTS_N	PE3	13
		PE2	12
	UT1RXD	PA5	7
		PA6	8
	UT1TXDA	PA6	8
		PA5	7
	UT1CTS_N	PA4	6
		PA7	9
	UT1RTS_N	PA7	9
		PA4	6
	UT2RXD	PD5	35
		PD6	36
	UT2TXDA	PD6	36
		PD5	35
	UT2CTS_N	PD3	33
		PD4	34
	UT2RTS_N	PD4	34
		PD3	33
	UT3RXD	PF3	53
		PF4	54
	UT3TXDA	PF4	54
		PF3	53
	UT3CTS_N	PF1	51
		PF2	52
	UT3RTS_N	PF2	52
		PF1	51

Table 3.2 Signal Connection List: UART ch4/EI2C/TSPI

Related reference manual	Function pin name	Port name	TMPM471F10FG (LQFP100)
Asynchronous serial communication circuit	UT4RXD	PG3	42
		PG4	43
	UT4TXDA	PG4	43
		PG3	42
	UT4CTS_N	PG1	38
		PG2	39
	UT4RTS_N	PG2	39
		PG1	38
I^2C interface version A	EI2C0SDA	PN0	100
	EI2C0SCL	PN1	99
	EI2C1SDA	PK0	72
	EI2C1SCL	PK1	71
Serial peripheral interface	TSPI0RXD	PE1	11
	TSPI0TXD	PE0	10
	TSPI0SCK	PE2	12
	TSPI0CSIN	PE3	13
	TSPI0CS0	PE4	15
	TSPI0CS1	PE5	16
	TSPI1RXD	PA6	8
	TSPI1TXD	PA5	7
	TSPI1SCK	PA4	6
	TSPI1CSIN	PA7	9
	TSPI1CS0	PA2	4
	TSPI1CS1	PA3	5
	TSPI2RXD	PD6	36
	TSPI2TXD	PD5	35
	TSPI2SCK	PD4	34
	TSPI2CSIN	PD3	33
	TSPI2CS0	PD1	31
	TSPI2CS1	PD2	32
	TSPI3RXD	PF4	54
	TSPI3TXD	PF3	53
	TSPI3SCK	PF2	52
	TSPI3CSIN	PF0	50
	TSPI3CS0	PF1	51
	TSPI3CS1	PB0	63

Table 3.3 Signal Connection List: T32A

Related reference manual	Function pin name	Port name	TMPM471F10FG (LQFP100)
32-bit timer event counter	T32A00INA0	PA0	2
	T32A00OUTA	PA1	3
	T32A00INB0	PN2	98
	T32A00OUTB	PN1	99
	T32A00INC0	PA0	2
	T32A00OUTC	PA1	3
	T32A01INA0	PA6	8
	T32A01OUTA	PA5	7
	T32A01INB0	PA2	4
	T32A01OUTB	PA3	5
	T32A01INC0	PA6	8
	T32A01OUTC	PA5	7
	T32A02INA0	PA7	9
	T32A02OUTA	PE3	13
	T32A02INB0	PE1	11
	T32A02OUTB	PE0	10
	T32A02INC0	PA7	9
	T32A02OUTC	PE3	13
	T32A03INA0	PE4	15
	T32A03OUTA	PE5	16
	T32A03INB0	PE6	17
	T32A03OUTB	PE7	18
	T32A03INC0	PE4	15
	T32A03OUTC	PE5	16
	T32A04INA0	PD0	30
	T32A04OUTA	PD1	31
	T32A04INB0	PF0	50
	T32A04OUTB	PF1	51
	T32A04INC0	PD0	30
	T32A04OUTC	PD1	31

Table 3.4 Signal Connection List: ADC

Related reference manual	Function pin name	Port name	TMPM471F10FG (LQFP100)
12-bit analog to digital converter	AINA12	PH0	96
	AINA13	PH1	95
	AINA14	PH2	94
	AINA15	PH3	93
	AINA16	PH4	92
	AINA17	PH5	91
	AINA18	PH6	90
	AINA19	PH7	89
	AINA20	PP0	88
	AINA21	PP1	85
	AINA22	PP2	84
	AINA23	PP3	83
	AINB12	PP1	85
	AINB13	PP2	84
	AINB14	PP3	83
	AINB15	PJ0	80
	AINB16	PJ1	79
	AINB17	PJ2	78
	AINB18	PJ3	77
	AINB19	PJ4	76
	AINB20	PJ5	75
	AINB21	PJ6	74
	AINB22	PJ7	73

Table 3.5 Signal Connection List: INT

Related reference manual	Function pin name	Port name	TMPM471F10FG (LQFP100)
Exception	INT0	PH0	96
	INT1	PH1	95
	INT2	PH2	94
	INT3	PA0	2
	INT4	PA2	4
	INT5	PE4	15
	INT6	PE6	17
	INT7	PE7	18
	INT8	PA7	9
	INT9	PD3	33
	INTA	PL1	21
	INTB	PL0	20
	INTC	PJ6	74
	INTD	PJ7	73
	INTE	PK0	72
	INTF	PK1	71

Table 3.6 Signal Connection List: A-PMD/A-ENC32

Related reference Manual	Function pin name	Port name	TMPM471F10FG (LQFP100)
Advanced programmable motor control circuit	EMG0	PC6	28
	OVV0	PC7	29
	UO0	PC0	22
	VO0	PC2	24
	WO0	PC4	26
	XO0	PC1	23
	YO0	PC3	25
	ZO0	PC5	27
	EMG1	PG6	45
	OVV1	PG7	46
	UO1	PG0	37
	VO1	PG2	39
	WO1	PG4	43
	XO1	PG1	38
	YO1	PG3	42
	ZO1	PG5	44
Advanced encoder input circuit (32-bit)	ENC0A	PD0	30
	ENC0B	PD1	31
	ENC0Z	PD2	32
	ENC1A	PF2	52
	ENC1B	PF3	53
	ENC1Z	PF4	54

Table 3.7 Signal Connection List: JTAG/SW/TRACE/Control Pin

Related reference manual	Function pin name	Port name	TMPM471F10FG (LQFP100)
Debug interface	TMS	PB3	66
	TCK	PB4	67
	TDO	PB5	68
	TDI	PB6	69
	TRST_N	PB7	70
	SWDIO	PB3	66
	SWCLK	PB4	67
	SWV	PB5	68
Debug interface (trace)	TRACECLK	PB0	63
	TRACEDATA0	PB1	64
	TRACEDATA1	PB2	65
	TRACEDATA2	PK1	71
	TRACEDATA3	PK0	72
Clock control and operation mode	X1	PR0	47
	EHCLKIN	PR0	47
	X2	PR1	49
Flash memory	BOOT_N	PF0	50

4. Registers

The following registers should be set appropriately to use the ports.

Each register is 32 bits. The configuration of the register depends on the port count and its function assignment.

"x" and "n" in the following table show a port name and a function number, respectively.

Register name		Type	Setting value	Description
[PxDATA]	Data register	R/W	0 or 1	Read from and write to a port.
[PxCR]	Output control register	R/W	0: Output disabled 1: Output enabled	Output control
[PxFRn]	Function register n	R/W	0: PORT 1: Function	Function setting. When 1 is set, the assigned function becomes available. Each function assigned to a port has its own function register. If multiple functions are assigned to one port, only one function should be enabled.
[PxOD]	Open-drain control register	R/W	0: CMOS 1: Open-drain	Programmable open-drain control. The programmable open-drain is a pseudo open- drain. An output buffer is disabled when the output data is 1, which is set by ***[PxOD]*** =1.
[PxPUP]	Pull-up control register	R/W	0: Pull-up disabled 1: Pull-up enabled	Programmable pull-up control.
[PxPDN]	Pull-down control register	R/W	0: Pull-down disabled 1: Pull-down enabled	Programmable pull-down control.
[PxIE]	Input control register	R/W	0: Input disabled 1: Input enabled	Input control. It takes 100ns (Max) that an external data is reflected on ***[PxDATA]*** after the ***[PxIE]*** is enabled.

4.1. List of Register

When the bit which is assigned to no functions is read, 0 is returned. The write to the bit is ignored.

Table 4.1 Ports Base Address

Peripheral function		Channel/Unit	Base address
Input/Output ports	PA	-	0x400E0000
	PB	-	0x400E0100
	PC	-	0x400E0200
	PD	-	0x400E0300
	PE	-	0x400E0400
	PF	-	0x400E0500
	PG	-	0x400E0600
	PH	-	0x400E0700
	PJ	-	0x400E0800
	PK	-	0x400E0900
	PL	-	0x400E0A00
	PN	-	0x400E0B00
	PP	-	0x400E0C00
	PR	-	0x400E0D00

Table 4.2 Register List

Register name	Address (Base+)	Port A	Port B	Port C	Port D	Port E	Port F
Data register	0x0000	***[PADATA]***	***[PBDATA]***	***[PCDATA]***	***[PDDATA]***	***[PEDATA]***	***[PFDATA]***
Output control register	0x0004	***[PACR]***	***[PBCR]***	***[PCCR]***	***[PDCR]***	***[PECR]***	***[PFCR]***
Function register 1	0x0008	***[PAFR1]***	-	-	***[PDFR1]***	***[PEFR1]***	***[PFFR1]***
Function register 2	0x000C	***[PAFR2]***	-	-	***[PDFR2]***	***[PEFR2]***	***[PFFR2]***
Function register 3	0x0010	***[PAFR3]***	***[PBFR3]***	-	***[PDFR3]***	***[PEFR3]***	***[PFFR3]***
Function register 4	0x0014	***[PAFR4]***	-	-	***[PDFR4]***	***[PEFR4]***	***[PFFR4]***
Function register 5	0x0018	***[PAFR5]***	-	-	***[PDFR5]***	***[PEFR5]***	-
Function register 6	0x001C	-	-	***[PCFR6]***	***[PDFR6]***	-	***[PFFR6]***
Function register 7	0x0020	-	***[PBFR7]***	-	-	-	-
Open-drain control register	0x0028	***[PAOD]***	***[PBOD]***	***[PCOD]***	***[PDOD]***	***[PEOD]***	***[PFOD]***
Pull-up control register	0x002C	***[PAPUP]***	***[PBPUP]***	***[PCPUP]***	***[PDPUP]***	***[PEPUP]***	***[PFPUP]***
Pull-down control register	0x0030	***[PAPDN]***	***[PBPDN]***	***[PCPDN]***	***[PDPDN]***	***[PEPDN]***	***[PFPDN]***
Input control register	0x0038	***[PAIE]***	***[PBIE]***	***[PCIE]***	***[PDIE]***	***[PEIE]***	***[PFIE]***

Register name	Address (Base+)	Port G	Port H	Port J	Port K	Port L	Port N
Data register	0x0000	***[PGDATA]***	***[PHDATA]***	***[PJDATA]***	***[PKDATA]***	***[PLDATA]***	***[PNDATA]***
Output control register	0x0004	***[PGCR]***	***[PHCR]***	***[PJCR]***	***[PKCR]***	***[PLCR]***	***[PNCR]***
Function register 1	0x0008	***[PGFR1]***	-	-	-	-	-
Function register 2	0x000C	***[PGFR2]***	-	-	-	-	-
Function register 3	0x0010	-	-	-	***[PKFR3]***	-	***[PNFR3]***
Function register 4	0x0014	-	-	-	-	-	***[PNFR4]***
Function register 5	0x0018	-	-	-	-	-	-
Function register 6	0x001C	***[PGFR6]***	-	-	-	-	-
Function register 7	0x0020	-	-	-	***[PKFR7]***	-	-
Open-drain control register	0x0028	***[PGOD]***	***[PHOD]***	***[PJOD]***	***[PKOD]***	***[PLOD]***	***[PNOD]***
Pull-up control register	0x002C	***[PGPUP]***	***[PHPUP]***	***[PJPUP]***	***[PKPUP]***	***[PLPUP]***	***[PNPUP]***
Pull-down control register	0x0030	***[PGPDN]***	***[PHPDN]***	***[PJPDN]***	***[PKPDN]***	***[PLPDN]***	***[PNPDN]***
Input control register	0x0038	***[PGIE]***	***[PHIE]***	***[PJIE]***	***[PKIE]***	***[PLIE]***	***[PNIE]***

Register name	Address (Base+)	Port P	Port R
Data register	0x0000	***[PPDATA]***	***[PRDATA]***
Output control register	0x0004	***[PPCR]***	-
Function register 1	0x0008	-	-
Function register 2	0x000C	-	-
Function register 3	0x0010	-	-
Function register 4	0x0014	-	-
Function register 5	0x0018	-	-
Function register 6	0x001C	-	-
Function register 7	0x0020	-	-
Open-drain control register	0x0028	***[PPOD]***	-
Pull-up control register	0x002C	***[PPPUP]***	-
Pull-down control register	0x0030	***[PPPDN]***	***[PRPDN]***
Input control register	0x0038	***[PPIE]***	***[PRIE]***

Note: Do not access the address described as "-".

4.2. List of Port Functions and Settings

It is explained about the viewpoint of a port register setting table.

The column of ***[PxFRn]*** shows the function register which should be set. When this register is set to "1", the corresponding function is enabled. (x is a port name and n is a function number.)

The bit in the N/A in the tables returns "0" when it is read. The write to the bit is ignored.

"0" or "1" in the tables shows the value which should be set. "0/1" means either value can be set.

PORT	Reset status / Function	Input/Output	PORT Type	Control register [PADATA]	[PACR]	[PAFRn]	[PAOD]	[PAPUP]	[PAPDN]	[PAIE]
PA0	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	TSPI0CSIN	Input	FTU1a	0/1	0	***[PAFR1]***	0/1	0/1	0/1	1
	T32A00INB0	Input	FTU1a	0/1	0	***[PAFR4]***	0/1	0/1	0/1	1
PA4	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT01a	Input	FTU4a	0/1	0	0	0/1	0/1	0/1	1
	TSPI0SCK	Input	FTU1a	0/1	0	***[PAFR1]***	0/1	0/1	0/1	1
		Output	FTU1a	0/1	1		0/1	0/1	0/1	0
	T32A00OUTB	Output	FTU1a	0/1	1	***[PAFR4]***	0/1	0/1	0/1	0
	TRGIN2	Input	FTU1a	0/1	0	***[PAFR7]***	0/1	0/1	0/1	1

[PxFRn]	Pin: TSPI0CSIN	T32A00INB0	TSPI0SCK	T32A00OUTB	TRGIN2	Input Port / Output Port
[PAFR1]<bit0>	1	0	0	0	0	0
[PAFR4]<bit0>	0	1	0	0	0	0
[PAFR1]<bit4>	0	0	1	0	0	0
[PAFR4]<bit4>	0	0	0	1	0	0
[PAFR7]<bit4>	0	0	0	0	1	0

4.2.1. Setting of Using Alternated Pin

To use the alternated pins as peripheral function output pins, set the peripheral function (***[PxFRn]***<bit m>=1) that uses the function register and enable output control register (***[PxCR]***<bit m>=1), and then set the peripheral functions. If output is enabled before setting the function register, the data register value of the port is output until the function register is set.

To use the alternated pins as input pins of the peripheral function, set the input control register of the port (***[PxIE]***<bit m>=1) and set the peripheral function that uses the function register (***[PxFRn]***<bit m>=1), and then set the peripheral functions.

To use peripheral functions such as I^2C, set the input control register of the port (***[PxIE]***<bit m>=1), set the peripheral function that uses the function register (***[PxFRn]***<bit m>=1) and set the output control register to output enable (***[PxCR]***<bit m>=1), and then set the peripheral function.

- When multiple functions are assigned same pin, please choose only one function for usage.
- When same function are assigned multiple pins, please the function use exclusively.

4.2.2. PORT A

Table 4.3 Port A Registers Setting

PORT	Reset status / Function	Input/Output	PORT type	Control register						
				[PADATA]	*[PACR]*	*[PAFRn]*	*[PAOD]*	*[PAPUP]*	*[PAPDN]*	*[PAIE]*
PA0	After reset	-	-	0	0	0	0	0	0	0
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	INT3	Input	FTU4a	0/1	0	0	0/1	0/1	0/1	1
	T32A00INA0	Input	FTU1a	0/1	0	***[PAFR4]***	0/1	0/1	0/1	1
	T32A00INC0	Input	FTU1a	0/1	0	***[PAFR5]***	0/1	0/1	0/1	1
PA1	After reset	-	-	0	0	0	0	0	0	0
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	T32A00OUTA	Output	FTU1a	0/1	1	***[PAFR4]***	0/1	0/1	0/1	0
	T32A00OUTC	Output	FTU1a	0/1	1	***[PAFR5]***	0/1	0/1	0/1	0
PA2	After reset	-	-	0	0	0	0	0	0	0
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	INT4	Input	FTU4a	0/1	0	0	0/1	0/1	0/1	1
	TSPI1CS0	Output	FTU1a	0/1	1	***[PAFR3]***	0/1	0/1	0/1	0
	T32A01INB0	Input	FTU1a	0/1	0	***[PAFR4]***	0/1	0/1	0/1	1
PA3	After reset	-	-	0	0	0	0	0	0	0
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	TSPI1CS1	Output	FTU1a	0/1	1	***[PAFR3]***	0/1	0/1	0/1	0
	T32A01OUTB	Output	FTU1a	0/1	1	***[PAFR4]***	0/1	0/1	0/1	0
PA4	After reset	-	-	0	0	0	0	0	0	0
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	UT1CTS_N	Input	FTU1a	0/1	0	***[PAFR1]***	0/1	0/1	0/1	1
	UT1RTS_N	Output	FTU1a	0/1	1	***[PAFR2]***	0/1	0/1	0/1	0
	TSPI1SCK	Input	FTU1a	0/1	0	***[PAFR3]***	0/1	0/1	0/1	1
		Output		0/1	1		0/1	0/1	0/1	0
PA5	After reset	-	-	0	0	0	0	0	0	0
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	UT1TXDA	Output	FTU1a	0/1	1	***[PAFR1]***	0/1	0/1	0/1	0
	UT1RXD	Input	FTU1a	0/1	0	***[PAFR2]***	0/1	0/1	0/1	1
	TSPI1TXD	Output	FTU2a	0/1	1	***[PAFR3]***	0/1	0/1	0/1	0
	T32A01OUTA	Output	FTU1a	0/1	1	***[PAFR4]***	0/1	0/1	0/1	0
	T32A01OUTC	Output	FTU1a	0/1	1	***[PAFR5]***	0/1	0/1	0/1	0
PA6	After reset	-	-	0	0	0	0	0	0	0
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	UT1RXD	Input	FTU1a	0/1	0	***[PAFR1]***	0/1	0/1	0/1	1
	UT1TXDA	Output	FTU1a	0/1	1	***[PAFR2]***	0/1	0/1	0/1	0
	TSPI1RXD	Input	FTU1a	0/1	0	***[PAFR3]***	0/1	0/1	0/1	1
	T32A01INA0	Input	FTU1a	0/1	0	***[PAFR4]***	0/1	0/1	0/1	1
	T32A01INC0	Input	FTU1a	0/1	0	***[PAFR5]***	0/1	0/1	0/1	1

PORT	Reset status / Function	Input/Output	PORT type	Control register						
				[PADATA]	*[PACR]*	*[PAFRn]*	*[PAOD]*	*[PAPUP]*	*[PAPDN]*	*[PAIE]*
PA7	After reset	-	-	0	0	0	0	0	0	0
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	INT8	Input	FTU4a	0/1	0	0	0/1	0/1	0/1	1
	UT1RTS_N	Output	FTU1a	0/1	1	***[PAFR1]***	0/1	0/1	0/1	0
	UT1CTS_N	Input	FTU1a	0/1	0	***[PAFR2]***	0/1	0/1	0/1	1
	TSPI1CSIN	Input	FTU1a	0/1	0	***[PAFR3]***	0/1	0/1	0/1	1
	T32A02INA0	Input	FTU1a	0/1	0	***[PAFR4]***	0/1	0/1	0/1	1
	T32A02INC0	Input	FTU1a	0/1	0	***[PAFR5]***	0/1	0/1	0/1	1

4.2.3. PORT B

Table 4.4 Port B Registers Setting

PORT	Reset status / Function	Input/Output	PORT type	Control register						
				[PADATA]	*[PACR]*	*[PAFRn]*	*[PAOD]*	*[PAPUP]*	*[PAPDN]*	*[PAIE]*
PB0	After reset	-	-	0	0	0	0	0	0	0
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	TSPI3CS1	Output	FTU1a	0/1	1	***[PBFR3]***	0/1	0/1	0/1	0
	TRACECLK	Output	FTU1a	0/1	1	***[PBFR7]***	0/1	0/1	0/1	0
PB1	After reset	-	-	0	0	0	0	0	0	0
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	TRACEDATA0	Output	FTU1a	0/1	1	***[PBFR7]***	0/1	0/1	0/1	0
PB2	After reset	-	-	0	0	0	0	0	0	0
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	TRACEDATA1	Output	FTU1a	0/1	1	***[PBFR7]***	0/1	0/1	0/1	0
PB3	After reset (TMS/SWDIO)	-	FTU2a	0	1 (Note)	***[PBFR7]***	0	1	0	1
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0
PB4	After reset (TCK/SWCLK)	-	FTU2a	0	0	***[PBFR7]***	0	0	1	1
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0
PB5	After reset (TDO/SWV)	-	FTU2a	0	1 (Note)	***[PBFR7]***	0	0	0	0
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0
PB6	After reset (TDI)	-	FTU2a	0	0	***[PBFR7]***	0	1	0	1
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0
PB7	After reset (TRST_N)	-	FTU3a	0	0	***[PBFR7]***	0	1	0	1
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0

Note: When receiving the command from TOOL, it becomes output.

4.2.4. PORT C

Table 4.5 Port C Registers Setting

PORT	Reset status / Function	Input/Output	PORT type	Control register						
				[PADATA]	*[PACR]*	*[PAFRn]*	*[PAOD]*	*[PAPUP]*	*[PAPDN]*	*[PAIE]*
PC0	After reset	-	-	0	0	0	0	0	0	0
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	UO0	Output	FTU2a	0/1	1	***[PCFR6]***	0/1	0/1	0/1	0
PC1	After reset	-	-	0	0	0	0	0	0	0
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	XO0	Output	FTU2a	0/1	1	***[PCFR6]***	0/1	0/1	0/1	0
PC2	After reset	-	-	0	0	0	0	0	0	0
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	VO0	Output	FTU2a	0/1	1	***[PCFR6]***	0/1	0/1	0/1	0
PC3	After reset	-	-	0	0	0	0	0	0	0
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	YO0	Output	FTU2a	0/1	1	***[PCFR6]***	0/1	0/1	0/1	0
PC4	After reset	-	-	0	0	0	0	0	0	0
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	WO0	Output	FTU2a	0/1	1	***[PCFR6]***	0/1	0/1	0/1	0
PC5	After reset	-	-	0	0	0	0	0	0	0
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	ZO0	Output	FTU2a	0/1	1	***[PCFR6]***	0/1	0/1	0/1	0
PC6	After reset	-	-	0	0	0	0	0	0	0
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	EMG0	Input	FTU1a	0/1	0	***[PCFR6]***	0/1	0/1	0/1	1
PC7	After reset	-	-	0	0	0	0	0	0	0
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	OVV0	Input	FTU1a	0/1	0	***[PCFR6]***	0/1	0/1	0/1	1

4.2.5. PORT D

Table 4.6 Port D Registers Setting

PORT	Reset status / Function	Input/Output	PORT type	Control register						
				[PADATA]	*[PACR]*	*[PAFRn]*	*[PAOD]*	*[PAPUP]*	*[PAPDN]*	*[PAIE]*
PD0	After reset	-	-	0	0	0	0	0	0	0
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	T32A04INA0	Input	FTU1a	0/1	0	***[PDFR4]***	0/1	0/1	0/1	1
	T32A04INC0	Input	FTU1a	0/1	0	***[PDFR5]***	0/1	0/1	0/1	1
	ENC0A	Input	FTU1a	0/1	0	***[PDFR6]***	0/1	0/1	0/1	1
PD1	After reset	-	-	0	0	0	0	0	0	0
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	TSPI2CS0	Output	FTU1a	0/1	1	***[PDFR3]***	0/1	0/1	0/1	0
	T32A04OUTA	Output	FTU1a	0/1	1	***[PDFR4]***	0/1	0/1	0/1	0
	T32A04OUTC	Output	FTU1a	0/1	1	***[PDFR5]***	0/1	0/1	0/1	0
	ENC0B	Input	FTU1a	0/1	0	***[PDFR6]***	0/1	0/1	0/1	1
PD2	After reset	-	-	0	0	0	0	0	0	0
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	TSPI2CS1	Output	FTU1a	0/1	1	***[PDFR3]***	0/1	0/1	0/1	0
	ENC0Z	Input	FTU1a	0/1	0	***[PDFR6]***	0/1	0/1	0/1	1
PD3	After reset	-	-	0	0	0	0	0	0	0
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	INT9	Input	FTU4a	0/1	0	0	0/1	0/1	0/1	1
	UT2RTS_N	Output	FTU1a	0/1	1	***[PDFR1]***	0/1	0/1	0/1	0
	UT2CTS_N	Input	FTU1a	0/1	0	***[PDFR2]***	0/1	0/1	0/1	1
	TSPI2CSIN	Input	FTU1a	0/1	0	***[PDFR3]***	0/1	0/1	0/1	1
PD4	After reset	-	-	0	0	0	0	0	0	0
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	UT2CTS_N	Input	FTU1a	0/1	0	***[PDFR1]***	0/1	0/1	0/1	1
	UT2RTS_N	Output	FTU1a	0/1	1	***[PDFR2]***	0/1	0/1	0/1	0
	TSPI2SCK	Input	FTU1a	0/1	0	***[PDFR3]***	0/1	0/1	0/1	1
		Output		0/1	1		0/1	0/1	0/1	0
PD5	After reset	-	-	0	0	0	0	0	0	0
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	UT2TXDA	Output	FTU1a	0/1	1	***[PDFR1]***	0/1	0/1	0/1	0
	UT2RXD	Input	FTU1a	0/1	0	***[PDFR2]***	0/1	0/1	0/1	1
	TSPI2TXD	Output	FTU2a	0/1	1	***[PDFR3]***	0/1	0/1	0/1	0
PD6	After reset	-	-	0	0	0	0	0	0	0
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	UT2RXD	Input	FTU1a	0/1	0	***[PDFR1]***	0/1	0/1	0/1	1
	UT2TXDA	Output	FTU1a	0/1	1	***[PDFR2]***	0/1	0/1	0/1	0
	TSPI2RXD	Input	FTU1a	0/1	0	***[PDFR3]***	0/1	0/1	0/1	1

4.2.6. PORT E

Table 4.7 Port E Registers Setting

PORT	Reset status / Function	Input/Output	PORT type	Control register						
				[PADATA]	*[PACR]*	*[PAFRn]*	*[PAOD]*	*[PAPUP]*	*[PAPDN]*	*[PAIE]*
PE0	After reset	-	-	0	0	0	0	0	0	0
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	UT0TXDA	Output	FTU1a	0/1	1	***[PEFR1]***	0/1	0/1	0/1	0
	UT0RXD	Input	FTU1a	0/1	0	***[PEFR2]***	0/1	0/1	0/1	1
	TSPI0TXD	Output	FTU2a	0/1	1	***[PEFR3]***	0/1	0/1	0/1	0
	T32A02OUTB	Output	FTU1a	0/1	1	***[PEFR4]***	0/1	0/1	0/1	0
PE1	After reset	-	-	0	0	0	0	0	0	0
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	UT0RXD	Input	FTU1a	0/1	0	***[PEFR1]***	0/1	0/1	0/1	1
	UT0TXDA	Output	FTU1a	0/1	1	***[PEFR2]***	0/1	0/1	0/1	0
	TSPI0RXD	Input	FTU1a	0/1	0	***[PEFR3]***	0/1	0/1	0/1	1
	T32A02INB0	Input	FTU1a	0/1	0	***[PEFR4]***	0/1	0/1	0/1	1
PE2	After reset	-	-	0	0	0	0	0	0	0
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	UT0CTS_N	Input	FTU1a	0/1	0	***[PEFR1]***	0/1	0/1	0/1	1
	UT0RTS_N	Output	FTU1a	0/1	1	***[PEFR2]***	0/1	0/1	0/1	0
	TSPI0SCK	Input	FTU1a	0/1	0	***[PEFR3]***	0/1	0/1	0/1	1
		Output		0/1	1		0/1	0/1	0/1	0
PE3	After reset	-	-	0	0	0	0	0	0	0
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	UT0RTS_N	Output	FTU1a	0/1	1	***[PEFR1]***	0/1	0/1	0/1	0
	UT0CTS_N	Input	FTU1a	0/1	0	***[PEFR2]***	0/1	0/1	0/1	1
	TSPI0CSIN	Input	FTU1a	0/1	0	***[PEFR3]***	0/1	0/1	0/1	1
	T32A02OUTA	Output	FTU1a	0/1	1	***[PEFR4]***	0/1	0/1	0/1	0
	T32A02OUTC	Output	FTU1a	0/1	1	***[PEFR5]***	0/1	0/1	0/1	0
PE4	After reset	-	-	0	0	0	0	0	0	0
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	INT5	Input	FTU4a	0/1	0	0	0/1	0/1	0/1	1
	TSPI0CS0	Output	FTU1a	0/1	1	***[PEFR3]***	0/1	0/1	0/1	0
	T32A03INA0	Input	FTU1a	0/1	0	***[PEFR4]***	0/1	0/1	0/1	1
	T32A03INC0	Input	FTU1a	0/1	0	***[PEFR5]***	0/1	0/1	0/1	1
PE5	After reset	-	-	0	0	0	0	0	0	0
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	TSPI0CS1	Output	FTU1a	0/1	1	***[PEFR3]***	0/1	0/1	0/1	0
	T32A03OUTA	Output	FTU1a	0/1	1	***[PEFR4]***	0/1	0/1	0/1	0
	T32A03OUTC	Output	FTU1a	0/1	1	***[PEFR5]***	0/1	0/1	0/1	0
PE6	After reset	-	-	0	0	0	0	0	0	0
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	INT6	Input	FTU4a	0/1	0	0	0/1	0/1	0/1	1
	T32A03INB0	Input	FTU1a	0/1	0	***[PEFR4]***	0/1	0/1	0/1	1
PE7	After reset	-	-	0	0	0	0	0	0	0
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	INT7	Input	FTU4a	0/1	0	0	0/1	0/1	0/1	1
	T32A03OUTB	Output	FTU1a	0/1	1	***[PEFR4]***	0/1	0/1	0/1	0

4.2.7. PORT F

Table 4.8 Port F Registers Setting

PORT	Reset status / Function	Input/Output	PORT type	Control register						
				[PADATA]	*[PACR]*	*[PAFRn]*	*[PAOD]*	*[PAPUP]*	*[PAPDN]*	*[PAIE]*
PF0	During reset (BOOT_N)	Input	FTU16a	0	0	0	0	0 (Note)	0	0 (Note)
	After reset	-	-	0	0	0	0	0	0	0
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	TSPI3CSIN	Input	FTU1a	0/1	0	***[PFFR3]***	0/1	0/1	0/1	1
	T32A04INB0	Input	FTU1a	0/1	0	***[PFFR4]***	0/1	0/1	0/1	1
PF1	After reset	-	-	0	0	0	0	0	0	0
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	UT3RTS_N	Output	FTU1a	0/1	1	***[PFFR1]***	0/1	0/1	0/1	0
	UT3CTS_N	Input	FTU1a	0/1	0	***[PFFR2]***	0/1	0/1	0/1	1
	TSPI3CS0	Output	FTU1a	0/1	1	***[PFFR3]***	0/1	0/1	0/1	0
	T32A04OUTB	Output	FTU1a	0/1	1	***[PFFR4]***	0/1	0/1	0/1	0
PF2	After reset	-	-	0	0	0	0	0	0	0
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	UT3CTS_N	Input	FTU1a	0/1	0	***[PFFR1]***	0/1	0/1	0/1	1
	UT3RTS_N	Output	FTU1a	0/1	1	***[PFFR2]***	0/1	0/1	0/1	0
	TSPI3SCK	Input	FTU1a	0/1	0	***[PFFR3]***	0/1	0/1	0/1	1
		Output		0/1	1		0/1	0/1	0/1	0
	ENC1A	Input	FTU1a	0/1	0	***[PFFR6]***	0/1	0/1	0/1	1
PF3	After reset	-	-	0	0	0	0	0	0	0
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	UT3TXDA	Output	FTU1a	0/1	1	***[PFFR1]***	0/1	0/1	0/1	0
	UT3RXD	Input	FTU1a	0/1	0	***[PFFR2]***	0/1	0/1	0/1	1
	TSPI3TXD	Output	FTU2a	0/1	1	***[PFFR3]***	0/1	0/1	0/1	0
	ENC1B	Input	FTU1a	0/1	0	***[PFFR6]***	0/1	0/1	0/1	1
PF4	After reset	-	-	0	0	0	0	0	0	0
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	UT3RXD	Input	FTU1a	0/1	0	***[PFFR1]***	0/1	0/1	0/1	1
	UT3TXDA	Output	FTU1a	0/1	1	***[PFFR2]***	0/1	0/1	0/1	0
	TSPI3RXD	Input	FTU1a	0/1	0	***[PFFR3]***	0/1	0/1	0/1	1
	ENC1Z	Input	FTU1a	0/1	0	***[PFFR6]***	0/1	0/1	0/1	1

Note: During the reset period by the reset pin (RESET_N), the state of the BOOT_N pin can be input to PF0 with pull-up enabled and input enabled.

4.2.8. PORT G

Table 4.9 Port G Registers Setting

PORT	Reset status / Function	Input/Output	PORT type	Control register						
				[PADATA]	*[PACR]*	*[PAFRn]*	*[PAOD]*	*[PAPUP]*	*[PAPDN]*	*[PAIE]*
PG0	After reset	-	-	0	0	0	0	0	0	0
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	UO1	Output	FTU2a	0/1	1	***[PGFR6]***	0/1	0/1	0/1	0
PG1	After reset	-	-	0	0	0	0	0	0	0
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	UT4RTS_N	Output	FTU1a	0/1	1	***[PGFR1]***	0/1	0/1	0/1	0
	UT4CTS_N	Input	FTU1a	0/1	0	***[PGFR2]***	0/1	0/1	0/1	1
	XO1	Output	FTU2a	0/1	1	***[PGFR6]***	0/1	0/1	0/1	0
PG2	After reset	-	-	0	0	0	0	0	0	0
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	UT4CTS_N	Input	FTU1a	0/1	0	***[PGFR1]***	0/1	0/1	0/1	1
	UT4RTS_N	Output	FTU1a	0/1	1	***[PGFR2]***	0/1	0/1	0/1	0
	VO1	Output	FTU2a	0/1	1	***[PGFR6]***	0/1	0/1	0/1	0
PG3	After reset	-	-	0	0	0	0	0	0	0
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	UT4TXDA	Output	FTU1a	0/1	1	***[PGFR1]***	0/1	0/1	0/1	0
	UT4RXD	Input	FTU1a	0/1	0	***[PGFR2]***	0/1	0/1	0/1	1
	YO1	Output	FTU2a	0/1	1	***[PGFR6]***	0/1	0/1	0/1	0
PG4	After reset	-	-	0	0	0	0	0	0	0
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	UT4RXD	Input	FTU1a	0/1	0	***[PGFR1]***	0/1	0/1	0/1	1
	UT4TXDA	Output	FTU1a	0/1	1	***[PGFR2]***	0/1	0/1	0/1	0
	WO1	Output	FTU2a	0/1	1	***[PGFR6]***	0/1	0/1	0/1	0
PG5	After reset	-	-	0	0	0	0	0	0	0
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	ZO1	Output	FTU2a	0/1	1	***[PGFR6]***	0/1	0/1	0/1	0
PG6	After reset	-	-	0	0	0	0	0	0	0
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	EMG1	Input	FTU1a	0/1	0	***[PGFR6]***	0/1	0/1	0/1	1
PG7	After reset	-	-	0	0	0	0	0	0	0
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	OVV1	Input	FTU1a	0/1	0	***[PGFR6]***	0/1	0/1	0/1	1

4.2.9. PORT H

Table 4.10 Port H Registers Setting

PORT	Reset status / Function	Input/Output	PORT type	Control register						
				[PADATA]	*[PACR]*	*[PAFRn]*	*[PAOD]*	*[PAPUP]*	*[PAPDN]*	*[PAIE]*
PH0	After reset	-	-	0	0	N/A	0	0	0	0
	Input port	Input	-	0/1	0	N/A	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	N/A	0/1	0/1	0/1	0
	INT0	input	FTU4a	0/1	0	N/A	0/1	0/1	0/1	1
	AINA12	Input	FTU5a	0/1	0	N/A	0/1	0	0	0
PH1	After reset	-	-	0	0	N/A	0	0	0	0
	Input port	Input	-	0/1	0	N/A	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	N/A	0/1	0/1	0/1	0
	INT1	input	FTU4a	0/1	0	N/A	0/1	0/1	0/1	1
	AINA13	Input	FTU5a	0/1	0	N/A	0/1	0	0	0
PH2	After reset	-	-	0	0	N/A	0	0	0	0
	Input port	Input	-	0/1	0	N/A	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	N/A	0/1	0/1	0/1	0
	INT2	input	FTU4a	0/1	0	N/A	0/1	0/1	0/1	1
	AINA14	Input	FTU5a	0/1	0	N/A	0/1	0	0	0
PH3	After reset	-	-	0	0	N/A	0	0	0	0
	Input port	Input	-	0/1	0	N/A	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	N/A	0/1	0/1	0/1	0
	AINA15	Input	FTU5a	0/1	0	N/A	0/1	0	0	0
PH4	After reset	-	-	0	0	N/A	0	0	0	0
	Input port	Input	-	0/1	0	N/A	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	N/A	0/1	0/1	0/1	0
	AINA16	Input	FTU5a	0/1	0	N/A	0/1	0	0	0
PH5	After reset	-	-	0	0	N/A	0	0	0	0
	Input port	Input	-	0/1	0	N/A	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	N/A	0/1	0/1	0/1	0
	AINA17	Input	FTU5a	0/1	0	N/A	0/1	0	0	0
PH6	After reset	-	-	0	0	N/A	0	0	0	0
	Input port	Input	-	0/1	0	N/A	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	N/A	0/1	0/1	0/1	0
	AINA18	Input	FTU5a	0/1	0	N/A	0/1	0	0	0
PH7	After reset	-	-	0	0	N/A	0	0	0	0
	Input port	Input	-	0/1	0	N/A	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	N/A	0/1	0/1	0/1	0
	AINA19	Input	FTU5a	0/1	0	N/A	0/1	0	0	0

Note: When using analog input (AINAx), ***[PHCR]*** should be output disable "0",***[PHIE]*** should be input disable "0", ***[PHPUP]*** should be pull-up disable"0" and ***[PHPDN]*** should be pull-down disable "0".

4.2.10. PORT J

Table 4.11 Port J Registers Setting

PORT	Reset status / Function	Input/Output	PORT type	Control register						
				[PADATA]	*[PACR]*	*[PAFRn]*	*[PAOD]*	*[PAPUP]*	*[PAPDN]*	*[PAIE]*
PJ0	After reset	-	-	0	0	N/A	0	0	0	0
	Input port	Input	-	0/1	0	N/A	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	N/A	0/1	0/1	0/1	0
	AINB15	Input	FTU5a	0/1	0	N/A	0/1	0	0	0
PJ1	After reset	-	-	0	0	N/A	0	0	0	0
	Input port	Input	-	0/1	0	N/A	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	N/A	0/1	0/1	0/1	0
	AINB16	Input	FTU5a	0/1	0	N/A	0/1	0	0	0
PJ2	After reset	-	-	0	0	N/A	0	0	0	0
	Input port	Input	-	0/1	0	N/A	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	N/A	0/1	0/1	0/1	0
	AINB17	Input	FTU5a	0/1	0	N/A	0/1	0	0	0
PJ3	After reset	-	-	0	0	N/A	0	0	0	0
	Input port	Input	-	0/1	0	N/A	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	N/A	0/1	0/1	0/1	0
	AINB18	Input	FTU5a	0/1	0	N/A	0/1	0	0	0
PJ4	After reset	-	-	0	0	N/A	0	0	0	0
	Input port	Input	-	0/1	0	N/A	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	N/A	0/1	0/1	0/1	0
	AINB19	Input	FTU5a	0/1	0	N/A	0/1	0	0	0
PJ5	After reset	Input	-	0	0	N/A	0	0	0	0
	Input port	Input	-	0/1	0	N/A	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	N/A	0/1	0/1	0/1	0
	AINB20	Input	FTU5a	0/1	0	N/A	0/1	0	0	0
PJ6	After reset	-	-	0	0	N/A	0	0	0	0
	Input port	Input	-	0/1	0	N/A	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	N/A	0/1	0/1	0/1	0
	INTC	input	FTU4a	0/1	0	N/A	0/1	0/1	0/1	1
	AINB21	Input	FTU5a	0/1	0	N/A	0/1	0	0	0
PJ7	After reset	-	-	0	0	N/A	0	0	0	0
	Input port	Input	-	0/1	0	N/A	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	N/A	0/1	0/1	0/1	0
	INTD	input	FTU4a	0/1	0	N/A	0/1	0/1	0/1	1
	AINB22	Input	FTU5a	0/1	0	N/A	0/1	0	0	0

Note: When using analog input (AINBx), ***[PJCR]*** should be output disable "0",***[PJIE]*** should be input disable "0", ***[PJPUP]*** should be pull-up disable"0" and ***[PJPDN]*** should be pull-down disable "0".

4.2.11. PORT K

Table 4.12 Port K Registers Setting

PORT	Reset status / Function	Input/Output	PORT type	Control register						
				[PADATA]	*[PACR]*	*[PAFRn]*	*[PAOD]*	*[PAPUP]*	*[PAPDN]*	*[PAIE]*
PK0	After reset	-	-	0	0	0	0	0	0	0
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	INTE	Input	FTU4a	0/1	0	0	0/1	0/1	0/1	1
	EI2C1SDA	Input/Output	FTU1a	0/1	1	***[PKFR3]***	1	0/1	0/1	1
	TRACEDATA3	Output	FTU1a	0/1	1	***[PKFR7]***	0/1	0/1	0/1	0
PK1	After reset	-	-	0	0	0	0	0	0	0
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	INTF	Input	FTU4a	0/1	0	0	0/1	0/1	0/1	1
	EI2C1SCL	Input/Output	FTU1a	0/1	1	***[PKFR3]***	1	0/1	0/1	1
	TRACEDATA2	Output	FTU1a	0/1	1	***[PKFR7]***	0/1	0/1	0/1	0

4.2.12. PORT L

Table 4.13 Port L Registers Setting

PORT	Reset status / Function	Input/Output	PORT type	Control register						
				[PADATA]	*[PACR]*	*[PAFRn]*	*[PAOD]*	*[PAPUP]*	*[PAPDN]*	*[PAIE]*
PL0	After reset	-	-	0	0	N/A	0	0	0	0
	Input port	Input	-	0/1	0	N/A	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	N/A	0/1	0/1	0/1	0
	INTB	Input	FTU4a	0/1	0	N/A	0/1	0/1	0/1	1
PL1	After reset	-	-	0	0	N/A	0	0	0	0
	Input port	Input	-	0/1	0	N/A	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	N/A	0/1	0/1	0/1	0
	INTA	Input	FTU4a	0/1	0	N/A	0/1	0/1	0/1	1

4.2.13. PORT N

Table 4.14 Port N Registers Setting

PORT	Reset status / Function	Input/Output	PORT type	Control register						
				[PADATA]	*[PACR]*	*[PAFRn]*	*[PAOD]*	*[PAPUP]*	*[PAPDN]*	*[PAIE]*
PN0	After reset	-	-	0	0	0	0	0	0	0
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	EI2C0SDA	Input/Output	FTU1a	0/1	1	***[PNFR3]***	1	0/1	0/1	1
PN1	After reset	-	-	0	0	0	0	0	0	0
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	EI2C0SCL	Input/Output	FTU1a	0/1	1	***[PNFR3]***	1	0/1	0/1	1
	T32A00OUTB	Output	FTU1a	0/1	1	***[PNFR4]***	0/1	0/1	0/1	0
PN2	After reset	-	-	0	0	0	0	0	0	0
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	T32A00INB0	Input	FTU1a	0/1	0	***[PNFR4]***	0/1	0/1	0/1	1

4.2.14. PORT P

Table 4.15 Port P Registers Setting

PORT	Reset status / Function	Input/Output	PORT type	Control register						
				[PADATA]	*[PACR]*	*[PAFRn]*	*[PAOD]*	*[PAPUP]*	*[PAPDN]*	*[PAIE]*
PP0	After reset	-	-	0	0	N/A	0	0	0	0
	Input port	Input	-	0/1	0	N/A	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	N/A	0/1	0/1	0/1	0
	AINA20	Input	FTU5a	0/1	0	N/A	0/1	0	0	0
PP1	After reset	-	-	0	0	N/A	0	0	0	0
	Input port	Input	-	0/1	0	N/A	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	N/A	0/1	0/1	0/1	0
	AINA21/ AINB12	Input	FTU5a	0/1	0	N/A	0/1	0	0	0
PP2	After reset	-	-	0	0	N/A	0	0	0	0
	Input port	Input	-	0/1	0	N/A	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	N/A	0/1	0/1	0/1	0
	AINA22/ AINB13	Input	FTU5a	0/1	0	N/A	0/1	0	0	0
PP3	After reset	-	-	0	0	N/A	0	0	0	0
	Input port	Input	-	0/1	0	N/A	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	N/A	0/1	0/1	0/1	0
	AINA23/ AINB14	Input	FTU5a	0/1	0	N/A	0/1	0	0	0

Note: When using analog input (AINAx/AINBx), ***[PPCR]*** should be output disable "0",***[PPIE]*** should be input disable "0", ***[PPPUP]*** should be pull-up disable"0" and ***[PPPDN]*** should be pull-down disable "0".

4.2.15. PORT R

Table 4.16 Port R Registers Setting

PORT	Reset status / Function	Input/Output	PORT type	Control register						
				[PADATA]	*[PACR]*	*[PAFRn]*	*[PAOD]*	*[PAPUP]*	*[PAPDN]*	*[PAIE]*
PR0	After reset	-	-	0	N/A	N/A	N/A	N/A	0	0
	Input port	Input	-	0/1	N/A	N/A	N/A	N/A	0/1	1
	X1	Input	FTU11a	0/1	N/A	N/A	N/A	N/A	0	0
	EHCLKIN	input	FTU11a	0/1	N/A	N/A	N/A	N/A	0	0/1
PR1	After reset	-	-	0	N/A	N/A	N/A	N/A	0	0
	Input port	Input	-	0/1	N/A	N/A	N/A	N/A	0/1	1
	X2	Output	FTU11a	0/1	N/A	N/A	N/A	N/A	0	0

5. Block Diagrams of Ports

The ports have these types of circuits, FTU1a to FTU5a, FTU11a and FTU16a. Each circuit diagram is shown in the following. The dot line block shows an equivalent circuit which is described in "Datasheet".

The "I/O Reset" shown in the circuit diagram is a signal from the power on reset (POR).

5.1. Type FTU1a

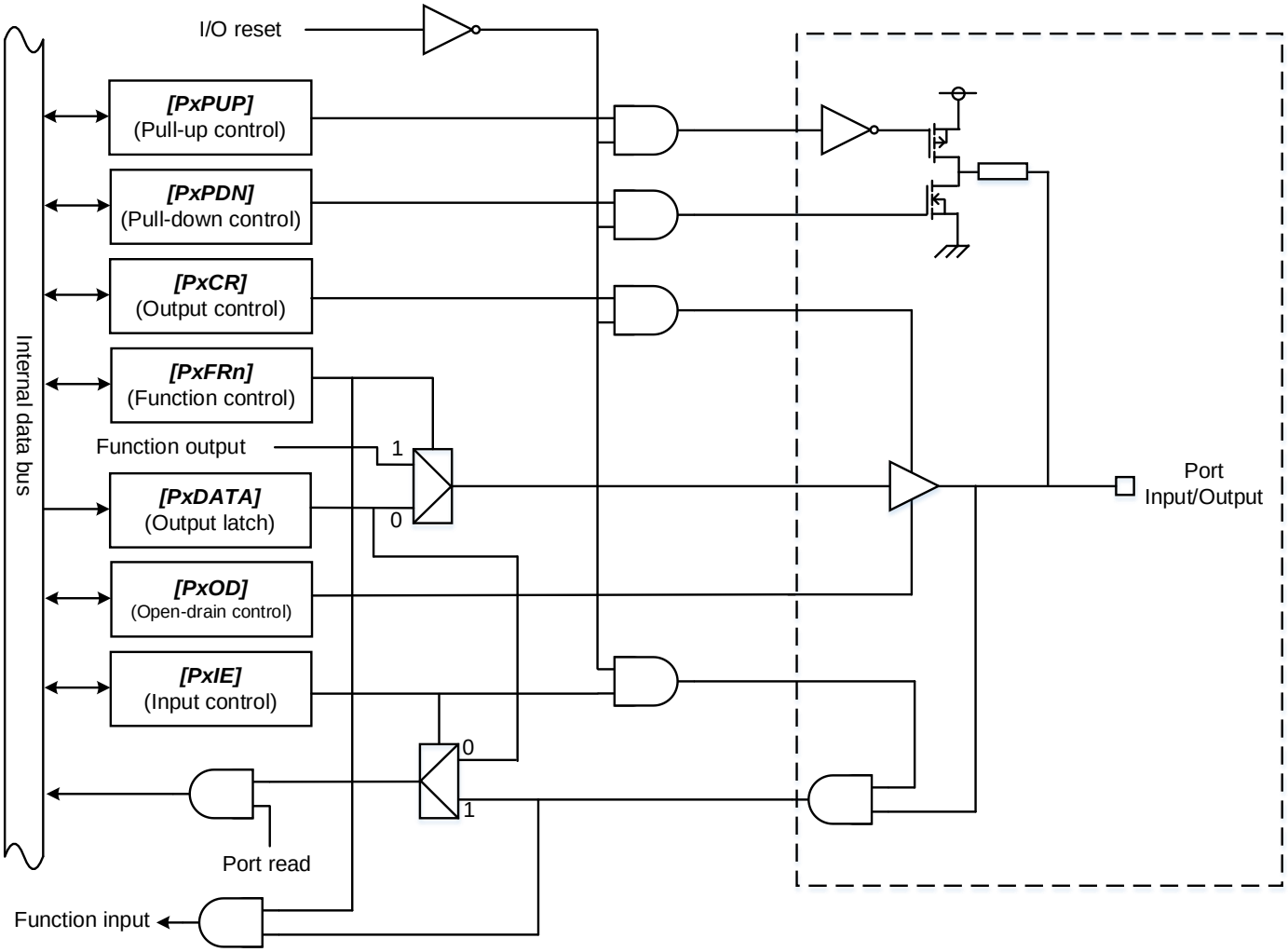

Figure 5.1 Port Type FTU1a

5.2. Type FTU2a

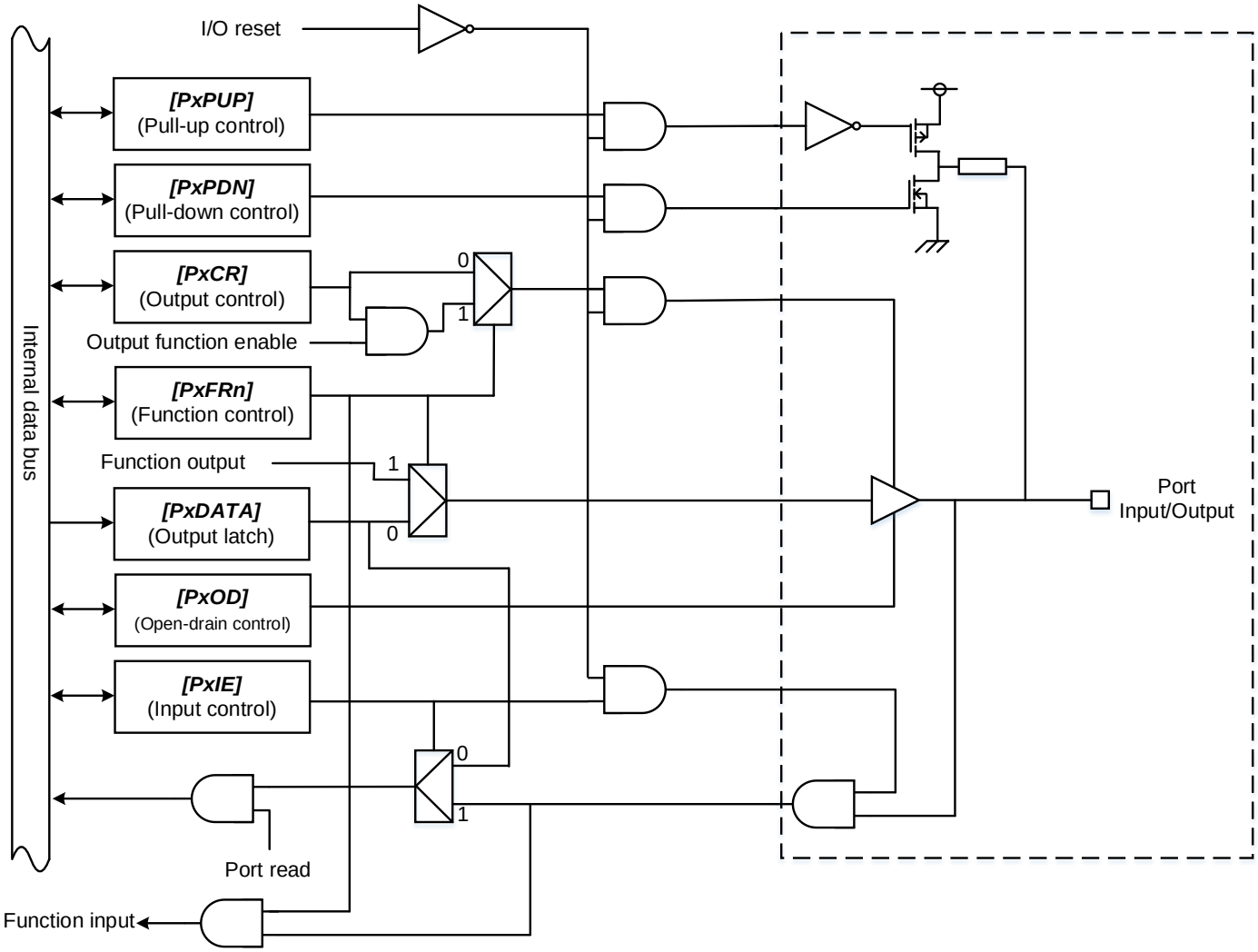

Figure 5.2 Port Type FTU2a

5.3. Type FTU3a

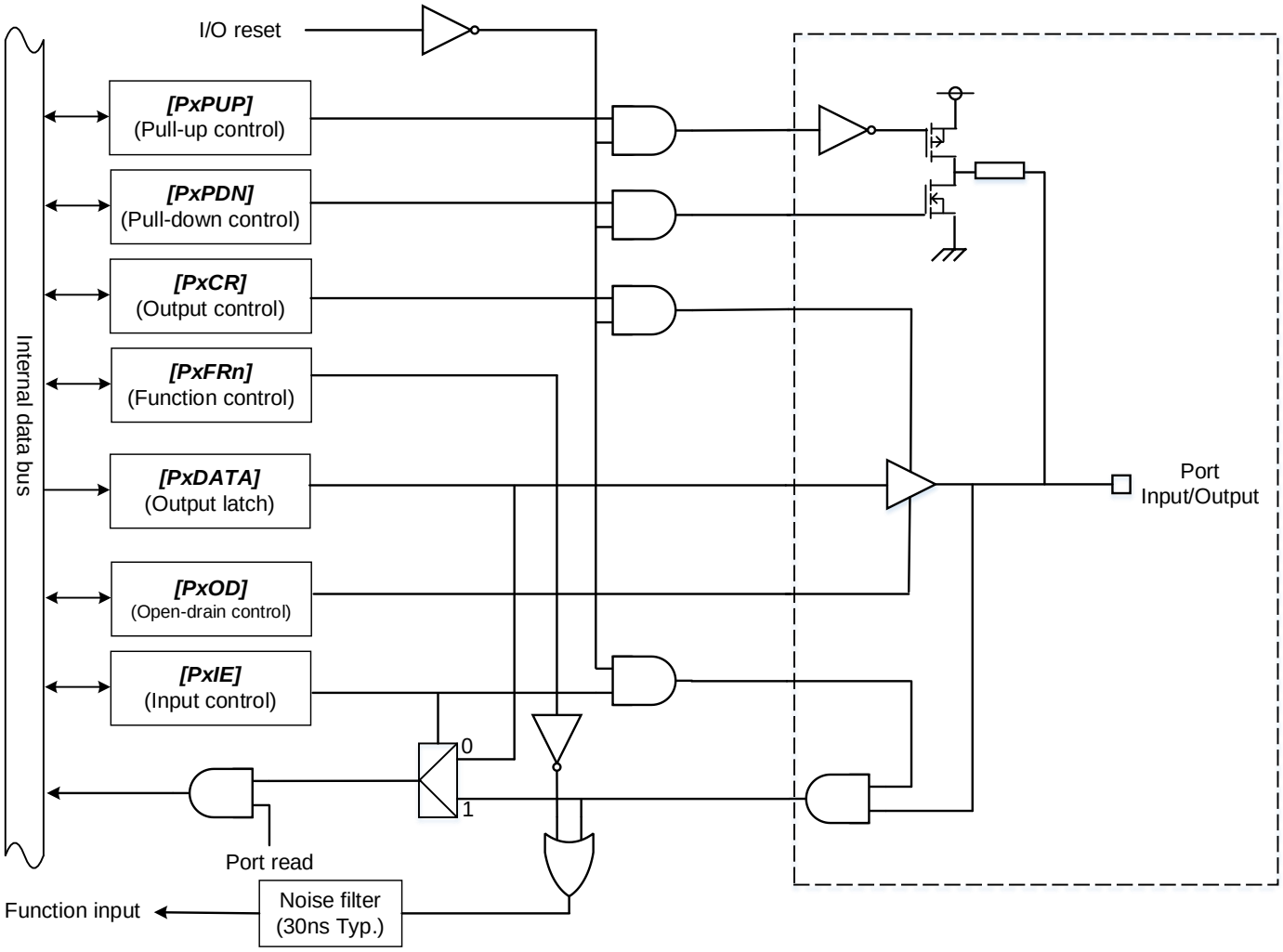

Figure 5.3 Port Type FTU3a

5.4. Type FTU4a

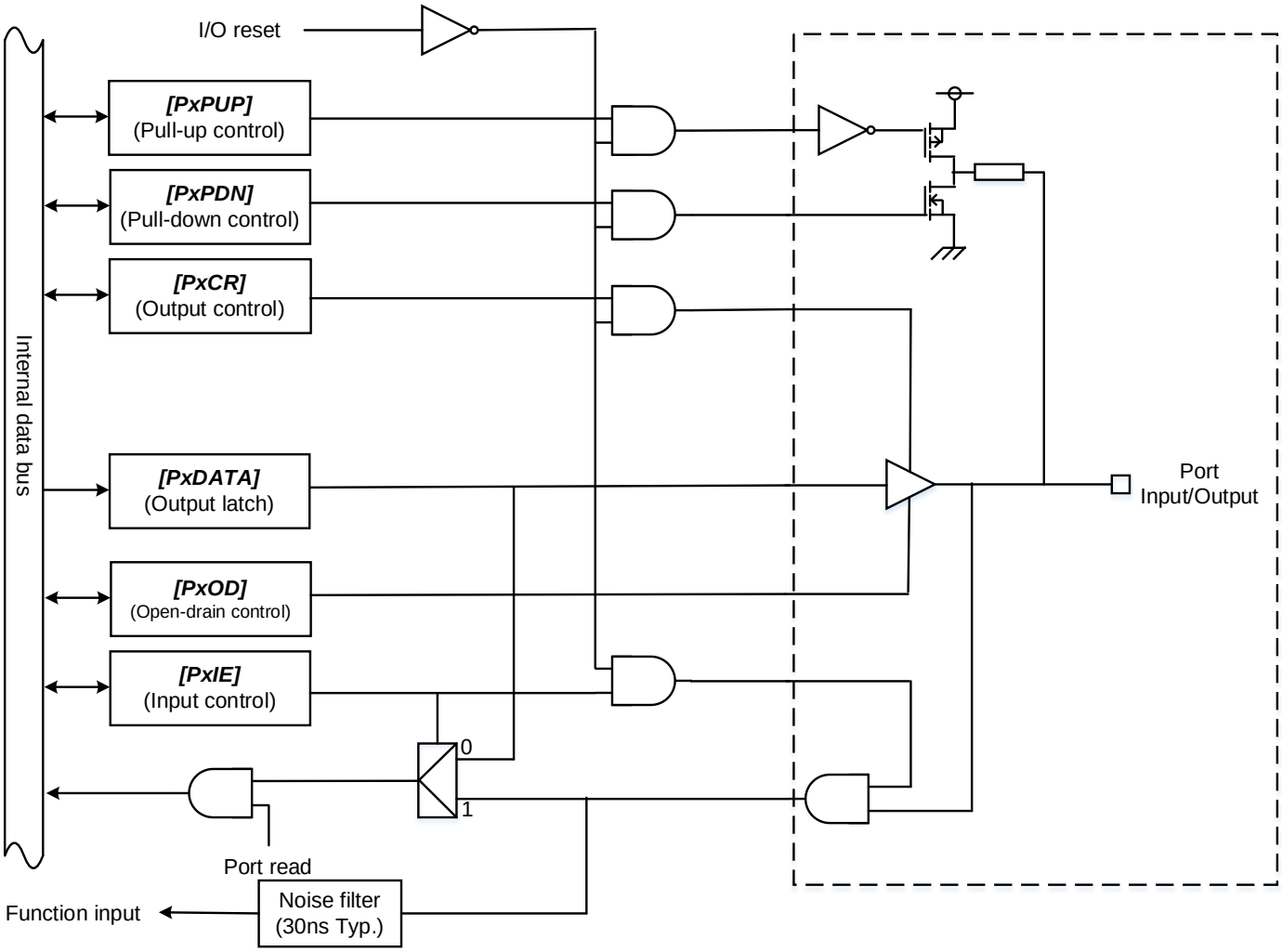

Figure 5.4 Port Type FTU4a

5.5. Type FTU5a

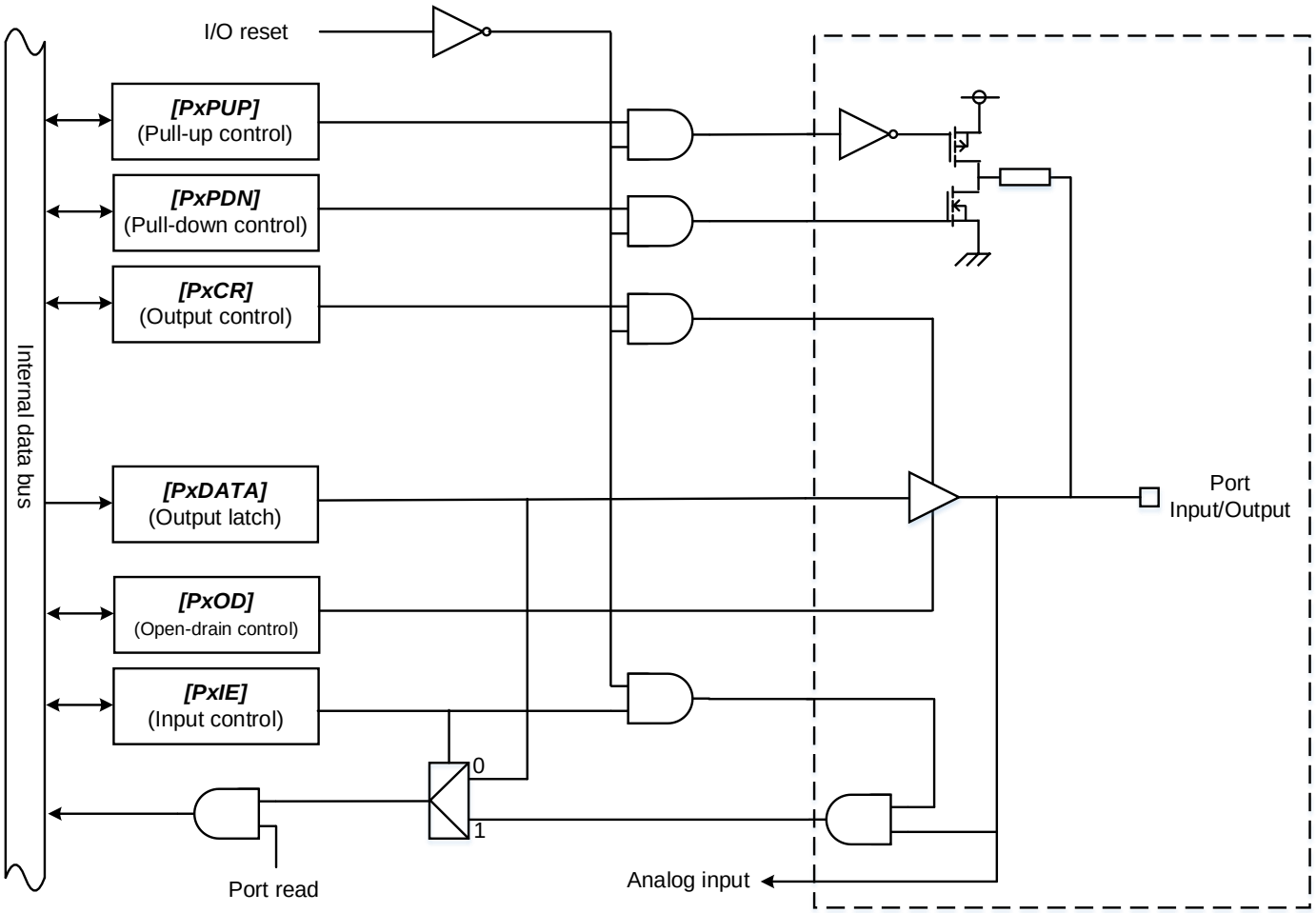

Figure 5.5 Port Type FTU5a

5.6. Type FTU11a

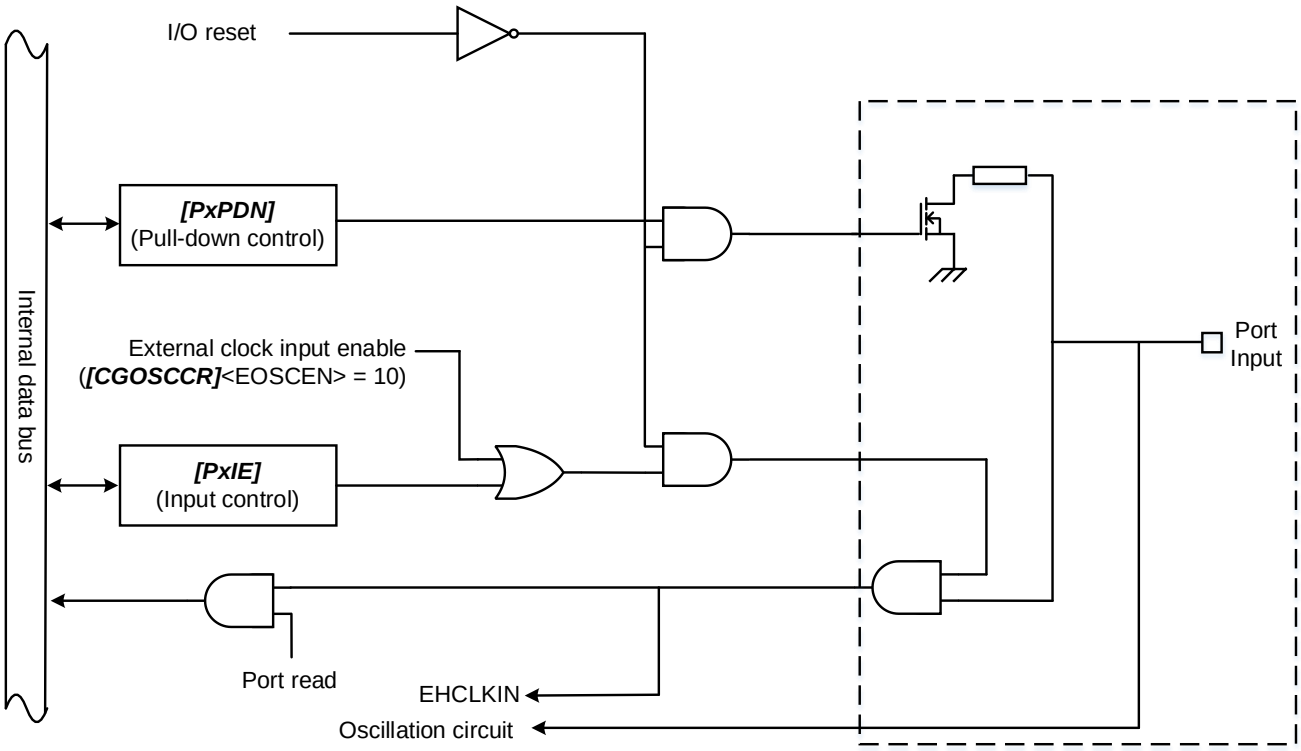

Figure 5.6 Port Type FTU11a

5.7. Type FTU16a

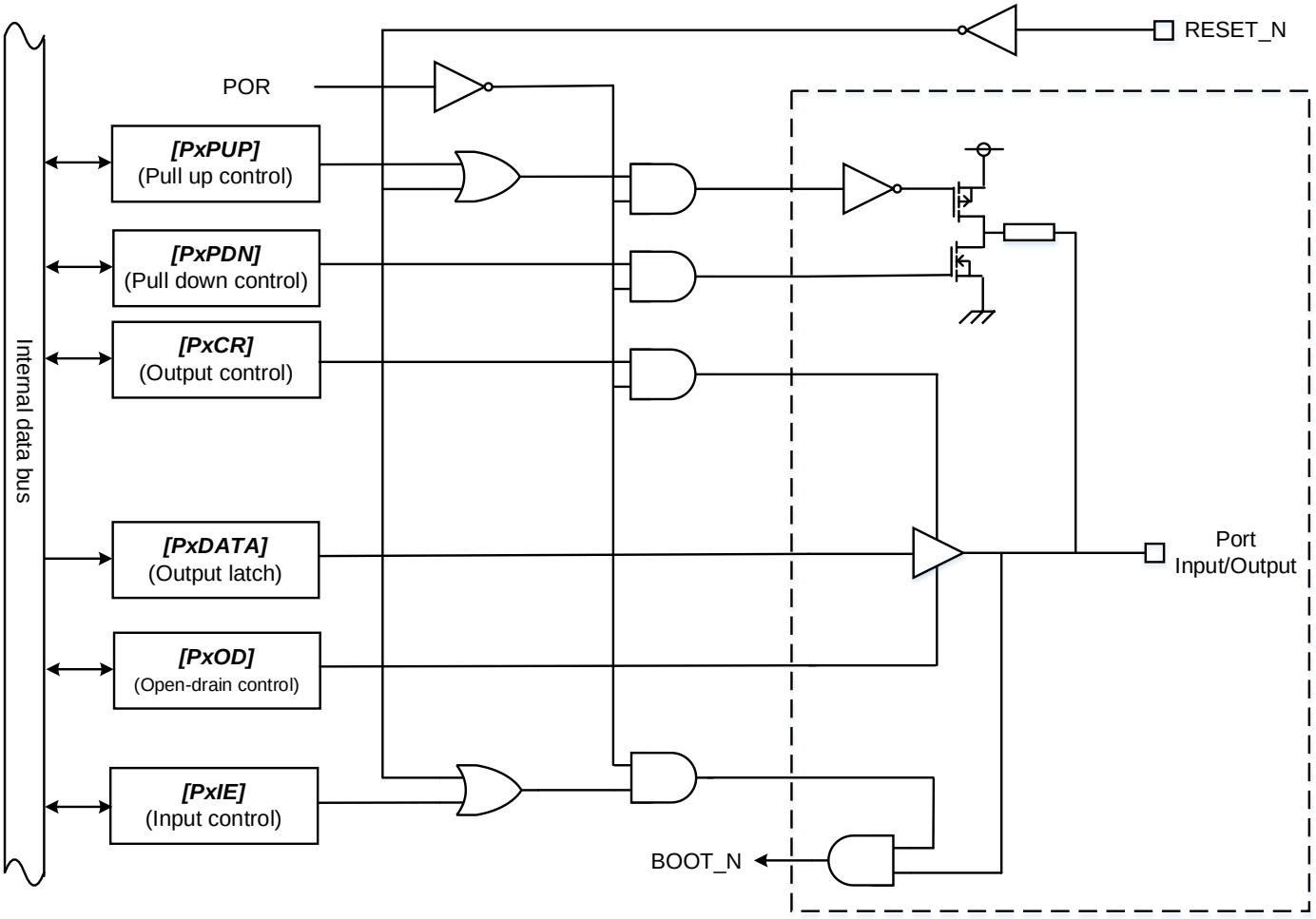

Figure 5.7 Port Type FTU16a

6. Precaution

6.1. Pin Status During Reset Period

During the reset period, the pin status is high-impedance except for below pins. And, the pull-up/pull-down is invalid.

- The debug interface alternate pins (PB3 to PB6) are debugging pin status.
- PF0 (BOOT_N) works as a BOOT function. It is enabled to be input and pulled-up during pin reset period. At the rising edge of the reset signal, if PF0 is "High", the device enters single chip mode and boots from the on chip flash memory. If PF0 is "Low", the device enters single BOOT mode and boots from the internal BOOT ROM program.

6.2. Unused Pin

We recommend that each unused pin should be connected to the power supply pins or GND pins via resistors.

Generally, if MCUs operate while the high-impedance pins left open, electrostatic damage or latch-up may occur in the internal LSI due to induced voltage influenced from external noise.

6.3. Important Points of Using Debug Interface Pins Used as General-purpose Ports

After releasing reset, if the debug interface pins are used as the general I/O ports by the user program, the debug tool cannot be connected

If the debug tool cannot be connected, it can recover debug connection to erase the flash memory using UART connection set as single BOOT mode from external. For details, please refer to the reference manual of "Flash memory".

7. Revision History

Table 7.1 Revision History

Revision	Date	Description
1.0	2024-08-30	- First release

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