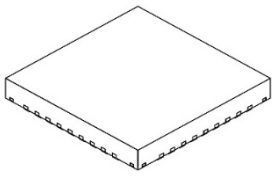
Toshiba Bi-CMOS Linear Integrated Circuits Silicon Monolithic

TB9084FTG

Automotive Gate Driver for Brushless Motor

1. Description

TB9084FTG is a gate driver IC for automotive brushless motors. It is equipped with a charge pump, motor current sensing circuit, oscillation circuit, SPI communication circuit, and multiple types of abnormality detection circuits. In addition, it allows abnormality detection conditions and reaction operation, after abnormality detection to be set by using SPI communication.



P-VQFN36-0606-0.50

2. Applications

Motor generators, electric oil pumps. Automotive body system applications such as power sliding doors, and power tail gates.

3. Features

- Used in a 12V battery system and a jump start environment (Operating voltage range: VB = 5.7 to 28V)
- MCU with 5V and 3.3V system IO ports controls this product (Operating voltage range: VCC = 3.0 to 5.5V)
- Low reset current at VCC=0V to prevent the battery from running out
- Can be used in a temperature environment for mechanically and electrically integrated type.
- Built-in charge pump circuit (VCP).
- Built-in gate drivers for driving 3-phase FETs (PWM control, up to 20kHz)
- Built-in gate driver (high-side switch) for driving a FET for reverse polarity protection (RPPO)
- Built-in motor current sensing circuit
- Built-in oscillation circuit, 4MHz(Typ.)
- Various built-in abnormality detection circuits
  VB, VCC, RPPO under voltage/VCC, VCP over voltage/Over temperature/VDS detection of 3-phase FET /Short to VB or GND fault detection for charge pump drive terminals (CP1SW, CP2SW) /SPI communication abnormality detection
- Built-in input circuit for gate driver emergency stop (ALRAM)
- Built-in SPI communication circuit
- Ambient temperature (Ta) = -40 to 150°C, Junction temperature (Tj) = -40 to 175°C
- Package: P-VQFN36-0606-0.50 (Wettable flank, 0.5mm pitch)
- AEC-Q100 (Rev-J), Q006 (Rev-A): Grade 0

Do not design your products or systems based on the information on this document. Please contact your Toshiba sales representative for updated information before designing your products.

Start of commercial production (schedule)
2025-08

[Notes for Users]
All the functional blocks, circuits, etc. in the block diagrams may be omitted or simplified for explanatory purposes.
Determine the peripheral circuits after thorough evaluation and check on unit boards assuming the operating environment.

Please note that the contents may change without advance notice, because the document status is preliminary one. We apologize for any inconvenience.

When “[[G]]/RoHS COMPATIBLE,” “[[G]]/RoHS [[Chemical symbol(s) of controlled substance(s),” “RoHS COMPATIBLE,” or “RoHS COMPATIBLE, [[Chemicalsymbol(s) of controlled substance(s)]]>MCV” is written on the packing box label, this product conforms to the EU RoHS Directive (2011/65/EU) as described.

4. Block Diagram

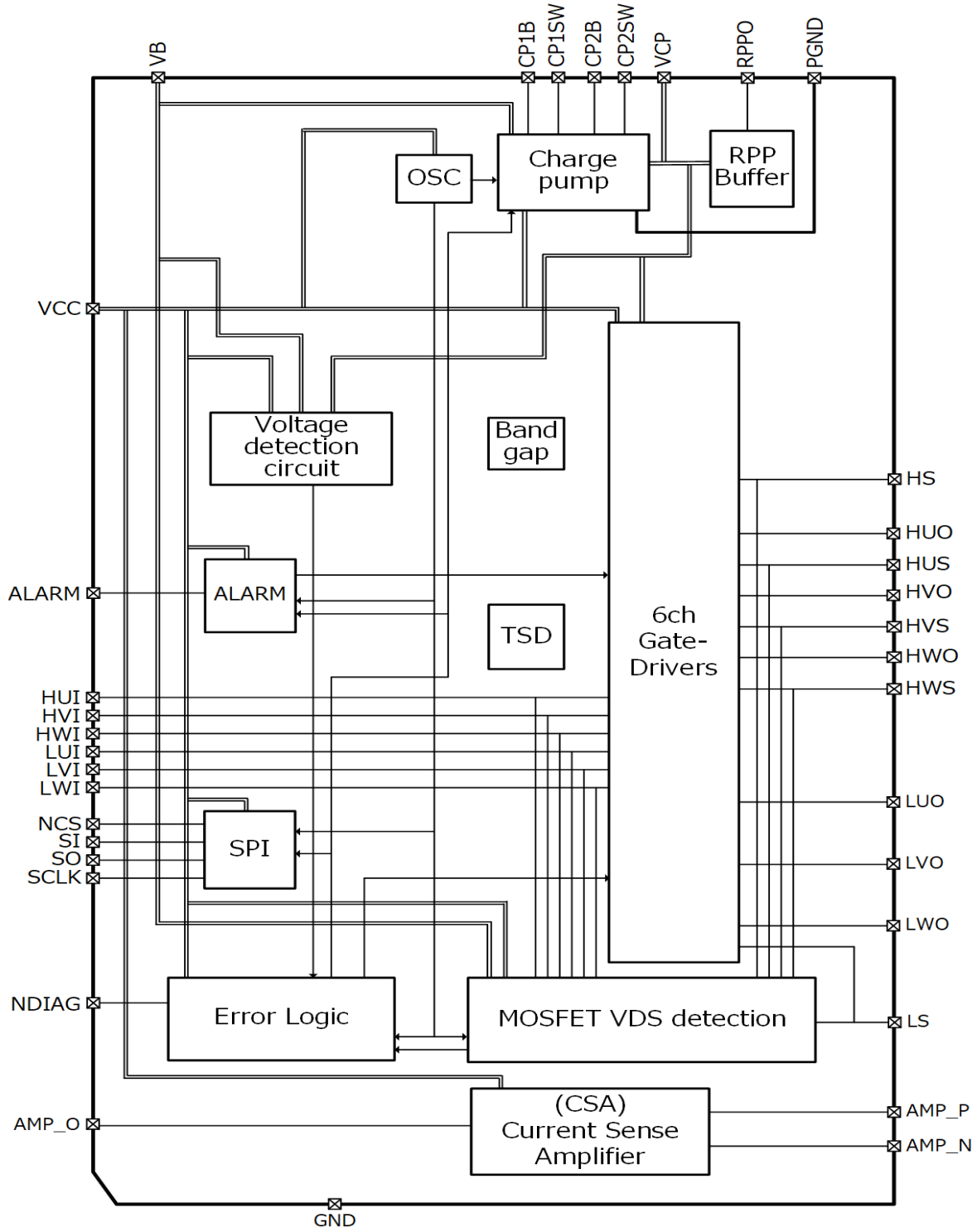


Fig. 4.1 Block Diagram

5. Pin Assignments Top view

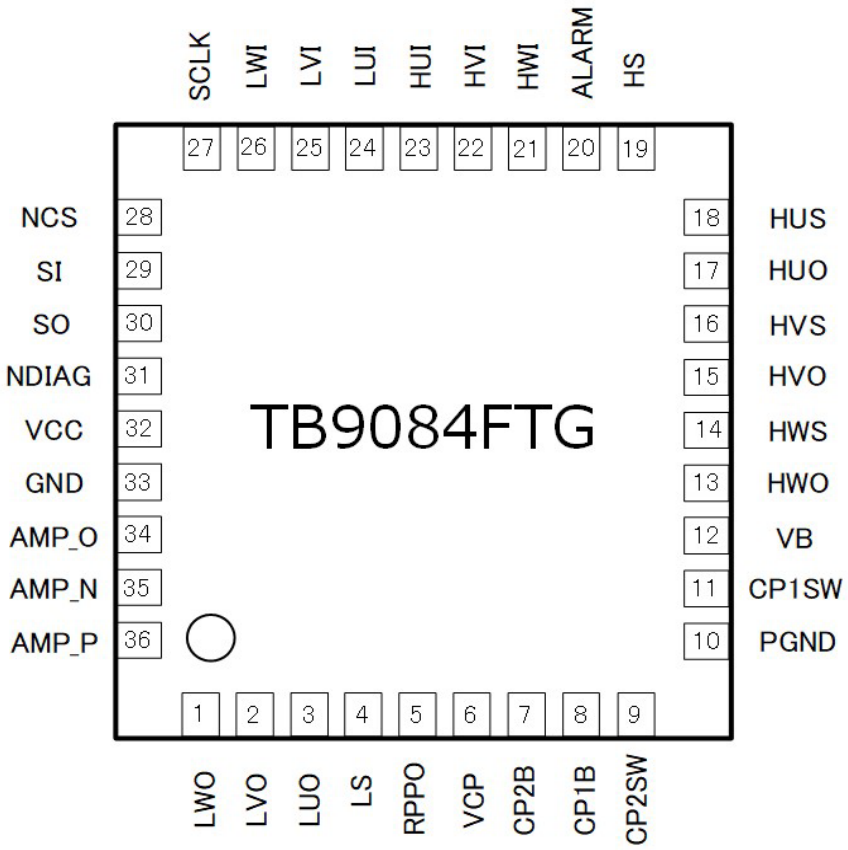


Fig. 5.1 Pin Assignments (top view)

6. Pin Description

Table 6.1 Pin Description

No.	Name	I/O	Function	Pull-up/down Resistance
1	LWO	OUT	Gate driver output (W phase low-side)	Pull-down to LS
2	LVO	OUT	Gate driver output (V phase low-side)	Pull-down to LS
3	LUO	OUT	Gate driver output (U phase low-side)	Pull-down to LS
4	LS	IN	Reference input for low-side gate drivers	-
5	RPPO	OUT	Output for driving FET for reverse polarity protection	-
6	VCP	Power supply	Charge pump voltage	Pull-down to VB
7	CP2B	I/O	Charge pump 2nd stage bias voltage	-
8	CP1B	I/O	Charge pump 1st stage bias voltage	-
9	CP2SW	OUT	Charge pump 2nd stage drive output	-
10	PGND	GND	Power ground	-
11	CP1SW	OUT	Charge pump 1st stage drive output	-
12	VB	Power supply	External battery power supply	-
13	HWO	OUT	Gate driver output (W phase high-side)	Pull-down to HWS
14	HWS	IN	Gate driver reference input (W phase high-side source)	-
15	HVO	OUT	Gate driver output (V phase high-side)	Pull-down to HVS
16	HVS	IN	Gate driver reference input (V phase high-side source)	-
17	HUO	OUT	Gate driver output (U phase high side)	Pull-down to HUS
18	HUS	IN	Gate driver reference input (U phase high-side source)	-
19	HS	IN	VDS detection input of 3-phase FET (high-side)	-
20	ALARM	IN	Gate driver emergency stop input	Pull-up to VCC
21	HWI	IN	Gate driver input (W phase high-side)	Pull-down to GND
22	HVI	IN	Gate driver input (V phase high-side)	Pull-down to GND
23	HUI	IN	Gate driver input (U phase high-side)	Pull-down to GND
24	LUI	IN	6-input mode (Polarity during power-on: “L”) Gate driver input (U phase low-side)	Pull-down to GND
25	LVI	IN	6-input mode (Polarity during power-on: “L”) Gate driver input (V phase low-side)	Pull-down to GND
26	LWI	IN	6-input mode (Polarity during power-on: “L”) Gate driver input (W phase low-side)	Pull-down to GND
27	SCLK	IN	SPI clock input	Pull-down to GND
28	NCS	IN	SPI chip select	Pull-up to VCC
29	SI	IN	SPI input	Pull-down to GND
30	SO	OUT	SPI output	-
31	NDIAG	OUT	Error output	-
32	VCC	Power supply	External 5V/3.3V power supply	-
33	GND	GND	Analog, digital ground	-
34	AMP_O	OUT	Current sensing amplifier output	-
35	AMP_N	IN	Current sensing amplifier (-) input	-
36	AMP_P	IN	Current sensing amplifier (+) input	-

7. Functional Description

7.1. Charge Pump Circuit

This product has a built-in charge pump circuit for the gate drivers to drive 3-phase FETs. The drive frequency is 250kHz (Typ.) as long as the switching operation is not stopped. With this drive frequency, the VB voltage is pumped up. The charge pump circuit requires two external ceramic capacitors.

The pumping up operation in the the circuit stops under the conditions below.

When Vcp > Vb+12V (Typ.) so that Vcp is not above the Vgs rating (±20V) of the 3-phase FET, its switching operation is stopped by the control of the internal circuit, and when Vcp≤Vb+12V (Typ.), its operation is resumed.

When Vb voltage is low and Vcp is lower than Vb+12V (Typ.), Vcp outputs characteristics depending on the charge pump circuit configuration and its capability.

In addition, when Vcp > 56V (Typ.) so that Vcp withstand voltage is not exceeded, detection operation is conducted depending on the register setting by SPI communication. And when Vcp≤56V (Typ.), detection release operation is conducted depending on the register setting by SPI communication as well. For details, see Chapter 7.6.5.

When the charge pump circuit is turned off after an abnormality detection, VCP voltage transitions to VB voltage.

Note: When a fault is detected and the charge pump circuit is turned off and a certain period has passed after the fault release, the motor operation is enabled. Details are shown in Chapter 7.6.

When the reset of this product is released, charge pump operation is started, and after the voltage has become sufficient, the gate driver operation is allowed. This sequence is to prevent the gate driver from malfunctioning. For details, see Fig. 7.6.1.2.

When an adjacent short circuit or a short to VB or ground of CP1SW terminal and CP2SW happen, the internal elements are protected with the abnormality detection circuits. The details are shown in chapter 7.6.8.

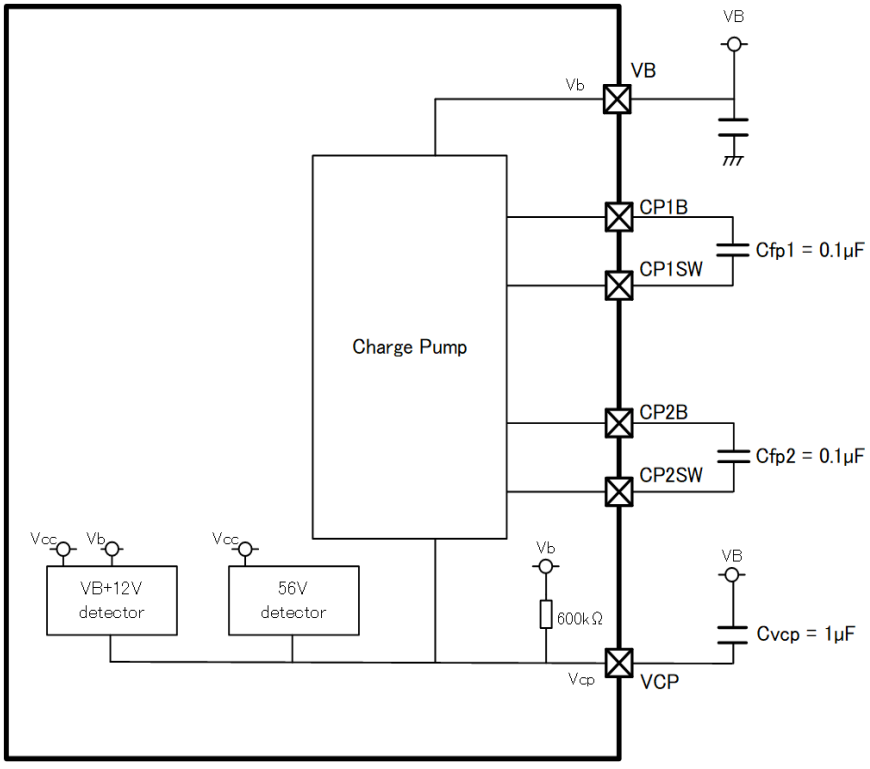


Fig. 7.1 Charge Pump Circuit Block Diagram

7.2. Gate Driver Circuits

As a gate driver to drive external FETs (7 units), this product is equipped with gate drivers (6 units) for 3-phase FETs and a gate driver (1 unit) for a FET for reverse polality protection.

7.2.1. Gate Drivers for Driving 3-Phase FETs

The gate driver circuits for 3-phase FETs are for high-side drive and low-side drive for motor drive.
Each of the gate driver circuits for high-side drive and low-side drive has an input terminal. This input terminal turns off the gate driver when an open fault happens.

The gate driver circuit has 6 output terminals to drive a 3-phase FET. The output stage configuration is of a switch type, and an external series resistor is recommended depending on the operation speed needed for the 3-phase FET.

For a gate driver that drives a high-side FET, when VB voltage is high enough, voltage clamped at H*S reference +10V is output. When VB voltage is low, charge pump voltage with GND reference is output via an internal switch so that enough voltage is applied to the FET gate, and the output voltage is 20V or lower not exceeding the Vgs withstand voltage of the FET. On the other hand, since a gate driver that drives a low-side FET is given Vcp power supply voltage enough to drive in the Vb operating voltage range, voltage clamped at LS reference +11V is always output. These outputs have electric current capability suitable for controlling FET gate that drives motors for applications shown in Chapter 2, and the propagation delay time from the input terminal to the output terminal and the relative deference time for on/off time and off/on time of high side and low side respectively on each phase are optimized. In addition, it has a pull-down resistor to stably turn the FET on and off while the motor’s phase input is in Hi-Z state.

Note that when a 3-phase FET is turned off, the effect of the electric current from H*S terminal of this product on the motor operation is negligible.

H*S terminal and LS terminal are robust enough against noise exceeding VB and noise below GND.

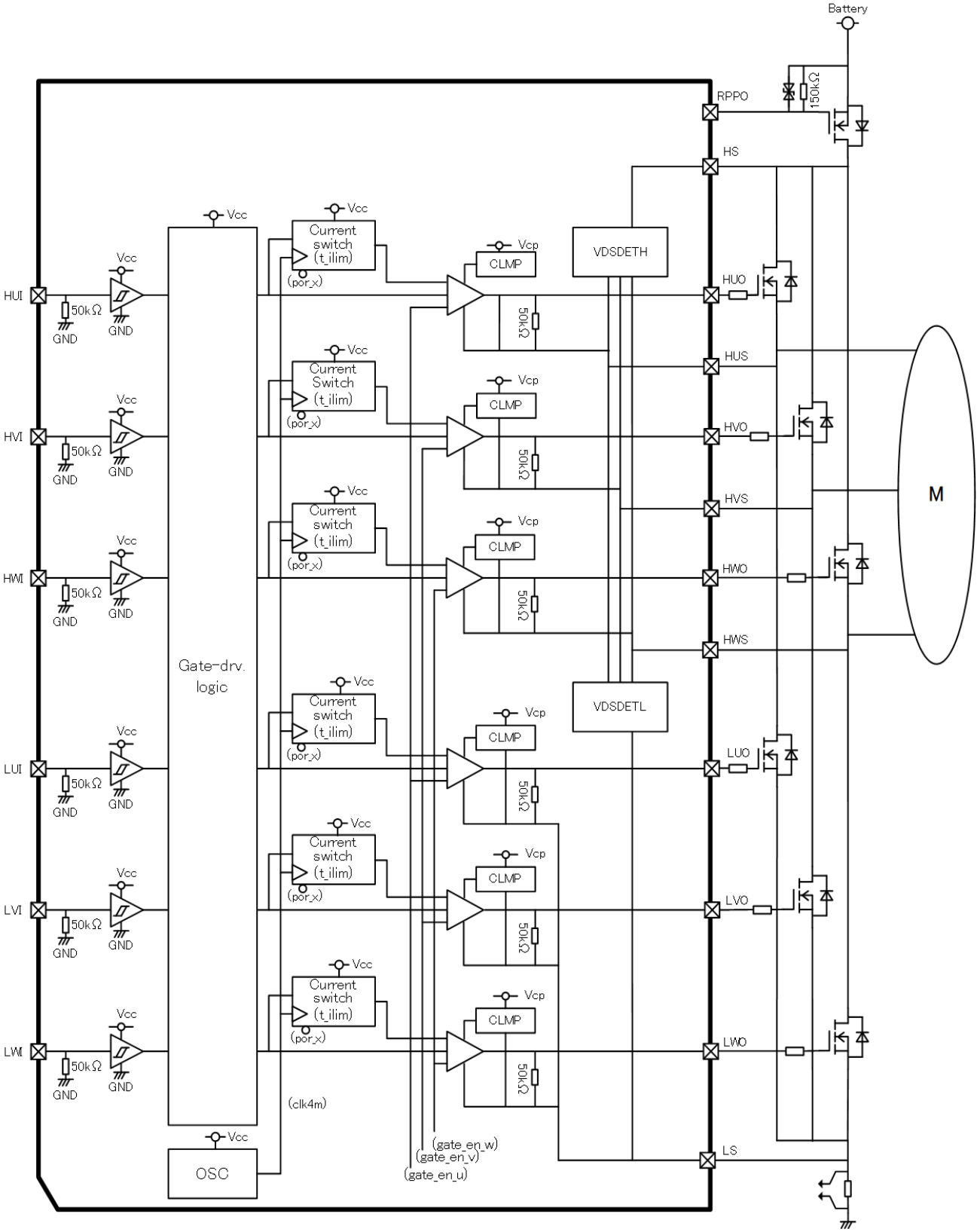


Fig. 7.2.1.1 Gate Driver Circuits Block Diagram

<High-side drive circuit, Low-side drive circuit>

A high-side drive circuit drives a high-side 3-phase FET. A low-side drive circuit drives a low-side 3-phase FET. This product is equipped with 3 channels of high-side and low-side circuits each. Input signals (HUI/HVI/HWI, LUI/LVI/LWI) are converted in the control block to generate output signals (HUO/HVO/HWO, LUO/LVO/LWO).

Current Limit Function

To protect this product from a short to power or ground, electric current of high-side drive and low-side drive circuits after a turn-on/turn-off is switched to a limited current (Io_lmth/Io_lmtl) after a set time “t_ilim” (“000” to “111”) of CONFIG4 register.

Prohibited Input Detection

Note: “*” means u, v and w or U, V and W.

This function is to prevent through-current from being generated by both upper and lower FETs in the same phase being turned on by an input signal. The truth table is shown in Table 7.2.1.1. The behavior when H*I=L*I="H" regardless of the period when the gate driver is enabled or disable (gate_en_*="H" or "L") can be selected by pl_op register in CONFIG4.

When pl*_dis bit is “L,” the input prohibition mode is enabled and the output is H*O=L*O=“L.”
At this time, whether the status register is set to “H” or NDIAG=“L” can be selected by pl_op.
When pl_op is set to “H,” set err_pl_* to “H.” When pl_op=“L,” do not set err_pl_* to “H.” NDIAG terminal follows the status register. To turn off a gate driver circuit for driving a 3-phase FET (6ch), drive the gate driver to “L” so that the FET that drives the motor is turned off. Turning off a gate driver circuit for driving a 3-phase FET (2ch) of a detected phase means driving the gate driver to “L” so that the H/L part FET of the detected phase is turned off.
When pl*_dis=“H,” detection of prohibited input itself is disabled, and the output can be H*O=L*O=“H”
For details of the internal signals (gate_en_*) in the truth table, see chapter 7.7.

Table 7.2.1.1 I/O Truth Table (High-side, Low-side drive circuits)

FET Drive Circuit(“*” means u, v and w or U, V and W)

Internal Signal	Input		Register Setting		Output		status	Remarks
(gate_en_*)	H*I	L*I	pl*_dis	pl_op	H*O	L*O	err_pl_*	
“L”	“L”	X	X	X	“L”	“L”	-	Inactive
	X	“L”	X	X			-	
	“H”	“H”	“0”	“0”			-	Prohibited Input Mode, Without Status
			“0”	“1”			“set”	Prohibited Input Mode, With Status
			“1”	X			-	Prohibited Input Mode Disabled (U phase)
“H”	“L”	“L”	X	X	“L”	“L”	-	Active
	“L”	“H”	X	X	“L”	“H”	-	
	“H”	“L”	X	X	“H”	“L”	-	
	“H”	“H”	“0”	“0”	“L”	“L”	-	Prohibited Input Mode, Without Status
			“0”	“1”	“L”	“L”	“set”	Prohibited Input Mode, With Status
			“1”	X	“H”	“H”	-	Prohibited Input Mode Disabled (U phase)

Note: X means “Don’t care”

Note: NDIAG terminal is linked with the status. The status can be cleared by setting err_pl_*_cl bit.

7.2.2. Gate Driver for FET for Reverse Polarity Protection

The gate driver for FET for reverse polarity protection is a circuit that drives FET placed between the battery and 3-phase FETs. Even when the FET for reverse polarity protection is turned off with the battery correctly connected, the battery provides current to 3-phase FETs through the body diode of the FET. When the battery is reversely connected, by turning the FET off via RPPO terminal, reverse current to the battery is shut off. In addition, this product has built in a 500Ω output series resistor and a diode that shuts off reverse current from the ground of the under voltage detection circuit when reversely connected.
This product is equipped with a switch that shuts off current flowing from RPPO terminal to GND via RPPO_UV in the reset state.

Drive Circuit for FET for Reverse polarity Protection (Gate-Drv.RPP)
The drive circuit for FET for reverse polarity protection is configured with a high-side switch. This switch is always ON as long as it has not received a disable signal (gate_dis_rpp).

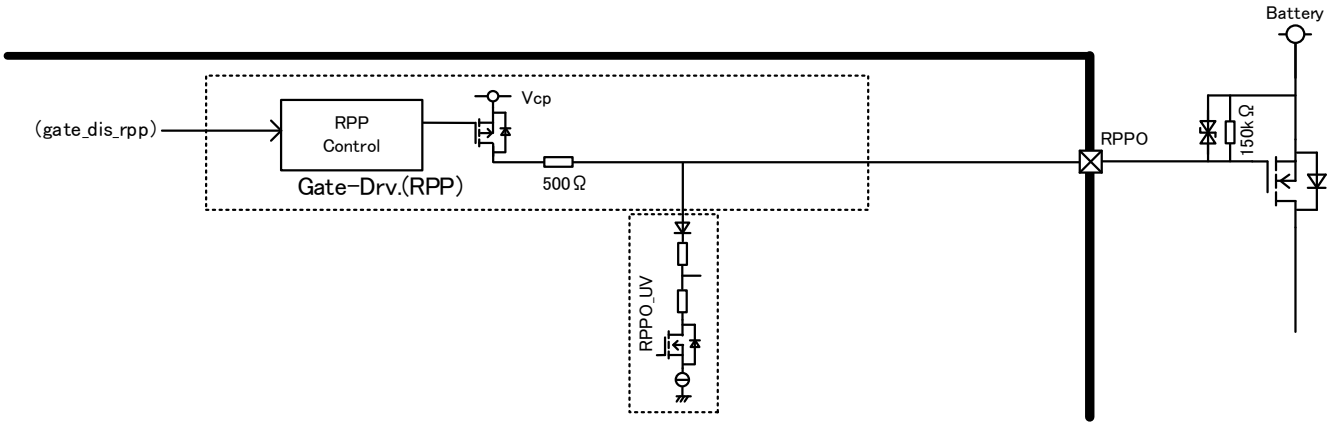


Fig. 7.2.2.1 Gate Driver Circuit for FET for Reverse Polarity Protection

7.3. Current Sensing Circuit

7.3.1. Configuration

This circuit has built in an amplifier for motor current sensing and an amplifier for generating reference voltage. The amplifier for generating reference voltage generates reference voltage based on Vcc voltage.

The motor current sensing amplifier amplifies differential voltage generated by the current flowing in external shunt resistor connected to the GND of the motor drive part. This amplified voltage is output from the reference voltage toward Vcc. Note that the direction of the motor current that can be sensed is from the power supply to GND only.

The gain can be set by SPI communication. The amplified voltage is output from AMP_O, and it is recommended that external low-pass filter is inserted between AMP_O and MCU to reduce noise. Performing calibration with no current flowing in the motor to correct offset variation among individual units improves output voltage accuracy. Note that the input voltage range in which this accuracy improvement can be expected is the one that has considered the voltage operating point of the shunt resistor in normal time. When a resistor is connected to the input terminal, it may cause another gain error.

In addition, this circuit has specific tolerance to noise of VCC power supply and noise around the shunt resistor.

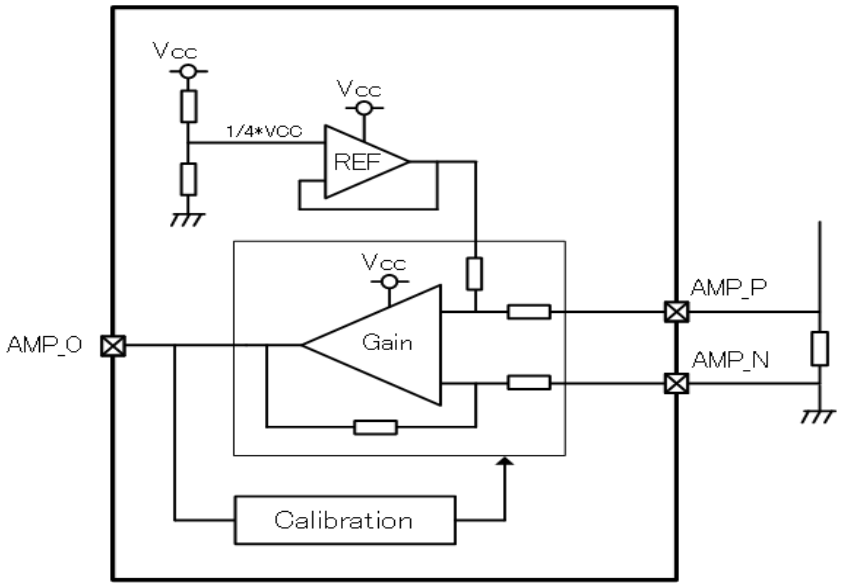


Fig. 7.3.1.1 Motor Current Sensing Circuit Block Diagram

7.3.2. Offset Calibration

Perform offset calibration when the input differential voltage is the same voltage (0V). When the input differential voltage is not zero, the calibration is not performed correctly.

By setting CONFIG5 register: cal_amp="1," calibration is started and cal_en="1." During the calibration, gain_amp ="101" (30 times) (fixed). During calibration, since the offset correction value is being searched for by comparing amplifier output and REF by changing CAL_DAT. When the calibration is completed, cal_en="0" and it is set to cal_pass. When cal_pass="1" is given, the result is kept as it is and used as an adjustment value. When cal_pass="0" is given, the adjustment result is discarded and returned to the default value at reset. When next calibration is started, cal_pass is automatically cleared to "0." By writing "1" to cal_pass_cl bit(STAT1_CLR), cal_pass can be cleared at any time, but CAL_DAT data is maintained. While cal_en is "1," calibration is being performed, and even if cal_amp is set during this period, it is discarded.

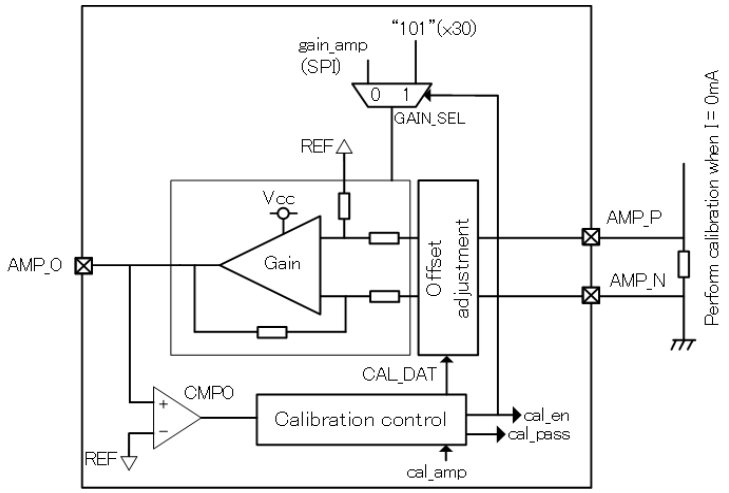


Fig. 7.3.2-1 Offset Calibration Block Diagram

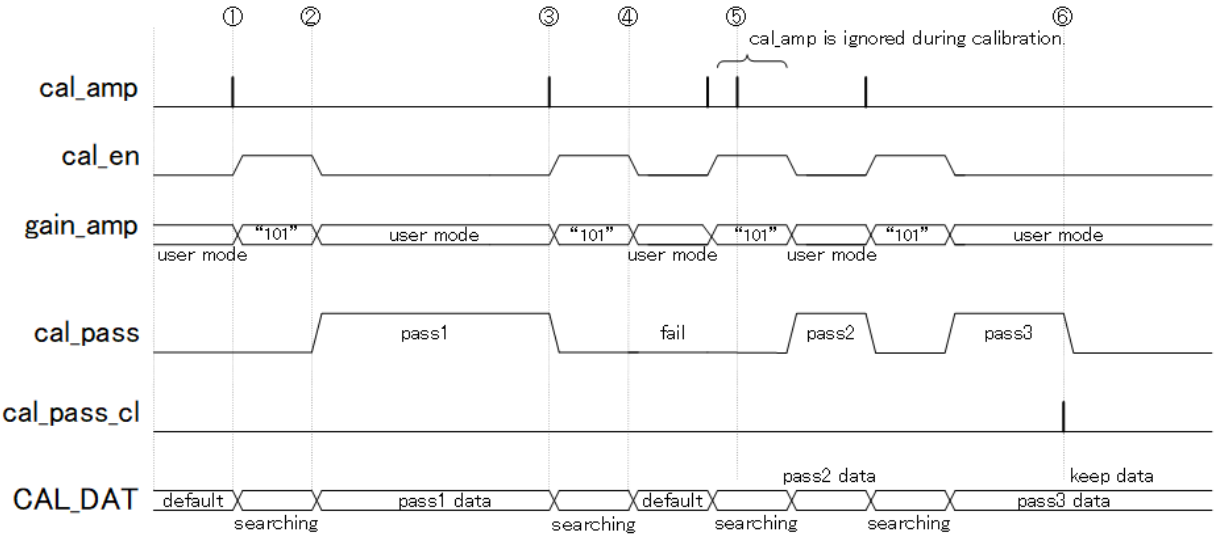


Fig. 7.3.2-2 Performing Offset Calibration

Note: Please note that this product is not equipped with a function that automatically connects AMP_P, and AMP_N terminals to GND.

Note: Since this product adopts a single-shunt configuration, please select components while considering the increase current flowing through the shunt resistor compared to a three-shunt configuration.

7.4. Oscillation Circuit

The oscillation circuit has built-in CR, and its frequency is 4MHz (Typ.).

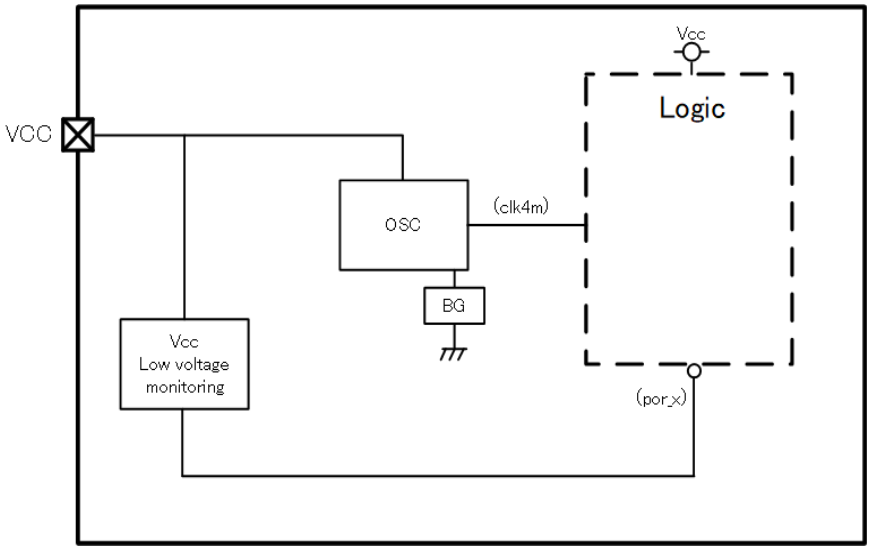


Fig. 7.4.1 Oscillation Circuit Block Diagram

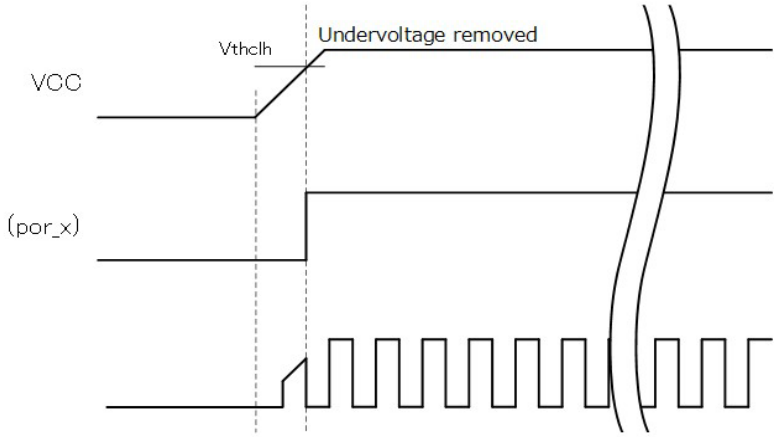


Fig. 7.4.2 Oscillation Circuit Timing Chart

7.5. Abnormality Flag Output Function

7.5.1. NDIAG Terminal Output

When this product does not detect abnormality, NDIAG terminal outputs “H.”
When this product has detected abnormality, NDIAG terminal outputs “L” or “H” depending on SPI communication setting.

Table 7.5.2.1 shows a list of abnormality detection functions in this product. In operation modes with “H” in the NDIAG column, NDIAG terminal does not become “L” even when an abnormality is detected. In operation modes with “L” in the NDIAG column, NDIAG terminal follows the status register of SPI communication (except VCC under voltage detection). While “1” is latched in the status register, NDIAG=“L” is output, and returns to NDIAG=“H” when all status registers are cleared to “0.” In operation modes where the status register is not latched at “1,” NDIAG returns to “NDIAG=“H” when the abnormality detection is resolved even if the status register is not cleared.

To avoid MCU misdetection caused by NDIAG terminal output reversing from “L” to “H” when VCC voltage goes below the under voltage detection criterion, NDIAG terminal maintains “L” until specified VCC voltage.

7.5.2. Status Registers in SPI communication

In settings with “-” in the Status Reg. column in Table 7.5.2.1, the status register does not become “1” even when abnormality is detected.
In settings with a status name in the Status Reg. column, “0” is set when abnormality is not detected, and “1” is set when abnormality is detected.

Status Clear
In settings with “-” in the Status Clear column in Table 7.5.2.1, the status bit is cleared accordingly when abnormality condition leaves.
In settings with a status clear name in the Status Clear column, when “1” is entered into the status register caused by abnormality detection, the bit remains latched after the abnormality leaves (NDIAG remains latched). To clear the latched bit, write “1”for the status clear bit (NDIAG returns to H).
When an abnormality condition doesn’t leave, the latched bit cannot be cleared.
In settings with (Latched) written in the “Operation at Detection” column, it is latched with the written operation. To return to the normal operation when abnormality leaves, clear the status register. In settings with (Latched) not written in the “Operation at Detection” column, the operation accordingly returns to normal when the abnormality leaves even if the status register is not cleared.

Table 7.5.2.1 Abnormality Detection Circuits

Abnormality Detection Circuit	Setting Reg. [Note 1]	Setting bit	Operation at Detection [Note 2] [Note 3]	Initial Value	Status Reg.	Status Clear	NDIAG
VCC under voltage	None	-	All gate drivers of 3-phase drive FETs to off. Turn off charge pump.	-	-	-	“L”
VB under voltage	uvb_op	“0”	All gate drivers of 3-phase drive FETs to off.	-	uvb	uvb_cl	“L”
		“1”	All gate drivers of 3-phase drive FETs to off. Turn off charge pump.	X		-	
VCP over voltage	ovcp_op	“000”	Disable detection.	X	-	-	“H”
		“001”	Continue operation.	-	ovcp	ovcp_cl	“L”
		“010”	All gate drivers of 3-phase drive FETs to off.	-			
		“011”	All gate drivers of 3-phase drive FETs to off (Latched).	-			
		“100”	All gate drivers of 3-phase drive FETs to off. Turn off charge pump.	-			
		“101”	All gate drivers of 3-phase drive FETs to off (Latched).	-			

			Turn off charge pump (Latched)				
VCC over voltage	ovcc_op	“000”	Disable detection.	-	-	-	“H”
		“001”	Continue operation.	-	ovcc	ovcc_cl	“L”
		“010”	All gate drivers of 3-phase drive FETs to off.	-			
		“011”	All gate drivers of 3-phase drive FETs to off (Latched).	X			
		“100”	All gate drivers of 3-phase drive FETs to off. Turn off charge pump.	X			
		“101”	All gate drivers of 3-phase drive FETs to off (Latched). Turn off charge pump (Latched).	-			
RPP under voltage	uvrpp_op	“000”	Disable detection.	-	-	-	“H”
		“001”	Continue operation.	X	uvrpp	uvrpp_cl	“L”
		“010”	All gate drivers of 3-phase and a gate driver of reverse polarity protection drive FETs to off.	X			
		“011”	All gate drivers of 3-phase drive FETs to off.	-			
		“100”	All gate drivers of 3-phase drive FETs to off (Latched).	-			
Thermal shutdown	tsd_op	“000”	Disable detection.	-	-	-	“H”
		“001”	Continue operation.	-	tsd	tsd_cl	“L”
		“010”	All gate drivers of 3-phase drive FETs to off.	X			
		“011”	All gate drivers of 3-phase drive FETs to off (Latched).	-			
		“100”	All gate drivers of 3-phase drive FETs to off. Turn off charge pump.	-			
		“101”	All gate drivers of 3-phase drive FETs to off (Latched). Turn off charge pump (Latched).	-			
Vds of 3-phase FET (High side)	vdsh_op	“000”	Disable detection.	-	-	-	“H”
		“001”	Continue operation.	-	vds_uh vds_vh vds_wh	vds_uh_cl vds_vh_cl vds_wh_cl	“L”
		“010”	H/L gate drivers of detected phase drive FETs to off	-			
		“011”	H/L gate drivers of detected phase drive FETs to off (Latched).	-			
		“100”	All gate drivers of 3-phase drive FETs to off.	-			
		“101”	All gate drivers of 3-phase drive FETs to off (Latched).	X			
		“110”	All gate drivers of 3-phase drive FETs to off. Turn off charge pump.	-			
		“111”	All gate drivers of 3-phase drive FETs to off (Latched). Turn off charge pump (Latched).	-			
Vds of 3-phase FET (Low side)	vdsl_op	“000”	Disable detection.	-	-	-	“H”
		“001”	Continue operation.	-	vds_ul vds_vl vds_wl	vds_ul_cl vds_vl_cl vds_wl_cl	“L”
		“010”	H/L gate drivers of detected phase drive FETs to off	-			
		“011”	H/L gate drivers of detected phase drive FETs to off (Latched).	-			
		“100”	All gate drivers of 3-phase drive FETs to off.	-			
		“101”	All gate drivers of 3-phase drive FETs to off (Latched).	X			
		“110”	All gate drivers of 3-phase drive FETs to off. Turn off charge pump.	-			
		“111”	All gate drivers of 3-phase drive FETs to off (Latched). Turn off charge pump (Latched).	-			
CP1SW,	cpsw_de	“0”	Continue operation	X	cp1sw	cp1sw	“L”

CP2SW terminal abnormality detection	t_op	“1”	All gate drivers of 3-phase drive FETs to off. Turn off charge pump (Latched).	-	_det cp2sw _det	_det_cl cp2sw _det_cl	
Gate driver prohibited input	pl_op	“0”	In the case of pl*_dis=”L”, H/L gate drivers of detected phase as prohibited input drive FETs to off.	X	-	-	“H”
		“1”		-	err_pl_u err_pl_v err_pl_w	err_pl_u_cl err_pl_v_cl err_pl_w_cl	“L”

[Note 1] The value of the setting register “xxxx_op” for each detection function can be changed at any time, but the “xxxx_op” setting is not reflected in the actual operation while the status register for its respective detection function is indicating that abnormality has been detected.

[Note 2] When the charge pump is turned off, the internal driver is stopped and voltage around VB is output at VCP terminal.

[Note 3] When all (7ch) gate driver circuits are turned off, the gate drivers are driven to “L” so that 3-phase FETs are turned off, and the high side switch is turned off so that the FET for reverse polarity protection is turned off. When gate driver circuits (6ch) for driving 3-phase FETs are turned off, the gate drivers are driven to “L” so that the FETs that drive the motor are turned off. When gate driver circuits (2ch) for driving 3-phase FETs of a detected phase are turned off, the gate drivers are driven to “L” so that both high side and low side FETs of the detected phase are turned off.

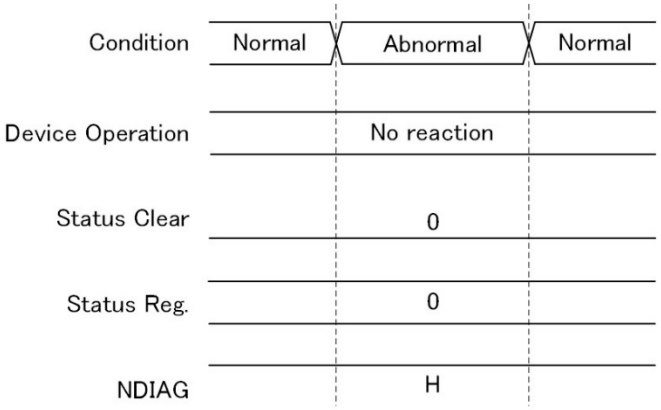


Fig. 7.5.2.1 When Status Reg. is “-” and Status Clear is “-”

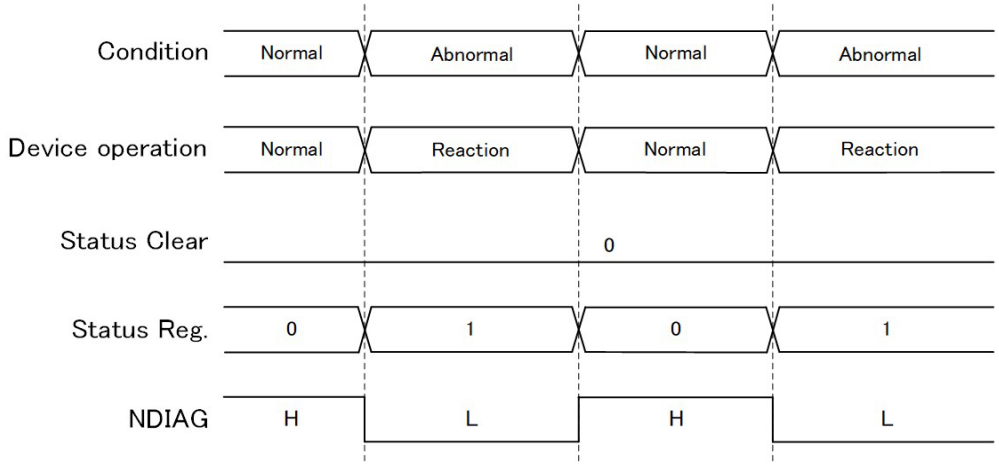


Fig. 7.5.2.2 When Operation at Detection is not “(Latched),” a bit name is in Status Reg. column, and no bit name is in Status Clear column

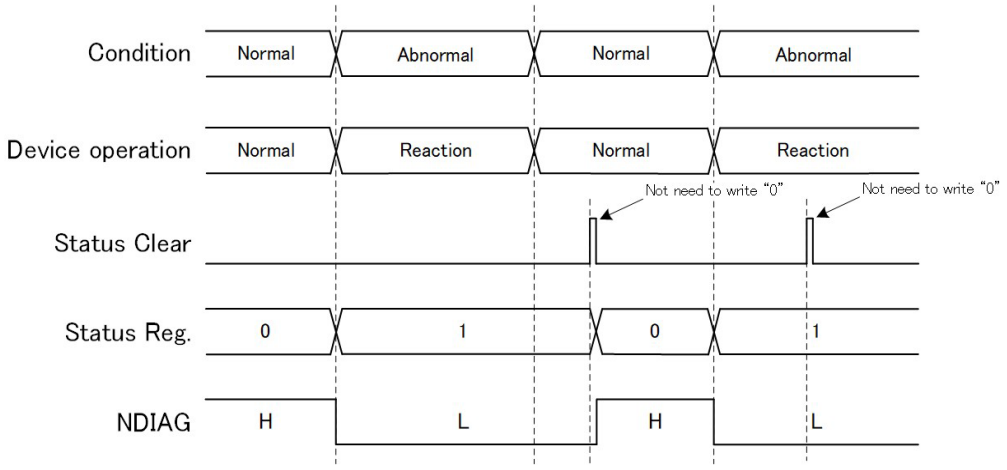


Fig. 7.5.2.3 When Operation at Detection is not "(Latched)," a bit name is in Status Reg. column, and a bit name is in Status Clear column

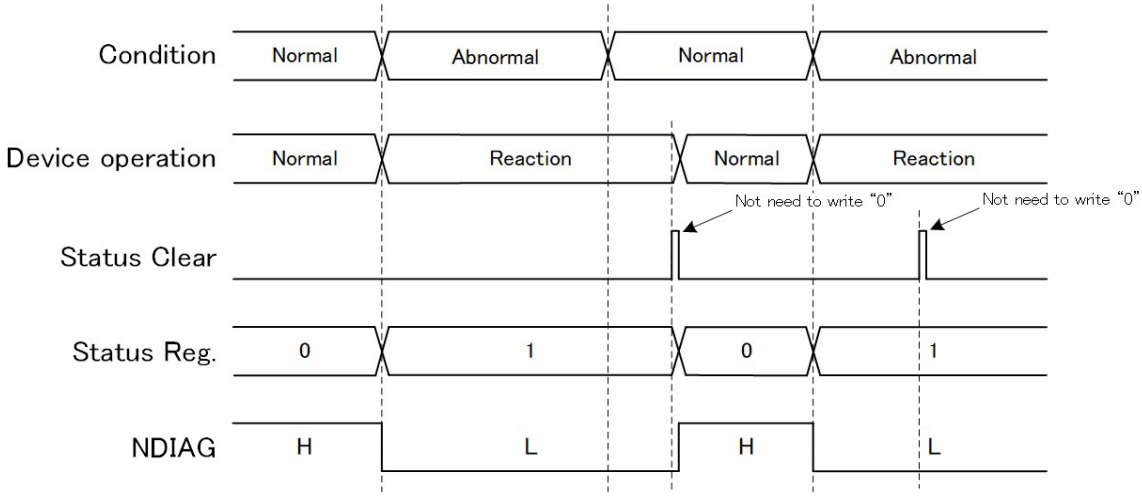


Fig. 7.5.2.4 When Operation at Detection is "(Latched)," a bit name is in Status Reg. column, and a bit name is in Status Clear column

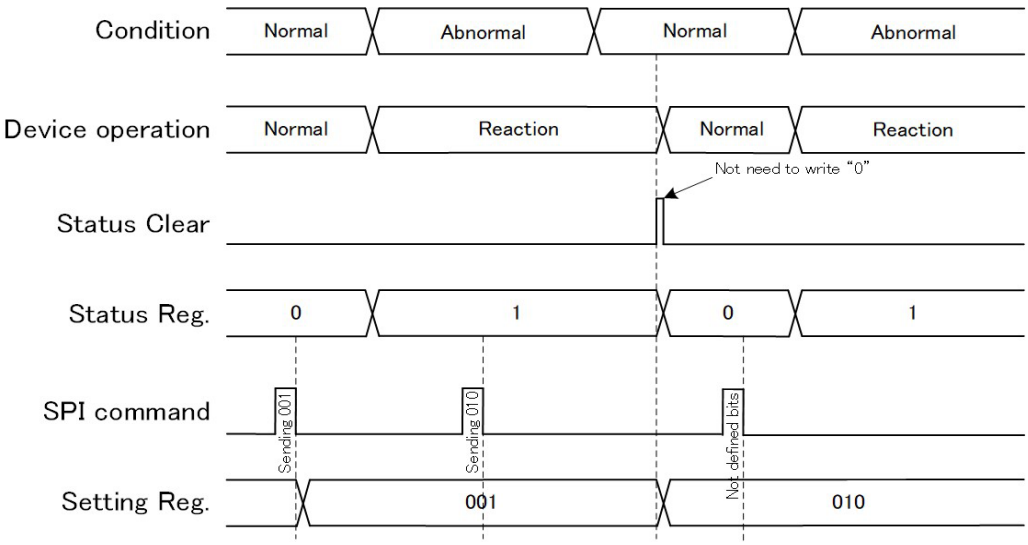


Fig. 7.5.2.5 How to Change Setting Reg.

7.6. Abnormality Detection Circuits

7.6.1. VCC Under Voltage Detection Function

The VCC under voltage detection circuit monitors voltage at VCC terminal to detect l under voltage. After detection, this product goes into a reset state. The detection comparator has hysteresis to prevent its output from chattering at the time of detection and detection release. In addition, this circuit ignores noise superimposed on VCC with a response time of 20us (Typ.).

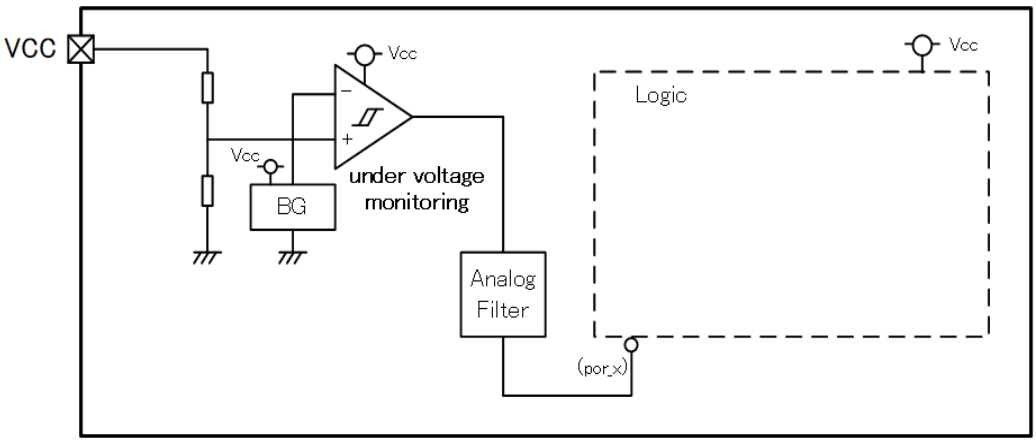


Fig. 7.6.1.1 VCC Under Voltage Detection Block Diagram

(1)VCC voltage goes down

When VCC voltage goes below the detected under voltage Vthcll, detection operation is started.

(2)VCC under voltage is detected

After a response time of Tcl, (por_x)="L," NDIAG="L" is output, and the gate driver circuits for driving 3-phase FETs are turned off. Until the under voltage is released, each circuit maintains its off state.

(3)VCC voltage recovers (Under voltage release)

When VCC voltage goes above Vthclh, the under voltage is released and (por_x)="H,"

Soon after that, charge pump circuit starts operation and the gate driver circuit for driving the FET for reverse polarity protection is turned on.

After Tpre_en has passed from (por_x)="H," NDIAG="H" is output, and the gate driver circuits for driving 3-phase FETs follow input signals.

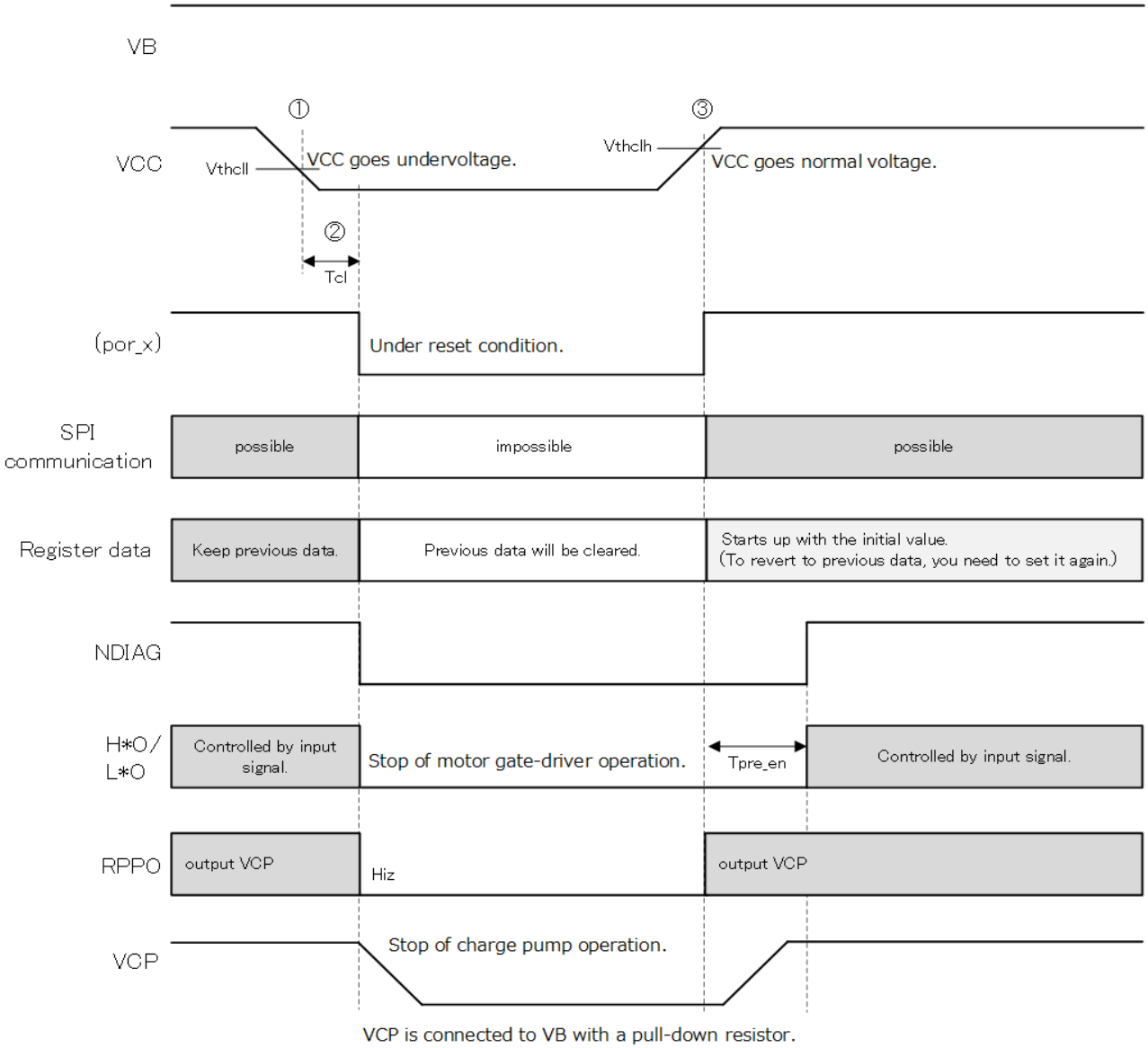


Fig. 7.6.1.2 VCC Under Voltage Detection Timing Chart

Note: When Vcc reaches the under voltage threshhold, this product goes into a reset state. Since the set values in digital circuits (such as set values using SPI) are cleared, resetting is required after the reset state is released.

Note: When Vcc under voltage is detected and the charge pump circuit is turned off, and NDIAG becomes "H" after Tpre_en has passed since the release of Vcc under voltage release, the motor operation is enabled.

7.6.2. VB Under Voltage Detection Function

The VB under voltage detection circuit monitors voltage at VB terminal to detect under voltage. The detection comparator has hysteresis to prevent its output from chattering at the time of detection and detection release. In addition, this circuit ignores noise superimposed on VB with a detection filtering time of 20us (Typ.).

In addition, SPI communication allows the operations below.

- Set operation after an abnormality has been detected.
- Read abnormality detection flag.
- Clear abnormality detection flag.

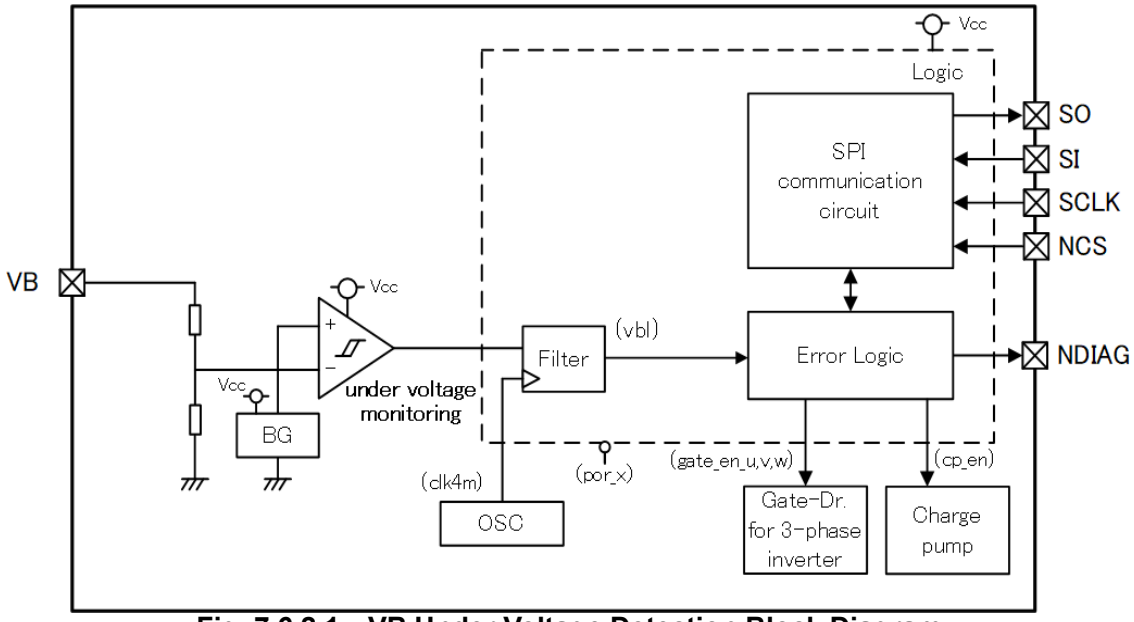


Fig. 7.6.2.1 VB Under Voltage Detection Block Diagram

(1)VB voltage goes down

When VB voltage goes below the detected under voltage Vthbll, detection operation is started.

(2)VB under voltage is detected

After a detection filtering time of Tbl has passed, a under voltage state is detected by VB under voltage detection signal (vbl)="H," the status register: uvb="1" and "NDIAG="L."

The operation after detection can be selected between 2 modes via SPI communication.

The gate driver circuit for driving the FET for reverse polarity protection maintains its ON state.

In the case of register: uvb_op="0," gate driver circuits for driving 3-phase FETs are turned off.

In the case of register: uvb_op="1," the charge pump and gate driver circuits for driving 3-phase FETs are turned off.

Even if setting is changed during detection, the change is not effective, and after the detection is released and register: uvb is cleared, the changed setting becomes effective.

While under voltage is detected, register: uvb cannot be cleared, and NDIAG remains "L".

(3)VB voltage recovers (Under voltage release)

When VB voltage goes above Vthblh, it results in VB under voltage detection signal (vbl)="L," and under voltage is released.

In the case of register: uvb_op="0," the status register: uvb="1" and NDIAG="L" are latched, and gate drivers for driving 3-phase FETs follow input signals. When register: uvb is cleared by SPI communication, after Tpre_en has passed, NDIAG="H. is output"

In the case of register: uvb_op="1," status register: uvb="0," NDIAG="H," and the charge pump circuit automatically recovers, and the gate driver circuits for driving 3-phase FETs follow the input signals.

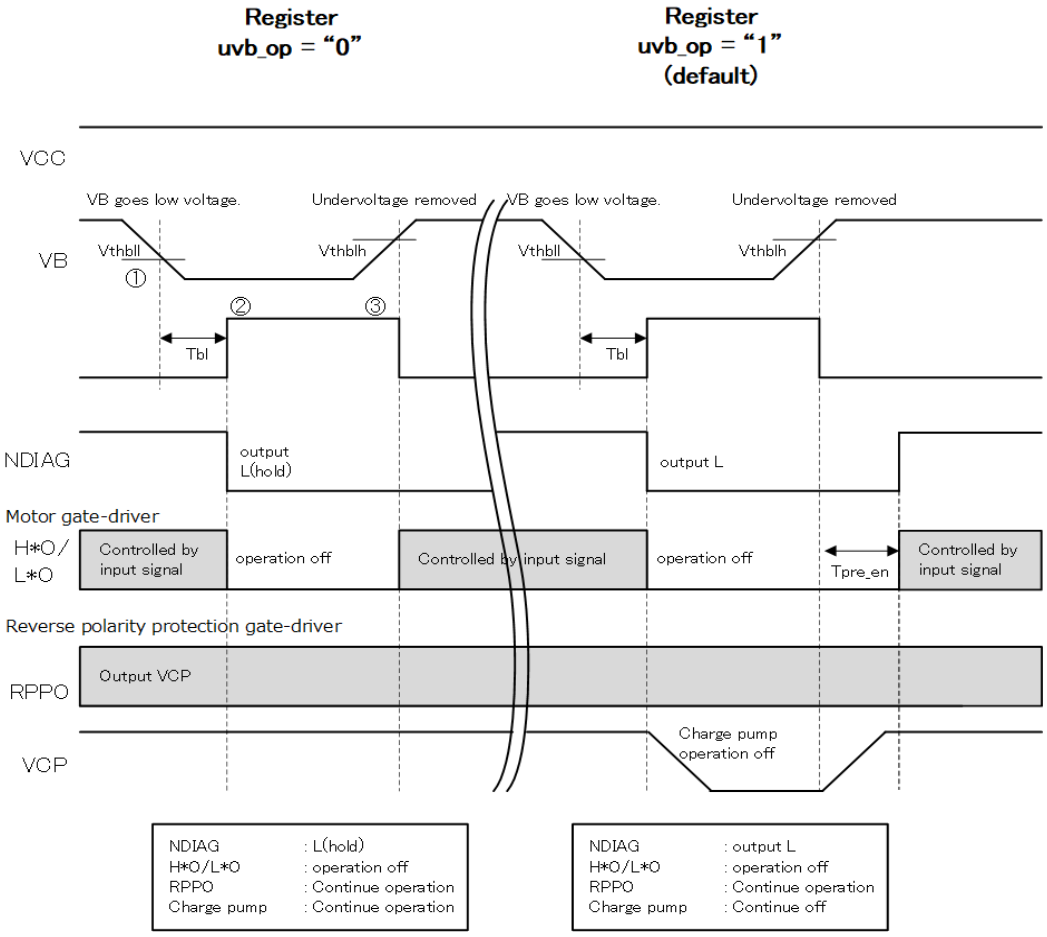


Fig. 7.6.2.2 VB Under Voltage Detection Timing Chart

Note: When Vb under voltage is detected and the charge pump circuit is turned off, and NDIAG becomes "H" after Tpre_en has passed since a release fo the Vb under voltage, the motor operation is enabled.

7.6.3. RPPO Under Voltage Detection Function

The RPPO under voltage detection circuit monitors differential voltage between Vcp voltage and RPPO voltage to detect insufficient driving state for the FET for reverse polarity protection. The detection comparator has hysteresis to prevent its output from chattering at the time of detection and detection release. In addition, this circuit ignores noise superimposed on RPPO terminal with a detection filtering time of 20us (Typ.).

In addition, SPI communication allows the operations below.

- Set operation after an abnormality has been detected.
- Read abnormality detection flag.Clear abnormality detection flag.

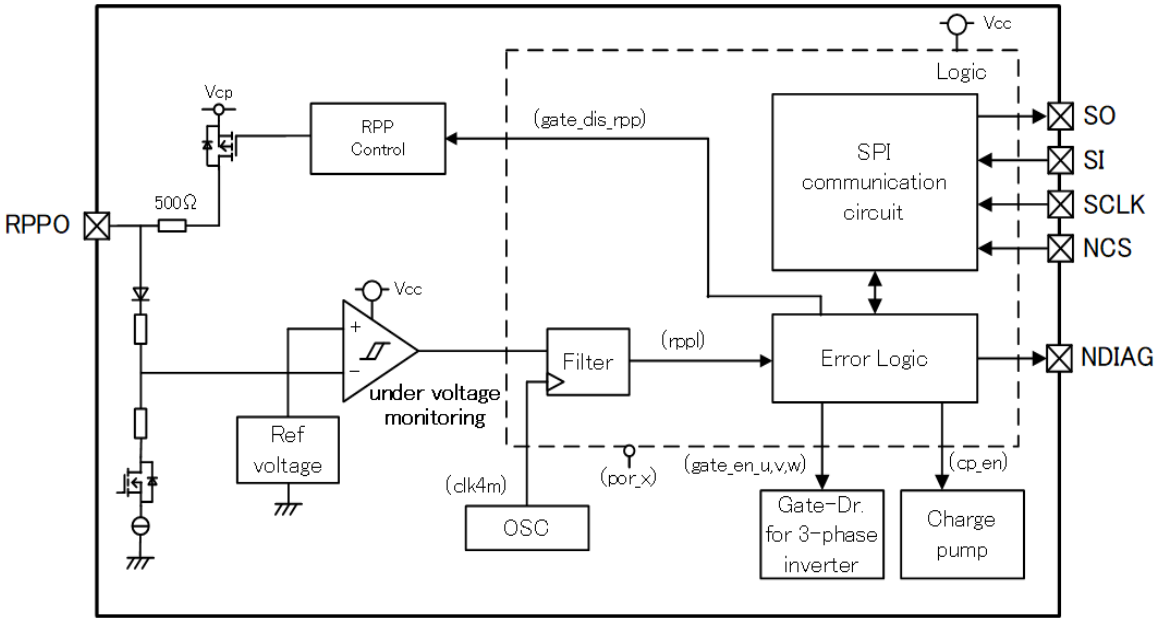


Fig. 7.6.3.1 RPPO Under Voltage Detection Block Diagram

(1)RPPO voltage goes down

Vcp voltage and RPPO voltage are compared, and when the difference goes below the detected under voltage Vthrppll, the detection operation is started.

(2)RPPO under voltage is detected

After a detection filtering time of Trppl has passed, a under voltage state is detected by RPPO under voltage detection signal (rppl)="H", resulting in the status register: uvrpp="1" and NDIAG="L."

The detection operation can be selected among 5 modes via SPI communication.

Note that in the case of register: uvrpp_op ="000," detection is disabled, and the status register: uvrpp="0" and NDIAG="H" are maintained, and each circuit continues its normal operation.

Whether RPPO terminal continues to be ON or is turned off after RPPO under voltage is detected can be selected by register setting.

Even if setting is changed during detection, the change is not effective, and after the detection is released and register: uvrpp is cleared, the changed setting becomes effective.

While under voltage is detected, register: uvrpp cannot be cleared, and NDIAG remains "L".

(3)RPPO voltage recovers (Under voltage release)

When register: uvrpp_op="010" is output and under voltage is detected, RPPO terminal is also turned off. So, to recovery the state, VCC needs to be turned off once and turned on after a certain period. In this case, in a period of por_x (L) and a period of Tpre_en (L), differential voltage between VCP voltage and RPPO voltage can be generated. So, the detection is disabled.

When register: uvrpp_op="011" is output and RPPO voltage is above Vthrpplh, it results in RPPO under voltage detection signal (rppl)="L" and the under voltage is released.

In the case of register: uvrpp_op ="100," gate drivers for driving 3-phase FETs stay in their OFF state, and the status register: uvrpp="1" and NDIAG="L" are latched even when the under voltage is released.

When register: uvrpp is cleared by SPI communication, each circuit operates normally and NDIAG="H" is output

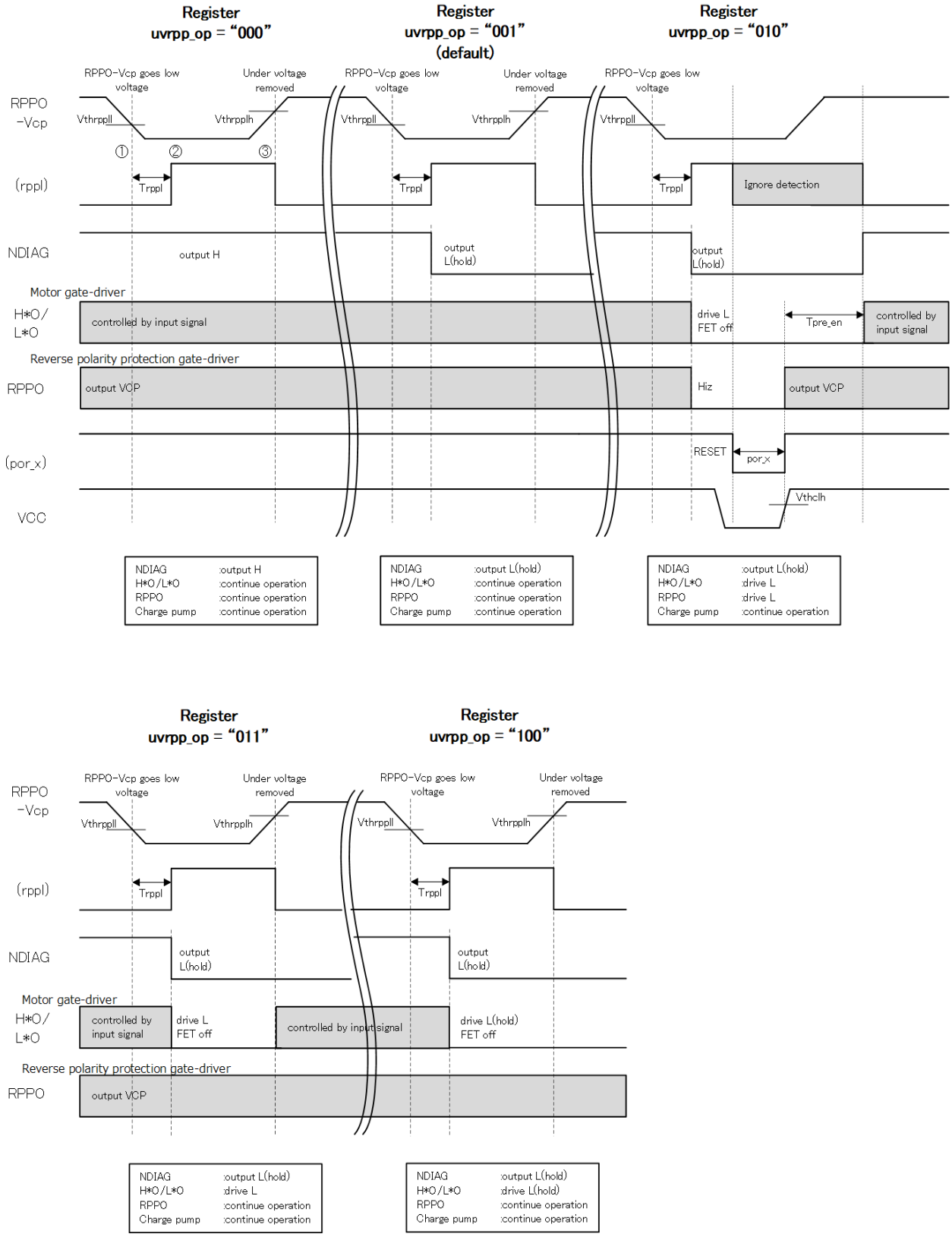


Fig. 7.6.3.2 RPPO Under Voltage Detection Timing Chart

Note: When RPPO under voltage is detected and Vcc is reset, the charge pump circuit is turned off. When Tpre_en has passed since a release of Vcc reset and NDIAG becomes "H," the motor operation is enabled.

7.6.4. VCC Over Voltage Detection Function

The VCC over voltage detection circuit monitors voltage at VCC terminal to detect over voltage. The detection comparator has hysteresis to prevent its output from chattering at the time of detection and detection release. In addition, this circuit ignores noise superimposed on VCC terminal with a detection filtering time of 20us (Typ.).
In addition, SPI communication allows the operations below.

- Set operation after an abnormality has been detected.
- Read abnormality detection flag.
- Clear abnormality detection flag.

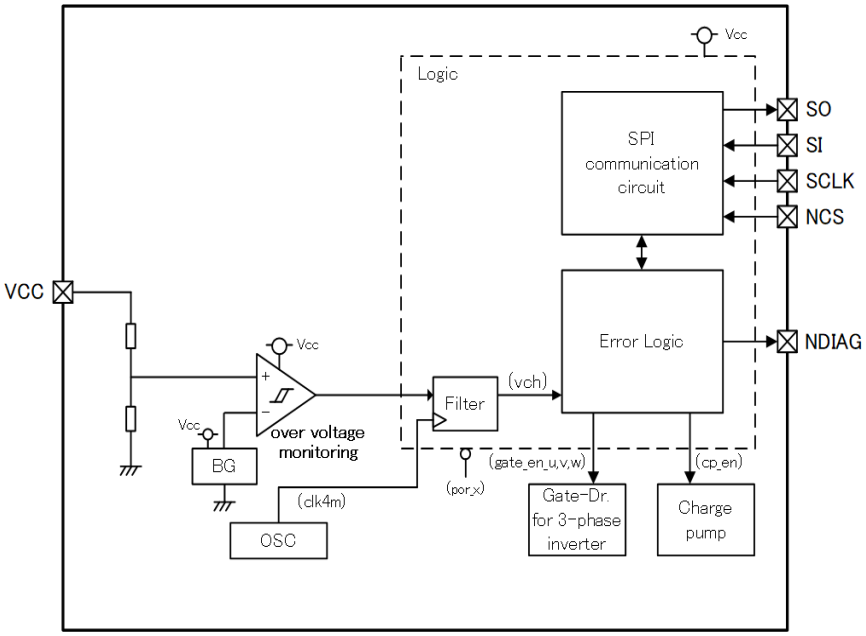


Fig. 7.6.4.1 VCC Over Voltage Detection Block Diagram

(1)VCC voltage increases.

When VCC voltage goes above the detected over voltage Vthchh, detection operation is started.

(2)VCC over voltage is detected.

After a detection filtering time of Tch has passed, an over voltage state is detected by VCC over voltage detection signal (vch)="H," resulting in the status register: ovcc="1" and NDIAG="L."
Operation after detection can be selected from 6 modes via SPI communication.
In the case of register: ovcc_op="001", each circuit continues its normal operation even when VCC over voltage is detected, but NDIAG="L" is latched.
However, in the case of register: ovcc_op="000," even when VCC over voltage has been detected, NDIAG="H" is output and each circuit continues its normal operation.
Even if setting is changed during detection, the change is not effective, and after the detection is released and register: ovcc is cleared, the changed setting becomes effective.
While over voltage is detected, register: ovcc cannot be cleared and NDIAG remains "L".

(3)VCC voltage recovers (Over voltage release)

When VCC voltage going below Vthchl, it results in VCC over voltage detection signal (vch)="L" and the over voltage is released.
In the case of register: ovcc_op="010" and the over voltage is released, gate drivers return to their normal operation, but NDIAG="L" remains latched.
In the case of register: ovcc_op="011" even when the over voltage is released, OFF state of gate drivers remains latched and NDIAG="L" remains latched.
In the case of register: ovcc_op ="100" and the over voltage is released, the charge pump and gate drivers return to their normal operation, but NDIAG="L" remains latched.
In the case of register: ovcc_op ="101" even when the over voltage is released, OFF states of the charge pump and gate drivers remain latched and NDIAG="L" remains latched.
When register: ovcc is cleared by SPI communication, each circuit operates normally and NDIAG="H" is output.

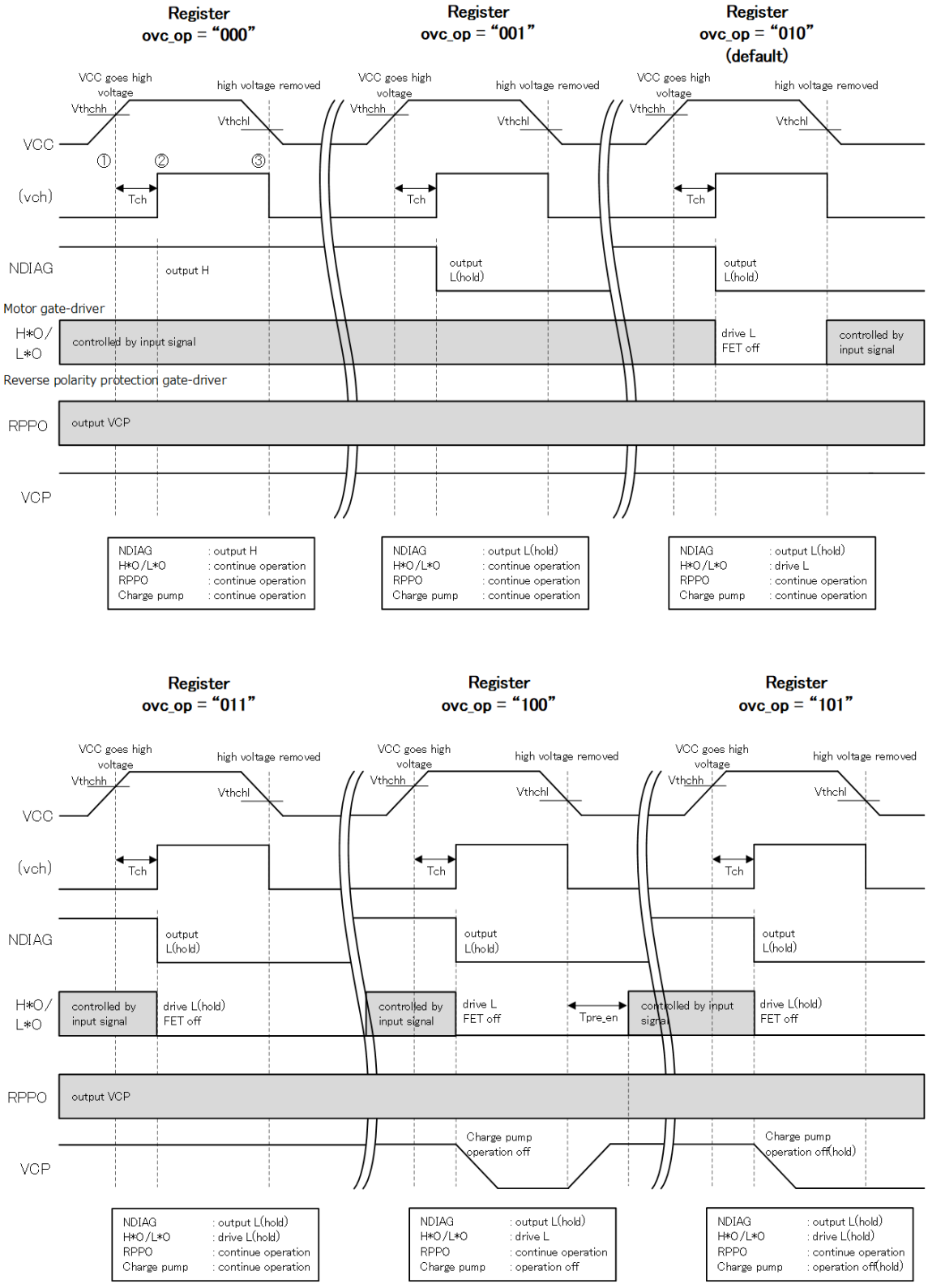


Fig. 7.6.4.2 VCC Over Voltage Detection Timing Chart

Note: When Vcc over voltage is detected and the charge pump circuit is turned off, and NDIAG becomes "H" after Tpre_en period has passed since the Vcc over voltage detection was released, the motor operation is enabled.

7.6.5. VCP Over Voltage Detection Function

To avoid excessive over voltage applied on elements, this circuit detects over voltage of charge pump voltage VCP. The detection comparator has hysteresis to prevent its output from chattering at the time of detection and detection release. In addition, this circuit ignores noise superimposed on RPPO terminal with a detection filtering time of 20us (Typ.).
In addition, SPI communication allows the operations below.

- Set operation after an abnormality has been detected.
- Read abnormality detection flag.
- Clear abnormality detection flag.

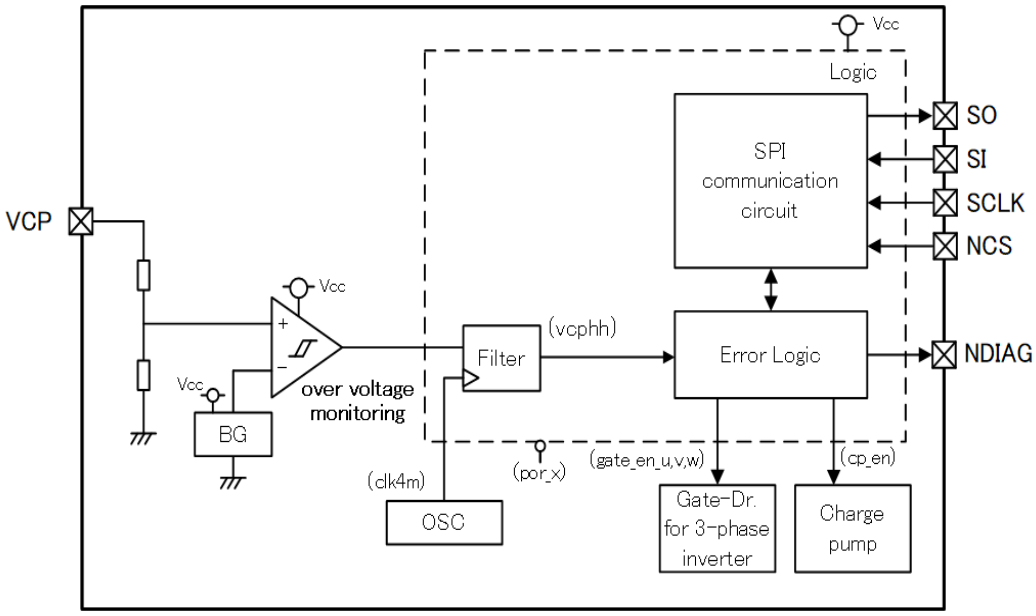


Fig. 7.6.5.1 VCP Over Voltage Detection Block Diagram

(1)VCP voltage increases.
When VCP voltage goes above the detected over voltage Vthcphh, detection operation is started.
(2)VCP over voltage is detected.
After a detection filtering time of Tcph has passed, an over voltage state is detected by VCP over voltage detection signal (vcp)="H", resulting in the status register: ovcp="1" and NDIAG="L".
Operation after detection can be selected from 6 modes via SPI communication.
In the case of register: ovcp_op="001", each circuit continues its normal operation even when VCP over voltage is detected, but NDIAG="L" is latched.
However, in the case of register: ovcp_op="000," even when VCP over voltage is detected, NDIAG="H" is output and each circuit continues its normal operation.
Even if setting is changed during detection, the change is not effective, and after the detection is released and register: ovcp is cleared, the changed setting becomes effective.
While over voltage is detected, register: ovcp cannot be cleared and NDIAG remains "L".
(3)VCP voltage recovers. (Over voltage release)
When VCP voltage goes below Vthcphl, it results in VCP over voltage detection signal (vcp)="L," and the over voltage is released.
In the case of register: ovcp_op="010" and the over voltage is released, gate drivers return to their normal operation, but NDIAG="L" remains latched.
In the case of register: ocph_op="011," even when the over voltage is released, OFF state of gate drivers remains latched and NDIAG="L" remains latched.
In the case of register: ocph_op="100" and the over voltage is released, the charge pump and gate drivers return to their normal operation, but NDIAG="L" remains latched.
In the case of register: ocph_op="101," even when the over voltage is released, OFF states of the charge pump and gate drivers remain latched and NDIAG="L" remains latched.
When register: ovcp is cleared by SPI communication, each circuit operates normally and NDIAG="H" is output.

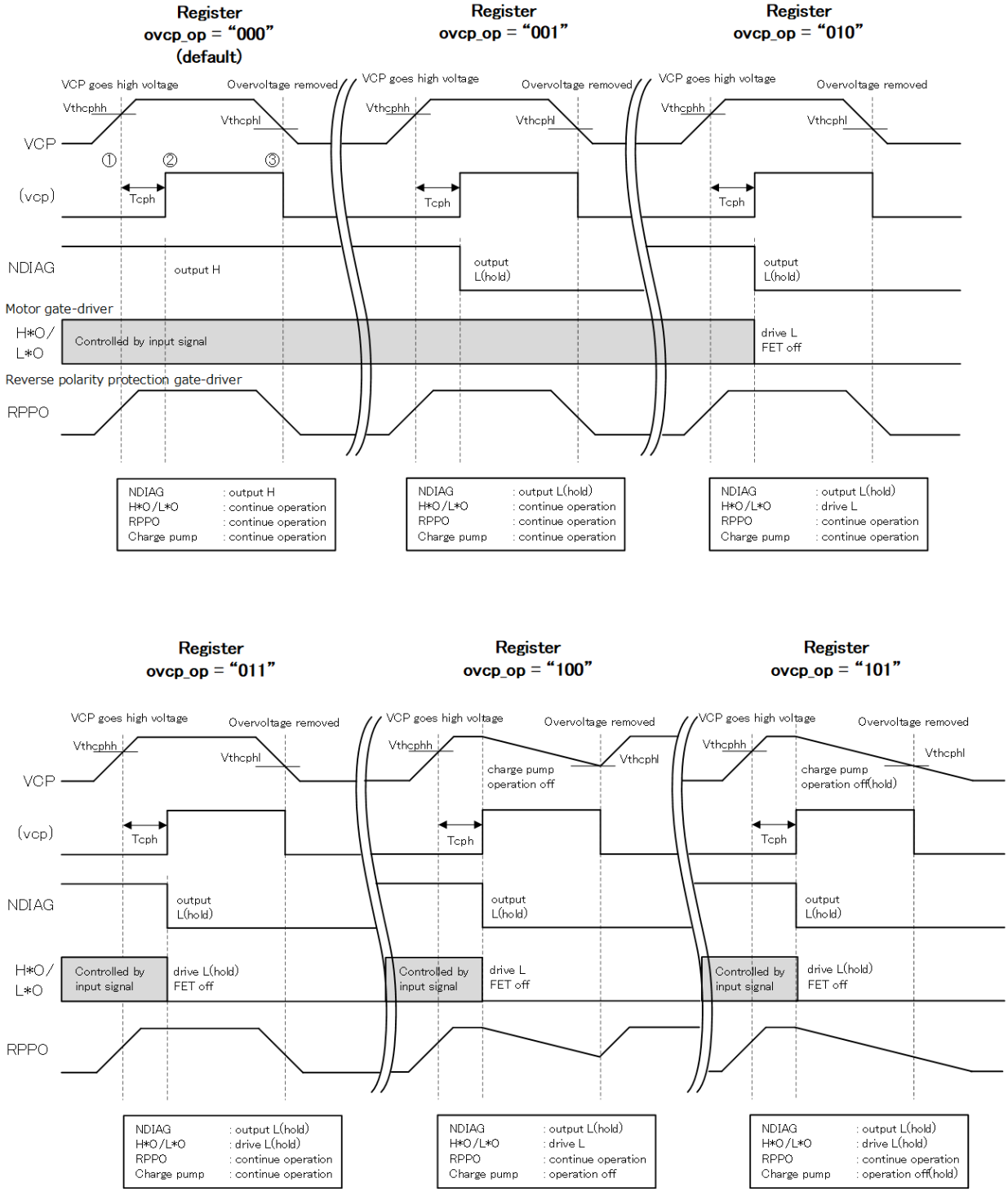


Fig. 7.6.5.2 VCP Over Voltage Detection Timing Chart

7.6.6. Over temperature Detection Function

The detection comparator has hysteresis to prevent its output from chattering at the time of detection and detection release. In addition, this circuit ignores noise superimposed on an internal node with a detection filtering time of 20us (Typ.) SPI communication allows the operations below.

- Set operation after abnormality has been detected.
- Read abnormality detection flag.
- Clear abnormality detection flag.

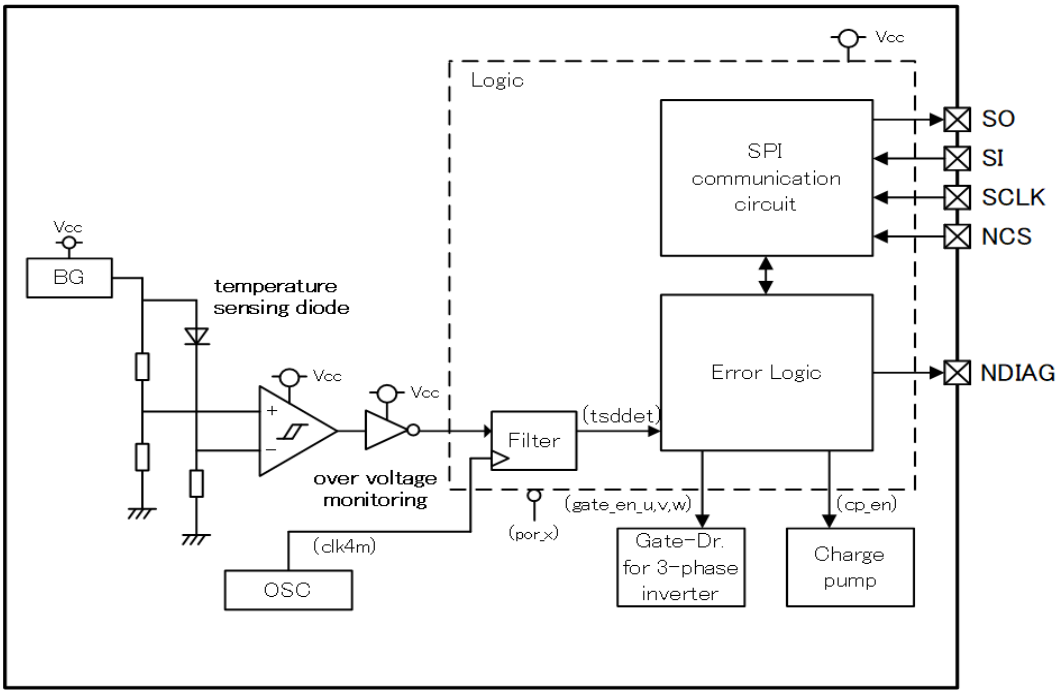


Fig. 7.6.6.1 Over Temperature Detection Block Diagram

(1)Chip temperature rises.

When the temperature monitored by a sensor in this product goes above Tsdh, the detection operation is started.

(2)Over temperature is detected.

After a detection filtering time of Ttsd has passed, an over temperature state is detected by over temperature detection signal (tsddet)="H," resulting in the status register: tsd="1," and "NDIAG="L".

Operation after detection can be selected from 6 modes via SPI communication.

In the case of register: tsd_op="001", each circuit continues its normal operation even when over temperature is detected, but NDIAG="L" is latched.

However, in the case of register: tsd_op="000," even when over temperature is detected, NDIAG="H" is output and each circuit continues its normal operation.

Even if setting is changed during detection, the change is not effective, and after the detection is released and register: tsd is cleared, the changed setting becomes effective.

While over temperature is detected, register: tsd cannot be cleared and NDIAG remains "L".

(3)Over temperature detection is released.

When the temperature goes below Tsdl, it results in over temperature detection signal (tsddet)="L," and over temperature detection is released.

In the case of register: tsd_op="010" and the over temperature is released, gate drivers return to their normal operation, but NDIAG="L" remains latched.

In the case of register: tsd_op="011," even when the over temperature is released, OFF state of gate drivers remains latched and NDIAG="L" remains latched.

In the case of register: tsd_op="100" and the over temperature is released, the charge pump and gate drivers return to their normal operation, but NDIAG="L" remains latched.

In the case of register: tsd_op="101," even when the over temperature is released, OFF states of the charge pump and gate drivers remain latched and NDIAG="L" remains latched.

When register: tsd is cleared by SPI communication, each circuit operates normally and NDIAG="H" is output.

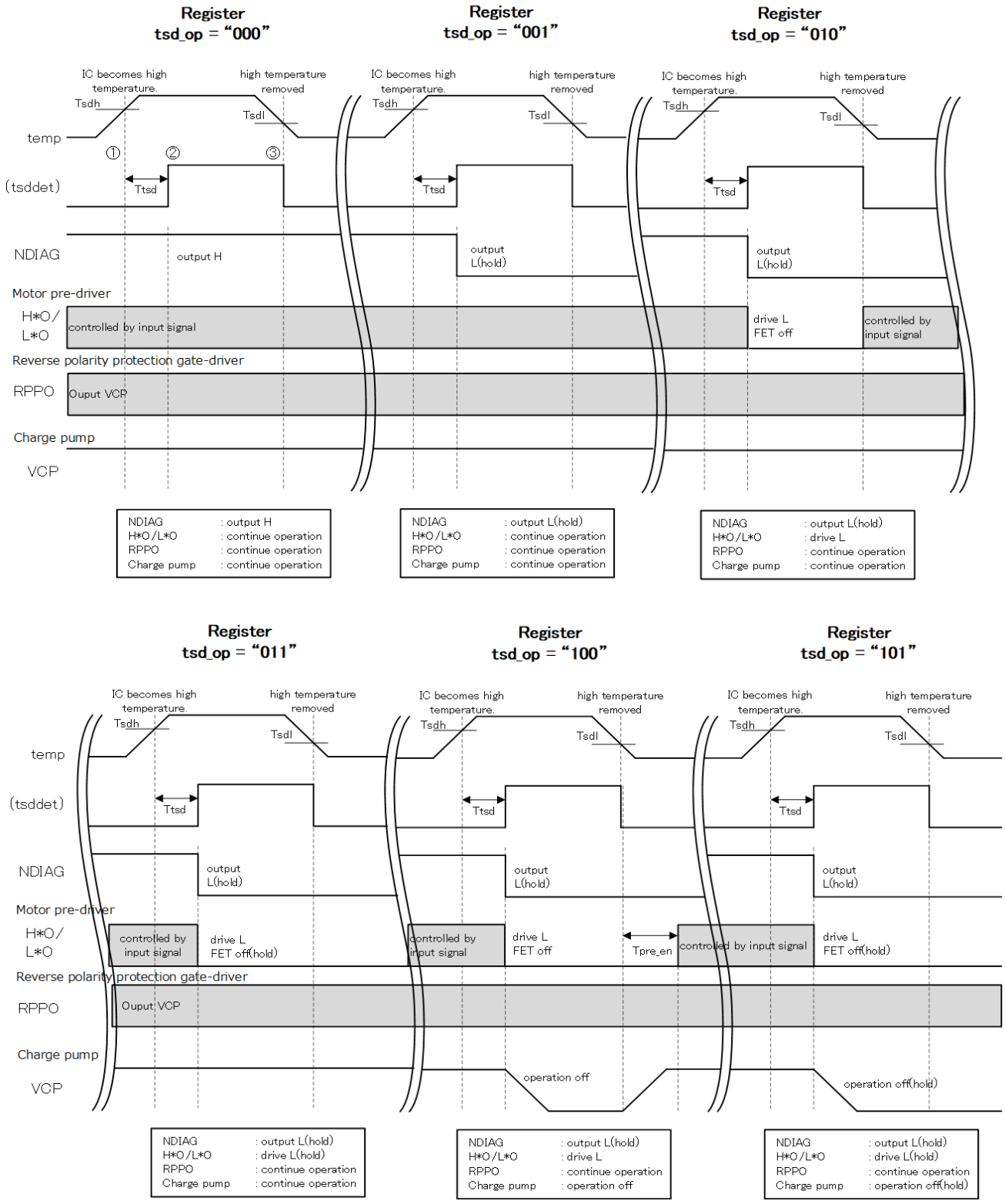


Fig. 7.6.6.2 Over Temperature Detection Timing Chart

Note: When over temperature is detected and the charge pump circuit is turned off, after Tpre_en has passed since the over temperature was released, the motor operation is enabled.

7.6.7. VDS Detection Function for 3-Phase FETs

In ON state operation of 3-phase FETs, differential voltage between HS and H*S terminals of this product is monitored for high-side FETs and differential voltage between H*S and LS terminals of this product is monitored for low-side FETs to detect abnormality. The threshold voltage can be set by SPI communication for high-side FETs and low-side FETs each. In addition, to avoid detecting a state before reaching a complete ON state, a mask time after the input terminal receives an ON command has been prepared, and this time can be set by SPI communication. Higher voltage than the threshold voltage is detected as abnormal and “1” is stored at the status register for each phase and for each side.

Operation after abnormality has been detected can be set by SPI communication (CONFIG2). Two types of setting are available: the OFF state of gate driver circuits for driving 3-phase FETs is not latched and it is latched. In the former type as well, the gate driver circuits for driving 3-phase FETs remains latched their OFF state while the input terminal is receiving “H.” In addition, in the “latched” setting, the “1” of the status register needs to be cleared to return to the normal operation.
In addition, SPI communicaton (CONFIG4) can enable/disable detection for each phase.

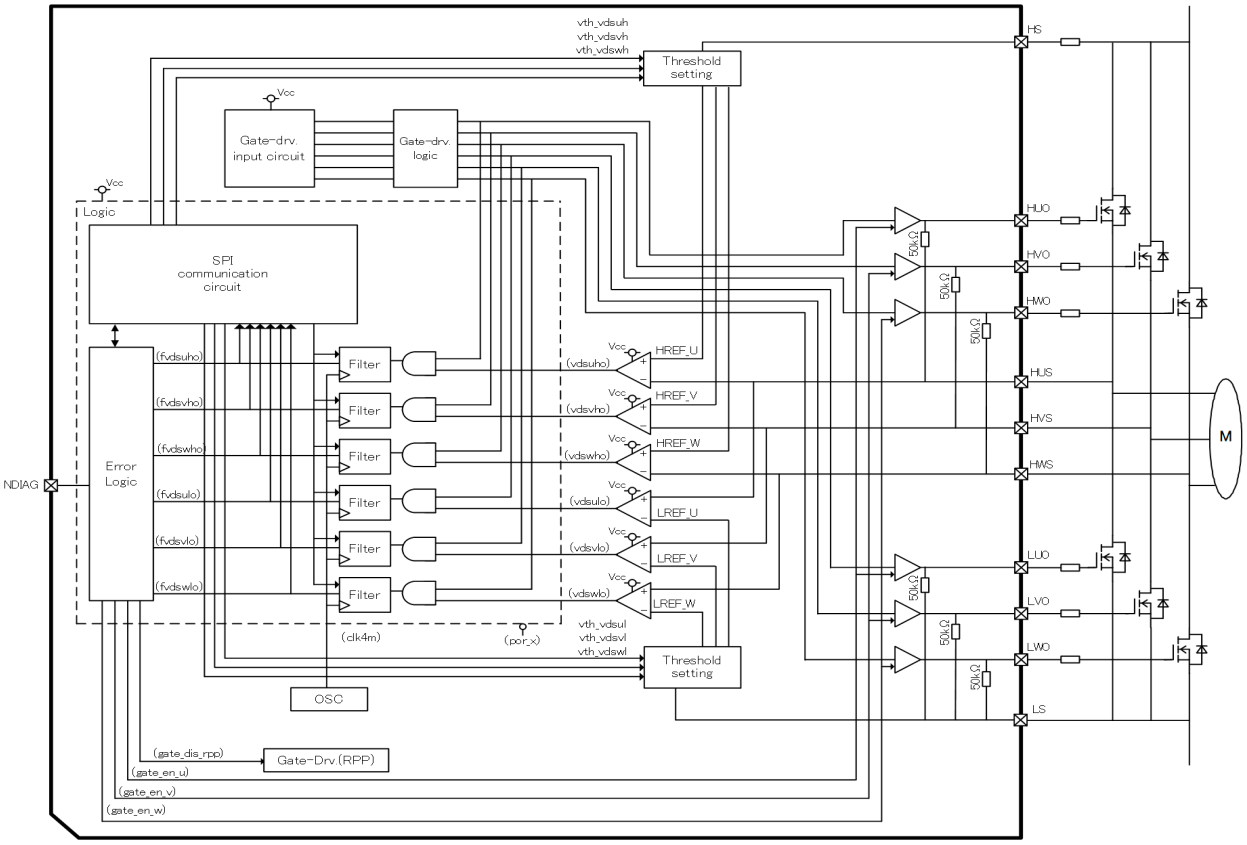


Fig. 7.6.7.1 Block Diagram of VDS Detection for 3-Phase FETs

Table 7.6.7.1 VDS Detection Scenarios

Comparison by Comparator	Comparator Output	Input Signal	Abnormal State
V_{HUS}-V_{LS} > $V_{thvdsul}$	(vdsulo) = “H”	LUI = “H”	FET VDS abnormal at LUO
V_{HVS}-V_{LS} > $V_{thvdsvl}$	(vdsvlo) = “H”	LVI = “H”	FET VDS abnormal at LVO
V_{HWS}-V_{LS} > $V_{thvdswl}$	(vdswlo) = “H”	LWI = “H”	FET VDS abnormal at LWO
V_{HS}-V_{HUS} > $V_{thvdsuh}$	(vdsuho) = “H”	HUI = “H”	FET VDS abnormal at HUO
V_{HS}-V_{HVS} > $V_{thvdsvh}$	(vdsvho) = “H”	HVI = “H”	FET VDS abnormal at HVO
V_{HS}-V_{HWS} > $V_{thvdswh}$	(vdswho) = “H”	HWI = “H”	FET VDS abnormal at HWO

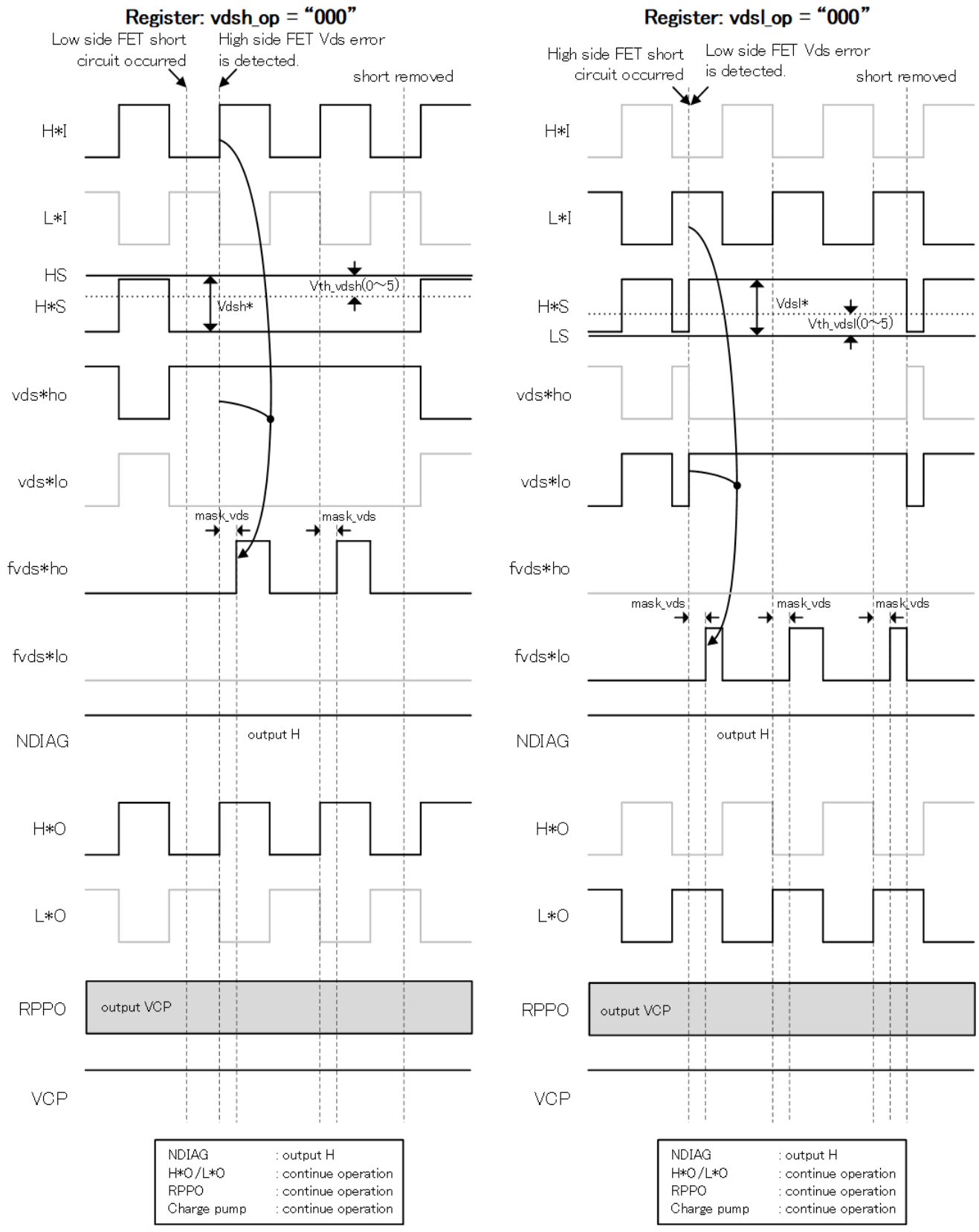


Fig. 7.6.7.2 Short-Circuit Detection Timing Chart (In the case of register: vdsl_op = vdsh_op "000")

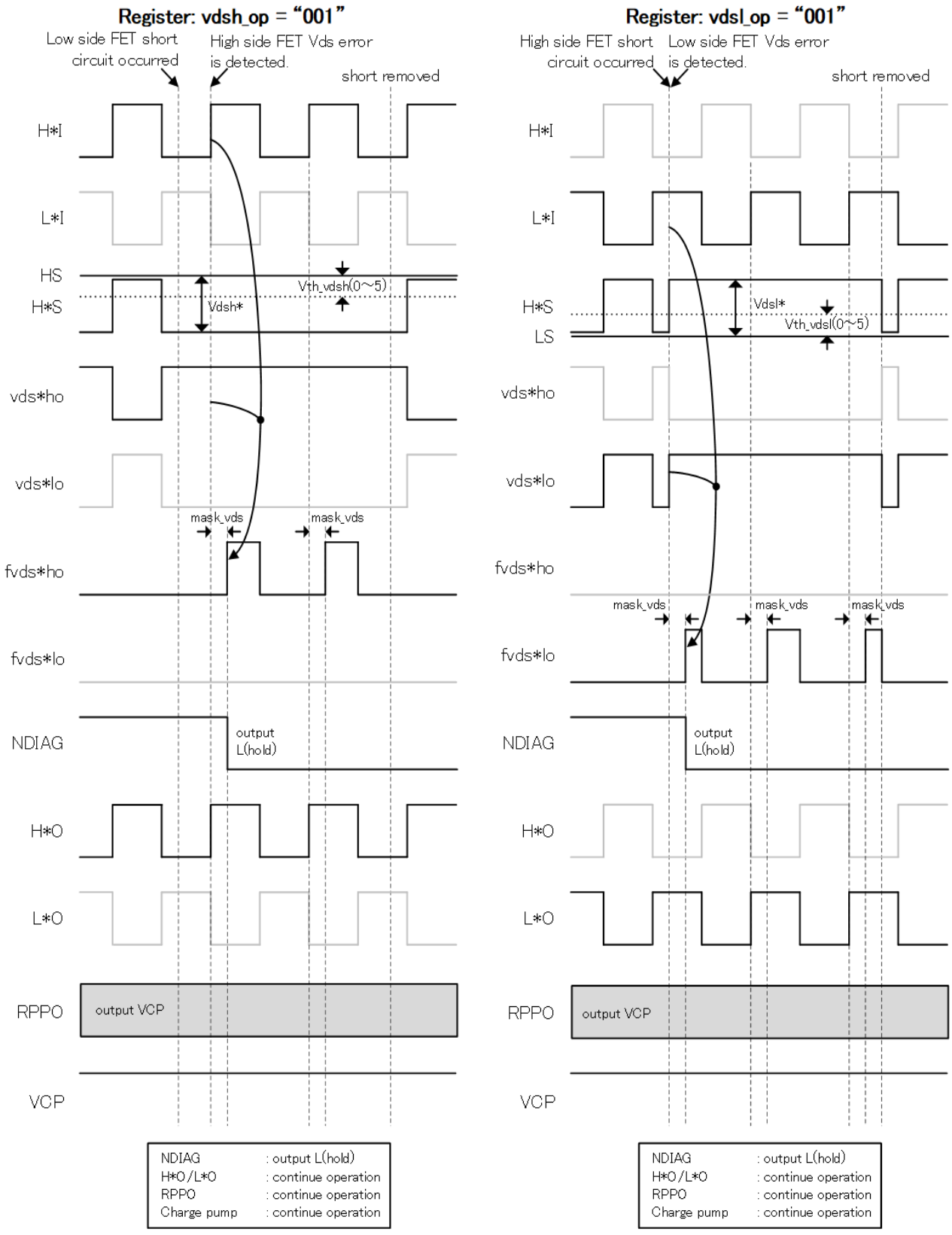


Fig. 7.6.7.3 Short-Circuit Detection Timing Chart (In the case of register: vdsl_op = vdsh_op "001")

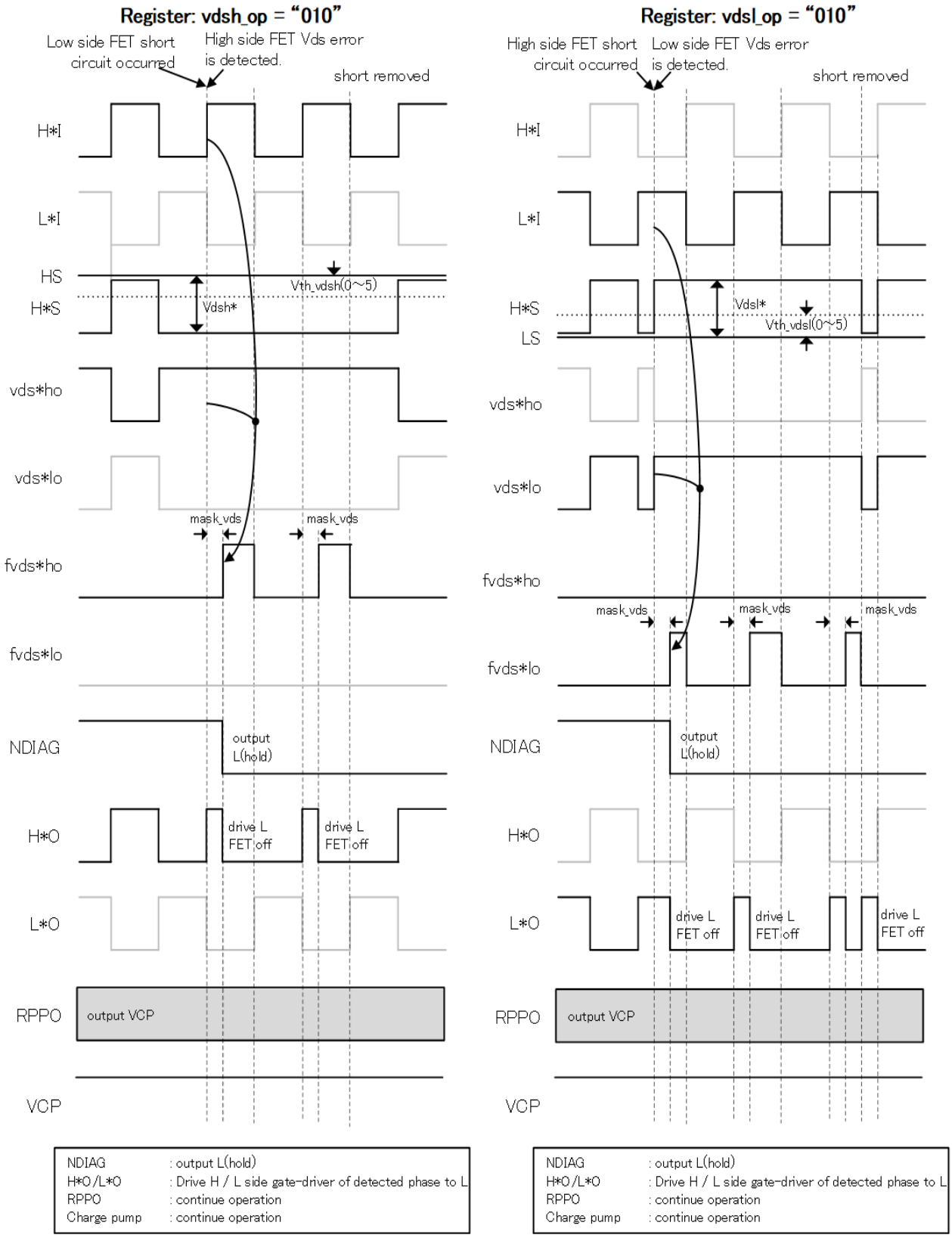


Fig. 7.6.7.4 Short-Circuit Detection Timing Chart (In the case of register: vdsl_op = vdsh_op "010")

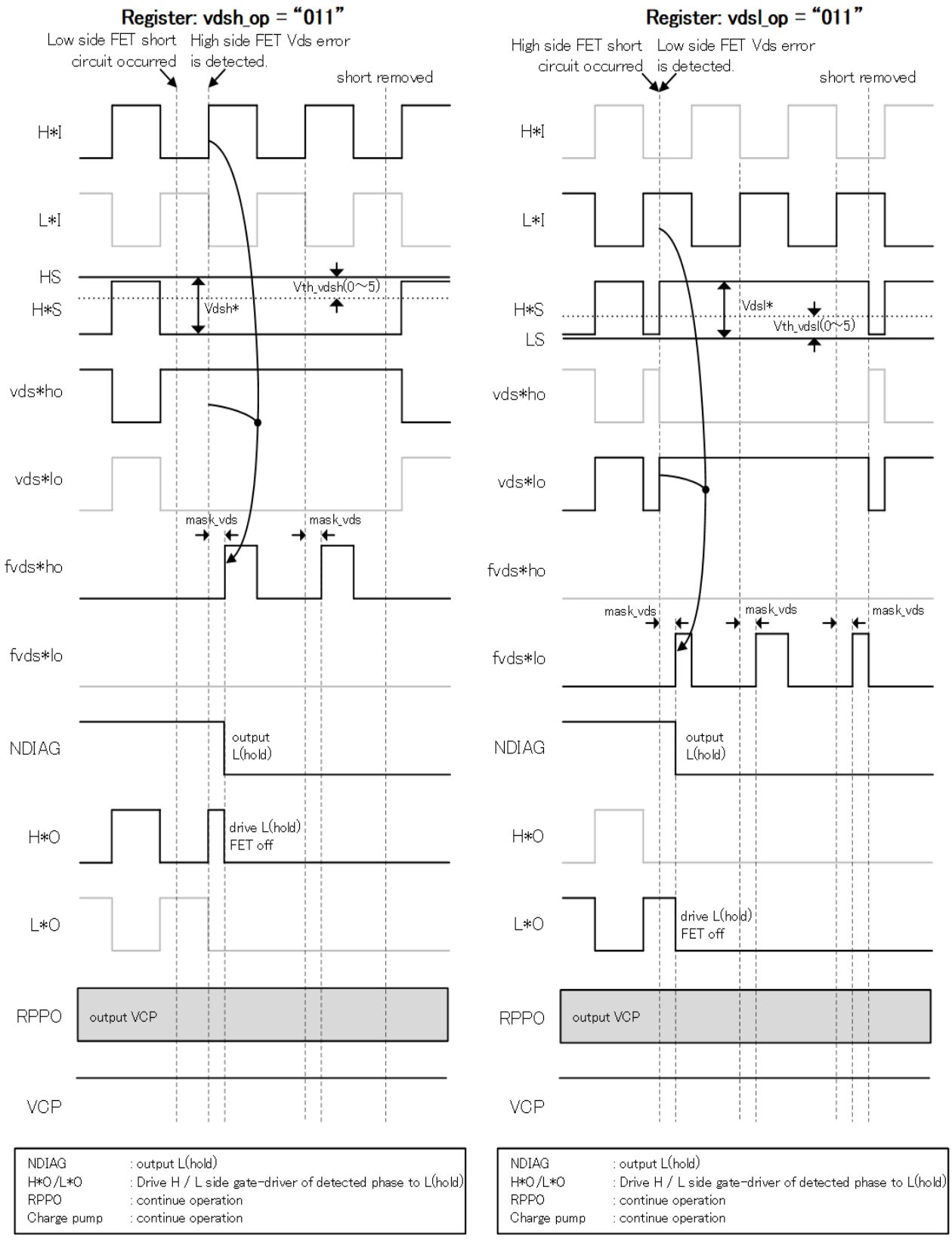


Fig. 7.6.7.5 Short-Circuit Detection Timing Chart (In the case of register: vdsl_op = vdsh_op "011")

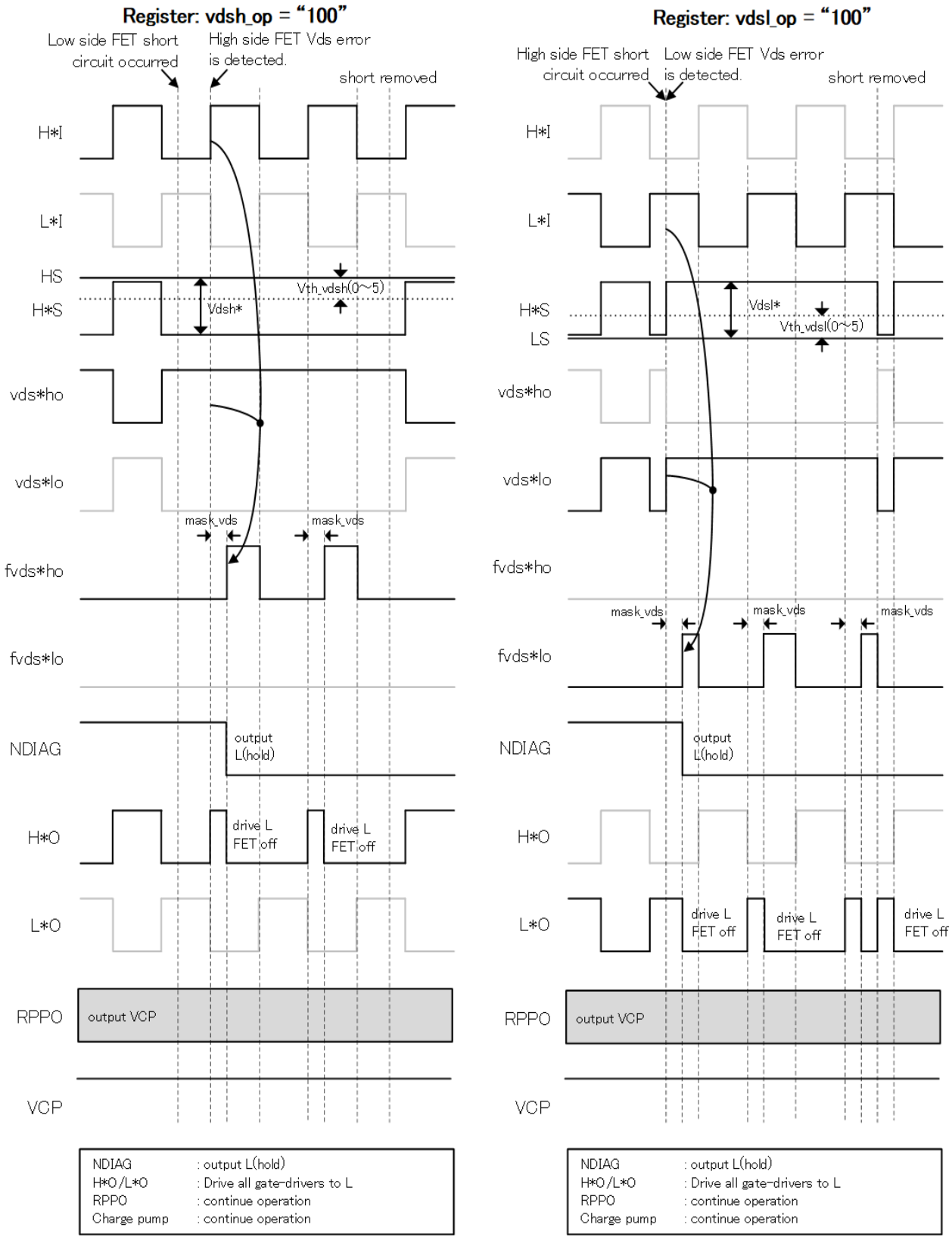


Fig. 7.6.7.6 Short-Circuit Detection Timing Chart (In the case of register: vdsl_op = vdsh_op "100")

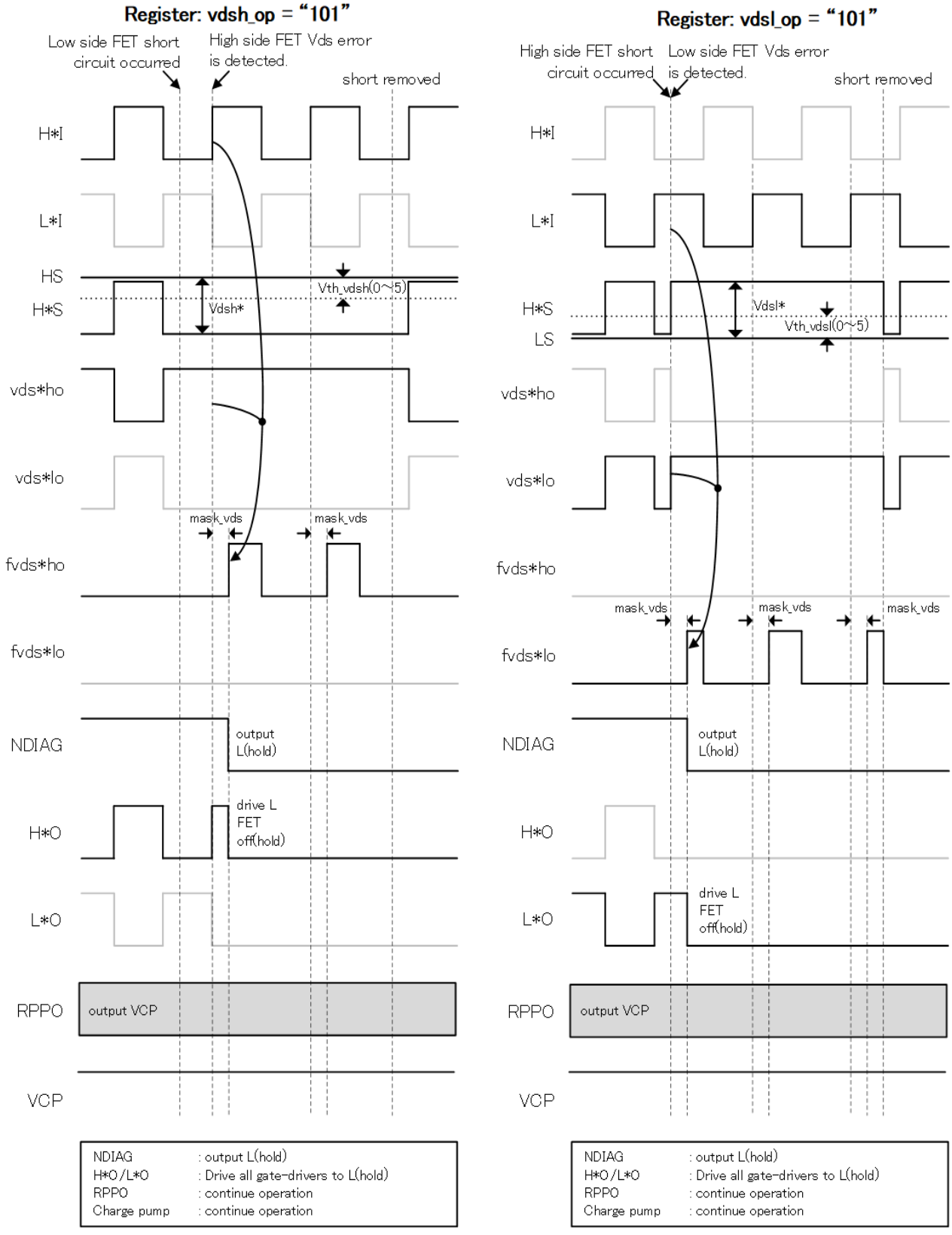


Fig. 7.6.7.7 Short-Circuit Detection Timing Chart (In the case of register: vdsl_op = vdsh_op "101")

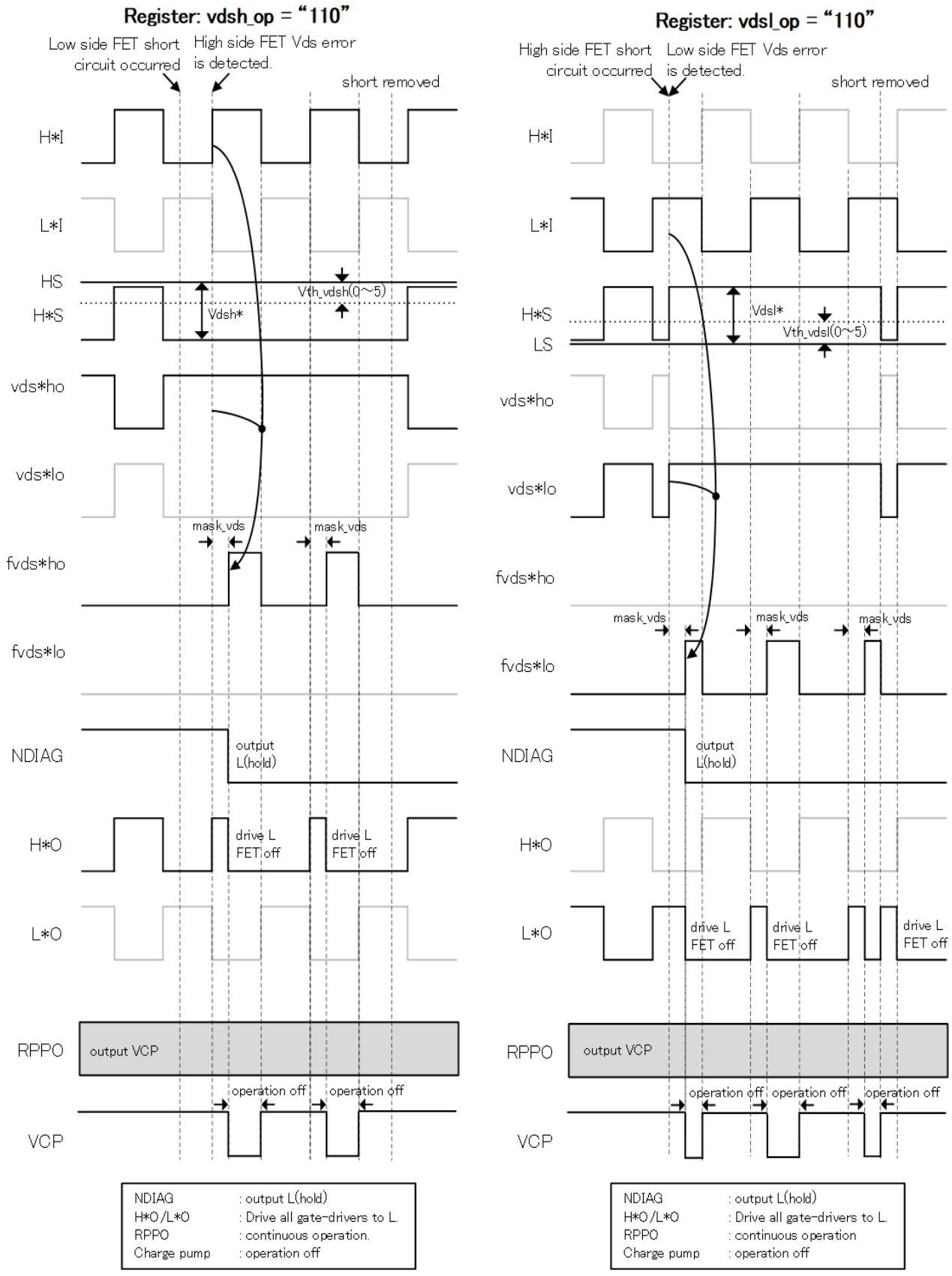


Fig. 7.6.7.8 Short-Circuit Detection Timing Chart (In the case of register: vdsl_op = vdsh_op "110")

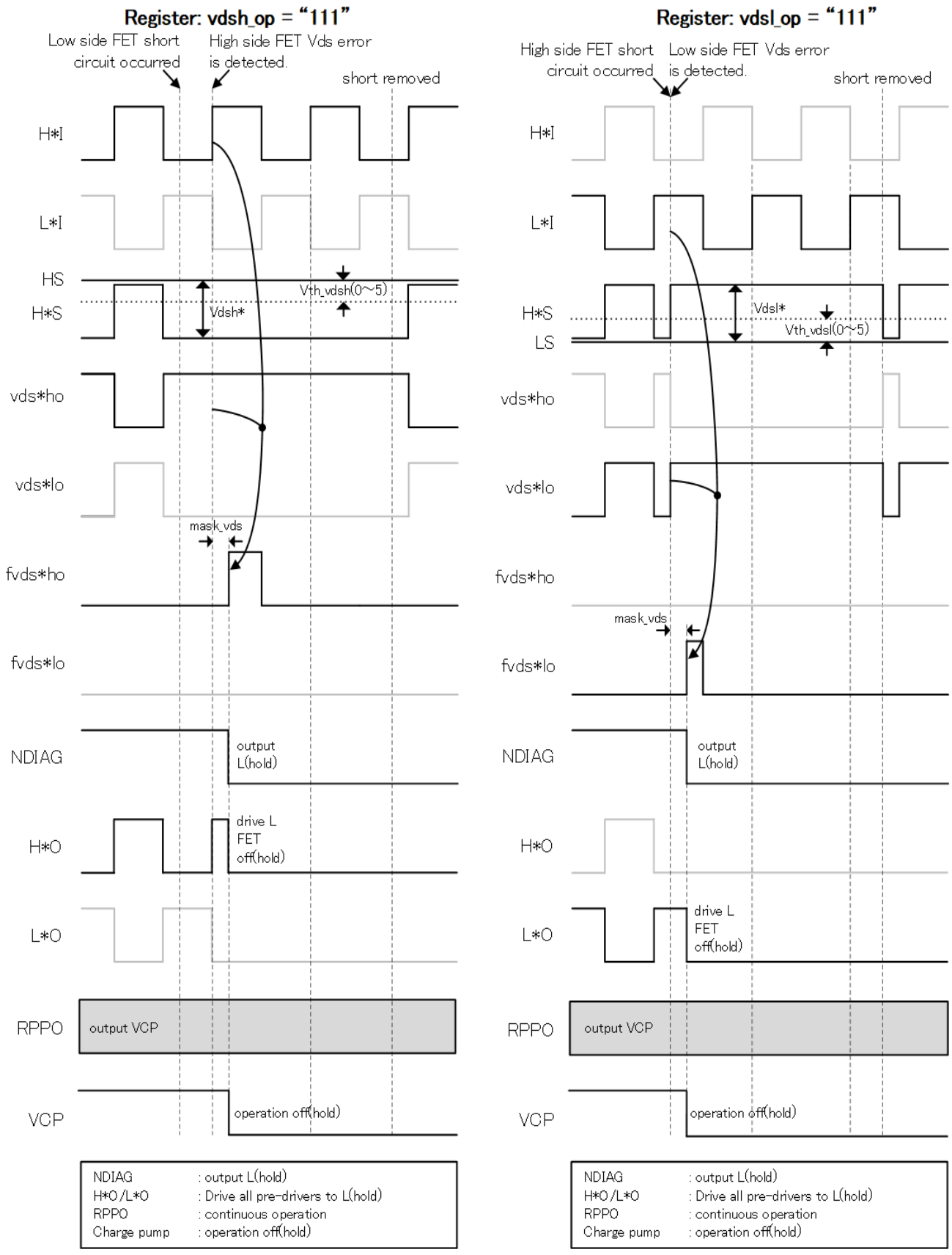


Fig. 7.6.7.9 Short-Circuit Detection Timing Chart (In the case of register: vdsl_op = vdsh_op "111")

7.6.8. Abnormality Detection for CP1SW and CP2SW Terminals

This function detects abnormality for the following cases.

- Short-circuit with adjacent terminals for CP1SW and CP2SW each
- Short circuit to VB
- Short circuit to GND
- Short circuit of an external flying capacitor

In addition, SPI communication allows the operations below.

- Set operation after abnormality has been detected (CONFIG5).
- Read abnormality detection flag (flag for CP1SW and CP2SW each) (STAT1).
- Clear abnormality detection flag (clear flag for CP1SW and CP2SW each) (STAT1_CLR).

7.7. Alarm Input Circuit

ALARM signal controls whether to Enable/Disable gate driver circuits (for driving both 3-phase FETs and reverse polarity protection FET) depending on external input.
In the case of ALARM="L," input of gate driver circuits and internal signals determine whether to Enable/Disable (normal operation).
In the case of ALARM="H," the operation follows as set by CONFIG2 register. "1" is set to the STAT1 status register and NDIAG="L" is output.
When ALARM is switched from "H" to "L," the status register returns to "0" and NDIAG follows the status register and outputs "H." In the input side of the ALARM terminal, a digital filter (D.F.) has been incorporated to remove noise. Whether the digital filter is used or not can be set by CONFIG3 register.
When ARARM terminal has an open fault, the gate driver circuits are controlled to disable.

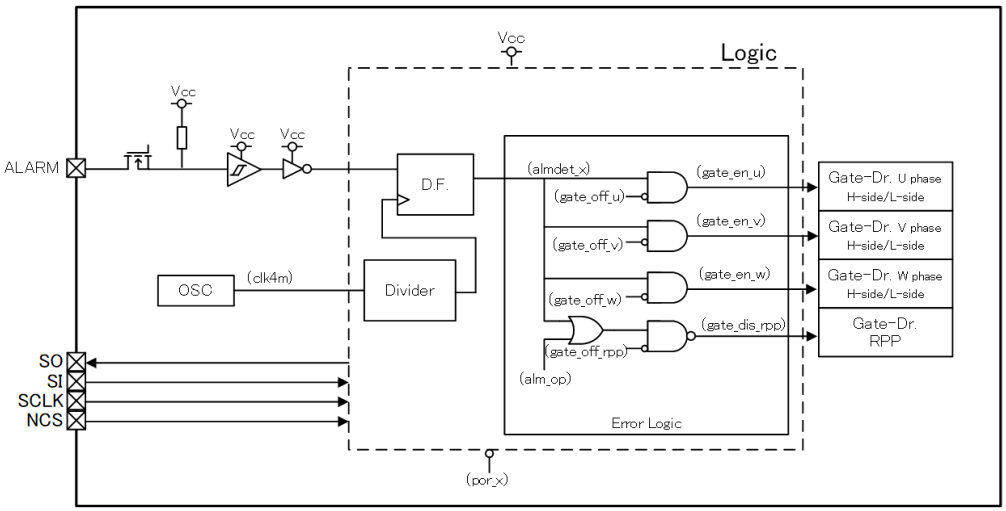


Fig. 7.7.1 ALARM Circuit Control Block Diagram

Table 7.7.1 ALARM Circuit Control Truth Table

por_x	ALARM	almdet_x	alm_op	gate_en_u	gate_en_v	gate_en_w	gate_dis_rpp
"L"	X	X	X	"L"	"L"	"L"	"H"
"H"	"H" (Abnormal)	"L" (Abnormal)	"0"	"L"	"L"	"L"	"H"
			"1"	"L"	"L"	"L"	gate_off_rpp
	"L" (Normal)	"H" (Normal)	X	gate_off_u_x	gate_off_v_x	gate_off_w_x	gate_off_rpp

Note: "X" means "Don't care"
Note: almdet_x is the signal after which ALRAM signal is inverted and passed through filter(Without filter: fil_alm=0, With a filter: fil_alm=1)
Note: gate_off_u_x, gate_off_v_x, gate_off_w_x, and gate_off_rpp are signals to stop gate drivers for reasons other than Alarm signal.(The suffix "_x" indicates that it is an inverted signal.)

Table 7.7.2 ALARM Settings (For how to see the table, see 7.5.1 and 7.5.2.)

Function	Setting Reg.	Setting bit	Operation at Detection	Initial Value	Status Reg.	Status Clear	NDIAG
ALARM	alm_op	"0"	Turn off gate driver circuits for driving 3-phase FETs (6ch), Turn off gate driver circuits for reverse polarity protection FET.	X	alm_det	-	"L"
		"1"	Turn off gate driver circuits for driving 3-phase FETs (6ch).	-			

7.8. SPI Communication Circuit

This product has a built-in SPI communication circuit configured with a mode of “CPOL=0 and CPHA=1” for a responder purpose.
The SPI communication circuit is configured with 4 terminals, where NCS, SI, and SCLK terminals judge input voltage a “H” level or “L” level. The SO terminal is a push-pull configuration, outputs “H” level or “L” level voltage and goes into Hi-Z state in the case of NCS=“H.” The maximum frequency of the communication is 2MHz.

Only in the case of NCS=“L,” is communication with MCU allowed.
After being switched to NCS=“L,” a wait time is required before SCLK input is started. In addition, a certain period is required for the Hi-Z state of SO to be released.
At a rising edge of the clock, MCU outputs data to SI. At the next falling edge, this product reads in data, and around the falling edge, a certain period is required to set up and hold the SI data.
At a rising edge of the clock, this product outputs data to SO with a certain delay time. MCU reads in the data at the next falling edge.
A certain period is necessary from the clock’s final falling to NCS=“H.” After a certain period from switching to NCS=“H,” SO goes into Hi-Z state.
From switching to NCS=“H” to the start of next transmission (NCS=“L”), a certain wait time is required.
As a complementary figure for above explanation, Fig. 9.9.1 is useful.

SI receives data bits from MCU in the order from MSB to LSB.
SO sends data bits to MCU in the order from MSB to LSB.
In addition, NCS terminal is pulled up by a resistor and SCLK and SI terminals are pulled down by a resistor in this product.

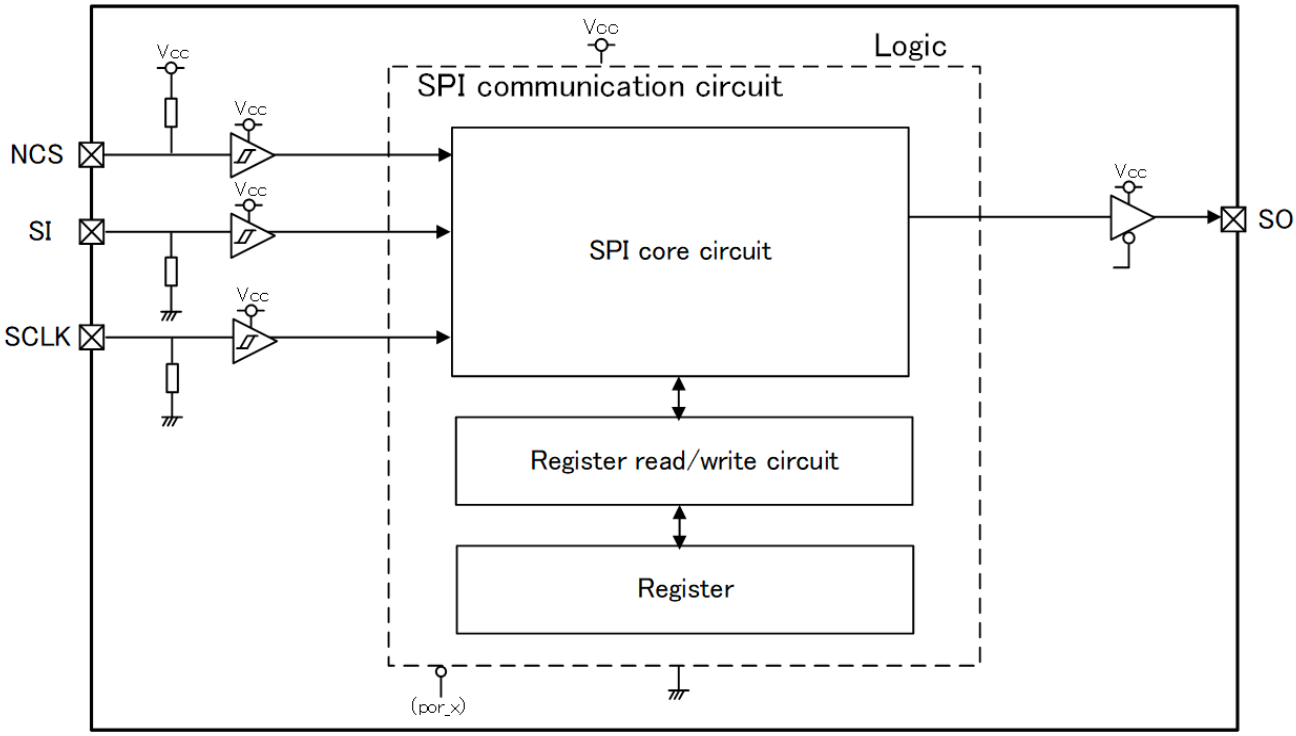


Fig. 7.8.1 SPI Communication Circuit Block Diagram

7.8.1. SPI Communication Operation

The frame length is 16. SI is formed of addressing bits: Addr[4:0], data bits: Data[9:0], and an even parity bit: P[0] for data check. In terms of functions, two types of operation are provided: read operation and write operation, and whether to read or write can be selected by “RW”bit (Addr[0]).

The frame structure is shown below.

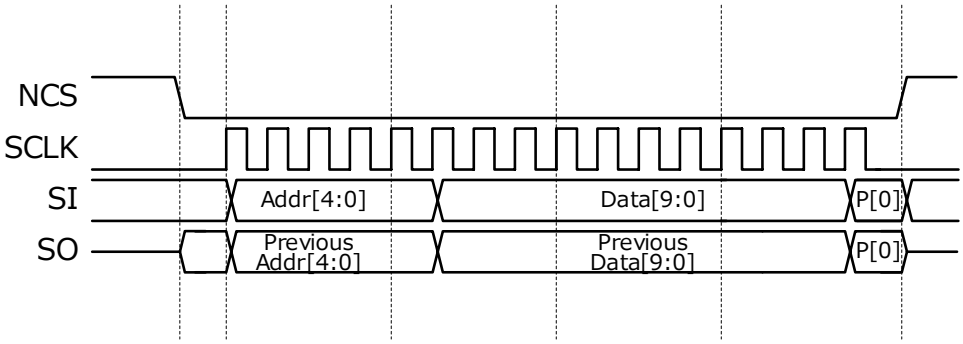


Fig. 7.8.1.1 Frame Format

To Write, with Addr[0]=0, specify the address shown in Table 7.8.3.1 Register Map. Then specify data to write in Data[9:0], and finally, specify an even parity check P[0] covering Addr[4:0] and Data[9:0]. In the next transmission, the write data are output in the order of Addr[4:0], Data[9:0], and P[0] from SO.

To read, with Addr[0]=“1,” specify the address shown in Table 7.8.3.1 Register Map. Then specify Data[9:0] all to “0,” and finally specify an even parity check P[0] covering Addr[4:0] and Data[9:0]. In the next transmission, the specified read data are output in the order of Addr[4:0], Data[9:0], and P[0] from SO. In this transmission, a dummy frame (NOP:No Operation) that does not affect the operation of this product can be used.

An example of normal SPI operation is shown in Fig. 7.8.1.2.

- Transfer 1: CONFIG1 is written.
- Transfer 2: Read command for STAT1 is written and written data in Transfer 1 is confirmed from SO.
- Transfer 3: CONFIG2 is written and read data that was commanded in Transfer 2 is confirmed from SO.

	SPI Transfer 1 (write)				SPI Transfer 2 (Read)				SPI Transfer 3 (Read)			
Pin SI MCU	Addr [4:1]	Addr RW[0]	Data [9:0]	Even Parity [0]	Addr [4:1]	Addr RW[0]	Data [9:0]	Even Parity [0]	Addr [4:1]	Addr RW[0]	Data [9:0]	Even Parity [0]
Value in Hex	02		3 09	1	0D		0 00	1	05		0 00	0
Value in Binary	0 001	0	11 0000 1001	1	0 110	1	00 0000 0000	1	0 010	1	00 0000 0000	0
Pin SO MCD	Addr [4:1]	Addr RW[0]	Data [9:0]	Even Parity [0]	Addr [4:1]	Addr RW[0]	Data [9:0]	Even Parity [0]	Addr [4:1]	Addr RW[0]	Data [9:0]	Even Parity [0]
Value in Hex	Previous Addr		Previous Data	Previous Parity	02		3 09	1	0D		0 10	1
Value in Binary					0 001	0	11 0000 1001	1	0 110	1	00 0001 0000	0

Fig. 7.8.1.2 An Example of Transmission in SPI Communication

7.8.2. Error Judgment

In SPI communication, errors below are judged.

- Parity error
- Addressing error
- Frame length error

The parity error check judges it an error when the even parity bit P[0] is set to an odd parity.
The addressing error check judges it an error when an address not in Table 7.8.3.1 Register Map is set, or Read/Write conditions not mentioned are set.
The frame length error check counts the number of SCLK in the L period of NCS. Assuming that an external noise interferes with the SCLK line during communication, the error is detected when the number of clock is between 1 and 15, or 17 and above. When the length is 17 clocks or more, SO outputs “0” from 17 clocks or later. In both cases, it is judged an error at the time of NCS (L to H).
When an error is detected, “1” is written to status register err_spi, and NDIAG=“L” is output. When an error occurs in writing, Data[9:0] becomes ineffective, writing to registers is not performed, and old data is maintained. Note that at the time when the NDIAG=“L” is recognized, it is possible that an error is happening in SPI communication, which might not be established from then on, but MCU should continue the communication, and for a frame to be used, an NOP frame which is unlikely to cause erroneous writing to registers is recommended.

When an SPI communication error is detected, a previous Addr[4:1]+ Addr[0], Data[9:0]=0x000, and an intentionally made wrong parity bit are returned in the next transmission. This makes MCU recognize that the cause of the previous NDIAG=“L” is an SPI communication error, but MCU continues communication and expects the parity bit to return to its normal.
After returning to normal, “1” of err_spi and NDIAG=“L” remains latched. After confirming that SPI communication has returned to normal, MCU writes “1” to err_spi_cl, sets err_spi to “0,” and returns NDIAG to “H.” After this, it is recommended that MCU compare various settings in registers with those before the abnormal state happens.

When Vcc under voltage has been detected

- SPI communication is not allowed.

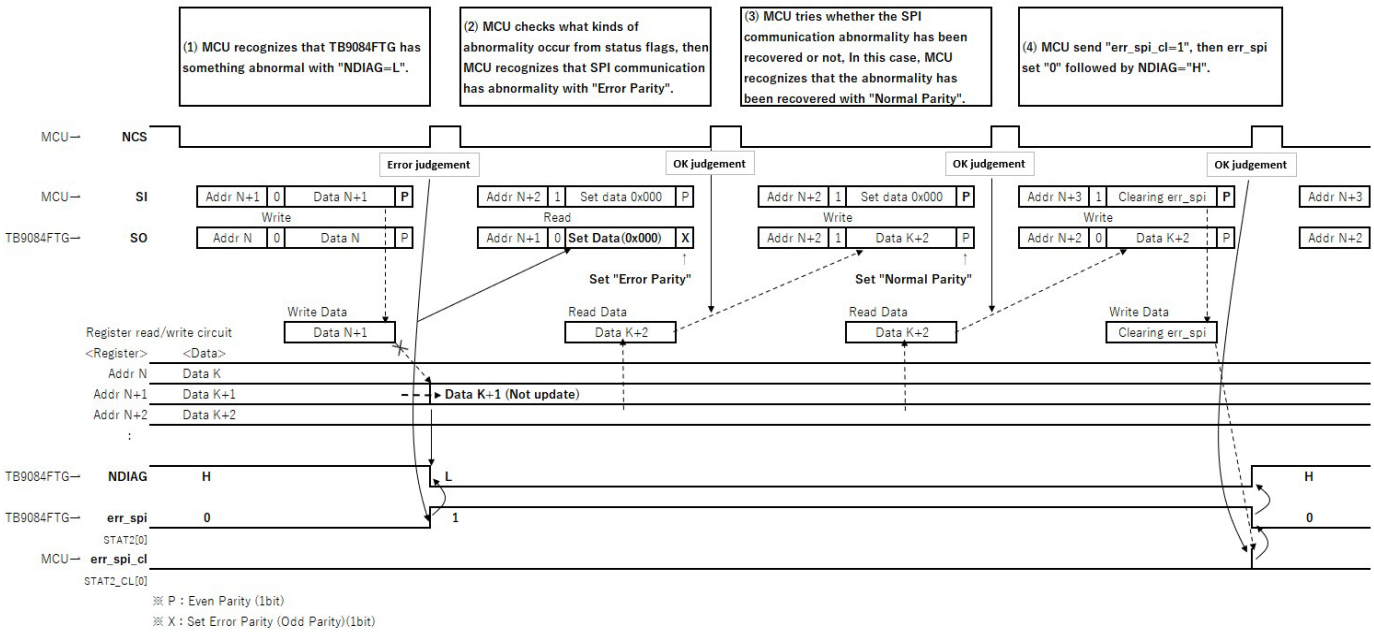


Fig. 7.8.2.1 Transmission example when a Communication Error Has Been Detected

Table 7.8.2.1 List of SPI Communication Error Settings (For how to see the table, see 7.5.1 and 7.5.2.)

Function	Setting Reg.	Setting bit	Operation at Detection	Initial Value	Status Reg.	Status Clear	NDIAG
SPI Communication Error	N/A	-	Continue operation	-	err_spi	err_spi_cl	“L”

7.8.3. Register Map

Table 7.8.3.1 Register Map

Symbol	Addr[4:1]		Addr[0] Write Read	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
CONFIG1	1h	0001b	W(0) R(1)	uvb_op	ovcp_op			ovcc_op			uvrpp_op		
CONFIG2	2h	0010b	W(0) R(1)	tsd_op			vdsh_op			vdsl_op			alm_op
CONFIG3	3h	0011b	W(0) R(1)	mask_vds			vth_vdsh			vth_vdsl			fil_alm
CONFIG4	4h	0100b	W(0) R(1)	t_ilim			plu_dis	plv_dis	plw_dis	vds_u_dis	vds_v_dis	vds_w_dis	pl_op
CONFIG5	5h	0101b	W(0) R(1)	gain_amp			cal_amp	-	-	-	-	cpsw_det_op	gd_in_sel
STAT1	6h	0110b	R(1)	uvb	ovcp	ovcc	uvrpp	tsd	cp2sw_det	cp1sw_det	cal_pass	cal_en	alm_det
STAT2	7h	0111b	R(1)	vds_uh	vds_vh	vds_wh	vds_ul	vds_vl	vds_wl	err_pl_u	err_pl_v	err_pl_w	err_spi
STAT1_CLR	8h	1000b	W(0)	uvb_cl	ovcp_cl	ovcc_cl	uvrpp_cl	tsd_cl	cp2sw_det_cl	cp1sw_det_cl	cal_pass_cl	-	set_dflt
STAT2_CLR	9h	1001b	W(0)	vds_uh_cl	vds_vh_cl	vds_wh_cl	vds_ul_cl	vds_vl_cl	vds_wl_cl	err_pl_u_cl	err_pl_v_cl	err_pl_w_cl	err_spi_cl
NOP	Fh	1111b	W(0) R(1)	-	-	-	-	-	-	-	-	-	-

Overall:

- When data is set to a bit that is not assigned (“-” is shown in the register map) to write, it is discarded. When the bit is read, the bit is read as “0.”
- A function is provided that one writing (set_dflt) returns all bits of set values (CONFIG1 to 5) and status (STAT1 to 2) to default values.
- Underlined register descriptions in chapter 7.8.3.1 to chapter 7.8.3.9 (Register Explanation) represent the default values.

CONFIG (Setting) registers:

- When a bit that is not shown as a set value is set, the set value is not updated, and the previous value is maintained.
- When detection of prohibited input has been disabled by pl*_dis bit of CONFIG4[6:4], the detection itself has been disabled. So, even when H*I=L*I=“H” is input, output is H*O=LO=“H,” the status bit is not set, and NDIAG terminal does not become “L.” (*: U/V/W). Refer to Table 7.2.1.1.

STAT (Status) registers:

- Returning of “1” to “0” is performed in two ways: Returning automatically depending on the result of detection of circuits, and writing “1” to the status clear register to return.
- Only cal_pass of STAT1[1] is “0” in an abnormal state.

STAT_CLR (status clear) registers:

- When “1” is written after transition to the normal state, the status bit is cleared. The cleared register becomes “0” (default value), In this case, NDIAG=“H” is output and normal operation is recovered.
- When abnormality has been detected, writing “1” does not clear status registers to be cleared.
- After writing “1,” writing back to “0” is not required.
- Writing “0” is ineffective.

Note: Due to the features of the parity check, in cases where transmitted data has changed in 2 bits or more and the number of “1” is the same, errors cannot be detected.

7.8.3.1. CONFIG1 Write Address=2h / Read Address=3h

Table 7.8.3.1.1 CONFIG1 Register Map

Symbol	Addr[4:1]		Addr[0] Write Read	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
CONFIG1	1h	0001b	W(0) R(1)	uvb_op	ovcp_op			ovcc_op			uvrpp_op		

Table 7.8.3.1.2 CONFIG1 Register Explanation

bit	Symbol	R/W	Function
CONFIG1 [9]	uvb_op	R/W	Select operation for VB under voltage detection. “0”=NDIAG:“L” output (latched), All gate drivers of 3-phase drive FETs to off. “1”=NDIAG:“L” output, All gate drivers of 3-phase drive FETs to off, turn charge pump off.
CONFIG1 [8:6]	ovcp_op	R/W	Select operation for VCP over voltage detection. “000”=NDIAG:“H”(continue), Continue operation [Disable detection] “001”=NDIAG:“L” output (latched), Continue operation. “010”=NDIAG:“L” output (latched), All gate drivers of 3-phase drive FETs to off. “011” =NDIAG:“L” output (latched), All gate drivers of 3-phase drive FETs to off (latched). “100”=NDIAG:“L” output (latched), All gate drivers of 3-phase drive FETs to off, turn charge pump off. “101”=NDIAG:“L” output (latched), All gate drivers of 3-phase drive FETs to off, turn charge pump off (latched).
CONFIG1 [5:3]	ovcc_op	R/W	Select operation for VCC over voltage detection. “000”=NDIAG:“H”(continue), Continue operation [Disable detection] “001”=NDIAG:“L” output (latched), Continue operation. “010”=NDIAG:“L” output (latched), All gate drivers of 3-phase drive FETs to off. “011”=NDIAG:“L” output (latched), All gate drivers of 3-phase drive FETs to off (latched). “100”=NDIAG:“L” output (latched), All gate drivers of 3-phase drive FETs to off, turn charge pump off. “101”=NDIAG:“L” output (latched), All gate drivers of 3-phase drive FETs to off (latched), turn charge pump off (latched).
CONFIG1 [2:0]	uvrpp_op	R/W	Select operation for RPPO under voltage detection. “000”=NDIAG:“H”(Continue), Continue operation [Disable detection] “001”=NDIAG:“L” output (latched), Continue operation. “010”=NDIAG:“L” output (latched), All gate drivers of 3-phase and reverse polarity protection drive FETs to off. “011”=NDIAG:“L” output (latched), All gate drivers of 3-phase drive FETs to off. “100”=NDIAG:“L” output (latched), All gate drivers of 3-phase drive FETs to off (latched).

7.8.3.2. CONFIG2 Write Address=4h / Read Address=5h

Table 7.8.3.2.1 CONFIG2 Register Map

Symbol	Addr[4:1]		Addr[0] Write Read	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
CONFIG2	2h	0010b	W(0) R(1)	tsd_op			vdsh_op			vdsl_op			alm_op

Table 7.8.3.2.2 CONFIG2 Register Explanation

bit	Symbol	R/W	Function
CONFIG2 [9:7]	tsd_op*1	R/W	Select operation for over temperature detection. “000”=NDIAG:“H”(continue), Continue operation [Disable detection] “001”=NDIAG:“L” output (latched), Continue operation. “010”=NDIAG:“L” output (latched), All gate drivers of 3-phase drive FETs to off. “011”=NDIAG:“L” output (latched), All gate drivers of 3-phase drive FETs to off (latched). “100”=NDIAG:“L” output (latched), All gate drivers of 3-phase drive FETs to off, turn charge pump off. “101”=NDIAG:“L” output (latched), All gate drivers of 3-phase drive FETs to off (latched), turn charge pump off (latched).
CONFIG2 [6:4]	vdsh_op	R/W	Select operation for VDS abnormality detection for 3-phase FETs (high side). “000”=NDIAG:“H”(continue), Continue operation [Disable detection] “001”=NDIAG:“L” output (latched), Continue operation. “010”=NDIAG:“L” output (latched), H/L gate drivers of detected phase drive FETs to off. “011”=NDIAG:“L” output (latched), H/L gate drivers of detected phase drive FETs to off (latched). “100”=NDIAG:“L” output (latched), All gate drivers of 3-phase drive FETs to off. “101”=NDIAG:“L” output (latched), All gate drivers of 3-phase drive FETs to off (latched). “110”=NDIAG:“L” output (latched), All gate drivers of 3-phase drive FETs to off, turn charge pump off. “111”=NDIAG:“L” output (latched), All gate drivers of 3-phase drive FETs to off (latched), turn charge pump off (latched).
CONFIG2 [3:1]	vdsl_op	R/W	Select operation for VDS abnormality detection for 3-phase FETs (low side). “000”=NDIAG:“H”(continue), Continue operation [Disable detection] “001”=NDIAG:“L” output (latched), Continue operation. “010”=NDIAG:“L” output (latched), H/L gate drivers of detected phase drive FETs to off. “011”=NDIAG:“L” output (latched), H/L gate drivers of detected phase drive FETs to off (latched). “100”=NDIAG:“L” output (latched), All gate drivers of 3-phase drive FETs to off.. “101”=NDIAG:“L” output (latched), All gate drivers of 3-phase drive FETs to off (latched). “110”=NDIAG:“L” output (latched), All gate drivers of 3-phase drive FETs to off, turn charge pump off. “111”=NDIAG:“L” output (latched), All gate drivers of 3-phase drive FETs to off (latched), turn charge pump off (latched).
CONFIG2 [0]	alm_op	R/W	Select operation for ALARM detection. “0”=NDIAG:“L” output, all gate drivers of 3-phase and reverse polarity protection drive FETs to off. “1”=NDIAG:“L” output, All gate drivers of 3-phase drive FETs to off.

7.8.3.3. CONFIG3 Write Address=6h / Read Address=7h

Table 7.8.3.3.1 CONFIG3 Register Map

Symbol	Addr[4:1]		Addr[0] Write Read	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
CONFIG3	3h	0011b	W(0) R(1)	mask_vds			vth_vdsh			vth_vdsl			fil_alm

Table 7.8.3.3.2 CONFIG3 Register Explanation

bit	Symbol	R/W	Function
CONFIG3 [9:7]	mask_vds	R/W	Selects VDS detection filtering time for 3-phase FETs (high side/low side). “000=6µs “001”=8µs “010”=10µs “011”=12µs “100”=16µs “101”=32µs “110”=64µs:This setting is automatically selected when 3-input system is selected. “111”=128µs
CONFIG3 [6:4]	vth_vdsh	R/W	Selects VDS detection threshold voltage for 3-phase FETs (high side). “000”=0.1V “001”=0.3V “010”=0.5V “011”=0.7V “100”=0.9V “101”=1.1V
CONFIG3 [3:1]	vth_vdsl	R/W	Selects VDS detection threshold voltage for 3-phase FETs (U phase low side). “000”=0.1V “001”=0.3V “010”=0.5V “011”=0.7V “100”=0.9V “101”=1.1V
CONFIG3 [0]	fil_alm	R/W	Sets ALARM digital filter (for both high side/low side) “0”= No filter “1”= 16µs *16x22x(1/4MHz)+(1/4MHz)

7.8.3.4. CONFIG4 (Write Address=8h / Read Address=9h

Table 7.8.3.4.1 CONFIG4 Register Map

Symbol	Addr[4:1]		Addr[0] Write Read	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
CONFIG4	4h	0100b	W(0) R(1)	t_ilim			plu_dis	plv_dis	plw_dis	vds_u_dis	vds_v_dis	vds_w_dis	pl_op

Table 7.8.3.4.2 CONFIG4 Register Explanation

bit	Symbol	R/W	Function
CONFIG4 [9:7]	t_ilim	R/W	Selects start time of output current control for gate drivers for driving 3-phase FETs. “000”=6μs “001”=8μs “010”=10μs “011”=12μs “100”=16μs “101”=32μs “110”=64μs Note: This setting is automatically selected when 3-input system is selected. “111”=128μs
CONFIG4 [6]	plu_dis	R/W	Selects whether to enable/disable prohibited input detection of U phase output (HUO, LUO) of gate drivers for 3-phase FETs. “0”= Enable detection for U phase. “1”= Disable detection for U phase.
CONFIG4 [5]	plv_dis	R/W	Selects whether to enable/disable prohibited input detection of V phase output (HVO, LVO) of gate drivers for 3-phase FETs. “0”= Enable detection for V phase. “1”= Disable detection of V phase.
CONFIG4 [4]	plw_dis	R/W	Selects whether to enable/disable prohibited input detection of W phase output (HWO, LWO) of gate drivers for 3-phase FETs. “0”= Enable detection for W phase. “1”= Disable detection for W phase.
CONFIG4 [3]	vds_u_dis	R/W	Selects whether to enable/disable VDS detection (U phase high side & low side) for 3-phase FETs. “0”= Enable detection for U phase. “1”= Disable detection for U phase (No new detection, no influence on already detected status).
CONFIG4 [2]	vds_v_dis	R/W	Selects whether to enable/disable VDS detection (V phase high side & low side) for 3-phase FETs. “0”= Enable detection for V phase. “1”= Disable detection for V phase (No new detection, no influence on already detected status).
CONFIG4 [1]	vds_w_dis	R/W	Selects whether to enable/disable VDS detection (W phase high side & low side) for 3-phase FETs. “0”= Enable detection for W phase. “1”= Disable detection for W phase (No new detection, no influence on already detected status).
CONFIG4 [0]	pl_op	R/W	Selects operation for prohibited input detection of gate drivers for driving 3-phase FETs. “0”= Do not set result of prohibited input detection to status register, NDIAG: “H” output. In the case of pl*_dis=”L”, H/L gate drivers of detected phase as prohibited input drive FETs to off. “1”= Set result of prohibited input detection to status register, NDIAG: “L” output (latched). In the case of pl*_dis=”L”, H/L gate drivers of detected phase as prohibited input drive FETs to off.

7.8.3.5. CONFIG5 Write Address=Ah / Read Address=Bh

Table 7.8.3.5.1 CONFIG5 Register Map

Symbol	Addr[4:1]		Addr[0] Write Read	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
CONFIG5	5h	0101b	W(0) R(1)	gain_amp			cal_amp	-	-	-	-	cpsw_det_op	gd_in_sel

Table 7.8.3.5.2 CONFIG5 Register Explanation

bit	Symbol	R/W	Function
CONFIG5 [9:7]	gain_amp	R/W	Selects current sense OPAMP gain. “000”=7.5 times “001”=10 times “010”=12.5 times “011”=15 times “100”=20 times “101”=30 times “110”=40 times “111”=40 times
CONFIG5 [6]	cal_amp	W	Selects OPAMP calibration. “0”= No OPAMP calibration “1”= Perform OPAMP calibration. Note: The setting is automatically cleared whether the calibration is completed or not.
CONFIG5 [5]	-	-	“0”
CONFIG5 [4]	-	-	“0”
CONFIG5 [3]	-	-	“0”
CONFIG5 [2]	-	-	“0”
CONFIG5 [1]	cpsw_det_op	R/W	Detects abnormality at CP1SW and SP2SW terminals. “0”=NDIAG:“L” output (latched), Continue operation. “1”= NDIAG:“L” output (latched), All gate drivers of 3-phase drive FETs to off (latched), turn charge pump off (latched).
CONFIG5 [0]	gd_in_sel	R/W	Selects the number of input terminals of gate drivers for driving 3-phase FETs. “0”=6-input “1”= Ineffective.

7.8.3.6. STAT1 / Read Address=Dh

Table 7.8.3.6.1 STAT1 Register Map

Symbol	Addr[4:1]		Addr[0] Write Read	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
STAT1	6h	0110b	R(1)	uvb	ovcp	ovcc	uvrpp	tsd	cp2sw_det	cp1sw_det	cal_pass	cal_en	alm_det

Table 7.8.3.6.2 STAT1 Register Explanation

bit	Symbol	R/W	Function
STAT1 [9]	uvb	R	VB under voltage detection “0”= Do not detect. “1”= Detect.
STAT1 [8]	ovcp	R	VCP over voltage detection “0”= Do not detect. “1”= Detect.
STAT1 [7]	ovcc	R	VCC over voltage detection “0”= Do not detect. “1”= Detect.
STAT1 [6]	uvrpp	R	RPP under voltage detection “0”= Do not detect. “1”= Detect.
STAT1 [5]	tsd	R	Over temperature detection “0”= Do not detect. “1”= Detect.
STAT1 [4]	cp2sw_det	R	CP2SW terminal abnormality detection “0”= Do not detect. “1”= Detect.
STAT1 [3]	cp1sw_det	R	CP1SW terminal abnormality detection “0”= Do not detect. “1”= Detect.
STAT1 [2]	cal_pass	R	Current sense AMP offset calibration check result flag “0”= Failure or calibration not performed “1”=Pass
STAT1 [1]	cal_en	R	Current sense AMP offset calibration operation flag “0”= Calibration stopped “1”= Calibration being performed
STAT1 [0]	alm_det	R	ALARM terminal state detection “0”= L level voltage input at ALRAM terminal “1”= H level voltage input at ALRAM terminal

7.8.3.7. STAT2 / Read Address=Fh

Table 7.8.3.7.1 STAT2 Register Map

Symbol	Addr[4:1]		Addr[0] Write Read	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
STAT2	7h	0111b	R(1)	vds_uh	vds_vh	vds_wh	vds_ul	vds_vl	vds_wl	err_pl_u	err_pl_v	err_pl_w	err_spi

Table 7.8.3.7.2 STAT2 Register Explanation

bit	Symbol	R/W	Function
STAT2 [9]	vds_uh	R	VDS detection for 3-phase FETs (U phase high side) "0"= Do not detect. "1"= Detect.
STAT2 [8]	vds_vh	R	VDS detection for 3-phase FETs (V phase high side) "0"= Do not detect. "1"= Detect.
STAT2 [7]	vds_wh	R	VDS detection for 3-phase FETs (W phase high side) "0"= Do not detect. "1"= Detect.
STAT2 [6]	vds_ul	R	VDS detection for 3-phase FETs (U phase low side) "0"= Do not detect. "1"= Detect.
STAT2 [5]	vds_vl	R	VDS detection for 3-phase FETs (V phase low side) "0"= Do not detect. "1"= Detect.
STAT2 [4]	vds_wl	R	VDS detection for 3-phase FETs (W phase low side) "0"= Do not detect. "1"= Detect.
STAT2 [3]	err_pl_u	R	Gate drivers for driving 3-phase FETs prohibited input error detection (U phase) "0"= Do not detect. "1"= Detect.
STAT2 [2]	err_pl_v	R	Gate drivers for driving 3-phase FETs prohibited input error detection (V phase) "0"= Do not detect. "1"= Detect.
STAT2 [1]	err_pl_w	R	Gate drivers for driving 3-phase FETs prohibited input error detection (W phase) "0"= Do not detect. "1"= Detect.
STAT2 [0]	err_spi	R	SPI communication error detection "0"= Do not detect. "1"= Detect.

7.8.3.8. STAT1_CLR Write Address=10h

Table 7.8.3.8.1 STAT1_CLR Register Map

Symbol	Addr[4:1]		Addr[0] Write Read	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
STAT1_CLR	8h	1000b	W(0)	uvb_cl	ovcp_cl	ovcc_cl	uvrpp_cl	tsd_cl	cp2sw_det_cl	cp1sw_det_cl	cal_pass_cl	-	set_dflt

Table 7.8.3.8.2 STAT1_CLR Register Explanation

bit	Symbol	R/W	Function
STAT1_CLR [9]	uvb_cl	W	Clears status bit uvb. "0"= Ineffective "1"= Clear status bit.
STAT1_CLR [8]	ovcp_cl	W	Clears status bit ovcp. "0"= Ineffective "1"= Clear status bit.
STAT1_CLR [7]	ovcc_cl	W	Clears status bit ovcc. "0"= Ineffective "1"= Clear status bit.
STAT1_CLR [6]	uvrpp_cl	W	Clears status bit uvrpp. "0"= Ineffective "1"= Clear status bit.
STAT1_CLR [5]	tsd_cl	W	Clears status bit tsd. "0"= Ineffective "1"= Clear status bit.
STAT1_CLR [4]	cp2sw_det_cl	W	Clears status bit cp2sw_det. "0"= Ineffective "1"= Clear status bit.
STAT1_CLR [3]	cp1sw_det_cl	W	Clears status bit cp1sw_det. "0"= Ineffective "1"= Clear status bit.
STAT1_CLR [2]	cal_pass_cl	W	Clears current sense AMP offset calibration check result flag. "0"= Ineffective "1"= Clear status bit.
STAT1_CLR [1]	-	-	"0"
STAT1_CLR [0]	set_dflt	W	Returns all bits of set values (CONFIG1 to 5) and status (STAT1 to 2) to default values. "0"= Maintain current setting. "1"= Switch current setting to default setting.

7.8.3.9. STAT2_CLR Write Address=12h

Table 7.8.3.9.1 STAT2_CLR Register Map

Symbol	Addr[4:1]		Addr[0] Write Read	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
STAT2_CLR	9h	1001b	W(0)	vds_uh_cl	vds_vh_cl	vds_wh_cl	vds_ul_cl	vds_vl_cl	vds_wl_cl	err_pl_u_cl	err_pl_v_cl	err_pl_w_cl	err_spi_cl

Table 7.8.3.9.2 STAT2_CLR Register Explanation

bit	Symbol	R/W	Function
STAT2_CLR [9]	vds_uh_cl	W	Clears status bit vds_uh. “0”= Ineffective “1”= Clear status bit.
STAT2_CLR [8]	vds_vh_cl	W	Clears status bit vds_vh. “0”= Ineffective “1”= Clear status bit.
STAT2_CLR [7]	vds_wh_cl	W	Clears status bit vds_wh. “0”= Ineffective “1”= Clear status bit.
STAT2_CLR [6]	vds_ul_cl	W	Clears status bit vds_ul. “0”= Ineffective “1”= Clear status bit.
STAT2_CLR [5]	vds_vl_cl	W	Clears status bit vds_vl. “0”= Ineffective “1”= Clear status bit.
STAT2_CLR [4]	vds_wl_cl	W	Clears status bit vds_wl. “0”= Ineffective “1”= Clear status bit.
STAT2_CLR [3]	err_pl_u_cl	W	Clears status bit err_pl_u. “0”= Ineffective “1”= Clear status bit.
STAT2_CLR [2]	err_pl_v_cl	W	Clears status bit err_pl_v. “0”= Ineffective “1”= Clear status bit.
STAT2_CLR [1]	err_pl_w_cl	W	Clears status bit err_pl_w. “0”= Ineffective “1”= Clear status bit.
STAT2_CLR [0]	err_spi_cl	W	Clears status bit err_spi. “0”= Ineffective “1”= Clear status bit.

7.8.3.10. NOP Write Address=Fh / Read Address=Fh

Table 7.8.3.10.1 NOP Register Map

Symbol	Addr[4:1]		Addr[0] Write Read	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
NOP	Fh	1111b	W(0) R(1)	-	-	-	-	-	-	-	-	-	-

NOP (No Operation) is a frame dedicated to output from SDO terminal in response to a Read request in the previous transmission. Addr [0] accepts both settings. D [9:0], which are bits not assigned and data set to which is discarded, accept both 0 and 1. In the next transmission after NOP, SDO outputs Addr [4:1] = Fh, Addr [0] = data set at NOP transmission, and D [9:0] = all 0s.

An example of transmission is shown in Fig. 7.8.3.10.1.

- Transfer 1: STAT1 is written.
- Transfer 2: Write command for NOP (Addr[0]=0) is written and read data in Transfer 1 is confirmed from SO.
- Transfer 3: Read command for NOP (Addr[0]=1) is written and read data (NOP: Addr[0]=0) in Transfer 2 is confirmed from SO.
- Transfer 4: CONFIG1 is written and read data (NOP: Addr[0]=1) in Transfer 3 is confirmed from SO.

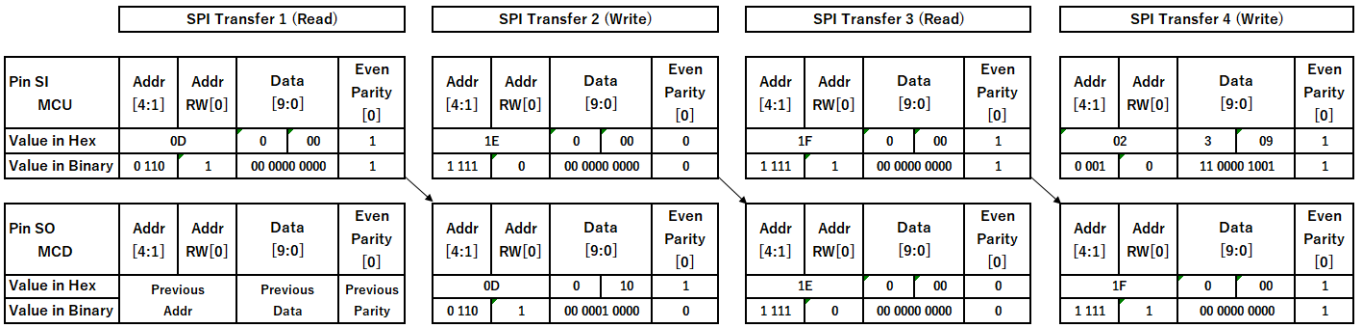


Fig. 7.8.3.10.1 Example of NOP Transmission in SPI Communication

8. Absolute Maximum Ratings (Ta = 25°C)

All voltage values use GND as reference unless otherwise specified.

Spec No.	Item	Terminal	Symbol	Rating	Unit	Conditions
8.1	Power source voltage	VB	Vb	-0.3 to 28(DC)	V	1V/s<Vb<8V/μs(Design value)
8.2				28 to 40(≤1s)		
8.3		VCP	Vcp	-0.3 to 60(DC)	V	-
8.4		VCC	Vcc	-0.3 to 6	V	1V/s<Vcc<0.3V/μs(Design value)
8.5	Voltage between GND-PGND	PGND	Vgnd	-0.3 to 0.3	V	-
8.6	Input voltage	HS	Vin1	-0.3 to 28(DC), 28 to 40(≤1s)	V	-
8.6a		ALARM	Vin1a	-0.3 to Vb+0.3	V	Vin1a≤28V(DC), Vin1a≤40V(≤1s)
8.7		HUS, HVS, HWS	Vin2	-7 to Vcp+0.3,	V	Vin2≤40V Voltage between HUO-HUS,HVO-HVS, and HWO- HWS ≤ 40V
8.8				-14 to -7(≤1μs,20kHz)		
8.9		LS	Vin3	-7 to Vcp+0.3,	V	Vin3≤40V Voltage between LUO-LS,LVO-LS, and LWO- LS ≤ 40V
8.10				-10 to -7(≤1μs,20kHz)		
8.11		LUI, LVI, LWI, HUI, HVI, HWI, SCLK, NCS, SI	Vin4	-0.3 to Vcc+0.3	V	Vin4≤6V
8.12		AMP_P, AMP_N	Vin5	-10 to -7(≤1μs,20kHz), -7 to 28(DC), 28 to 40(≤1s)	V	-
8.14	Output voltage	CP1B, CP2B	Vout1	-0.3 to Vcp+0.3	V	Vout1≤60V
8.15		RPPO	Vout2	-18 to Vcp+0.3	V	Vcp -Vout2≤60V -18V assumes a reversely polarity battery. (For detailed conditions, see SPEC-9.4.19.)
8.16		HUO, HVO, HWO	Vout3	-7 to Vcp+0.3(DC)	V	Vout3≤60V Voltage between HUO-HUS, HVO-HVS, and HWO- HWS ≤40V
8.17				-14 to -7(≤1μs,20kHz)		
8.18		CP1SW, CP2SW	Vout4	-0.3 to Vb+0.3	V	Vout4≤28V(DC), Vout4≤40V(≤1s)
8.19		LUO, LVO, LWO	Vout5	-7 to Vcp+0.3(DC)	V	Vout5≤60V Voltage between LUO-LS, LVO-LS, and LWO- LS ≤40V
8.20				-10 to -7(≤1μs,20kHz)		
8.21		AMP_O	Vout6	-0.3 to Vcc+0.3	V	Vout6≤6V
8.22		NDIAG, SO	Vout7	-0.3 to Vcc+0.3	V	Vout7≤6V
8.23	Input current	HUS, HVS, HWS	Iin1	(-1.5)	A	The number in the bracket is a design value. t=0.2μs
8.23 a		LS	Iin1a	(-3)	A	The number in the bracket is a design value. t=0.2μs
8.24		AMP_P, AMP_N	Iin2	-0.5 to 2	mA	-
8.25	Output current	HUO, HVO, HWO, LUO, LVO, LWO	Iout1	-20 to 20	mA	Limited output current after output current switching time (Tsw) has passed
8.26			Iout2	(-2 to 1.5)	A	The number in the bracket is a design value. t=0.2μs
8.27		CP1B, CP2B	Iout3	(-0.1)	A	The number in the bracket is a design value.
8.28		VCP	Iout4	(-0.1)	A	The number in the bracket is a design

						value.
8.29		AMP_O	Iout3	±5	mA	-
8.30		NDIAG, SO	Iout4	±10	mA	-
8.31	Operating ambient temperature	-	Ta	-40 to 150	°C	-
8.32	Junction temperature (Max)	-	Tj	175	°C	-
8.33	Storage temperature	-	Tstg	-55 to 150	°C	-
8.34	Allowable power dissipation	-	P_D	0.774	W	JEDEC 4-layer board Ta=150°C, Thermal resistance 32.3°C /W

Note: The absolute maximum ratings are standard values that must not be exceeded even momentarily, and even in a single item.
Note: The absolute maximum ratings are limited to the ranges in the “Conditions” column.
Note: Electric current flowing into this product is shown with ‘+’ and that flowing out is with ‘-.’
Note: Symbols in the table of absolute maximum ratings (Vb, Vcp, Vcc) show the applied voltage and output voltage at each terminal (VB, VCP, VCC).
Note: For the power supply voltage at VB, under the condition VB=28 to 40 (≤1s), this product may stop momentarily to protect itself.
Note: Voltage up to VB may be applied to ALARM terminal but use this product with voltage up to VCC applied to the terminal to avoid possible malfunctioning.
Note: When operating a sine wave drive at Ta = 125°C or higher, please be aware that it may exceed the P_D specified in SPEC-8.34.

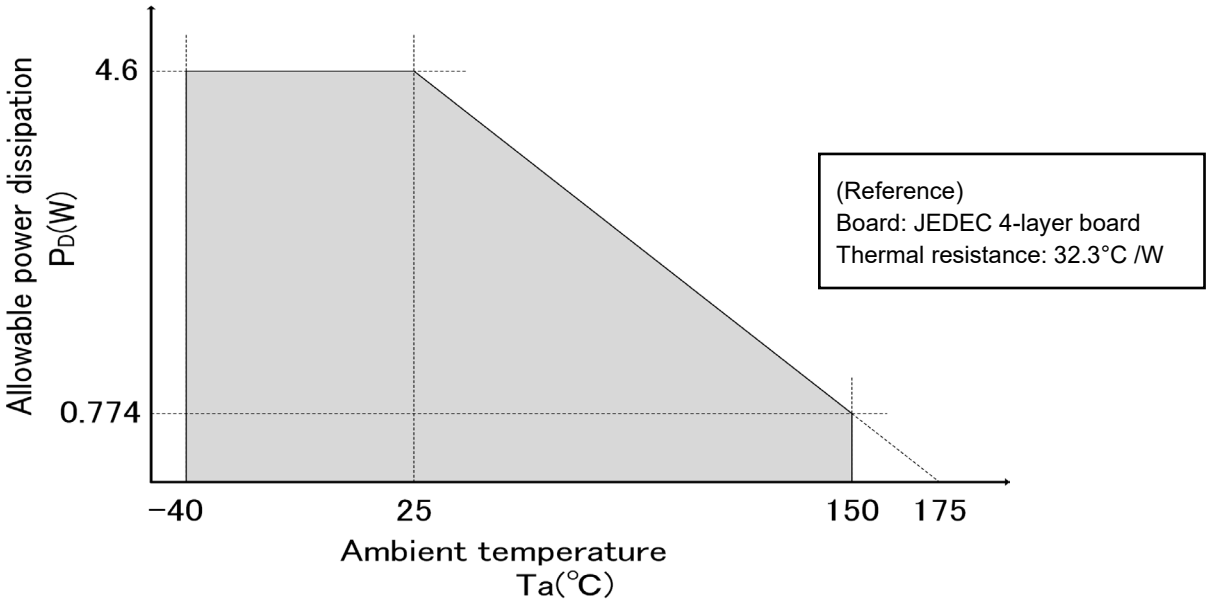


Fig. 8.1 Allowable Power Dissipation Curve

9. Electrical Characteristics

9.1. Operating Voltage Ranges

Spec No.	Item	Terminal	Symbol	Operating Range	Unit	Conditions
9.1.1	Input voltage	VB	Vb	5.7 to 28	V	DC
9.1.2		VCC	Vcc	3.0 to 5.5	V	DC

Note: This product assumes that it is used with a 12V battery.

9.2. Consumption Current

Vb=5.7 to 28V, Vcc=3.0 to 5.5V, Tj=-40 to 175°C unless otherwise specified.

Spec No.	Item	Terminal	Symbol	Test Conditions	Min	Typ.	Max	Unit	Remarks
9.2.1	Current at reset (Battery)	VB VCP RPPO HS	Istb1	Vb=VCP=RPPO=HS=12V, Vcc= 0V, -40≤Ta<85°C	0	-	1	μA	-
9.2.2			Istb2	Vb=VCP=RPPO=HS=12V, Vcc=0V, 85≤Ta<125°C	0	-	1	μA	-
9.2.3			Istb3	Vb=VCP=RPPO=HS=12V, Vcc=0V, 125≤Ta≤150°C	0	-	3	μA	-
9.2.4	Consumption current (Vb)	VB	Ib1	Vb=13.5V HUO, HVO, HWO=20kHz LUO, LVO, LWO=20kHz Gate driver output load: Rload=10Ω, Cload=6100pF RPPO=150kΩ(to VB)	25	46	67	mA	-
9.2.5			Ib2	Vb=16V HUO,HVO,HWO=20kHz LUO,LVO,LWO=20kHz Gate driver output load: Rload=10Ω, Cload=6100pF RPPO=150kΩ(to VB)	25	46	67	mA	-
9.2.6			Ib3	Vb=28V HUO,HVO,HWO=20kHz LUO,LVO,LWO=20kHz Gate driver output load: Rload=10Ω, Cload=6100pF RPPO=150kΩ(to VB)	16	32	48	mA	-
9.2.7	Consumption current (Vcc)	VCC	Icc1	Vcc=5V	4	6.3	10	mA	-
9.2.8			Icc2	Vcc=3.3V	2.7	5.7	7.9	mA	-

Note: When Vcc reaches Vcc under voltage detection voltage, this product goes into a reset state. Current in the reset state is specified by Istb1, Istb2, Istb3 each.
Note: Current depending on the Vb state is specified by Ib1, Ib2, Ib3 each. External constants of the charge pump are as shown in Fig. 9.3.1.
Note: Current depending on the Vcc state is specified by Icc1, Icc2 each.

9.3. Charge Pump Circuit

Vb=5.7 to 28V, Vcc=3.0 to 5.5V, Tj=-40 to 175°C unless otherwise specified.

Spec No.	Item	Terminal	Symbol	Test Conditions	Min	Typ.	Max	Unit	Remarks
9.3.1	Output voltage	VCP	Vcph1	5.7V≤Vb<7V load = -10μA to -13mA	Vb+7.5	Vb+9.3	Vb+12.5	V	-
9.3.2			Vcph2	7V≤Vb≤28V Iload = -10μA to -13mA	Vb+9	Vb+12	Vb+14.5	V	-
9.3.3	Operating frequency	-	clk_cp	-	162	250	338	kHz	Including variation of oscillating frequency ±35%
9.3.4	Time to enable gate driver	-	Tpre_en	Time from release of reset to gate driver ON permission	1.2	1.7	2.7	ms	Including variation of oscillating frequency ±35%

Note: For reference values of the charge pump capacitance Cfp and charge pump voltage terminal capacitance Cvcp, see Fig. 9.3.1.

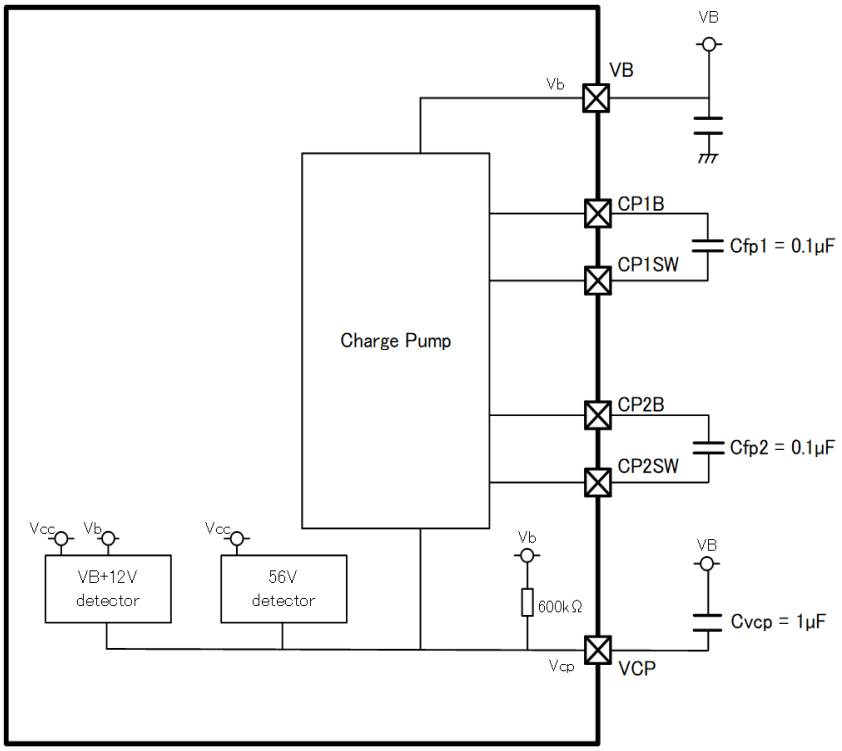


Fig. 9.3.1 Charge Pump Application Circuit Diagram

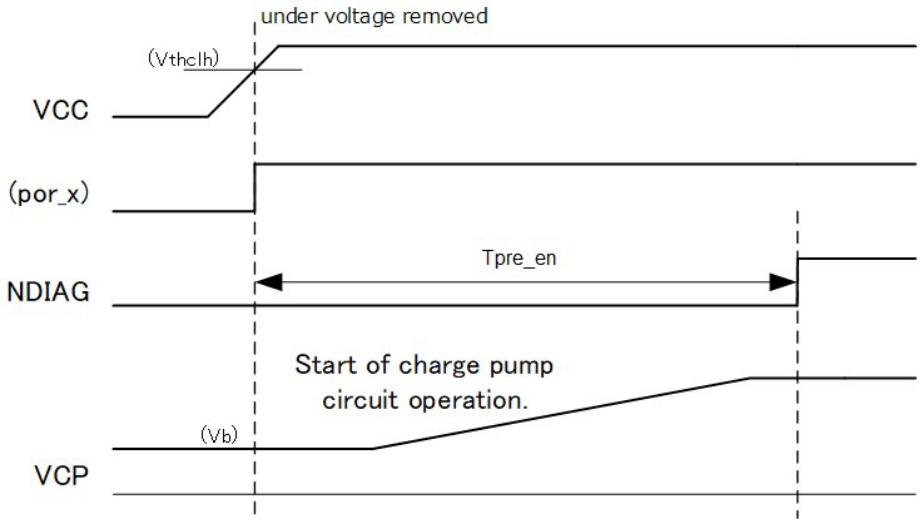


Fig. 9.3.2 Charge Pump Circuit Timing Chart

Note: A Tpre_en period is required after the release of Vcc under voltage detection for the charge pump voltage to stabilize.

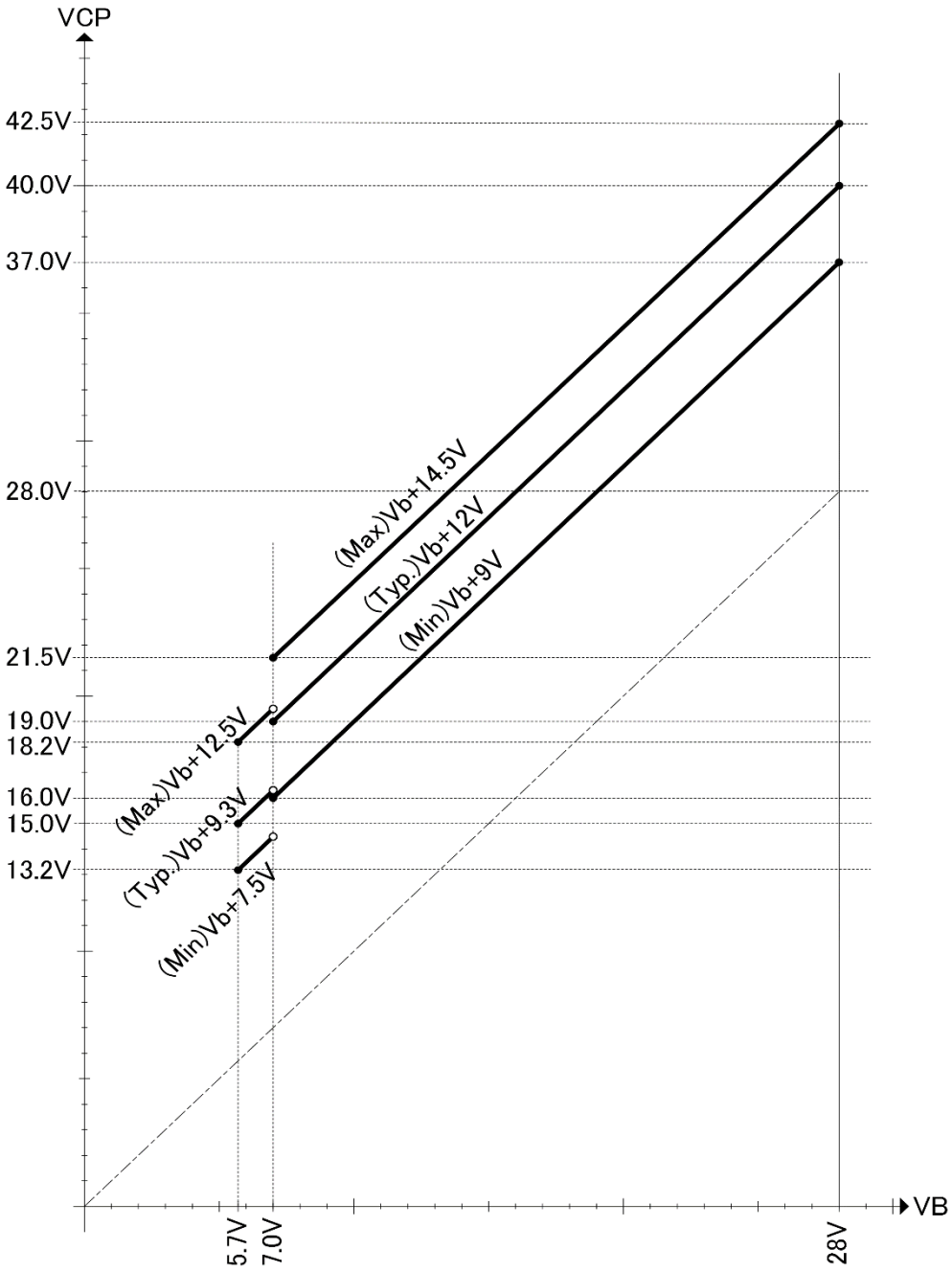


Fig. 9.3.3 Charge Pump Voltage vs power supply voltage

9.4. Gate Driver Circuits

Vb=5.7 to 28V, Vcc=3.0 to 5.5V, Tj=-40 to 175°C unless otherwise specified.

Spec No.	Item	Terminal	Symbol	Test Conditions	Min	Typ.	Max	Unit	Remarks
9.4.1	High level input current	HUI, HVI, HWI, LUI, LVI, LWI	Iih	Vcc= 5.0V, Vin = 5.0V	50	100	200	μA	-
9.4.2	Low level input current	HUI, HVI, HWI, LUI, LVI, LWI	Iil	Vcc = 5.0V, Vin = 0V	-5	-	5	μA	-
9.4.3	High level input detection voltage	HUI, HVI, HWI, LUI, LVI, LWI	Vih	-	0.75 ×Vcc	-	-	V	-
9.4.4	Low level input detection voltage	HUI, HVI, HWI, LUI, LVI, LWI	Vil	-	-	-	0.25 ×Vcc	V	-
9.4.5	Output voltage 1	HUO,HVO,HWO	Voh1	Voltage between H*O-H*S Iload=-100μA 7V≤Vb≤28V H*S=0V	7	10	12	V	-
9.4.6			Voh1_2	Voltage between H*O- H*S Iload=-100μA 5.7V≤Vb<7V H*S=0V	Vcp -0.3	-	Vcp	V	-
9.4.7			Vol1	Voltage between H*O-H*S Iload=100μA	0	-	0.2	V	-
9.4.8	Output voltage 2	LUO,LVO,LWO	Voh2	Voltage between L*O-LS LS=0V Iload=-100μA	6.7	11	12	V	-
9.4.9			Vol2	Voltage between L*O-LS LS=0V Iload=100μA	0	-	0.2	V	-
9.4.10	Output voltage 3	RPPO	Voh3	Iload=-110μA	Vcp -0.2	-	Vcp	V	A series resistor 500Ω incorporated.
9.4.11	Output resistance 1	HUO,HVO,HWO	Rohh	HUI,HVI,HWI = VCC Iload = -50 mA	-	8.8	24	Ω	-
9.4.12			Rohl	HUI,HVI,HWI = 0V Iload = 50 mA	-	3	6	Ω	-
9.4.13	Output resistance 2	LUO,LVO,LWO	Rolh	LUI,LVI,LWI = VCC Iload = -50 mA	-	8.8	24	Ω	-
9.4.14			Roll	LUI,LVI,LWI = 0V Iload = 50 mA	-	3	6	Ω	-
9.4.16	Pull-down resistance 1	HUO,HVO,HWO	Rpd1	-	25	50	100	kΩ	-
9.4.17	Pull-down resistance 2	LUO,LVO,LWO	Rpd2	-	25	50	100	kΩ	-

Vb=5.7 to 28V, Vcc=3.0 to 5.5V, Tj=-40 to 175°C unless otherwise specified.

Spec No.	Item	Terminal	Symbol	Test Conditions	Min	Typ.	Max	Unit	Remarks
9.4.17a	Pull-down resistance 3	VCP	Rpd3	-	200	600	1200	kΩ	-
9.4.18	Leak current when RPPO output is off	RPPO	Ioff _rppo	Internal high side switch is OFF. RPPO=VB	-5	0	5	μA	-
9.4.19	Leak current when VB is reverse polarity	RPPO	Iol	RPPO= 0V GND=PGND=18V VB=VCC=open	0	0.1	10	μA	-
9.4.20	Limited output current	HUO,HVO, HWO,LUO, LVO,LWO	Io_lmth	After Tsw at turn-on	-	-10	-	mA	See Fig. 9.4.2
9.4.21			Io_lmtl	After Tsw at turn-off	-	10	-	mA	See Fig. 9.4.2
9.4.22	Output current switching time	HUO,HVO, HWO,LUO, LVO,LWO	Tsw0	-	3.7	6	10.5	μs	t_ilim = “000” See Fig. 9.4.2
9.4.23			Tsw1	-	5	8	14	μs	t_ilim = “001” See Fig. 9.4.2
9.4.24			Tsw2	-	6.2	10	17.5	μs	t_ilim = “010” See Fig. 9.4.2
9.4.25			Tsw3	-	7.5	12	21	μs	t_ilim = “011” See Fig. 9.4.2
9.4.26			Tsw4	-	10	16	28	μs	t_ilim = “100” See Fig. 9.4.2
9.4.27			Tsw5	-	20	32	56	μs	t_ilim = “101” See Fig. 9.4.2
9.4.28			Tsw6	-	40	64	112	μs	t_ilim = “110” See Fig. 9.4.2
9.4.29			Tsw7	-	80	128	224	μs	t_ilim = “111” See Fig. 9.4.2
9.4.30	Turn on Input propagation delay time	HUI, HVI, HWI, HUO, HVO, HWO	Tdonh	-	20	180	350	ns	See Fig. 9.4.1 and Fig. 9.4.2.
9.4.31		LUI, LVI, LWI, LUO, LVO, LWO	Tdonl	-	20	180	350	ns	See Fig. 9.4.1 and Fig. 9.4.2.
9.4.32	Turn off Input propagation delay time	HUI, HVI, HWI, HUO, HVO, HWO	Tdoffh	-	20	180	350	ns	See Fig. 9.4.1 and Fig. 9.4.2.
9.4.33		LUI, LVI, LWI, LUO, LVO, LWO	Tdoffl	-	20	180	350	ns	See Fig. 9.4.1 and Fig. 9.4.2.
9.4.34	Difference in input propagation delay time	HUI, HVI, HWI, LUI, LVI, LWI, HUO,HVO, HWO,LUO, LVO, LWO	Dtd	Tdonh-Tdoffl, Tdonl-Tdoffh	-125	-	125	ns	Difference between high side/low side in the same UVW phase.

Note: For the test circuit, see Fig. 9.4.1.

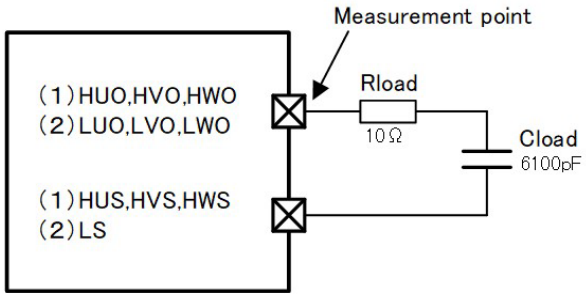


Fig. 9.4.1 Test Circuit Diagram (High side/Low side)

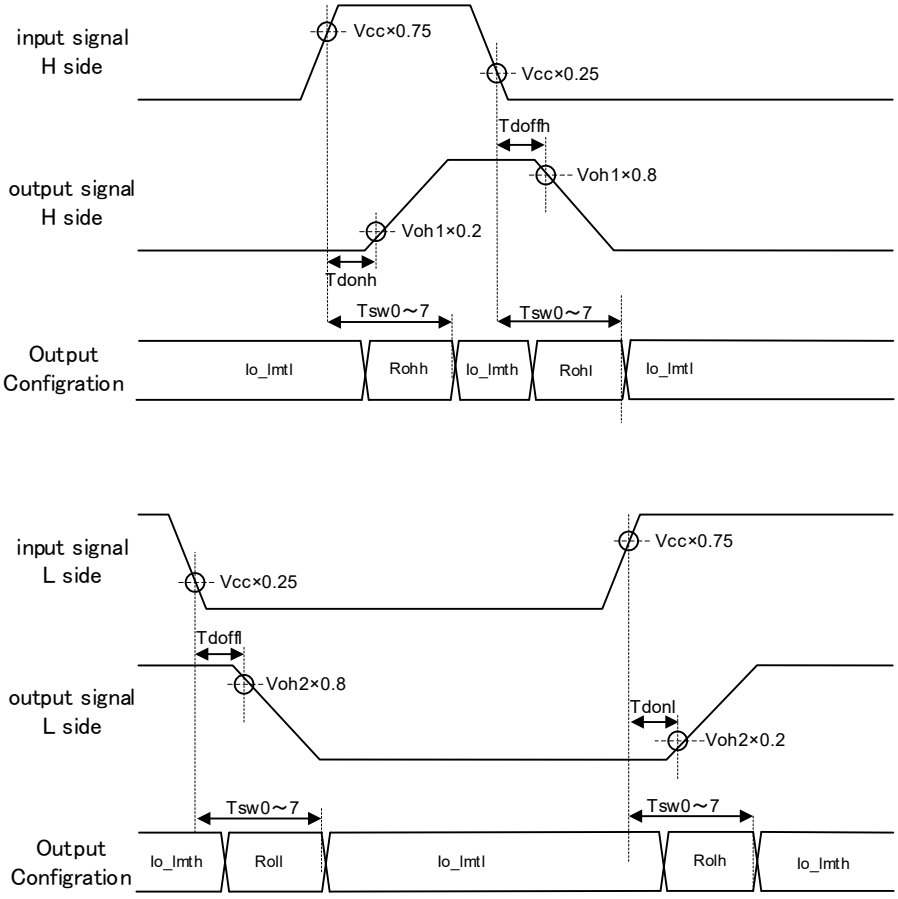


Fig. 9.4.2 Output Current Switching Time, Input Propagation Delay Time Timing Chart

9.5. Current Sense Amplifier Circuit

Vb=5.7 to 28V, Vcc=3.0 to 5.5V, Tj=-40 to 175°C unless otherwise specified.

Spec No.	Item	Terminal	Symbol	Test Conditions	Min	Typ.	Max	Unit	Remarks
9.5.1	Input offset voltage 1	AMP_P, AMP_N,	Voff1	After calibration Ta=25°C Gain=15 Comvin=0V Iload=0.5mA	-1	-	1	mV	gain_amp="011"
9.5.2	Input offset voltage 2	AMP_P, AMP_N,	Voff2	Before calibration Ta=25°C Gain=15 Comvin=0V Iload=0.5mA	-7	-	7	mV	gain_amp="011"
9.5.3	Input offset voltage temperature coefficient 1	AMP_P, AMP_N,	VoffdT1	After calibration Gain=15 Comvin=0V Iload=0.5mA	(-10)	-	(10)	µV /°C	gain_amp="011" The number in the bracket is a design value.
9.5.4	Input offset voltage temperature coefficient 2	AMP_P, AMP_N,	VoffdT2	Before calibration Gain=15, Comvin=0V Iload=0.5mA	(-10)	-	(10)	µV /°C	gain_amp="011" The number in the bracket is a design value.
9.5.5	Input offset current 1	AMP_P, AMP_N,	Iin1	Combination calculation formula of (AMP_P,AMP_N) = (-0.5V,-0.5V) (2V,2V): I(AMP_P)-I(AMP_N)	-5	-	5	µA	SPEC 9.5.21 cited for input voltage conditions.
9.5.5a	Input offset current 2	AMP_P, AMP_N,	Iin2	Combination calculation formula of (AMP_P,AMP_N) = (2V,-0.5V): I(AMP_P)-I(AMP_N)	30	-	130	µA	SPEC 9.5.21 cited for input voltage conditions.
9.5.6	Output voltage 1	AMP_O	Vohop	Gain=15 Vinr=0.1×Vcc Iload = -500µA	Vcc -0.15	-	Vcc	V	-
9.5.8	Reference voltage1	-	Vref1	4.5V≤VCC≤5.5V	Typ.-9	1/4 *VCC	Typ.+9	mV	-
9.5.8a	Reference voltage2	-	Vref2	3.0V≤VCC<4.5V	Typ.-9	1/4 *VCC	Typ. +13	mV	-
9.5.10	GAIN	AMP_P, AMP_N,	Gain0	Vinr=(Vcc*0.75-0.15)/7.5, Comvin=0V, Iload= No load	-1%	7.5	1%	-	gain_amp="000"
9.5.11			Gain1	Vinr=(Vcc*0.75-0.15)/10, Comvin=0V, Iload= No load	-1%	10	1%	-	gain_amp="001"
9.5.12			Gain2	Vinr=(Vcc*0.75-0.15)/12.5, Comvin=0V, Iload= No load	-1%	12.5	1%	-	gain_amp="010"
9.5.13			Gain3	Vinr=(Vcc*0.75-0.15)/15, Comvin=0V, Iload= No load	-1%	15	1%	-	gain_amp="011"
9.5.14			Gain4	Vinr=(Vcc*0.75-0.15)/20, Comvin=0V, Iload= No load	-1%	20	1%	-	gain_amp="100"
9.5.15			Gain5	Vinr=(Vcc*0.75-0.15)/30, Comvin=0V, Iload= No load	-1%	30	1%	-	gain_amp="101"
9.5.15a			Gain6	Vinr=(Vcc*0.75-0.15)/40, Comvin=0V, Iload= No load	-1.25 %	40	1.25%	-	gain_amp="110", "111"
9.5.16	Slew rate	AMP_O	Sr1	VCC=5.0V Gain=15 Rload=1kΩ,Cload=220pF	4.5	10	20	V/µs	Gain is set by register using SPI. See Fig. 9.5.2.

				Vinr=0V→(Vcc*0.75-0.15)/15 Vout=2.25V→4.0V Slew rates are as shown above.					
9.5.17				VCC=3.3V Gain=15 Rload=1kΩ,Cload=220pF Vinr=0V→(Vcc*0.75-0.15)/15 Vout=1.485V→2.64V Slew rates are as shown above.	4.5	10	20	V/μs	Gain is set by register using SPI. See Fig. 9.5.2.
9.5.18			Sr2	VCC=5.0V Gain=15 Rload=1kΩ,Cload=220pF Vinr= (Vcc*0.75-0.15)/15→0V Vout=4.0V→2.25V Slew rates are as shown above.	-20	-10	-4.5	V/μs	Gain is set by register using SPI. See Fig. 9.5.2.
9.5.19				VCC=3.3V Gain=15 Rload=1kΩ,Cload=220pF Vinr= (Vcc*0.75-0.15)/15→0V Vout=2.64V→1.485V Slew rates are as shown above.	-20	-10	-4.5	V/μs	Gain is set by register using SPI. See Fig. 9.5.2.
9.5.20	Settling Time	AMP_O	Tset	Rload=1kΩ,Cload=220pF Time for output voltage to converge within ±2%.	-	-	(1.5)	μs	The number in the bracket is a design value.
9.5.21	Input common voltage range	AMP_P, AMP_N,	Comvin	-	-0.5	-	2.0	V	-
9.5.22	PSRR	VCC	Psrrop	1KHz input to VCC, excluding influence of VREF.	-	60	-	dB	Reference value
9.5.23	CMRR	AMP_P, AMP_N,	Cmrrop	Vcc=5V,Gain=15, Comvin=20mVp-p,100KHz	-	100	-	dB	Reference value
9.5.24	Offset calibration time	-	$T_{ampofscal}$	-	-	-	122	μs	-

Note: The number in the bracket is a design value and not tested for shipment.
Note: For the test circuit, see Fig. 9.5.1. Differential voltage across Rsh when a current flows to GND is defined as Vinr.

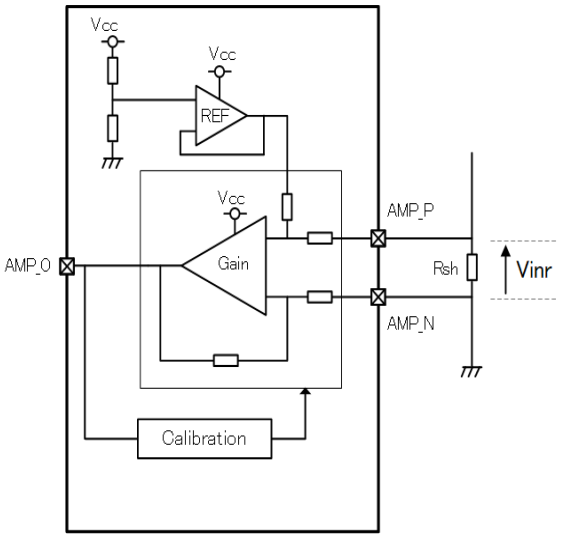


Fig. 9.5.1 Test Circuit Diagram

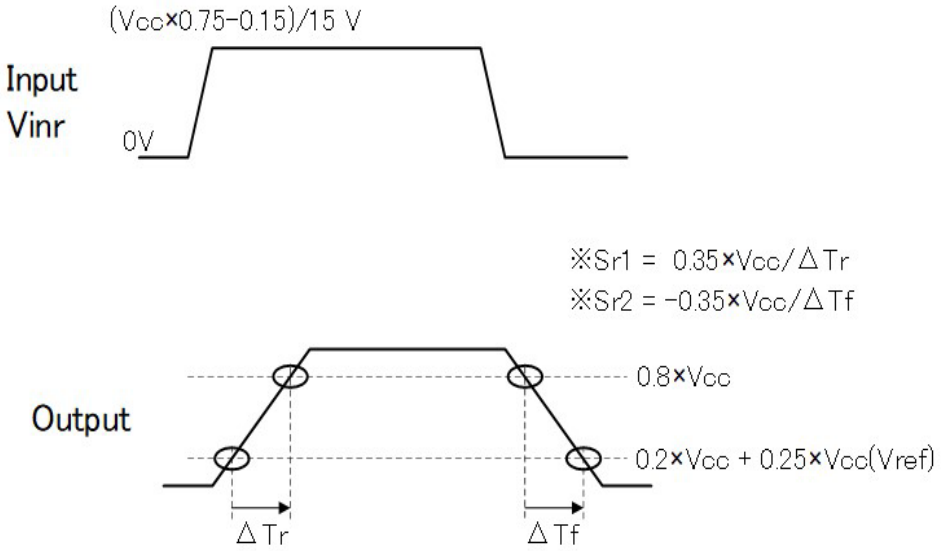


Fig. 9.5.2 Slew Rates Timing Chart

9.6. Oscillation Circuit

Vb=5.7 to 28V, Vcc=3.0 to 5.5V, Tj=-40 to 175°C unless otherwise specified.

Spec No.	Item	Terminal	Symbol	Test Conditions	Min	Typ.	Max	Unit	Remarks
9.6.1	Internal oscillating frequency	-	Fc	-	2.6	4	5.4	MHz	Variation of oscillating frequency: ±35%

9.7. Abnormality Detection Circuits

Vb=5.7 to 28V, Vcc=3.0 to 5.5V, Tj=-40 to 175°C unless otherwise specified.

Spec No.	Item	Terminal	Symbol	Test Conditions	Min	Typ.	Max	Unit	Remarks
9.7.1	VCC under voltage detection threshold	VCC	Vthcll	-	2.55	2.75	2.95	V	A reset state
9.7.2	VCC under voltage detection release threshold		Vthclh	-	2.65	2.85	3.05	V	Reset released.
9.7.3	VCC under voltage response time		Tcl	-	5	20	55	µs	-
9.7.4	VB under voltage detection threshold	VB	Vthbll	-	4.8	5.1	5.4	V	-
9.7.5	VB under voltage detection release threshold		Vthblh	-	5.1	5.4	5.7	V	-
9.7.6	VB under voltage detection filtering time		Tbl	-	12	20	34	µs	-
9.7.7	VCP over voltage detection threshold	VCP	Vthcphh	-	53.0	56.0	59.0	V	-
9.7.8	VCP over voltage detection release threshold		Vthcphl	-	49.0	52.0	55.0	V	-
9.7.9	VCP over voltage detection filtering time		Tcph	-	12	20	34	µs	-
9.7.10	VCC over voltage detection threshold	VCC	Vthchh	-	5.5	5.75	6.0	V	-
9.7.11	VCC over voltage detection release threshold		Vthchl	-	5.4	5.65	5.9	V	-
9.7.12	VCC over voltage detection filtering time		Tch	-	12	20	34	µs	-
9.7.13	RPPO under voltage detection threshold	RPPO	Vthrppll	-	-	Vcp - 3	Vcp - 2	V	-
9.7.14	RPPO under voltage detection release threshold	RPPO	Vthrpplh	-	-	Vcp - 2	Vcp - 1	V	-
9.7.15	RPPO under voltage detection filtering time	RPPO	Trppl		12	20	34	µs	-
9.7.16	Over temperature detection	-	Tsdh	-	(175)	(195)	(215)	°C	The number in the bracket is a design value.
9.7.17	Over temperature detection release		Tsdl	-	(165)	(185)	(205)	°C	The number in the bracket is a design value.
9.7.18	Over temperature detection filtering time		Ttsd	-	(12)	(20)	(34)	µs	The number in the bracket is a design value.
9.7.20	Output current 1 when 3-phase FET off	HUS, HVS, HWS	I_vds1_Roff	VB=HS=H*S=13.5V H*I=L	-650	-400	-200	µA	-
9.7.21	Output current 2 when 3-phase FET off	HUS, HVS, HWS	I_vds2_Roff	VB=HS=13.5V H*S=0V H*I= L	-650	-450	-250	µA	-

Note: The number in the bracket is a design value and are not tested for shipment.
Note: When Vcc reaches Vcc under voltage detection voltage, this product goes into a reset state.
Note: Circuits for under voltage detection (VB, VCC, RPPO), over voltage detection (VCP, VCC), and over temperature detection have hysteresis.

Spec No.	Item	Terminal	Symbol	Test Conditions	Min	Typ.	Max	Unit	Remarks
9.7.23	FETs VDS detection mask time	-	mask_vds	-	-35%	Set value	+35%	μs	-
9.7.24	VDS detection threshold voltage for high side of 3-phase FETs	-	Vth_vdsh0	-	0.04	0.1	0.16	V	vth_vdsh ="000"
9.7.25			Vth_vdsh1	-	0.24	0.3	0.36	V	vth_vdsh ="001"
9.7.26			Vth_vdsh2	-	0.44	0.5	0.56	V	vth_vdsh ="010"
9.7.27			Vth_vdsh3	-	0.63	0.7	0.77	V	vth_vdsh ="011"
9.7.28			Vth_vdsh4	-	0.81	0.9	0.99	V	vth_vdsh ="100"
9.7.29			Vth_vdsh5	-	0.99	1.1	1.21	V	vth_vdsh ="101"
9.7.30	VDS detection threshold voltage for low side of 3-phase FETs	-	Vth_vdsl0	VCC= 3.135 to 5.5V LS= -0.5 to 0.535V	0.04	0.1	0.16	V	vth_vdsl = "000"
9.7.31			Vth_vdsl1		0.24	0.3	0.36	V	vth_vdsl = "001"
9.7.32			Vth_vdsl2		0.44	0.5	0.56	V	vth_vdsl = "010"
9.7.33			Vth_vdsl3		0.63	0.7	0.77	V	vth_vdsl = "011"
9.7.34			Vth_vdsl4		0.81	0.9	0.99	V	vth_vdsl = "100"
9.7.35			Vth_vdsl5		0.99	1.1	1.21	V	vth_vdsl = "101"
9.7.36	NDIAG output voltage	NDIAG	Voh	Ioh = -5mA	0.9 ×Vcc	-	-	V	-
9.7.37			Vol	Iol = 5mA	-	-	0.1 ×Vcc	V	-
9.7.38	NDIAG L holding voltage	NDIAG	Vlk	Vcc=1.1V to Vthcll Iol = 100μA	0	-	0.3	V	See Fig. 9.7.1.

Note: VDS detection threshold voltage (high side) is specified as voltage between HS-H*S terminals of the IC.
Note: VDS detection threshold voltage (low side) is specified as voltage between H*S-LS terminals of the IC.
Note: "*" is U, V, W.

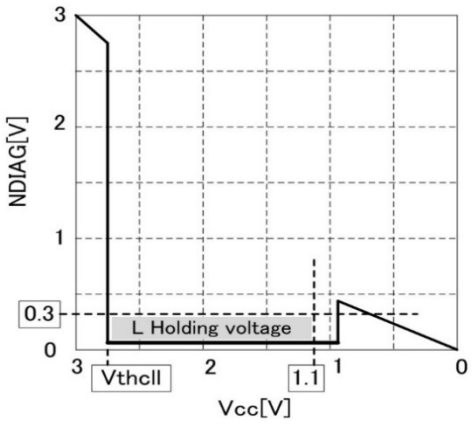


Fig. 9.7.1 NDIAG_L Holding Voltage

9.8. Alarm Input Circuit

Vb=5.7 to 28V, Vcc=3.0 to 5.5V, Tj=-40 to 175°C unless otherwise specified.

Spec No.	Item	Terminal	Symbol	Test Conditions	Min	Typ.	Max	Unit	Remarks
9.8.1	High level input current	ALARM	Iih	Vcc = 5.0V, Vin = 5.0V	-5	-	5	μA	-
9.8.2	Low level input current		Iil	Vcc = 5.0V, Vin = 0V	50	100	200	μA	VCC pullup
9.8.3	High level input detection voltage	ALARM	Vih	-	0.75× Vcc	-	-	V	-
9.8.4	Low level input detection voltage		Vil	-	-	-	0.25× Vcc	V	-
9.8.5	Input detection pulse width	ALARM	Twmin0	High, Low level detection	10.5	-	-	μs	fil_alm="1" $16x2^2x(1/4MHz)+(1/4MHz)$
9.8.6	Input removal pulse width	ALARM	Twmax0	High, Low level detection	-	-	20.0	μs	fil_alm="1" $15x2^2x(1/4MHz)-(1/4MHz)$

Note: Input detection pulse width (Twmin) is the width of pulses that come to the output passing through the digital filter, and input removal pulse width (Twmax) is the width of pulses removed by the digital filter (Refer to Fig. 9.8.1).
Note: Calculated assuming ALARM digital filter setting: (1/4MHz)=250[ns].

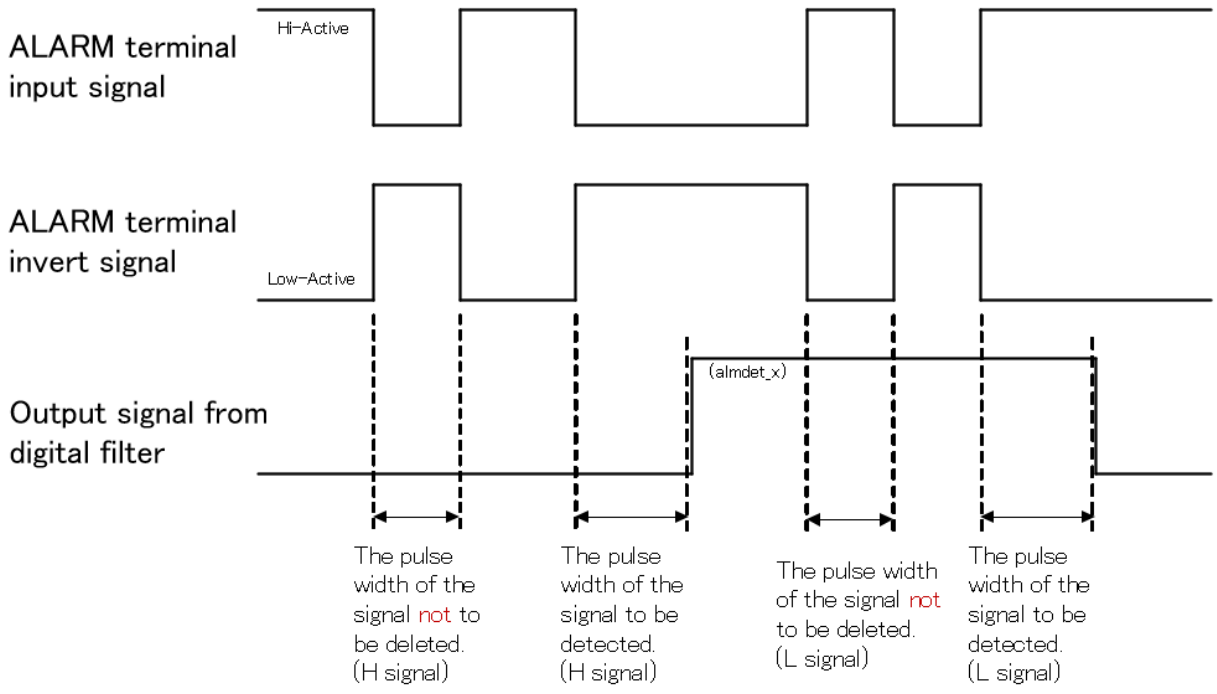


Fig. 9.8.1 Input Removal Pulse Width (with a Filter) and Input Detection Pulse Width (with a Filter)

9.9. SPI Communication Circuit

SPI Communication Specifications (AC)

Vb=5.7 to 28V, Vcc=3.0 to 5.5V, Tj=-40 to 175°C unless otherwise specified.

Spec No.	Item	Terminal	Symbol	Test Conditions	Min	Typ.	Max	Unit	Remarks
9.9.1	NCS fall – SO delay time	NCS SO	Tcsdo	Cload=100pF	-	-	100	ns	Time from NCS fall to release of Hi-Z at SO
9.9.2	Effective wait time	NCS, SCLK	Tcsck	Fop = 2MHz	100	-	-	ns	Time from NCS fall to SCLK rise
9.9.3	Ineffective wait time	SCLK, NCS	Tckcs	-	100	-	-	ns	Time from last SCLK fall to NCS rise
9.9.4	SI setup time	SI, SCLK	Tdick	-	50	-	-	ns	SI data setup time
9.9.5	SI hold time	SI, SCLK	Tckdi	-	50	-	-	ns	SI data hold time
9.9.6	SO delay time	SCLK, SO	Tckdo	Cload=100pF	-	-	100	ns	Time from SCLK rise to SO data output
9.9.7	NCS ineffective time	NCS	Tcsh	-	2	-	-	µs	Time from NCS rise to NCS fall
9.9.8	SO-NCS rise delay time	NCS, SO	Tdocs	Cload=100pF	-	-	100	ns	Time from NCS rise to SO being Hi-Z
9.9.9	Communication frequency	SCLK	Fop	-	-	-	2	MHz	-

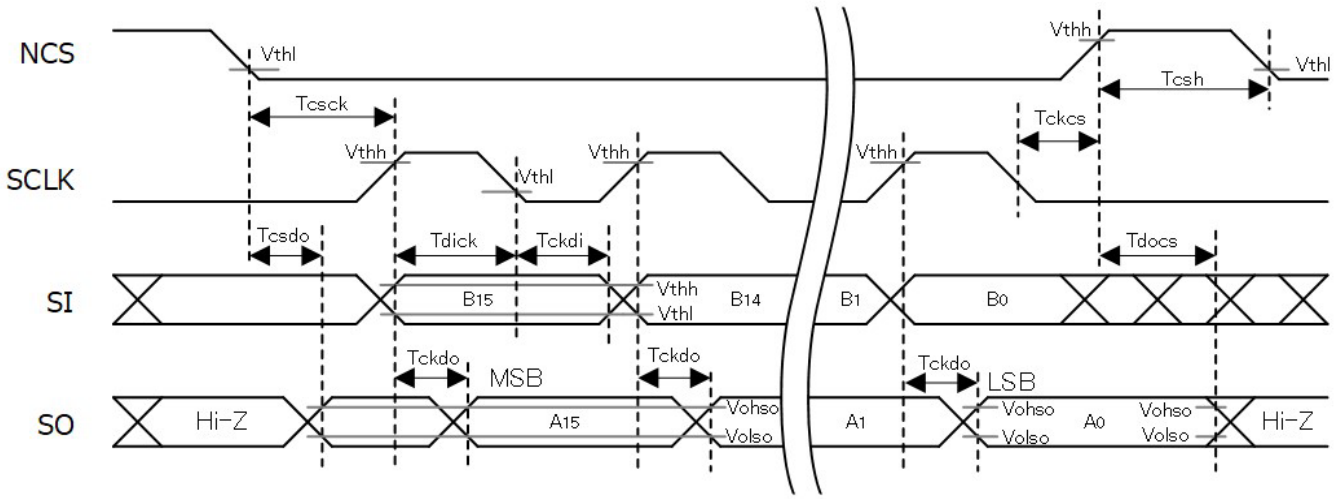


Fig. 9.9.1 SPI Timing Chart

SPI Communication Specifications (DC)

Vb=5.7 to 28V, Vcc=3.0 to 5.5V, Tj=-40 to 175°C unless otherwise specified.

Spec No.	Item	Terminal	Symbol	Test Conditions	Min	Typ.	Max	Unit	Remarks
9.9.10	High level input voltage	SI, SCLK, NCS	Vthh	-	0.75× Vcc	-	-	V	-
9.9.11	Low level input voltage		Vthl	-	-	-	0.25× Vcc	V	-
9.9.12	High level input current	NCS	Iih	Vcc = 5.0V, Vin = 5.0V	-5	-	5	µA	-
9.9.13	Low level input current		Iil	Vcc = 5.0V, Vin = 0V	-200	-100	-50	µA	-
9.9.14	High level input current	SI, SCLK	Iih	Vcc = 5.0V, Vin = 5.0V	50	100	200	µA	-
9.9.15	Low level input current		Iil	Vcc = 5.0V, Vin = 0V	-5	-	5	µA	-
9.9.16	High level output voltage	SO	Vohso	Iohso = -5mA	0.9× Vcc	-	-	V	-
9.9.17	Low level output voltage		Volso	Iolso = 5mA	-	-	0.1× Vcc	V	-
9.9.18	Off-leak current		Vohiz	SO=VCC or GND	-10	-	10	µA	In Hiz state

10. Application Circuit Example

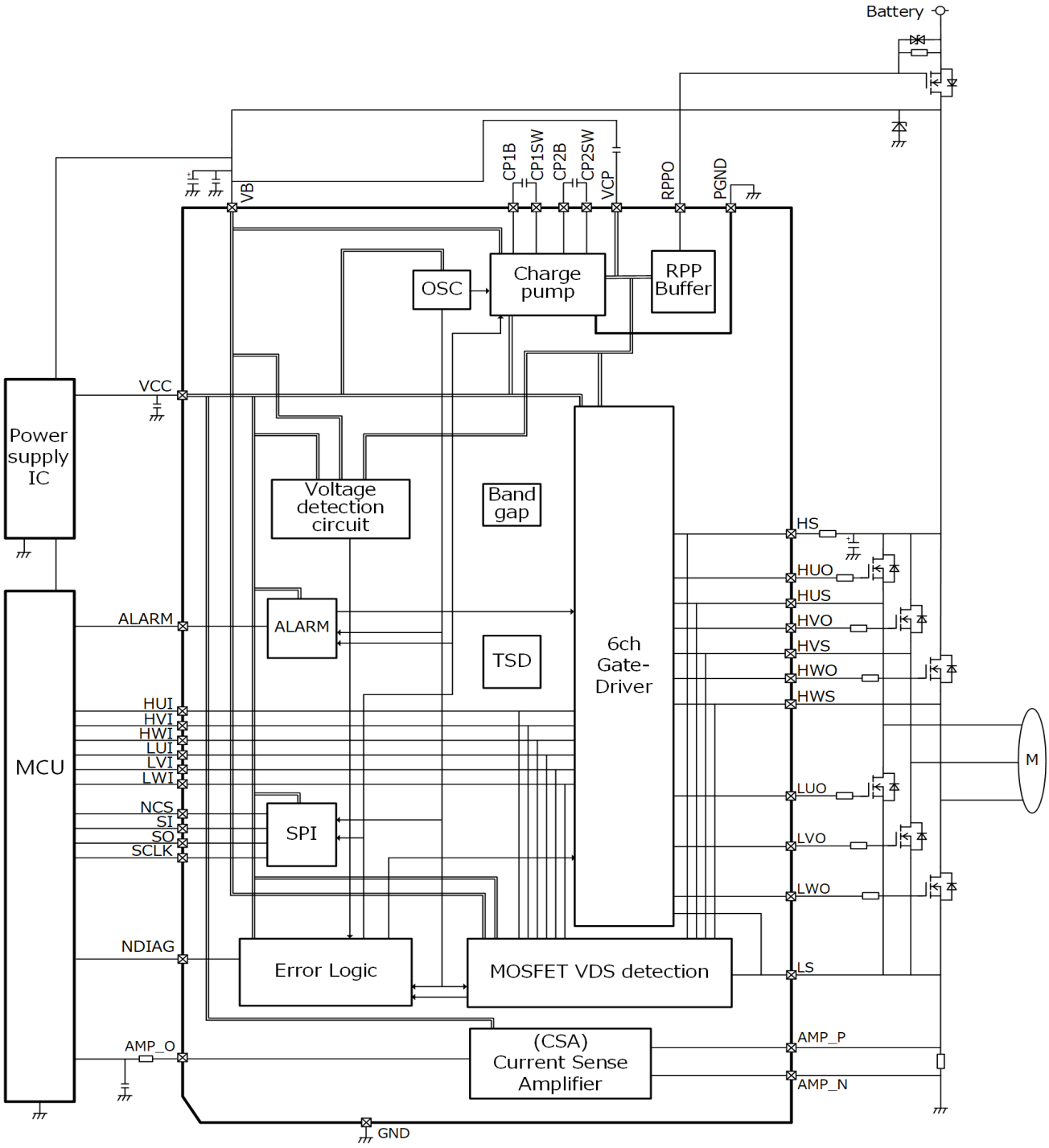


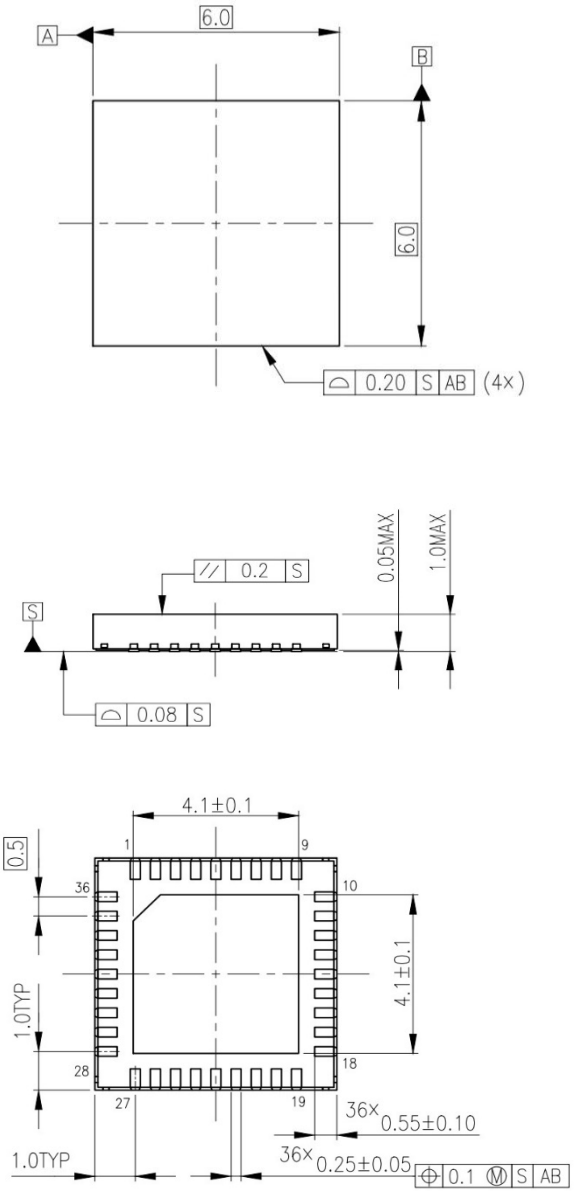
Fig. 10.1 Application Circuit Example

Note: Circuit constants shown here are for this application circuit example and not guaranteed. Determine peripheral circuits based on thorough evaluation and check under conditions assuming an operating environment on a board.
Note: Place smoothing capacitors externally connected to the power source terminals (VB, VCC, VCP) as close to the base of the IC as possible.
Note: Use solid GND (the same potential ±0.3V) on the board for GND terminal.
Note: In designing a unit, take into notes for each block into consideration as well.
Note: Do not connect this product incorrectly. It may break this IC and/or damage the equipment.

11. Package Outlines

Package dimensions

P-VQFN36-0606-0.50 "Unit:mm"



Weight: 95 mg (typ.)

Before creating and producing designs and using, customers must also refer to and comply with the latest versions of all relevant TOSHIBA information and the instructions for the application that Product will be used with or for.

12. Revision History

Revision#	Change contents	Date
-	Preliminary release	12.Sep.2024

13. Abbreviation Collection

CPOL : Clock POLarity
CPHA : Clock PHAse
RPPO : Reverse Polarity Protection Output
P-VQFN : Plastic-Very thin Quad Flat Non-leaded package
SPI : Serial Peripheral Interface
AEC : Automotive Electronics Council
CSA : Current Sense Amplifier

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