32-bit RISC Microcontroller

TX Family
TMPM471F10FG

Reference Manual
Product Information
(PINFO-TMPM471F10FG)

Revision 1.0

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Conventions

- Numeric formats follow the rules as shown below:
  Hexadecimal: 0xABC
  Decimal: 123 or 0d123 - Only when it needs to be explicitly shown that they are decimal numbers.
  Binary: 0b111 - It is possible to omit the "0b" when the number of bits can be distinctly understood from a sentence.
- "_N" is added to the end of signal names to indicate low active signals.
- It is called "assert" that a signal moves to its active level, deassert" to its inactive level.
- When two or more signal names are referred, they are described like as [m:n].
  Example: S[3:0] shows four signal names S3, S2, S1 and S0 together.
- The characters surrounded by ***[ ]*** defines the register.
  Example: ***[ABCD]***
- "n" substitutes suffix number of two or more same kind of registers, fields, and bit names.
  Example: ***[XYZ1]***, ***[XYZ2]***, ***[XYZ3]*** → ***[XYZn]***
- "x" substitutes suffix number or character of units and channels in the register list.
- In case of unit, "x" means A, B, and C, ...
  Example: ***[ADACR0]***, ***[ADBCR0]***, ***[ADCCR0]*** → ***[ADxCR0]***
- In case of channel, "x" means 0, 1, and 2, ...
  Example: ***[T32A0RUNA]***, ***[T32A1RUNA]***, ***[T32A2RUNA]*** → ***[T32AxRUNA]***
- The bit range of a register is written like as [m: n].
  Example: Bit[3: 0] expresses the range of bit 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.
  Example: ***[ABCD]***<EFG> = 0x01 (hexadecimal), ***[XYZn]***<VW> = 1 (binary)
- Word and byte represent the following bit length.
  Byte: 8 bits
  Half word: 16 bits
  Word: 32 bits
  Double word: 64 bits
- Properties of each bit in a register are expressed as follows:
  R: Read only
  W: Write only
  R/W: Read and write are possible.
- Unless otherwise specified, register access supports only word access.
- The register defined as "Reserved" must not be rewritten. Moreover, do not use the read value.
- The value read from the bit having default value of "-" is unknown.
- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value, In the cases that default is "-", follow the definition of each register.
- Reserved bits of the write-only register should be written with their default value. In the cases that default is "-", follow the definition of each register.
- Do not use read-modified-write processing to the register of a definition which is different by writing and read out.

Terms and Abbreviations

Some of abbreviations used in this document are as follows:

ADC	Analog to Digital Converter
A-ENC32	Advanced Encoder input Circuit (32-bit)
A-PMD	Advanced Programmable Motor Control Circuit
CRC	Cyclic Redundancy Check
DMAC	Direct Memory Access Controller
DNF	Digital Noise Filter
EHOSC	External High-Speed Oscillator
EI2C	I^2C Interface Version A
IHOSC	Internal High-Speed Oscillator
INT	Interrupt
LVD	Voltage Detection Circuit
NMI	Non-Maskable Interrupt
OFD	Oscillation Frequency Detector
RAMP	RAM Parity
SIWDT	Clock Selective Watchdog Timer
TRGSEL	Trigger Selection Circuit
TRM	Trimming Circuit
TSPI	Serial Peripheral Interface
T32A	32-bit Timer Event Counter
UART	Asynchronous Serial Communication Circuit

1. Overview

This chapter describes number of channels or units, information of pins and product-specific function information related to peripheral functions. Use this chapter in conjunction with Reference Manual for Peripheral Function.

2. Information of Peripheral Function

2.1. Register Base Address

The following table shows the type of base address of each peripheral.

Table 2.1 Type of Register Base Address (1/2)

Peripheral function			Type of base address (✓: Applicable, -: N/A)			Base address
			TYPE1	TYPE2	TYPE3	
Voltage Detection Circuit	LVD	-	✓	-	-	0x4003EC00
RAM Parity	RAMP	ch 0	-	-	✓	0x40043000
		ch 1	-	✓	-	0x400A3000
CRC Calculation Circuit	CRC	-	-	-	✓	0x40043100
Digital Noise Filter Circuit	DNF	unit A	-	✓	-	0x400A0200
Clock Selective Watchdog Timer	SIWDT	ch 0	-	✓	-	0x400A0600
Direct Memory Access Controller	DMAC	unit A	-	✓	-	0x400A4000
12-bit Analog to Digital Converter	ADC	unit A	-	-	✓	0x4005A000
		unit B				0x4005A400
32-bit Timer Event Counter	T32A	ch 0	-	✓	-	0x400C1000
		ch 1				0x400C1400
		ch 2				0x400C1800
		ch 3				0x400C1C00
		ch 4				0x400C2000
Serial Peripheral Interface	TSPI	ch 0	-	✓	-	0x400CA000
		ch 1				0x400CA400
		ch 2				0x400CA800
		ch 3				0x400CAC00
Universal Asynchronous Receiver Transmitter Circuit	UART	ch 0	-	✓	-	0x400CE000
		ch 1				0x400CE400
		ch 2				0x400CE800
		ch 3				0x400CEC00
		ch 4				0x400CF000
I^2C Interface Version A	EI2C	ch 0	-	-	✓	0x400D1000
		ch 1				0x400D2000

Table 2.2 Type of Register Base Address (2/2)

Peripheral function			Type of base address (✓: Applicable, -: N/A)			Base address
			TYPE1	TYPE2	TYPE3	
Trimming Circuit	TRM	-	-	✓	-	0x400E3100
Oscillation Frequency Detector	OFD	-	-	✓	-	0x400E4000
Advanced Programmable Motor Control Circuit	A-PMD	ch 0	-	-	✓	0x40089000
		ch 1				0x40089400
Advanced Encoder Input Circuit (32-bit)	A-ENC32	ch 0	-	-	✓	0x4008A000
		ch 1				0x4008A400
Flash Memory	Flash	-	✓	-	-	0x5DFF0000

To develop each peripheral function, please refer to the above type of base address.

2.2. Trigger Selector (TRGSEL)

The trigger selector is the circuit which chooses the one trigger and outputs the trigger signal to the peripheral function from two or more triggers inputted from the peripheral function, the port, etc.

The trigger chosen from eight triggers by ***[TSEL0CRn]***<INSELm> is outputted to the peripheral function of a connection destination.

"Figure 2.1 Example of Trigger Selector Connection" is the example of the DMAC transfer completion interrupts are connected to DMAC (channel 29) via the trigger selector. The setup of input trigger selection, edge detection condition selection, trigger output selection, and trigger output control is performed by ***[TSEL0CR4]***.

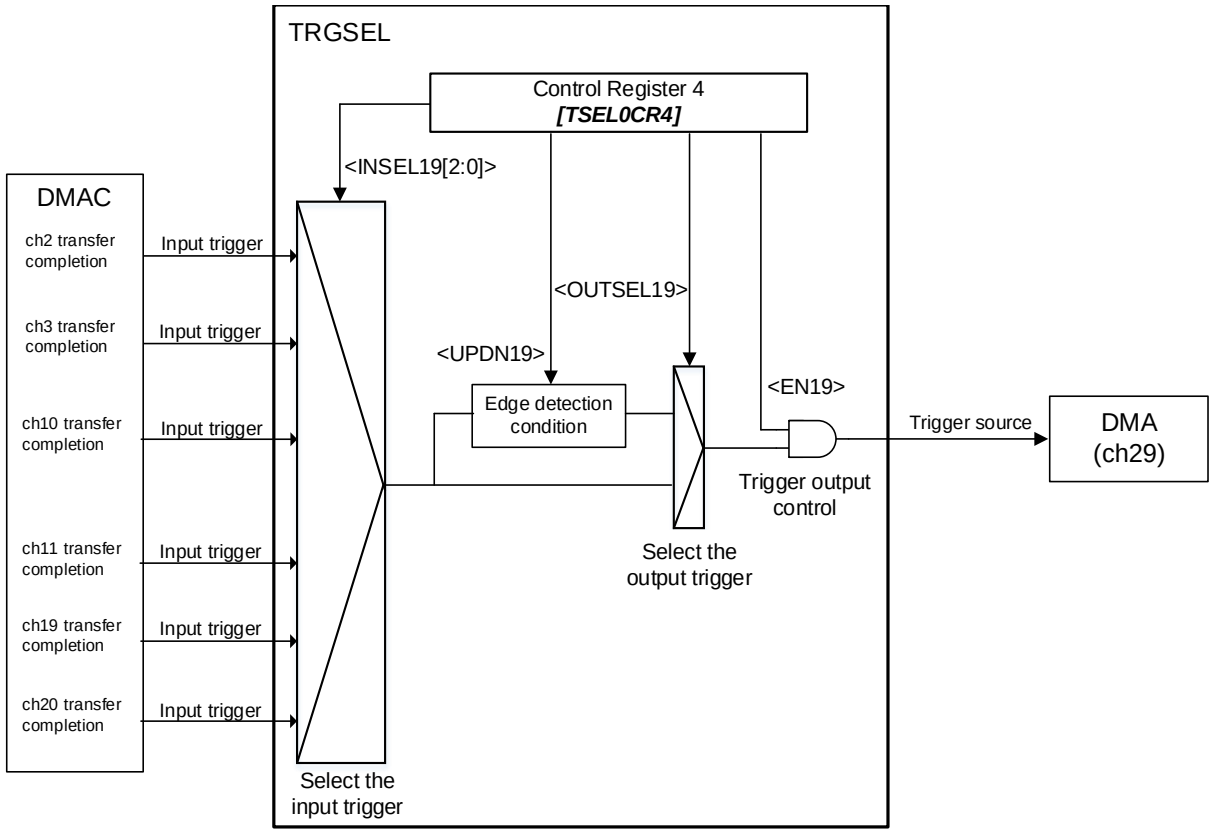

Figure 2.1 Example of Trigger Selector Connection

2.2.1. Operation and Setting

When using TRGSEL, please set an applicable clock enable bit to "1" (clock supply) in fsys supply stop register A (***[CGFSYSENA]***, ***[CGFSYSMENA]***), fsys supply stop register B (***[CGFSYSMENB]***), and fc supply stop register (***[CGFCEN]***).

An applicable register and the bit position vary according to a product. Therefore, the register may not exist with the product. Please refer to the reference manual "Clock Control and Operation Mode" the reference manual for the details.

Setting procedure of Trigger selector is as following.

(1) Selection of an input trigger (***[TSEL0CRn]***<INSELm>)

Selection of the input trigger used for the trigger source is performed.

Please set up selection of the input trigger by the input trigger selector bit (***[TSEL0CRn]***<INSELm>) of the control register. (n: register number, m: trigger number)

(2) Selection of edge detection conditions (***[TSEL0CRn]***<UPDNm>)

For the input trigger signal which needs edge detection, selection of rising edge or falling edge detection is performed.

Please set up selection of edge detection conditions in the selection bit (***[TSEL0CRn]***<UPDNm>) of a control register.

The following shows the trigger signal which needs edge detection.

- External trigger input (TRGIN0, TRGIN1, and TRGIN2)

(3) Selection of a trigger output (***[TSEL0CRn]***<OUTSELm>)

Selection of an output without or with edge detection is performed.

Please set up selection of a trigger output in the selection bit (***[TSEL0CRn]***<OUTSELm>) of a control register.

(4) Output enable (***[TSEL0CRn]***<ENm>)

The output (enable/disable) of the selected trigger signal is chosen.

Please set up selection of output (enable/disable) in the setting bit (***[TSEL0CRn]***<ENm>) of a control register. A trigger output will be enabled if ***[TSEL0CRn]***<ENm> is set to "1".

2.2.2. List of Registers

The table below shows control registers and their addresses.

Peripheral function		Channel/Unit	Base address
Trigger selector	TRGSEL	ch0	0x400A0400

Register name		Address(Base+)
Control Register 0	***[TSELxCR0]***	0x0000
Control Register 1	***[TSELxCR1]***	0x0004
Control Register 2	***[TSELxCR2]***	0x0008
Control Register 3	***[TSELxCR3]***	0x000C
Control Register 4	***[TSELxCR4]***	0x0010
Control Register 5	***[TSELxCR5]***	0x0014
Control Register 6	***[TSELxCR6]***	0x0018
Control Register 7	***[TSELxCR7]***	0x001C
Control Register 8	***[TSELxCR8]***	0x0020
Control Register 9	***[TSELxCR9]***	0x0024
Control Register 10	***[TSELxCR10]***	0x0028

2.2.3. Details of Registers

The following sections show the detail of registers. The symbol in the parenthesis in function column of each table expresses each function signal name.

2.2.3.1. *[TSELxCR0]* (Control Register 0)

Bit	Bit symbol	After reset	Type	Function
31	-	0	R	Read as "0"
30:28	INSEL3[2:0]	000	R/W	Select the input trigger (DMA ch3) 000: TSPI ch1 transmit DMA request (TSPI1TX_DMA) 001: UART ch1 transmission DMA request ((UART1TX_DMAREQ) 010: Reserved 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved
27	-	0	R	Read as "0"
26	UPDN3	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
25	OUTSEL3	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
24	EN3	0	R/W	Trigger output control 0: Disable 1: Enable
23	-	0	R	Read as "0"
22:20	INSEL2[2:0]	000	R/W	Select the input trigger (DMA ch2) 000: TSPI ch1 receive DMA request (TSPI1RX_DMA) 001: UART ch1 reception DMA request (UART1RX_DMAREQ) 010: Reserved 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved
19	-	0	R	Read as "0"
18	UPDN2	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
17	OUTSEL2	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
16	EN2	0	R/W	Trigger output control 0: Disable 1: Enable
15	-	0	R	Read as "0"

Bit	Bit symbol	After reset	Type	Function
14:12	INSEL1[2:0]	000	R/W	Select the input trigger (DMA ch1) 000: TSPI ch0 transmit DMA request (TSPI0TX_DMA) 001: UART ch0 transmission DMA request ((UART0TX_DMAREQ) 010: Reserved 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved
11	-	0	R	Read as "0"
10	UPDN1	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
9	OUTSEL1	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
8	EN1	0	R/W	Trigger output control 0: Disable 1: Enable
7	-	0	R	Read as "0"
6:4	INSEL0[2:0]	000	R/W	Select the input trigger (DMA ch0) 000: TSPI ch0 receive DMA request (TSPI0RX_DMA) 001: UART ch0 reception DMA request (UART0RX_DMAREQ) 010: Reserved 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved
3	-	0	R	Read as "0"
2	UPDN0	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
1	OUTSEL0	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
0	EN0	0	R/W	Trigger output control 0: Disable 1: Enable

2.2.3.2. *[TSELxCR1]* (Control Register 1)

Bit	Bit symbol	After reset	Type	Function
31	-	0	R	Read as "0"
30:28	INSEL7[2:0]	000	R/W	Select the input trigger (DMA ch7) 000: TSPI ch3 transmit DMA request (TSPI3TX_DMA) 001: UART ch3 transmission DMA request ((UART3TX_DMAREQ) 010: Reserved 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved
27	-	0	R	Read as "0"
26	UPDN7	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
25	OUTSEL7	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
24	EN7	0	R/W	Trigger output control 0: Disable 1: Enable
23	-	0	R	Read as "0"
22:20	INSEL6[2:0]	000	R/W	Select the input trigger (DMA ch6) 000: TSPI ch3 receive DMA request (TSPI3RX_DMA) 001: UART ch3 reception DMA request (UART3RX_DMAREQ) 010: Reserved 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved
19	-	0	R	Read as "0"
18	UPDN6	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
17	OUTSEL6	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
16	EN6	0	R/W	Trigger output control 0: Disable 1: Enable
15	-	0	R	Read as "0"
14:12	INSEL5[2:0]	000	R/W	Select the input trigger (DMA ch5) 000: TSPI ch2 transmit DMA request (TSPI2TX_DMA) 001: UART ch2 transmission DMA request ((UART2TX_DMAREQ) 010: Reserved 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved

Bit	Bit symbol	After reset	Type	Function
11	-	0	R	Read as "0"
10	UPDN5	0	R/W	Edge detection 0: Rising edge detection 1: falling edge detection
9	OUTSEL5	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
8	EN5	0	R/W	Trigger output control 0: Disable 1: Enable
7	-	0	R	Read as "0"
6:4	INSEL4[2:0]	000	R/W	Select the input trigger (DMA ch4) 000: TSPI ch2 receive DMA request (TSPI2RX_DMA) 001: UART ch2 reception DMA request (UART2RX_DMAREQ) 010: Reserved 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved
3	-	0	R	Read as "0"
2	UPDN4	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
1	OUTSEL4	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
0	EN4	0	R/W	Trigger output control 0: Disable 1: Enable

2.2.3.3. *[TSELxCR2]* (Control Register 2)

Bit	Bit symbol	After reset	Type	Function
31	-	0	R	Read as "0"
30:28	INSEL11[2:0]	000	R/W	Select the input trigger (DMA ch20) 000: T32A ch2 DMA request at match A1 register (T32A02DMAREQCMPA1) 001: T32A ch2 DMA request at match C1 register (T32A02DMAREQCMPC1) 010: T32A ch3 DMA request at match A1 register (T32A03DMAREQCMPA1) 011: T32A ch3 DMA request at match C1 register (T32A03DMAREQCMPC1) 100: T32A ch4 DMA request at match A1 register (T32A04DMAREQCMPA1) 101: T32A ch4 DMA request at match C1 register (T32A04DMAREQCMPC1) 110: Reserved 111: Reserved
27	-	0	R	Read as "0"
26	UPDN11	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
25	OUTSEL11	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
24	EN11	0	R/W	Trigger output control 0: Disable 1: Enable
23	-	0	R	Read as "0"
22:20	INSEL10[2:0]	000	R/W	Select the input trigger (DMA ch19) 000: T32A ch0 DMA request at match A1 register (T32A00DMAREQCMPA1) 001: T32A ch0 DMA request at match C1 register (T32A00DMAREQCMPC1) 010: T32A ch1 DMA request at match A1 register (T32A01DMAREQCMPA1) 011: T32A ch1 DMA request at match C1 register (T32A01DMAREQCMPC1) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
19	-	0	R	Read as "0"
18	UPDN10	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
17	OUTSEL1	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
16	EN10	0	R/W	Trigger output control 0: Disable 1: Enable
15	-	0	R	Read as "0"
14:12	INSEL9[2:0]	000	R/W	Select the input trigger (DMA ch17) 000: ADC unit B general purpose trigger DMA request (ADBTRG_DMAREQ) 001: ADC unit B single conversion DMA request (ADBSGL_DMAREQ) 010: ADC unit B continue conversion DMA request (ADBCNT_DMAREQ) 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved

Bit	Bit symbol	After reset	Type	Function
11	-	0	R	Read as "0"
10	UPDN9	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
9	OUTSEL9	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
8	EN9	0	R/W	Trigger output control 0: Disable 1: Enable
7	-	0	R	Read as "0"
6:4	INSEL8[2:0]	000	R/W	Select the input trigger (DMA ch16) 000: ADC unit A general purpose trigger DMA request (ADATRG_DMAREQ) 001: ADC unit A single conversion DMA request (ADASGL_DMAREQ) 010: ADC unit A continue conversion DMA request (ADACNT_DMAREQ) 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved
3	-	0	R	Read as "0"
2	UPDN8	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
1	OUTSEL8	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
0	EN8	0	R/W	Trigger output control 0: Disable 1: Enable

2.2.3.4. *[TSELxCR3]* (Control Register 3)

Bit	Bit symbol	After reset	Type	Function
31	-	0	R	Read as "0"
30:28	INSEL15[2:0]	000	R/W	Select the input trigger (DMA ch25) 000: T32A ch4 DMA request at capture A0 register (T32A04DMAREQCAPA0) 001: T32A ch4 DMA request at capture A1 register (T32A04DMAREQCAPA1) 010: T32A ch4 DMA request at capture C0 register (T32A04DMAREQCAPC0) 011: T32A ch4 DMA request at capture C1 register (T32A04DMAREQCAPC1) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
27	-	0	R	Read as "0"
26	UPDN15	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
25	OUTSEL15	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
24	EN15	0	R/W	Trigger output control 0: Disable 1: Enable
23	-	0	R	Read as "0"
22:20	INSEL14[2:0]	000	R/W	Select the input trigger (DMA ch24) 000: T32A ch2 DMA request at capture A0 register (T32A02DMAREQCAPA0) 001: T32A ch2 DMA request at capture A1 register (T32A02DMAREQCAPA1) 010: T32A ch3 DMA request at capture A0 register (T32A03DMAREQCAPA0) 011: T32A ch3 DMA request at capture A1 register (T32A03DMAREQCAPA1) 100: T32A ch2 DMA request at capture C0 register (T32A02DMAREQCAPC0) 101: T32A ch2 DMA request at capture C1 register (T32A02DMAREQCAPC1) 110: T32A ch3 DMA request at capture C0 register (T32A03DMAREQCAPC0) 111: T32A ch3 DMA request at capture C1 register (T32A03DMAREQCAPC1)
19	-	0	R	Read as "0"
18	UPDN14	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
17	OUTSEL14	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
16	EN14	0	R/W	Trigger output control 0: Disable 1: Enable
15	-	0	R	Read as "0"
14:12	INSEL13[2:0]	000	R/W	Select the input trigger (DMA ch23) 000: T32A ch0 DMA request at capture A0 register (T32A00DMAREQCAPA0) 001: T32A ch0 DMA request at capture A1 register (T32A00DMAREQCAPA1) 010: T32A ch1 DMA request at capture A0 register (T32A01DMAREQCAPA0) 011: T32A ch1 DMA request at capture A1 register (T32A01DMAREQCAPA1) 100: T32A ch0 DMA request at capture C0 register (T32A00DMAREQCAPC0) 101: T32A ch0 DMA request at capture C1 register (T32A00DMAREQCAPC1) 110: T32A ch1 DMA request at capture C0 register (T32A01DMAREQCAPC0) 111: T32A ch1 DMA request at capture C1 register (T32A01DMAREQCAPC1)

Bit	Bit symbol	After reset	Type	Function
11	-	0	R	Read as "0"
10	UPDN13	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
9	OUTSEL13	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
8	EN13	0	R/W	Trigger output control 0: Disable 1: Enable
7	-	0	R	Read as "0"
6:4	INSEL12[2:0]	000	R/W	Select the input trigger (DMA ch22) 000: T32A ch0 DMA request at match B1 register (T32A00DMAREQCMPB1) 001: T32A ch1 DMA request at match B1 register (T32A01DMAREQCMPB1) 010: T32A ch2 DMA request at match B1 register (T32A02DMAREQCMPB1) 011: T32A ch3 DMA request at match B1 register (T32A03DMAREQCMPB1) 100: T32A ch4 DMA request at match B1 register (T32A04DMAREQCMPB1) 101: Reserved 110: Reserved 111: Reserved
3	-	0	R	Read as "0"
2	UPDN12	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
1	OUTSEL12	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
0	EN12	0	R/W	Trigger output control 0: Disable 1: Enable

2.2.3.5. *[TSELxCR4]* (Control Register 4)

Bit	Bit symbol	After reset	Type	Function
31	-	0	R	Read as "0"
30:28	INSEL19[2:0]	000	R/W	Select the input trigger (DMA ch29) 000: DMAC ch2 transfer completion (INTDMAATC2) 001: DMAC ch3 transfer completion (INTDMAATC3) 010: DMAC ch10 transfer completion (INTDMAATC10) 011: DMAC ch11 transfer completion (INTDMAATC11) 100: DMAC ch19 transfer completion (INTDMAATC19) 101: DMAC ch20 transfer completion (INTDMAATC20) 110: Reserved 111: Reserved
27	-	0	R	Read as "0"
26	UPDN19	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
25	OUTSEL19	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
24	EN19	0	R/W	Trigger output control 0: Disable 1: Enable
23	-	0	R	Read as "0"
22:20	INSEL18[2:0]	000	R/W	Select the input trigger (DMA ch28) 000: DMAC ch0 transfer completion (INTDMAATC0) 001: DMAC ch1 transfer completion (INTDMAATC1) 010: DMAC ch8 transfer completion (INTDMAATC8) 011: DMAC ch9 transfer completion (INTDMAATC9) 100: DMAC ch16 transfer completion (INTDMAATC16) 101: DMAC ch17 transfer completion (INTDMAATC17) 110: DMAC ch26 transfer completion (INTDMAATC26) 111: DMAC ch27 transfer completion (INTDMAATC27)
19	-	0	R	Read as "0"
18	UPDN18	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
17	OUTSEL18	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
16	EN18	0	R/W	Trigger output control 0: Disable 1: Enable
15	-	0	R	Read as "0"
14:12	INSEL17[2:0]	000	R/W	Select the input trigger (DMA ch27) 000: T32A ch3 DMA request at capture B0 register (T32A03DMAREQCAPB0) 001: T32A ch3 DMA request at capture B1 register (T32A03DMAREQCAPB1) 010: T32A ch4 DMA request at capture B0 register (T32A04DMAREQCAPB0) 011: T32A ch4 DMA request at capture B1 register (T32A04DMAREQCAPB1) 100: Reserved 101: Reserved 110: Reserved 111: Reserved

Bit	Bit symbol	After reset	Type	Function
11	-	0	R	Read as "0"
10	UPDN17	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
9	OUTSEL17	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
8	EN17	0	R/W	Trigger output control 0: Disable 1: Enable
7	-	0	R	Read as "0"
6:4	INSEL16[2:0]	000	R/W	Select the input trigger (DMA ch26) 000: T32A ch0 DMA request at capture B0 register (T32A00DMAREQCAPB0) 001: T32A ch0 DMA request at capture B1 register (T32A00DMAREQCAPB1) 010: T32A ch1 DMA request at capture B0 register (T32A01DMAREQCAPB0) 011: T32A ch1 DMA request at capture B1 register (T32A01DMAREQCAPB1) 100: T32A ch2 DMA request at capture B0 register (T32A02DMAREQCAPB0) 101: T32A ch2 DMA request at capture B1 register (T32A02DMAREQCAPB1) 110: Reserved 111: Reserved
3	-	0	R	Read as "0"
2	UPDN16	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
1	OUTSEL16	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
0	EN16	0	R/W	Trigger output control 0: Disable 1: Enable

2.2.3.6. *[TSELxCR5]* (Control Register 5)

Bit	Bit symbol	After reset	Type	Function
31	-	0	R	Read as "0"
30:28	INSEL23[2:0]	000	R/W	Select the input trigger (ADC unit B trigger input) 000: T32A ch2 timer register A1 match trigger (T32A02TRGOUTCMPA1) 001: T32A ch2 timer register B1 match trigger (T32A02TRGOUTCMPB1) 010: Reserved 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved
27	-	0	R	Read as "0"
26	UPDN23	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
25	OUTSEL23	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
24	EN23	0	R/W	Trigger output control 0: Disable 1: Enable
23	-	0	R	Read as "0"
22:20	INSEL22[2:0]	000	R/W	Select the input trigger (ADC unit A trigger input) 000: T32A ch0 timer register A1 match trigger (T32A00TRGOUTCMPA1) 001: T32A ch0 timer register B1 match trigger (T32A00TRGOUTCMPB1) 010: Reserved 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved
19	-	0	R	Read as "0"
18	UPDN22	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
17	OUTSEL22	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
16	EN22	0	R/W	Trigger output control 0: Disable 1: Enable
15	-	0	R	Read as "0"
14:12	INSEL21[2:0]	000	R/W	Select the input trigger (DMA ch31) 000: DMAC ch6 transfer completion (INTDMAATC6) 001: DMAC ch7 transfer completion (INTDMAATC7) 010: DMAC ch14 transfer completion (INTDMAATC14) 011: DMAC ch15 transfer completion (INTDMAATC15) 100: DMAC ch24 transfer completion (INTDMAATC24) 101: DMAC ch25 transfer completion (INTDMAATC25) 110: Reserved 111: Reserved

Bit	Bit symbol	After reset	Type	Function
11	-	0	R	Read as "0"
10	UPDN21	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
9	OUTSEL21	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
8	EN21	0	R/W	Trigger output control 0: Disable 1: Enable
7	-	0	R	Read as "0"
6:4	INSEL20[2:0]	000	R/W	Select the input trigger (DMA ch30) 000: DMAC ch4 transfer completion (INTDMAATC4) 001: DMAC ch5 transfer completion (INTDMAATC5) 010: DMAC ch12 transfer completion (INTDMAATC12) 011: DMAC ch13 transfer completion (INTDMAATC13) 100: DMAC ch22 transfer completion (INTDMAATC22) 101: DMAC ch23 transfer completion (INTDMAATC23) 110: Reserved 111: Reserved
3	-	0	R	Read as "0"
2	UPDN20	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
1	OUTSEL20	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
0	EN20	0	R/W	Trigger output control 0: Disable 1: Enable

2.2.3.7. *[TSELxCR6]* (Control Register 6)

Bit	Bit symbol	After reset	Type	Function
31	-	0	R	Read as "0"
30:28	INSEL27[2:0]	000	R/W	Select the input trigger (TSPI/UART ch3 trigger input) 000: T32A ch4 timer register A1 match trigger (T32A04TRGOUTCMPA1) 001: T32A ch4 timer register B1 match trigger (T32A04TRGOUTCMPB1) 010: Reserved 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved
27	-	0	R	Read as "0"
26	UPDN27	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
25	OUTSEL27	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
24	EN27	0	R/W	Trigger output control 0: Disable 1: Enable
23	-	0	R	Read as "0"
22:20	INSEL26[2:0]	000	R/W	Select the input trigger (TSPI/UART ch2 trigger input) 000: T32A ch1 timer register A1 match trigger (T32A01TRGOUTCMPA1) 001: T32A ch1 timer register B1 match trigger (T32A01TRGOUTCMPB1) 010: Reserved 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved
19	-	0	R	Read as "0"
18	UPDN26	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
17	OUTSEL26	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
16	EN26	0	R/W	Trigger output control 0: Disable 1: Enable
15	-	0	R	Read as "0"
14:12	INSEL25[2:0]	000	R/W	Select the input trigger (TSPI/UART ch1 trigger input) 000: T32A ch1 timer register A1 match trigger (T32A01TRGOUTCMPA1) 001: T32A ch1 timer register B1 match trigger (T32A01TRGOUTCMPB1) 010: Reserved 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved

Bit	Bit symbol	After reset	Type	Function
11	-	0	R	Read as "0"
10	UPDN25	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
9	OUTSEL25	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
8	EN25	0	R/W	Trigger output control 0: Disable 1: Enable
7	-	0	R	Read as "0"
6:4	INSEL24[2:0]	000	R/W	Select the input trigger (TSPI/UART ch0 trigger input) 000: T32A ch3 timer register A1 match trigger (T32A03TRGOUTCMPA1) 001: T32A ch3 timer register B1 match trigger (T32A03TRGOUTCMPB1) 010: Reserved 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved
3	-	0	R	Read as "0"
2	UPDN24	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
1	OUTSEL24	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
0	EN24	0	R/W	Trigger output control 0: Disable 1: Enable

2.2.3.8. *[TSELxCR7]* (Control Register 7)

Bit	Bit symbol	After reset	Type	Function
31	-	0	R	Read as "0"
30:28	INSEL31[2:0]	000	R/W	Select the input trigger (INSEL29 input) 000: ADC unit A general purpose trigger interrupt (INTADATRG) 001: ADC unit A single conversion interrupt (INTADASGL) 010: ADC unit A continuous conversion interrupt (INTADACNT) 011: ADC unit A monitor function 0 Interrupt (INTADACP0) 100: ADC unit A monitor function 1 Interrupt (INTADACP1) 101: Reserved 110: Reserved 111: Reserved
27	-	0	R	Read as "0"
26	UPDN31	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
25	OUTSEL31	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
24	EN31	0	R/W	Trigger output control 0: Disable 1: Enable
23	-	0	R	Read as "0"
22:20	INSEL30[2:0]	000	R/W	Select the input trigger (T32A ch0 timer B internal trigger input) 000: T32A ch0 timer register A0 match trigger (T32A00TRGOUTCMPA0) 001: T32A ch0 timer register A1 match trigger (T32A00TRGOUTCMPA1) 010: T32A ch0 timer A overflow trigger (T32A00TRGOUTOFA) 011: T32A ch0 timer A underflow trigger (T32A00TRGOUTUFA) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
19	-	0	R	Read as "0"
18	UPDN30	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
17	OUTSEL30	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
16	EN30	0	R/W	Trigger output control 0: Disable 1: Enable
15	-	0	R	Read as "0"
14:12	INSEL29[2:0]	000	R/W	Select the input trigger (T32A ch0 timer A internal trigger input) 000: T32A ch0 timer register B0 match trigger (T32A00TRGOUTCMPB0) 001: T32A ch0 timer register B1 match trigger (T32A00TRGOUTCMPB1) 010: T32A ch0 timer B overflow trigger (T32A00TRGOUTOFB) 011: T32A ch0 timer B underflow trigger (T32A00TRGOUTUFB) 100: Reserved 101: Reserved 110: Reserved 111: INSEL31 output

Bit	Bit symbol	After reset	Type	Function
11	-	0	R	Read as "0"
10	UPDN29	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
9	OUTSEL29	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
8	EN29	0	R/W	Trigger output control 0: Disable 1: Enable
7	-	0	R	Read as "0"
6:4	INSEL28[2:0]	000	R/W	Select the input trigger (UART ch4 trigger input) 000: T32A ch4 timer register A1 match trigger (T32A04TRGOUTCMPA1) 001: T32A ch4 timer register B1 match trigger (T32A04TRGOUTCMPB1) 010: Reserved 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved
3	-	0	R	Read as "0"
2	UPDN28	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
1	OUTSEL28	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
0	EN28	0	R/W	Trigger output control 0: Disable 1: Enable

2.2.3.9. *[TSELxCR8]* (Control Register 8)

Bit	Bit symbol	After reset	Type	Function
31	-	0	R	Read as "0"
30:28	INSEL35[2:0]	000	R/W	Select the input trigger (T32A ch2 timer B internal trigger input) 000: T32A ch2 timer register A0 match trigger (T32A02TRGOUTCMPA0) 001: T32A ch2 timer register A1 match trigger (T32A02TRGOUTCMPA1) 010: T32A ch2 timer A overflow trigger (T32A02TRGOUTOFA) 011: T32A ch2 timer A underflow trigger (T32A02TRGOUTUFA) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
27	-	0	R	Read as "0"
26	UPDN35	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
25	OUTSEL35	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
24	EN35	0	R/W	Trigger output control 0: Disable 1: Enable
23	-	0	R	Read as "0"
22:20	INSEL34[2:0]	000	R/W	Select the input trigger (T32A ch2 timer A internal trigger input) 000: T32A ch2 timer register B0 match trigger (T32A02TRGOUTCMPB0) 001: T32A ch2 timer register B1 match trigger (T32A02TRGOUTCMPB1) 010: T32A ch2 timer B overflow trigger (T32A02TRGOUTOFB) 011: T32A ch2 timer B underflow trigger (T32A02TRGOUTUFB) 100: Reserved 101: Reserved 110: Reserved 111: INSEL41 output
19	-	0	R	Read as "0"
18	UPDN34	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
17	OUTSEL34	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
16	EN34	0	R/W	Trigger output control 0: Disable 1: Enable
15	-	0	R	Read as "0"
14:12	INSEL33[2:0]	000	R/W	Select the input trigger (T32A ch1 timer B internal trigger input) 000: T32A ch1 timer register A0 match trigger (T32A01TRGOUTCMPA0) 001: T32A ch1 timer register A1 match trigger (T32A01TRGOUTCMPA1) 010: T32A ch1 timer A overflow trigger (T32A01TRGOUTOFA) 011: T32A ch1 timer A underflow trigger (T32A01TRGOUTUFA) 100: Reserved 101: Reserved 110: Reserved 111: Reserved

Bit	Bit symbol	After reset	Type	Function
11	-	0	R	Read as "0"
10	UPDN33	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
9	OUTSEL33	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
8	EN33	0	R/W	Trigger output control 0: Disable 1: Enable
7	-	0	R	Read as "0"
6:4	INSEL32[2:0]	000	R/W	Select the input trigger (T32A ch1 timer A internal trigger input) 000: T32A ch1 timer register B0 match trigger (T32A01TRGOUTCMPB0) 001: T32A ch1 timer register B1 match trigger (T32A01TRGOUTCMPB1) 010: T32A ch1 timer B overflow trigger (T32A01TRGOUTOFB) 011: T32A ch1 timer B underflow trigger (T32A01TRGOUTUFB) 100: Reserved 101: Reserved 110: Reserved 111: INSEL40 output
3	-	0	R	Read as "0"
2	UPDN32	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
1	OUTSEL32	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
0	EN32	0	R/W	Trigger output control 0: Disable 1: Enable

2.2.3.10. *[TSELxCR9]* (Control Register 9)

Bit	Bit symbol	After reset	Type	Function
31	-	0	R	Read as "0"
30:28	INSEL39[2:0]	000	R/W	Select the input trigger (T32A ch4 timer B internal trigger input) 000: T32A ch4 timer register A0 match trigger (T32A04TRGOUTCMPA0) 001: T32A ch4 timer register A1 match trigger (T32A04TRGOUTCMPA1) 010: T32A ch4 timer A overflow trigger (T32A04TRGOUTOFA) 011: T32A ch4 timer A underflow trigger (T32A04TRGOUTUFA) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
27	-	0	R	Read as "0"
26	UPDN39	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
25	OUTSEL39	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
24	EN39	0	R/W	Trigger output control 0: Disable 1: Enable
23	-	0	R	Read as "0"
22:20	INSEL38[2:0]	000	R/W	Select the input trigger (T32A ch4 timer A internal trigger input) 000: T32A ch4 timer register B0 match trigger (T32A04TRGOUTCMPB0) 001: T32A ch4 timer register B1 match trigger (T32A04TRGOUTCMPB1) 010: T32A ch4 timer B overflow trigger (T32A04TRGOUTOFB) 011: T32A ch4 timer B underflow trigger (T32A04TRGOUTUFB) 100: Reserved 101: Reserved 110: Reserved 111: INSEL43 output
19	-	0	R	Read as "0"
18	UPDN38	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
17	OUTSEL38	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
16	EN38	0	R/W	Trigger output control 0: Disable 1: Enable
15	-	0	R	Read as "0"
14:12	INSEL37[2:0]	000	R/W	Select the input trigger (T32A ch3 timer B internal trigger input) 000: T32A ch3 timer register A0 match trigger (T32A03TRGOUTCMPA0) 001: T32A ch3 timer register A1 match trigger (T32A03TRGOUTCMPA1) 010: T32A ch3 timer A overflow trigger (T32A03TRGOUTOFA) 011: T32A ch3 timer A underflow trigger (T32A03TRGOUTUFA) 100: Reserved 101: Reserved 110: Reserved 111: Reserved

Bit	Bit symbol	After reset	Type	Function
11	-	0	R	Read as "0"
10	UPDN37	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
9	OUTSEL37	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
8	EN37	0	R/W	Trigger output control 0: Disable 1: Enable
7	-	0	R	Read as "0"
6:4	INSEL36[2:0]	000	R/W	Select the input trigger (T32A ch3 timer A internal trigger input) 000: T32A ch3 timer register B0 match trigger (T32A03TRGOUTCMPB0) 001: T32A ch3 timer register B1 match trigger (T32A03TRGOUTCMPB1) 010: T32A ch3 timer B overflow trigger (T32A03TRGOUTOFB) 011: T32A ch3 timer B underflow trigger (T32A03TRGOUTUFB) 100: Reserved 101: Reserved 110: Reserved 111: INSEL42 output
3	-	0	R	Read as "0"
2	UPDN36	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
1	OUTSEL36	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
0	EN36	0	R/W	Trigger output control 0: Disable 1: Enable

2.2.3.11. *[TSELxCR10]* (Control Register 10)

Bit	Bit symbol	After reset	Type	Function
31	-	0	R	Read as "0"
30:28	INSEL43[2:0]	000	R/W	Select the input trigger (INSEL38 input) 000: UART ch3 transmission completion trigger (UART3TXTRG) 001: UART ch3 reception completion trigger (UART3RXTRG) 010: TSPI ch3 transmit completion trigger (TSPI3TXEND) 011: TSPI ch3 receive completion trigger (TSPI3RXEND) 100: UART ch4 transmission completion trigger (UART4TXTRG) 101: UART ch4 reception completion trigger (UART4RXTRG) 110: EI2C ch1 status interrupt (INTI2C1ST) 111: A-ENC32 ch1 divided pulse signal (ENC1TIMPLS)
27	-	0	R	Read as "0"
26	UPDN43	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
25	OUTSEL43	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
24	EN43	0	R/W	Trigger output control 0: Disable 1: Enable
23	-	0	R	Read as "0"
22:20	INSEL42[2:0]	000	R/W	Select the input trigger (INSEL36 input) 000: UART ch0 transmission completion trigger (UART0TXTRG) 001: UART ch0 reception completion trigger (UART0RXTRG) 010: TSPI ch0 transmit completion trigger (TSPI0TXEND) 011: TSPI ch0 receive completion trigger (TSPI0RXEND) 100: EI2C ch0 status interrupt (INTI2C0ST) 101: A-ENC32 ch0 divided pulse signal (ENC0TIMPLS) 110: Reserved 111: Reserved
19	-	0	R	Read as "0"
18	UPDN42	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
17	OUTSEL42	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
16	EN42	0	R/W	Trigger output control 0: Disable 1: Enable
15	-	0	R	Read as "0"
14:12	INSEL41[2:0]	000	R/W	Select the input trigger (INSEL34 input) 000: ADC unit B general purpose trigger interrupt (INTADBTRG) 001: ADC unit B single conversion interrupt (INTADBSGL) 010: ADC unit B continuous conversion interrupt (INTADBCNT) 011: ADC unit B monitor function 0 Interrupt (INTADBCP0) 100: ADC unit B monitor function 1 Interrupt (INTADBCP1) 101: Reserved 110: Reserved 111: Reserved

Bit	Bit symbol	After reset	Type	Function
11	-	0	R	Read as "0"
10	UPDN41	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
9	OUTSEL41	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
8	EN41	0	R/W	Trigger output control 0: Disable 1: Enable
7	-	0	R	Read as "0"
6:4	INSEL40[2:0]	000	R/W	Select the input trigger (INSEL32 input) 000: UART ch1 transmission completion trigger (UART1TXTRG) 001: UART ch1 reception completion trigger (UART1RXTRG) 010: TSPI ch1 transmit completion trigger (TSPI1TXEND) 011: TSPI ch1 receive completion trigger (TSPI1RXEND) 100: UART ch2 transmission completion trigger (UART2TXTRG) 101: UART ch2 reception completion trigger (UART2RXTRG) 110: TSPI ch2 transmit completion trigger (TSPI2TXEND) 111: TSPI ch2 receive completion trigger (TSPI2RXEND)
3	-	0	R	Read as "0"
2	UPDN40	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
1	OUTSEL40	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
0	EN40	0	R/W	Trigger output control 0: Disable 1: Enable

2.3. Clock Selective Watchdog Timer (SIWDT)

2.3.1. Built-in Channel

The following table shows the SIWDT built-in channel.

Table 2.3 SIWDT Built-in Channel

Product	SIWDT channel (✓: Available, -: N/A)
	ch0
TMPM471F10FG	✓

2.3.2. Count Clock

The Clock Selective Watchdog Timer can select the clock to count.
The following table shows the selectable clock.

Table 2.4 SIWDT Count Clock

Clock	Signal	Selection
System clock	fsysm	Selected by ***[SIWD0MOD]***<WDCLS>
Internal high-speed oscillator1 clock	f_{IHOSC1}	
Internal high-speed oscillator2 clock	f_{IHOSC2}	

2.3.3. Oscillation Clock Protection Function

If the internal high-speed oscillator 2(f_{IHOSC2}) is selected, rewriting of the internal high-speed oscillator 2 can be forbidden.

Table 2.5 SIWDT Oscillation Clock Protection Function

Output control	Signal name	Remark
Protect signal of Internal high-speed oscillator 2 control bit (***[CGOSCCR]***<IHOSC2EN>)	OSCPRO	Setting by ***[SIWD0OSCCR]***<OSCPRO>

2.4. Oscillation Frequency Detector (OFD)

2.4.1. Built-in List

The following table shows the built-in list.

Table 2.6 OFD Built-in List

Product	Built-in OFD (✓: Available, -: N/A)
TMPM471F10FG	✓

2.4.2. Reference Clock

The oscillation frequency detection circuit operates considering the clock of the following tables as a reference clock.

Table 2.7 OFD Reference Clock

Reference clock	Signal name	Divide value
Internal high-speed oscillator 2	f_{IHOSC2}	128

2.4.3. Clock for Detection

The oscillation frequency detection circuit chooses the clock to monitor from the detection object clock of the following tables.

Table 2.8 OFD Clock for Detection

Clock for detection		Signal name
Input signal	External high-speed oscillator clock	f_{EHOSC}
	Selected clock by the ***[CGOSCCR]***<OSCSEL> and ***[CGPLL0SEL]***<PLL0SEL> in CG(Clock control block)	fc

2.5. Debug Interface

2.5.1. Debug Interface Pin List

Table 2.9 Debug Interface Pin List

Debug function	Debug pin	Port
Serial wire	SWDIO	PB3
	SWCLK	PB4
	SWV	PB5
JTAG	TMS	PB3
	TCK	PB4
	TDO	PB5
	TDI	PB6
	TRST_N	PB7
ETM trace	TRACECLK	PB0
	TRACEDATA0	PB1
	TRACEDATA1	PB2
	TRACEDATA2	PK1
	TRACEDATA3	PK0

2.5.2. Trace Clock Division Ratio

Table 2.10 Trace Clock Division Ratio

Source clock	division ratio	Output
fsysh	1/4	TRACECLK

2.6. Flash Memory

TMPM471F10FG has only code flash memory.

2.6.1. Clock for Programming/Erasing

As for flash memory, the clock of the following tables is used for programming/erasing of the code flash memory.

Table 2.11 Clock for Programming/Erasing

Clock for programming/erasing
f_{IHOSC1}

Note: The oscillation control register is ***[CGOSCCR]***<IHOSC1EN>.

2.6.2. Code Flash Memory Block Configuration

The code flash memory has a block configuration as shown in the table below.

Table 2.12 Code Flash Memory

Area	Block name		Block size (KB)
0	Block0	PG0	4
		PG1	4
		PG2	4
		PG3	4
		PG4	4
		PG5	4
		PG6	4
		PG7	4
	Block1		32
	Block2		32
	Block3		32
	Block4		32
	Block5		32
	Block6		32
	Block7		32
	Block8		32
	Block9		32
	Block10		32
	Block11		32
	Block12		32
	Block13		32
	Block14		32
	Block15		32

Area	Block name	Block size (KB)
1	Block16	32
	Block17	32
	Block18	32
	Block19	32
	Block20	32
	Block21	32
	Block22	32
	Block23	32
	Block24	32
	Block25	32
	Block26	32
	Block27	32
	Block28	32
	Block29	32
	Block30	32
	Block31	32

2.6.3. Access Control Register Setting

The settings of access control register ***[FCACCR]*** <FCLC[2:0]> are as follows:

Table 2.13 Access Control Register *[FCACCR]*<FCLC[2:0]> Setting

Bit	Bit symbol	After reset	Function
2:0	<FCLC[2:0]>	100	Code flash read clock control 101: fsysh > 120MHz 100: 120MHz ≥ fsysh > 80MHz 011: 80MHz ≥ fsysh

2.6.4. Macro Code at ID-Read

The macro code values for this product are as follows:

Table 2.14 Macro Code at ID-Read

Code	ID[15:0]
Macro code (Code Flash)	0x0402

2.6.5. Single Boot Resource

The peripheral function of the following table is used in single boot.

Table 2.15 Single Boot Resource

Peripheral function	Channel	Function	Pin name
BOOT	-	-	PF0 (BOOT_N)
UART	ch0	RXD	PE0/PE1 (UT0RXD)
		TXD	PE1/PE0 (UT0TXDA)
T32A	ch0	-	-

The range of the RAM address transmitted by the RAM loader command should use the following table.

Table 2.16 Address in which RAM Transmission is Possible

Address in which RAM transmission is possible
0x20000400 to 0x2000DFFF

2.7. Direct Memory Access Controller (DMAC)

2.7.1. Built-in Unit

The following table shows the built-in unit.

Table 2.17 DMAC Built-in Unit

Product name	Unit (✓: Available, -: N/A)
	A
TMPM471F10FG	✓

2.7.2. DMA Transfer Request list

The following tables show the DMA transfer request list.

As for the channel which has a register name in the trigger selector column of a table, choose the request by a trigger selector.

"-" in the table does not have an applicable function.

Table 2.18 DMA Transfer Request List (1/3)

ch	Single transfer request			Burst transfer request		
	Trigger selector		Signal name	Trigger selector		Signal name
0	*[TSEL0CR0]* <INSEL0>	TSPI ch0 receive DMA request	TSPI0RX_DMA	*[TSEL0CR0]* <INSEL0>	TSPI ch0 receive DMA request	TSPI0RX_DMA
		UART ch0 reception DMA request	UART0RX_DMAREQ		UART ch0 reception DMA request	UART0RX_DMAREQ
1	*[TSEL0CR0]* <INSEL1>	TSPI ch0 transmit DMA request	TSPI0TX_DMA	*[TSEL0CR0]* <INSEL1>	TSPI ch0 transmit DMA request	TSPI0TX_DMA
		UART ch0 transmission DMA request	UART0TX_DMAREQ		UART ch0 transmission DMA request	UART0TX_DMAREQ
2	*[TSEL0CR0]* <INSEL2>	TSPI ch1 receive DMA request	TSPI1RX_DMA	*[TSEL0CR0]* <INSEL2>	TSPI ch1 receive DMA request	TSPI1RX_DMA
		UART ch1 reception DMA request	UART1RX_DMAREQ		UART ch1 reception DMA request	UART1RX_DMAREQ
3	*[TSEL0CR0]* <INSEL3>	TSPI ch1 transmit DMA request	TSPI1TX_DMA	*[TSEL0CR0]* <INSEL3>	TSPI ch1 transmit DMA request	TSPI1TX_DMA
		UART ch1 transmission DMA request	UART1TX_DMAREQ		UART ch1 transmission DMA request	UART1TX_DMAREQ
4	*[TSEL0CR1]* <INSEL4>	TSPI ch2 receive DMA request	TSPI2RX_DMA	*[TSEL0CR1]* <INSEL4>	TSPI ch2 receive DMA request	TSPI2RX_DMA
		UART ch2 reception DMA request	UART2RX_DMAREQ		UART ch2 reception DMA request	UART2RX_DMAREQ
5	*[TSEL0CR1]* <INSEL5>	TSPI ch2 transmit DMA request	TSPI2TX_DMA	*[TSEL0CR1]* <INSEL5>	TSPI ch2 transmit DMA request	TSPI2TX_DMA
		UART ch2 transmission DMA request	UART2TX_DMAREQ		UART ch2 transmission DMA request	UART2TX_DMAREQ
6	*[TSEL0CR1]* <INSEL6>	TSPI ch3 receive DMA request	TSPI3RX_DMA	*[TSEL0CR1]* <INSEL6>	TSPI ch3 receive DMA request	TSPI3RX_DMA
		UART ch3 reception DMA request	UART3RX_DMAREQ		UART ch3 reception DMA request	UART3RX_DMAREQ
7	*[TSEL0CR1]* <INSEL07>	TSPI ch3 transmit DMA request	TSPI3TX_DMA	*[TSEL0CR1]* <INSEL07>	TSPI ch3 transmit DMA request	TSPI3TX_DMA
		UART ch3 transmission DMA request	UART3TX_DMAREQ		UART ch3 transmission DMA request	UART3TX_DMAREQ
8	-	UART ch4 reception DMA request	UART4RX_DMAREQ	-	UART ch4 reception DMA request	UART4RX_DMAREQ
9	-	UART ch4 transmission DMA request	UART4TX_DMAREQ	-	UART ch4 transmission DMA request	UART4TX_DMAREQ
10	-	-	-	-	EI2C ch0 receiving DMA request	I2C0ARXDMAREQ
11	-	-	-	-	EI2C ch0 transmitting DMA request	I2C0ATXDMAREQ
12	-	-	-	-	EI2C ch1 receiving DMA request	I2C1ARXDMAREQ
13	-	-	-	-	EI2C ch1 transmitting DMA request	I2C1ATXDMAREQ
14	-	-	-	-	A-PMD ch0 PWM interrupt	INTPWM0
15	-	-	-	-	A-PMD ch1 PWM interrupt	INTPWM1

Note: Each of ch0 to 7 is set by the trigger source of DMA request. For the detail of connection, refer to the "2.2.Trigger Selector (TRGSEL)".

Table 2.19 DMA Transfer Request List (2/3)

ch	Single transfer request			Burst transfer request		
	Trigger selector		Signal name	Trigger selector		Signal name
16	-	-	-	*[TSEL0CR2]* <INSEL8>	AD unit A general purpose trigger DMA request	ADATRG_DMAREQ
					AD unit A single conversion DMA request	ADASLG_DMAREQ
					AD unit A continue conversion DMA request	ADACNT_DMAREQ
17	-	-	-	*[TSEL0CR2]* <INSEL9>	AD unit B general purpose trigger DMA request	ADBTRG_DMAREQ
					AD unit B single conversion DMA request	ADBSLG_DMAREQ
					AD unit B continue conversion DMA request	ADBCNT_DMAREQ
18	-	-	-	-	-	-
19	-	-	-	*[TSEL0CR2]* <INSEL10>	T32A ch0 DMA request at match A1 register	T32A00DMAREQCMPA1
					T32A ch0 DMA request at match C1 register	T32A00DMAREQCMPC1
					T32A ch1 DMA request at match A1 register	T32A01DMAREQCMPA1
					T32A ch1 DMA request at match C1 register	T32A01DMAREQCMPC1
20	-	-	-	*[TSEL0CR2]* <INSEL11>	T32A ch2 DMA request at match A1 register	T32A02DMAREQCMPA1
					T32A ch2 DMA request at match C1 register	T32A02DMAREQCMPC1
					T32A ch3 DMA request at match A1 register	T32A03DMAREQCMPA1
					T32A ch3 DMA request at match C1 register	T32A03DMAREQCMPC1
					T32A ch4 DMA request at match A1 register	T32A04DMAREQCMPA1
					T32A ch4 DMA request at match C1 register	T32A04DMAREQCMPC1
21	-	-	-	-	-	-
22	-	-	-	*[TSEL0CR3*] <INSEL12>	T32A ch0 DMA request at match B1 register	T32A00DMAREQCMPB1
					T32A ch1 DMA request at match B1 register	T32A01DMAREQCMPB1
					T32A ch2 DMA request at match B1 register	T32A02DMAREQCMPB1
					T32A ch3 DMA request at match B1 register	T32A03DMAREQCMPB1
					T32A ch4 DMA request at match B1 register	T32A04DMAREQCMPB1
23	-	-	-	*[TSEL0CR3]* <INSEL13>	T32A ch0 DMA request at capture A0 register	T32A00DMAREQCAPA0
					T32A ch0 DMA request at capture A1 register	T32A00DMAREQCAPA1
					T32A ch1 DMA request at capture A0 register	T32A01DMAREQCAPA0
					T32A ch1 DMA request at capture A1 register	T32A01DMAREQCAPA1
					T32A ch0 DMA request at capture C0 register	T32A00DMAREQCAPC0
					T32A ch0 DMA request at capture C1 register	T32A00DMAREQCAPC1
					T32A ch1 DMA request at capture C0 register	T32A01DMAREQCAPC0
					T32A ch1 DMA request at capture C1 register	T32A01DMAREQCAPC1
24	-	-	-	*[TSEL0CR3]* <INSEL14>	T32A ch2 DMA request at capture A0 register	T32A02DMAREQCAPA0
					T32A ch2 DMA request at capture A1 register	T32A02DMAREQCAPA1
					T32A ch3 DMA request at capture A0 register	T32A03DMAREQCAPA0
					T32A ch3 DMA request at capture A1 register	T32A03DMAREQCAPA1
					T32A ch2 DMA request at capture C0 register	T32A02DMAREQCAPC0
					T32A ch2 DMA request at capture C1 register	T32A02DMAREQCAPC1
					T32A ch3 DMA request at capture C0 register	T32A03DMAREQCAPC0
					T32A ch3 DMA request at capture C1 register	T32A03DMAREQCAPC1

Note: Each of ch16 to 24 is set by the trigger source of DMA request. For the detail of connection, refer to the "2.2.Trigger Selector (TRGSEL)".

Table 2.20 DMA Transfer Request List (3/3)

ch	Single transfer request			Burst transfer request		
	Trigger selector		Signal name	Trigger selector		Signal name
25	-	-	-	***[TSEL0CR3]*** <INSEL15>	T32A ch4 DMA request at capture A0 register	T32A04DMAREQCAPA0
					T32A ch4 DMA request at capture A1 register	T32A04DMAREQCAPA1
					T32A ch4 DMA request at capture C0 register	T32A04DMAREQCAPC0
					T32A ch4 DMA request at capture C1 register	T32A04DMAREQCAPC1
26	-	-	-	***[TSEL0CR4]*** <INSEL16>	T32A ch0 DMA request at capture B0 register	T32A00DMAREQCAPB0
					T32A ch0 DMA request at capture B1 register	T32A00DMAREQCAPB1
					T32A ch1 DMA request at capture B0 register	T32A01DMAREQCAPB0
					T32A ch1 DMA request at capture B1 register	T32A01DMAREQCAPB1
					T32A ch2 DMA request at capture B0 register	T32A02DMAREQCAPB0
					T32A ch2 DMA request at capture B1 register	T32A02DMAREQCAPB1
27	-	-	-	***[TSEL0CR4]*** <INSEL17>	T32A ch3 DMA request at capture B0 register	T32A03DMAREQCAPB0
					T32A ch3 DMA request at capture B1 register	T32A03DMAREQCAPB1
					T32A ch4 DMA request at capture B0 register	T32A04DMAREQCAPB0
					T32A ch4 DMA request at capture B1 register	T32A04DMAREQCAPB1
28	-	-	-	***[TSEL0CR4]*** <INSEL18>	DMAC ch0 transfer completion interrupt	INTDMAATC0
					DMAC ch1 transfer completion interrupt	INTDMAATC1
					DMAC ch8 transfer completion interrupt	INTDMAATC8
					DMAC ch9 transfer completion interrupt	INTDMAATC9
					DMAC ch16 transfer completion interrupt	INTDMAATC16
					DMAC ch17 transfer completion interrupt	INTDMAATC17
					DMAC ch26 transfer completion interrupt	INTDMAATC26
					DMAC ch27 transfer completion interrupt	INTDMAATC27
29	-	-	-	***[TSEL0CR4]*** <INSEL19>	DMAC ch2 transfer completion interrupt	INTDMAATC2
					DMAC ch3 transfer completion interrupt	INTDMAATC3
					DMAC ch10 transfer completion interrupt	INTDMAATC10
					DMAC ch11 transfer completion interrupt	INTDMAATC11
					DMAC ch19 transfer completion interrupt	INTDMAATC19
					DMAC ch20 transfer completion interrupt	INTDMAATC20
30	-	-	-	***[TSEL0CR5]*** <INSEL20	DMAC ch4 transfer completion interrupt	INTDMAATC4
					DMAC ch5 transfer completion interrupt	INTDMAATC5
					DMAC ch12 transfer completion interrupt	INTDMAATC12
					DMAC ch13 transfer completion interrupt	INTDMAATC13
					DMAC ch22 transfer completion interrupt	INTDMAATC22
					DMAC ch23 transfer completion interrupt	INTDMAATC23
31	-	-	-	***[TSEL0CR5]*** <INSEL21>	DMAC ch6 transfer completion interrupt	INTDMAATC6
					DMAC ch7 transfer completion interrupt	INTDMAATC7
					DMAC ch14 transfer completion interrupt	INTDMAATC14
					DMAC ch15 transfer completion interrupt	INTDMAATC15
					DMAC ch24 transfer completion interrupt	INTDMAATC24
					DMAC ch25 transfer completion interrupt	INTDMAATC25

Note: Each of ch25 to 31 is set by the trigger source of DMA request. For the detail of connection, refer to the "2.2.Trigger Selector (TRGSEL)".

2.8. Advanced Programmable Motor Control Circuit (A-PMD)

2.8.1. Built-in Channel

The following table shows the A-PMD built-in channel.

Table 2.21 A-PMD Built-in Channel

Product	A-PMD channel (✓: Available, -: N/A)	
	ch0	ch1
TMPM471F10FG	✓	✓

2.8.2. System Clock

The A-PMD operates with the clock in the following table as the system clock.

Table 2.22 A-PMD System Clock

Clock	Signal name
System clock	fsysh

2.8.3. Function Pin and Port

The function pins are assigned to the port of the following table.

Table 2.23 A-PMD Function Pin

Channel	Function pin		Port
ch0	UO0	Output	PC0
	VO0	Output	PC2
	WO0	Output	PC4
	XO0	Output	PC1
	YO0	Output	PC3
	ZO0	Output	PC5
	EMG0	Input	PC6
	OVV0	Input	PC7
ch1	UO1	Output	PG0
	VO1	Output	PG2
	WO1	Output	PG4
	XO1	Output	PG1
	YO1	Output	PG3
	ZO1	Output	PG5
	EMG1	Input	PG6
	OVV1	Input	PG7

2.8.4. DMA Request

The following table shows the DMA request in the A-PMD.

Table 2.24 A-PMD DMA Request

Channel	Request	Signal name	Trigger selector	DMA request channel		
					Single transfer	Burst transfer
ch0	PWM interrupt	INTPWM0	-	14	-	✓
ch1	PWM interrupt	INTPWM1	-	15	-	✓

Note: ✓: Available, -: N/A

2.8.5. Internal Signal Connection Specification

2.8.5.1. Other Connection

In the A-PMD, there is a signal connected with the peripheral function inside in addition to this as shown in the following table.

Table 2.25 A-PMD inside Connection List: Input

Channel	Function input		Input source	
		Signal name		Signal name
ch0	ADC conversion signal	ADABUSY	ADC unit A	ADABUSY
	ADC monitor function 0 (OVV detection)	ADACMP0L_N		ADACP0L_N
	ADC monitor function 1 (OVV detection)	ADACMP1L_N		ADACP1L_N
	ADC conversion completion interrupt A	INTADAPDA		INTADAPDA
	ADC conversion completion interrupt B	INTADAPDB		INTADAPDB
	ADC conversion completion interrupt C	INTADxPDC	-	-
	ADC conversion completion interrupt D	INTADxPDD		
	ADC conversion priority interrupt	INTADxPFLG		
	Commutation trigger (A-ENC position detect synchronous)	INTENC00	A-ENC32 ch0	INTENC00
	Commutation trigger (General purpose timer synchronous)	PMD0TMR	T32A ch0 timer A	T32A00TRGOUTCMPA0
	Commutation trigger (A-ENC MCMP completion synchronous)	ENC0CTRGO	A-ENC32 ch0	ENC0CTRGO
	VE U-phase PWM duty	VExCMPU	-	-
	VE V-phase PWM duty	VExCMPV		
	VE W-phase PWM duty	VExCMPW		
	VE Trigger comparison 0	VExTRGCMP0		
	VE Trigger comparison 1	VExTRGCMP1		
	VE Trigger output selection	VExTRGSEL		
	VE Conduction control/Output control	VExOUTCR		
	VE EMG release	VExEMGRS		
	VE Task transition signal	VExTASKP		
	VE interrupt	INTVCNx		
ch1	ADC conversion signal	ADBBUSY	ADC unit B	ADBBUSY
	ADC monitor function 0 (OVV detection)	ADBCMP0L_N		ADBCP0L_N
	ADC monitor function1 (OVV detection)	ADBCMP1L_N		ADBCP1L_N
	ADC conversion completion interrupt A	INTADBPDA		INTADBPDA
	ADC conversion completion interrupt B	INTADBPDB		INTADBPDB
	ADC conversion completion interrupt C	INTADxPDC	-	-
	ADC conversion completion interrupt D	INTADxPDD		
	ADC conversion priority interrupt	INTADxPFLG		
	Commutation trigger (A-ENC position detect synchronous)	INTENC10	A-ENC32 ch1	INTENC10
	Commutation trigger (General purpose timer synchronous)	PMD1TMR	T32A ch1 timer A	T32A01TRGOUTCMPA0
	Commutation trigger (A-ENC MCMP completion synchronous)	ENC1CTRGO	A-ENC32 ch1	ENC1CTRGO
	VE U-phase PWM duty	VExCMPU	-	-
	VE V-phase PWM duty	VExCMPV		
	VE W-phase PWM duty	VExCMPW		
	VE Trigger comparison 0	VExTRGCMP0		
	VE Trigger comparison 1	VExTRGCMP1		
	VE Trigger output selection	VExTRGSEL		
	VE Conduction control/Output control	VExOUTCR		
	VE EMG release	VExEMGRS		
	VE Task transition signal	VExTASKP		
	VE interrupt	INTVCNx		

Table 2.26 A-PMD inside Connection List: Output

Channel	Function output		Output destination	
		Signal name		Signal name
ch0	ADC synchronous trigger output 0	PMD0TRG0	ADC unit A	PMDTRG0
			ADC unit B	PMDTRG0
	ADC synchronous trigger output 1	PMD0TRG1	ADC unit A	PMDTRG1
			ADC unit B	PMDTRG1
	ADC synchronous trigger output 2	PMD0TRG2	ADC unit A	PMDTRG2
			ADC unit B	PMDTRG2
	ADC synchronous trigger output 3	PMD0TRG3	ADC unit A	PMDTRG3
			ADC unit B	PMDTRG3
	ADC synchronous trigger output 4	PMD0TRG4	ADC unit A	PMDTRG4
			ADC unit B	PMDTRG4
	ADC synchronous trigger output 5	PMD0TRG5	ADC unit A	PMDTRG5
			ADC unit B	PMDTRG5
	PWM signal for the encoder input	PMD0PWMON	A-ENC32 ch0	ENC0PWMON
	PWM interrupt	INTPWM0	-	-
ch1	ADC synchronous trigger output 0	PMD1TRG0	ADC unit A	PMDTRG6
			ADC unit B	PMDTRG6
	ADC synchronous trigger output 1	PMD1TRG1	ADC unit A	PMDTRG7
			ADC unit B	PMDTRG7
	ADC synchronous trigger output 2	PMD1TRG2	ADC unit A	PMDTRG8
			ADC unit B	PMDTRG8
	ADC synchronous trigger output 3	PMD1TRG3	ADC unit A	PMDTRG9
			ADC unit B	PMDTRG9
	ADC synchronous trigger output 4	PMD1TRG4	ADC unit A	PMDTRG10
			ADC unit B	PMDTRG10
	ADC synchronous trigger output 5	PMD1TRG5	ADC unit A	PMDTRG11
			ADC unit B	PMDTRG11
	PWM signal for the encoder input	PMD1PWMON	A-ENC32 ch1	ENC1PWMON
	PWM interrupt	INTPWM1	-	-

2.8.5.2. Inter-Channel Synchronous Control Connection

The PMD is synchronously connected between the channels as shown in the table below.

Table 2.27 PMD Inter-Channel Synchronous Control Connection

Master			Slave		
Channel	**Function (output)**	**Signal name**	**Channel**	**Function (input)**	**Signal name**
ch0	Synchronization output for PWM enable	PMD0SYNCMDENO	ch1	Synchronization input for PWM enable	PMD1SYNCMDENI
	Synchronization output for EMG protection	PMD0SYNCEMGO	ch1	Synchronization input for EMG protection	PMD1SYNCEMGI
	Synchronization output for OVV protection	PMD0SYNCOVVO	ch1	Synchronization input for OVV protection	PMD1SYNCOVVI

2.9. Advanced Encoder Input Circuit (32-bit) (A-ENC32)

2.9.1. Built-in Channel

The following table shows the A-ENC built-in channel.

Table 2.28 A-ENC32 Built-in Channel

Product	A-ENC32 channel (✓: Available, -: N/A)	
	ch0	ch1
TMPM471F10FG	✓	✓

2.9.2. Function Pin and Port

The function pins are assigned to the port of the following table.

Table 2.29 A-ENC32 Function Pin

Channel	Function		Port
ch0	ENC0A	Input	PD0
	ENC0B	Input	PD1
	ENC0Z	Input	PD2
ch1	ENC1A	Input	PF2
	ENC1B	Input	PF3
	ENC1Z	Input	PF4

2.9.3. Internal Signal Connection Specification

2.9.3.1. T32A/A-PMD Connection

In the A-ENC32, there is a signal connected with the peripheral function inside in addition to this as shown in the following table.

"-" in the table does not have an applicable function.

Table 2.30 A-ENC32 Internal Connection Specification: Input

Channel	Function input		Input signal		
		Signal name	Peripheral function		Signal name
ch0	General purpose timer output signal	ENC0PSGI	T32A ch0	T32A timer A output	T32A00OUTA
	PWM signal for sampling	ENC0PWMON	A-PMD ch0	A-PMD PWM signal	PMD0PWMON
ch1	General purpose timer output signal	ENC1PSGI	T32A ch1	T32A timer A output	T32A01OUTA
	PWM signal for sampling	ENC1PWMON	A-PMD ch1	A-PMD PWM signal	PMD1PWMON

Table 2.31 A-ENC32 Internal Connection Specification: Output

Channel	Function output		Trigger selector	Output destination		
		Signal name		Peripheral function		Signal name
ch0	Divided pulse	ENC0TIMPLS	***[TSEL0CR10]*** <INSEL42>	TRGSEL	INSEL36 input	-
	Commutation trigger output for PMD	ENC0CTRGO	-	A-PMD ch0	PMD commutation trigger (Electrical angle synchronous)	ENC0CTRGO
	Encoder input interrupt 0	INTENC00	-		PMD commutation trigger (ENC position detection synchronous)	INTENC00
ch1	Divided pulse	ENC1TIMPLS	***[TSEL0CR10]*** <INSEL43>	TRGSEL	INSEL38 input	-
	Commutation trigger output for PMD	ENC1CTRGO	-	A-PMD ch1	PMD commutation trigger (Electrical angle synchronous)	ENC1CTRGO
	Encoder input interrupt 0	INTENC10	-		PMD commutation trigger (ENC position detection synchronous)	INTENC10

2.10. 12-bit Analog to Digital Converter (ADC)

2.10.1. Built-in Unit

The following table shows the ADC built-in unit.

Table 2.32 ADC Built-in Unit

Product	Unit (✓: Available, -: N/A)	
	A	B
TMPM471F10FG	✓	✓

2.10.2. Corresponding Registers

The following table shows the correspondence registers for each unit of TMPM471F10FG.

Table 2.33 ADC Corresponding Registers for each Unit

Unit	General purpose start-up factor program register	Conversion result storage register
A	*[ADATSET0] to [ADATSET15]*	*[ADAREG0] to [ADAREG15]*
B	*[ADBTSET0] to [ADBTSET15]*	*[ADBREG0] to [ADBREG15]*

2.10.3. Function Pin and Port

The function pins are assigned to the port of the following table.

Table 2.34 ADC Function Pin and Port

Unit	Signal input	Function pin	Port
A	AINA12	AINA12	PH0
	AINA13	AINA13	PH1
	AINA14	AINA14	PH2
	AINA15	AINA15	PH3
	AINA16	AINA16	PH4
	AINA17	AINA17	PH5
	AINA18	AINA18	PH6
	AINA19	AINA19	PH7
	AINA20	AINA20	PP0
	AINA21	AINA21	PP1
	AINA22	AINA22	PP2
	AINA23	AINA23	PP3
	AINA24 (Note1)	VREFH	-
	AINA25 (Note1)	VREFL	-
	AINA26 (Note1)	Reference power (Note2)	-
B	AINB12	AINB12	PP1
	AINB13	AINB13	PP2
	AINB14	AINB14	PP3
	AINB15	AINB15	PJ0
	AINB16	AINB16	PJ1
	AINB17	AINB17	PJ2
	AINB18	AINB18	PJ3
	AINB19	AINB19	PJ4
	AINB20	AINB20	PJ5
	AINB21	AINB21	PJ6
	AINB22	AINB22	PJ7
	AINB23 (Note1)	VREFH	-
	AINB24 (Note1)	VREFL	-
	AINB25 (Note1)	Reference power (Note2)	-

Note1: AINA24/AINA25/AINA26 of unit A and AINB23/AINB24/AINB25 of unit B are connected to internal signal of MCU for self-check function.

Note2: For the reference power supply, refer to the electrical characteristics of "TMPM471F10FG Datasheet".

2.10.4. Analog Reference Pins

The analog reference pin of ADC is common to units A/B. The following table shows the pin assignment of the analog reference pin of each ADC unit.

Table 2.35 Analog Reference Pin Assignment

Unit	Analog reference pin	TMPM471F10FG
A	VREFHA/VREFLA	87/86
B	VREFHB/VREFLB	

2.10.5. Conversion Clock for ADC

The ADC uses the clock of the following table as a conversion clock.

Table 2.36 Conversion Clock for ADC

Clock
ADCLK

2.10.6. Setting Value of Mode Setting Register 2

For the setting value of mode setting register 2 (***[ADxMOD2]***), set the values in the table below.

Table 2.37 Setting Value of ADC Mode Setting Register 2

Register name	Value
[ADxMOD2]<MOD2[31:0]>	0x00000000

2.10.7. Trimming Setting Register Setting Value

For the trimming setting register (***[ADxTRM]***), set the values in the table below.

Table 2.38 Setting Value of Trimming Setting Register

Register name	Value
[ADxTRM]<TRM[31:0]>	0x00000000

2.10.8. DMA Request

The following table shows the DMA request in the ADC.

Table 2.39 ADC DMA Request

Unit	Request	Signal name	Trigger selector	DMA request channel		
					Single transfer	Burst transfer
A	General purpose trigger DMA request	ADATRG_DMAREQ	***[TSEL0CR2]*** <INSEL8>	16	-	✓
	Single conversion DMA request	ADASGL_DMAREQ			-	✓
	Continuous conversion DMA request	ADACNT_DMAREQ			-	✓
B	General purpose trigger DMA request	ADBTRG_DMAREQ	***[TSEL0CR2]*** <INSEL9>	17	-	✓
	Single conversion DMA request	ADBSGL_DMAREQ			-	✓
	Continuous conversion DMA request	ADBCNT_DMAREQ			-	✓

Note: ✓: Available, -: N/A

2.10.9. Internal Signal Connection Specification

2.10.9.1. Startup Trigger

The 12-bit ADC has an AD conversion function with the Trigger signal.

As for the input trigger signal which has the register in the trigger selector column of the following table, choose the input trigger by the register.

"-" in the table does not have an applicable function.

Table 2.40 ADC Startup Trigger: Input

Unit	Function input		Trigger selector	Input source	
		Signal name			Signal name
A	PMD0 PMD trigger 0	PMDTRG0	-	A-PMD ch0	PMD0TRG0
	PMD0 PMD trigger 1	PMDTRG1	-		PMD0TRG1
	PMD0 PMD trigger 2	PMDTRG2	-		PMD0TRG2
	PMD0 PMD trigger 3	PMDTRG3	-		PMD0TRG3
	PMD0 PMD trigger 4	PMDTRG4	-		PMD0TRG4
	PMD0 PMD trigger 5	PMDTRG5	-		PMD0TRG5
	PMD1 PMD trigger 0	PMDTRG6		A-PMD ch1	PMD1TRG0
	PMD1 PMD trigger 1	PMDTRG7	-		PMD1TRG1
	PMD1 PMD trigger 2	PMDTRG8	-		PMD1TRG2
	PMD1 PMD trigger 3	PMDTRG9	-		PMD1TRG3
	PMD1 PMD trigger 4	PMDTRG10	-		PMD1TRG4
	PMD1 PMD trigger 5	PMDTRG11	-		PMD1TRG5
	General purpose trigger	ADATRGIN	***[TSEL0CR5]*** <INSEL22>	T32A ch0	T32A00TRGOUTCMPA1
					T32A00TRGOUTCMPB1
B	PMD0 PMD trigger 0	PMDTRG0	-	A-PMD ch0	PMD0TRG0
	PMD0 PMD trigger 1	PMDTRG1	-		PMD0TRG1
	PMD0 PMD trigger 2	PMDTRG2	-		PMD0TRG2
	PMD0 PMD trigger 3	PMDTRG3	-		PMD0TRG3
	PMD0 PMD trigger 4	PMDTRG4	-		PMD0TRG4
	PMD0 PMD trigger 5	PMDTRG5	-		PMD0TRG5
	PMD1 PMD trigger 0	PMDTRG6		A-PMD ch1	PMD1TRG0
	PMD1 PMD trigger 1	PMDTRG7	-		PMD1TRG1
	PMD1 PMD trigger 2	PMDTRG8	-		PMD1TRG2
	PMD1 PMD trigger 3	PMDTRG9	-		PMD1TRG3
	PMD1 PMD trigger 4	PMDTRG10	-		PMD1TRG4
	PMD1 PMD trigger 5	PMDTRG11	-		PMD1TRG5
	General purpose trigger	ADBTRGIN	***[TSEL0CR5]*** <INSEL23>	T32A ch2	T32A02TRGOUTCMPA1
					T32A02TRGOUTCMPB1

Note: The trigger source for the start trigger is selected by the trigger selector: ***[TSEL0CR5]***<INSEL22><INSEL23>. For the detail of connection, refer to the "2.2.Trigger Selector (TRGSEL)".

2.10.9.2. Other Connection

In the ADC, there is a signal connected with the peripheral function inside in addition to this as shown in the following table.

"-" in the table does not have an applicable function.

Table 2.41 ADC inside Connection: Output

Unit	Function output		Trigger selector	Output destination	
		Signal name			Signal name
A	General purpose trigger interrupt	INTADATRG	***[TSEL0CR7]*** <INSEL31>	TRGSEL INSEL29 input	-
	Single conversion interrupt	INTADASGL			
	Continuous conversion interrupt	INTADACNT			
	Monitor function 0 interrupt	INTADACP0			
	Monitor function 1 interrupt	INTADACP1			
	Monitor function 0 output for PMD protect function	ADACP0L_N	-	A-PMD ch0	ADACMP0L_N
	Monitor function 1 output for PMD protect function	ADACP1L_N	-		ADACMP1L_N
	PMD trigger interrupt A	INTADAPDA	-		INTADAPDA
	PMD trigger interrupt B	INTADAPDB	-		INTADAPDB
	AD conversion flag	ADABUSY	-		ADABUSY
B	General purpose trigger interrupt	INTADBTRG	***[TSEL0CR10]*** <INSEL41>	TRGSEL INSEL34 input	-
	Single conversion interrupt	INTADBSGL			
	Continuous conversion interrupt	INTADBCNT			
	Monitor function 0 interrupt	INTADBCP0			
	Monitor function 1 interrupt	INTADBCP1			
	Monitor function 0 output for PMD protect function	ADBCP0L_N	-	A-PMD ch1	ADBCMP0L_N
	Monitor function 1 output for PMD protect function	ADBCP1L_N	-		ADBCMP1L_N
	PMD trigger interrupt A	INTADBPDA	-		INTADBPDA
	PMD trigger interrupt B	INTADBPDB	-		INTADBPDB
	AD conversion flag	ADBBUSY	-		ADBBUSY

2.11. 32-bit Timer Event Counter (T32A)

2.11.1. Built-in Channel

The following table shows the T32A built-in channel.

Table 2.42 T32A Built-in Channel

Product	Channel (✓: Available, -: N/A)				
	ch0	ch1	ch2	ch3	ch4
TMPM471F10FG	✓	✓	✓	✓	✓

2.11.2. Function Pin and Port

The function pins are assigned to the port of the following table.
Please do not use simultaneously the same function currently assigned to two or more pins.

Table 2.43 T32A Function Pin and Port (1/2)

Channel	Function pin		Port
ch0	T32A00INA0	Input	PA0
	T32A00OUTA	Output	PA1
	T32A00INB0	Input	PN2
	T32A00OUTB	Output	PN1
	T32A00INC0	Input	PA0
	T32A00OUTC	Output	PA1
ch1	T32A01INA0	Input	PA6
	T32A01OUTA	Output	PA5
	T32A01INB0	Input	PA2
	T32A01OUTB	Output	PA3
	T32A01INC0	Input	PA6
	T32A01OUTC	Output	PA5
ch2	T32A02INA0	Input	PA7
	T32A02OUTA	Output	PE3
	T32A02INB0	Input	PE1
	T32A02OUTB	Output	PE0
	T32A02INC0	Input	PA7
	T32A02OUTC	Output	PE3

Table 2.44 T32A Function Pin and Port (2/2)

Channel	Function pin		Port
ch3	T32A03INA0	Input	PE4
	T32A03OUTA	Output	PE5
	T32A03INB0	Input	PE6
	T32A03OUTB	Output	PE7
	T32A03INC0	Input	PE4
	T32A03OUTC	Output	PE5
Ch4	T32A04INA0	Input	PD0
	T32A04OUTA	Output	PD1
	T32A04INB0	Input	PF0
	T32A04OUTB	Output	PF1
	T32A04INC0	Input	PD0
	T32A04OUTC	Output	PD1

2.11.3. Clock for Prescaler

The T32A uses the clock of the following table as a prescaler clock.

Table 2.45 T32A clock for Prescaler

Clock
ΦT0m

2.11.4. Internal Signal Connection Specification

2.11.4.1. Capture Trigger Signal Connection

In the T32A, capture trigger signals are connected to signals of the following table.

As for the input trigger signal which has the register in the trigger selector column of the following tables, choose the input trigger by the register.

Table 2.46 Capture Trigger Connection (1/2)

Channel			Trigger source		
	Timer	Input signal name of capture trigger	Trigger selector	Input trigger signal	Signal name
ch0	Timer A	T32A00TRGINAPHCK (Other timer output)	-	T32A ch0 timer B output	T32A00OUTB
		T32A00TRGINAPCK (internal trigger input)	***[TSEL0CR7]*** <INSEL29>	T32A ch0 timer register B0 match trigger	T32A00TRGOUTCMPB0
				T32A ch0 timer register B1 match trigger	T32A00TRGOUTCMPB1
				T32A ch0 timer B overflow trigger	T32A00TRGOUTOFB
				T32A ch0 timer B underflow trigger	T32A00TRGOUTUFB
				INSEL31 output	-
	Timer B	T32A00TRGINBPHCK (Other timer output)	-	T32A ch0 timer A output	T32A00OUTA
		T32A00TRGINBPCK (Internal trigger input)	***[TSEL0CR7]*** <INSEL30>	T32A ch0 timer register A0 match trigger	T32A00TRGOUTCMPA0
				T32A ch0 timer register A1 match trigger	T32A00TRGOUTCMPA1
				T32A ch0 timer A overflow trigger	T32A00TRGOUTOFA
				T32A ch0 timer A underflow trigger	T32A00TRGOUTUFA
	Timer C	T32A00TRGINCPHCK (Other timer output)	-	-	-
		T32A00TRGINCPCK (Internal trigger input)			
ch1	Timer A	T32A01TRGINAPHCK (Other timer output)	-	T32A ch1 timer B output	T32A01OUTB
		T32A01TRGINAPCK (internal trigger input)	***[TSEL0CR8]*** <INSEL32>	T32A ch1 timer register B0 match trigger	T32A01TRGOUTCMPB0
				T32A ch1 timer register B1 match trigger	T32A01TRGOUTCMPB1
				T32A ch1 timer B overflow trigger	T32A01TRGOUTOFB
				T32A ch1 timer B underflow trigger	T32A01TRGOUTUFB
				INSEL40 output	-
	Timer B	T32A01TRGINBPHCK (Other timer output)	-	T32A ch1 timer A output	T32A01OUTA
		T32A01TRGINBPCK (Internal trigger input)	***[TSEL0CR8]*** <INSEL33>	T32A ch1 timer register A0 match trigger	T32A01TRGOUTCMPA0
				T32A ch1 timer register A1 match trigger	T32A01TRGOUTCMPA1
				T32A ch1 timer A overflow trigger	T32A01TRGOUTOFA
				T32A ch1 timer A underflow trigger	T32A01TRGOUTUFA
	Timer C	T32A01TRGINCPHCK (Other timer output)	-	-	-
		T32A01TRGINCPCK (Internal trigger input)			
ch2	Timer A	T32A02TRGINAPHCK (Other timer output)	-	T32A ch2 timer B output	T32A02OUTB
		T32A02TRGINAPCK (Internal trigger input)	***[TSEL0CR8]*** <INSEL34>	T32A ch2 timer register B0 match trigger	T32A02TRGOUTCMPB0
				T32A ch2 timer register B1 match trigger	T32A02TRGOUTCMPB1
				T32A ch2 timer B overflow trigger	T32A02TRGOUTOFB
				T32A ch2 timer B underflow trigger	T32A02TRGOUTUFB
				INSEL41 output	-
	Timer B	T32A02TRGINBPHCK (Other timer output)	-	T32A ch2 timer A output	T32A02OUTA
		T32A02TRGINBPCK (Internal trigger input)	***[TSEL0CR8]*** <INSEL35>	T32A ch2 timer register A0 match trigger	T32A02TRGOUTCMPA0
				T32A ch2 timer register A1 match trigger	T32A02TRGOUTCMPA1
				T32A ch2 timer A overflow trigger	T32A02TRGOUTOFA
				T32A ch2 timer A underflow trigger	T32A02TRGOUTUFA
	Timer C	T32A02TRGINCPHCK (Other timer output)	-	-	-
		T32A02TRGINCPCK (Internal trigger input)			

Note: The trigger source for the internal trigger is selected by the trigger selector: ***[TSEL0CRn]***<INSELm>. For the detail of connection, refer to the "2.2.Trigger Selector (TRGSEL)".

Table 2.47 Capture Trigger Connection (2/2)

Channel			Trigger source		
	Timer	Input signal name of capture trigger	Trigger selector	Input trigger signal	Signal name
ch3	Timer A	T32A03TRGINAPHCK (Other timer output)	-	T32A ch3 timer B output	T32A03OUTB
		T32A03TRGINAPCK (Internal trigger input)	***[TSEL0CR9]*** <INSEL36>	T32A ch3 timer register B0 match trigger	T32A03TRGOUTCMPB0
				T32A ch3 timer register B1 match trigger	T32A03TRGOUTCMPB1
				T32A ch3 timer B overflow trigger	T32A03TRGOUTOFB
				T32A ch3 timer B underflow trigger	T32A03TRGOUTUFB
				INSEL42 output	-
	Timer B	T32A03TRGINBPHCK (Other timer output)	-	T32A ch3 timer A output	T32A03OUTA
		T32A03TRGINBPCK (Internal trigger input)	***[TSEL0CR9]*** <INSEL37>	T32A ch3 timer register A0 match trigger	T32A03TRGOUTCMPA0
				T32A ch3 timer register A1 match trigger	T32A03TRGOUTCMPA1
				T32A ch3 timer A overflow trigger	T32A03TRGOUTOFA
				T32A ch3 timer A underflow trigger	T32A03TRGOUTUFA
	Timer C	T32A03TRGINCPHCK (Other timer output)	-	-	-
		T32A03TRGINCPCK (Internal trigger input)			
ch4	Timer A	T32A04TRGINAPHCK (Other timer output)	-	T32A ch4 timer B output	T32A04OUTB
		T32A04TRGINAPCK (Internal trigger input)	***[TSEL0CR9]*** <INSEL38>	T32A ch4 timer register B0 match trigger	T32A04TRGOUTCMPB0
				T32A ch4 timer register B1 match trigger	T32A04TRGOUTCMPB1
				T32A ch4 timer B overflow trigger	T32A04TRGOUTOFB
				T32A ch4 timer B underflow trigger	T32A04TRGOUTUFB
				INSEL43 output	-
	Timer B	T32A04TRGINBPHCK (Other timer output)	-	T32A ch4 timer A output	T32A04OUTA
		T32A04TRGINBPCK (Internal trigger input)	***[TSEL0CR9]*** <INSEL39>	T32A ch4 timer register A0 match trigger	T32A04TRGOUTCMPA0
				T32A ch4 timer register A1 match trigger	T32A04TRGOUTCMPA1
				T32A ch4 timer A overflow trigger	T32A04TRGOUTOFA
				T32A ch4 timer A underflow trigger	T32A04TRGOUTUFA
	Timer C	T32A04TRGINCPHCK (Other timer output)	-	-	-
		T32A04TRGINCPCK (Internal trigger input)			

Note: The trigger source for the internal trigger is selected by the trigger selector: ***[TSEL0CRn]***<INSELm> .
For the detail of connection, refer to the "2.2.Trigger Selector (TRGSEL)".

2.11.4.2. Other Connection

Table 2.48 T32A Trigger Output Connection List (1/2)

Channel		Function output		Trigger selector	Output destination	
	Timer		Signal name			Signal name
ch0	Timer A	Timer A output	T32A00OUTA	-	T32A ch0 timer B	T32A00TRGINBPHCK
				-	A-ENC32 ch0	ENC0PSGI
		Timer register A0 match trigger	T32A00TRGOUTCMPA0	-	A-PMD ch0	PMD0TMR
				[TSEL0CR7] <INSEL30>	T32A ch0 timer B	T32A00TRGINBPCK
		Timer register A1 match trigger	T32A00TRGOUTCMPA1	***[TSEL0CR5]*** <INSEL22>	ADC unit A	ADATRGIN
		Timer A overflow trigger	T32A00TRGOUTOFA	***[TSEL0CR7]*** <INSEL30>	T32A ch0 timer B	T32A00TRGINBPCK
		Timer A underflow trigger	T32A00TRGOUTUFA			
	Timer B	Timer B output	T32A00OUTB	-	T32A ch0 timer A	T32A00TRGINAPHCK
		Timer B overflow trigger	T32A00TRGOUTOFB	***[TSEL0CR7]*** <INSEL29>	T32A ch0 timer A	T32A00TRGINAPCK
		Timer B underflow trigger	T32A00TRGOUTUFB			
		Timer register B0 match trigger	T32A00TRGOUTCMPB0			
		Timer register B1 match trigger	T32A00TRGOUTCMPB1	***[TSEL0CR5]*** <INSEL22>	ADC unit A	ADATRGIN
	Timer C	Timer C output	T32A00OUTC	-	-	-
		Timer C overflow trigger	T32A00TRGOUTOFC			
		Timer C underflow trigger	T32A00TRGOUTUFC			
		Timer register C0 match trigger	T32A00TRGOUTCMPC0			
		Timer register C1 match trigger	T32A00TRGOUTCMPC1			
ch1	Timer A	Timer A output	T32A01OUTA	-	T32A ch1 timer B	T32A01TRGINBPHCK
				-	A-ENC32 ch1	ENC1PSGI
		Timer register A0 match trigger	T32A01TRGOUTCMPA0	-	A-PMD ch1	PMD1TMR
				[TSEL0CR8] <INSEL33>	T32A ch1 timer B	T32A01TRGINBPCK
		Timer register A1 match trigger	T32A01TRGOUTCMPA1	***[TSEL0CR6]*** <INSEL25>	TSPI ch1	TSPI1TRG
					UART ch1	UART1TRGIN
				[TSEL0CR6] <INSEL26>	TSPI ch2	TSPI2TRG
					UART ch2	UART2TRGIN
		Timer A overflow trigger	T32A01TRGOUTOFA	***[TSEL0CR8]*** <INSEL33>	T32A ch1 timer B	T32A01TRGINBPCK
		Timer A underflow trigger	T32A01TRGOUTUFA			
	Timer B	Timer B output	T32A01OUTB	-	T32A ch1 timer A	T32A01TRGINAPHCK
		Timer B overflow trigger	T32A01TRGOUTOFB	***[TSEL0CR8]*** <INSEL32>	T32A ch1 timer A	T32A01TRGINAPCK
		Timer B underflow trigger	T32A01TRGOUTUFB			
		Timer register B0 match trigger	T32A01TRGOUTCMPB0			
		Timer register B1 match trigger	T32A01TRGOUTCMPB1	***[TSEL0CR6]*** <INSEL25>	TSPI ch1	TSPI1TRG
					UART ch1	UART1TRGIN
				[TSEL0CR6] <INSEL26>	TSPI ch2	TSPI2TRG
					UART ch2	UART2TRGIN
	Timer C	Timer C output	T32A01OUTC	-	-	-
		Timer C overflow trigger	T32A01TRGOUTOFC			
		Timer C underflow trigger	T32A01TRGOUTUFC			
		Timer register C0 match trigger	T32A01TRGOUTCMPC0			
		Timer register C1 match trigger	T32A01TRGOUTCMPC1			

Note: The trigger source for the internal trigger is selected by the trigger selector: ***[TSEL0CRn]***<INSELm>. For the detail of connection, refer to the "2.2.Trigger Selector (TRGSEL)".

Table 2.49 T32A Trigger Output Connection List (2/2)

Channel	Timer	Function output		Trigger selector	Output destination	
			Signal name			Signal name
ch2	Timer A	Timer A output	T32A02OUTA	-	T32A ch2 timer B	T32A02TRGINBPHCK
		Timer register A0 match trigger	T32A02TRGOUTCMPA0	***[TSEL0CR8]*** <INSEL35>	T32A ch2 timer B	T32A02TRGINBPCK
		Timer register A1 match trigger	T32A02TRGOUTCMPA1			
		Timer A overflow trigger	T32A02TRGOUTOFA			
		Timer A underflow trigger	T32A02TRGOUTUFA			
	Timer B	Timer B output	T32A02OUTB	-	T32A ch2 timer A	T32A02TRGINAPHCK
		Timer B overflow trigger	T32A02TRGOUTOFB	***[TSEL0CR8]*** <INSEL34>	T32A ch2 timer A	T32A02TRGINAPCK
		Timer B underflow trigger	T32A02TRGOUTUFB			
		Timer register B0 match trigger	T32A02TRGOUTCMPB0			
		Timer register B1 match trigger	T32A02TRGOUTCMPB1			
				[TSEL0CR5] <INSEL23>	ADC unit B	ADBTRGIN
	Timer C	Timer C output	T32A02OUTC	-	-	-
		Timer C overflow trigger	T32A02TRGOUTOFC			
		Timer C underflow trigger	T32A02TRGOUTUFC			
		Timer register C0 match trigger	T32A02TRGOUTCMPC0			
		Timer register C1 match trigger	T32A02TRGOUTCMPC1			
ch3	Timer A	Timer A output	T32A03OUTA	-	T32A ch3 timer B	T32A03TRGINBPHCK
		Timer A overflow trigger	T32A03TRGOUTOFA	***[TSEL0CR9]*** <INSEL37>	T32A ch3 timer B	T32A03TRGINBPCK
		Timer A underflow trigger	T32A03TRGOUTUFA			
		Timer register A0 match trigger	T32A03TRGOUTCMPA0			
		Timer register A1 match trigger	T32A03TRGOUTCMPA1	***[TSEL0CR6]*** <INSEL24>	TSPI ch0	TSPI0TRG
					UART ch0	UART0TRGIN
	Timer B	Timer B output	T32A03OUTB	-	T32A ch3 timer A	T32A03TRGINAPHCK
		Timer B overflow trigger	T32A03TRGOUTOFB	***[TSEL0CR9]*** <INSEL36>	T32A ch3 timer A	T32A03TRGINAPCK
		Timer B underflow trigger	T32A03TRGOUTUFB			
		Timer register B0 match trigger	T32A03TRGOUTCMPB0			
		Timer register B1 match trigger	T32A03TRGOUTCMPB1	***[TSEL0CR6]*** <INSEL24>	TSPI ch0	TSPI0TRG
					UART ch0	UART0TRGIN
	Timer C	Timer C output	T32A03OUTC	-	-	-
		Timer C overflow trigger	T32A03TRGOUTOFC			
		Timer C underflow trigger	T32A03TRGOUTUFC			
		Timer register C0 match trigger	T32A03TRGOUTCMPC0			
		Timer register C1 match trigger	T32A03TRGOUTCMPC1			
ch4	Timer A	Timer A output	T32A04OUTA	-	T32A ch4 timer B	T32A04TRGINBPHCK
		Timer A overflow trigger	T32A04TRGOUTOFA	***[TSEL0CR9]*** <INSEL39>	T32A ch4 timer B	T32A04TRGINBPCK
		Timer A underflow trigger	T32A04TRGOUTUFA			
		Timer register A0 match trigger	T32A04TRGOUTCMPA0			
		Timer register A1 match trigger	T32A04TRGOUTCMPA1			
	Timer B	Timer B output	T32A04OUTB	-	T32A ch4 timer A	T32A04TRGINAPHCK
		Timer B overflow trigger	T32A04TRGOUTOFB	***[TSEL0CR9]*** <INSEL38>	T32A ch4 timer A	T32A04TRGINAPCK
		Timer B underflow trigger	T32A04TRGOUTUFB			
		Timer register B0 match trigger	T32A04TRGOUTCMPB0			
		Timer register B1 match trigger	T32A04TRGOUTCMPB1	***[TSEL0CR6]*** <INSEL27>	TSPI ch3	TSPI3TRG
					UART ch3	UART3TRGIN
				[TSEL0CR7] <INSEL28>	UART ch4	UART4TRGIN
	Timer C	Timer C output	T32A04OUTC	-	-	-
		Timer C overflow trigger	T32A04TRGOUTOFC			
		Timer C underflow trigger	T32A04TRGOUTUFC			
		Timer register C0 match trigger	T32A04TRGOUTCMPC0			
		Timer register C1 match trigger	T32A04TRGOUTCMPC1			

Note: The trigger source for the internal trigger is selected by the trigger selector: ***[TSEL0CRn]***<INSELm>. For the detail of connection, refer to the "2.2.Trigger Selector (TRGSEL)".

2.11.4.3. Synchronous Control Connection

In the T32A, as shown in the following table, synchronous connection of the timer is carried out within the same channel.

Table 2.50 Synchronous Control Connection Specifications

Channel	Timer	Master		Timer	Slave	
		Function (output)	Signal name		Function (input)	Signal name
ch0	Timer A	Synchronous start output A	T32A00SYNCSTARTOUTA	Timer B	Synchronous start B	T32A00SYNCSTARTB
		Synchronous stop output A	T32A00SYNCSTOPOUTA		Synchronous stop B	T32A00SYNCSTOPB
		Synchronous Reload output A	T32A00SYNCRELOADOUTA		Synchronous Reload B	T32A00SYNCRELOADB
ch1	Timer A	Synchronous start output A	T32A01SYNCSTARTOUTA	Timer B	Synchronous start B	T32A01SYNCSTARTB
		Synchronous stop output A	T32A01SYNCSTOPOUTA		Synchronous stop B	T32A01SYNCSTOPB
		Synchronous Reload output A	T32A01SYNCRELOADOUTA		Synchronous Reload B	T32A01SYNCRELOADB
ch2	Timer A	Synchronous start output A	T32A02SYNCSTARTOUTA	Timer B	Synchronous start B	T32A02SYNCSTARTB
		Synchronous stop output A	T32A02SYNCSTOPOUTA		Synchronous stop B	T32A02SYNCSTOPB
		Synchronous Reload output A	T32A02SYNCRELOADOUTA		Synchronous Reload B	T32A02SYNCRELOADB
ch3	Timer A	Synchronous start output A	T32A03SYNCSTARTOUTA	Timer B	Synchronous start B	T32A03SYNCSTARTB
		Synchronous stop output A	T32A03SYNCSTOPOUTA		Synchronous stop B	T32A03SYNCSTOPB
		Synchronous Reload output A	T32A03SYNCRELOADOUTA		Synchronous Reload B	T32A03SYNCRELOADB
ch4	Timer A	Synchronous start output A	T32A04SYNCSTARTOUTA	Timer B	Synchronous start B	T32A04SYNCSTARTB
		Synchronous stop output A	T32A04SYNCSTOPOUTA		Synchronous stop B	T32A04SYNCSTOPB
		Synchronous Reload output A	T32A04SYNCRELOADOUTA		Synchronous Reload B	T32A04SYNCRELOADB

2.11.5. Pulse Counter List

The 32-bit timer event counter is the pulse counter as shown in the table below.

Table 2.51 T32A Pulse Counter List

Channel	Support mode
ch0	1-phase pulse count
ch1	1-phase pulse count
ch2	1-phase pulse count
ch3	1-phase pulse count
ch4	1-phase pulse count

2.11.6. DMA Request

The T32A has the DMA request shown in the following tables.
When there is mention of the register name in the trigger selector column of the table, please select a request to use with a trigger selector.

Table 2.52 T32A DMA Request (1/2)

Channel	Request	Signal name	Trigger selector	DMA request channel		
					Single transfer	Burst transfer
ch0	DMA request at match A1 register	T32A00DMAREQCMPA1	***[TSEL0CR2]*** <INSEL10>	19	-	✓
	DMA request at match C1 register	T32A00DMAREQCMPC1				
	DMA request at match B1 register	T32A00DMAREQCMPB1	***[TSEL0CR3]*** <INSEL12>	22	-	✓
	DMA request at capture A0 register	T32A00DMAREQCAPA0	***[TSEL0CR3]*** <INSEL13>	23	-	✓
	DMA request at capture A1 register	T32A00DMAREQCAPA1				
	DMA request at capture C0 register	T32A00DMAREQCAPC0				
	DMA request at capture C1 register	T32A00DMAREQCAPC1				
	DMA request at capture B0 register	T32A00DMAREQCAPB0	***[TSEL0CR4]*** <INSEL16>	26	-	✓
	DMA request at capture B1 register	T32A00DMAREQCAPB1				
ch1	DMA request at match A1 register	T32A01DMAREQCMPA1	***[TSEL0CR2]*** <INSEL10>	19	-	✓
	DMA request at match C1 register	T32A01DMAREQCMPC1				
	DMA request at match B1 register	T32A01DMAREQCMPB1	***[TSEL0CR3]*** <INSEL12>	22	-	✓
	DMA request at capture A0 register	T32A01DMAREQCAPA0	***[TSEL0CR3]*** <INSEL13>	23	-	✓
	DMA request at capture A1 register	T32A01DMAREQCAPA1				
	DMA request at capture C0 register	T32A01DMAREQCAPC0				
	DMA request at capture C1 register	T32A01DMAREQCAPC1				
	DMA request at capture B0 register	T32A01DMAREQCAPB0	***[TSEL0CR4]*** <INSEL16>	26	-	✓
	DMA request at capture B1 register	T32A01DMAREQCAPB1				
ch2	DMA request at match A1 register	T32A02DMAREQCMPA1	***[TSEL0CR2]*** <INSEL11>	20	-	✓
	DMA request at match C1 register	T32A02DMAREQCMPC1				
	DMA request at match B1 register	T32A02DMAREQCMPB1	***[TSEL0CR3]*** <INSEL12>	22	-	✓
	DMA request at capture A0 register	T32A02DMAREQCAPA0	***[TSEL0CR3]*** <INSEL14>	24	-	✓
	DMA request at capture A1 register	T32A02DMAREQCAPA1				
	DMA request at capture C0 register	T32A02DMAREQCAPC0				
	DMA request at capture C1 register	T32A02DMAREQCAPC1				
	DMA request at capture B0 register	T32A02DMAREQCAPB0	***[TSEL0CR4]*** <INSEL16>	26	-	✓
	DMA request at capture B1 register	T32A02DMAREQCAPB1				

Note: ✓: Available, -: N/A

Table 2.53 T32A DMA Request (2/2)

Channel	Request	Signal name	Trigger selector	DMA request channel		
					Single transfer	Burst transfer
ch3	DMA request at match A1 register	T32A03DMAREQCMPA1	***[TSEL0CR2]*** <INSEL11>	20	-	✓
	DMA request at match C1 register	T32A03DMAREQCMPC1				
	DMA request at match B1 register	T32A03DMAREQCMPB1	***[TSEL0CR3]*** <INSEL12>	22	-	✓
	DMA request at capture A0 register	T32A03DMAREQCAPA0	***[TSEL0CR3]*** <INSEL14>	24	-	✓
	DMA request at capture A1 register	T32A03DMAREQCAPA1				
	DMA request at capture C0 register	T32A03DMAREQCAPC0				
	DMA request at capture C1 register	T32A03DMAREQCAPC1				
	DMA request at capture B0 register	T32A03DMAREQCAPB0	***[TSEL0CR4]*** <INSEL17>	27	-	✓
	DMA request at capture B1 register	T32A03DMAREQCAPB1				
ch4	DMA request at match A1 register	T32A04DMAREQCMPA1	***[TSEL0CR2]*** <INSEL11>	20	-	✓
	DMA request at match C1 register	T32A04DMAREQCMPC1				
	DMA request at match B1 register	T32A04DMAREQCMPB1	***[TSEL0CR3]*** <INSEL12>	22	-	✓
	DMA request at capture A0 register	T32A04DMAREQCAPA0	***[TSEL0CR3]*** <INSEL15>	25	-	✓
	DMA request at capture A1 register	T32A04DMAREQCAPA1				
	DMA request at capture C0 register	T32A04DMAREQCAPC0				
	DMA request at capture C1 register	T32A04DMAREQCAPC1				
	DMA request at capture B0 register	T32A04DMAREQCAPB0	***[TSEL0CR4]*** <INSEL17>	27	-	✓
	DMA request at capture B1 register	T32A04DMAREQCAPB1				

Note: ✓: Available, -: N/A

2.11.7. Unsupported Interrupt

Every count interrupt (INTT32AxEVRYC) does not correspond in the TMPM471F10FG.

2.12. Universal Asynchronous Receiver Transmitter Circuit (UART)

2.12.1. Built-in Channel

The following table shows the UART built-in channel.
In TMPM471F10FG, maximum communication speed of UART is 5.0 Mbps.

Table 2.54 UART Built-in Channel

Product	UART channel (✓: Available, -: N/A)				
	ch0	ch1	ch2	ch3	ch4
TMPM471F10FG	✓	✓	✓	✓	✓

2.12.2. Function Pin and Port

The function pins are assigned to the port of the following table.
Please do not use simultaneously the same function currently assigned to two or more pins.

Table 2.55 UART Function Pin and Port

Channel	Function pin		Port
ch0	UT0TXDA	Output	PE0
			PE1
	UT0RXD	Input	PE0
			PE1
	UT0CTS_N	Output	PE2
			PE3
	UT0RTS_N	Input	PE2
			PE3
ch1	UT1TXDA	Output	PA5
			PA6
	UT1RXD	Input	PA5
			PA6
	UT1CTS_N	Output	PA4
			PA7
	UT1RTS_N	Input	PA4
			PA7
ch2	UT2TXDA	Output	PD5
			PD6
	UT2RXD	Input	PD5
			PD6
	UT2CTS_N	Output	PD3
			PD4
	UT2RTS_N	Input	PD3
			PD4
ch3	UT3TXDA	Output	PF3
			PF4
	UT3RXD	Input	PF3
			PF4
	UT3CTS_N	Output	PF1
			PF2
	UT3RTS_N	Input	PF1
			PF2
ch4	UT4TXDA	Output	PG3
			PG4
	UT4RXD	Input	PG3
			PG4
	UT4CTS_N	Output	PG1
			PG2
	UT4RTS_N	Input	PG1
			PG2

2.12.3. Half Clock Mode Support

Half clock mode of the UART corresponds to 1-pin mode only.

2.12.4. Clock for Prescaler

The UART uses the clock of the following table as a prescaler clock.

Table 2.56 UART Clock for Prescaler

Clock
ΦT0m

2.12.5. DMA Request

The following table shows the DMA request in the UART.

Table 2.57 UART DMA Request

Channel	Request	Signal name	Trigger selector	DMA request channel		
					Single transfer	Burst transfer
ch0	Reception DMA request	UART0RX_DMAREQ	***[TSEL0CR0]*** <INSEL0>	0	✓	✓
	Transmission DMA request	UART0TX_DMAREQ	***[TSEL0CR0]*** <INSEL1>	1	✓	✓
ch1	Reception DMA request	UART1RX_DMAREQ	***[TSEL0CR0]*** <INSEL2>	2	✓	✓
	Transmission DMA request	UART1TX_DMAREQ	***[TSEL0CR0]*** <INSEL3>	3	✓	✓
ch2	Reception DMA request	UART2RX_DMAREQ	***[TSEL0CR1]*** <INSEL4>	4	✓	✓
	Transmission DMA request	UART2TX_DMAREQ	***[TSEL0CR1]*** <INSEL5>	5	✓	✓
ch3	Reception DMA request	UART3RX_DMAREQ	***[TSEL0CR1]*** <INSEL6>	6	✓	✓
	Transmission DMA request	UART3TX_DMAREQ	***[TSEL0CR1]*** <INSEL7>	7	✓	✓
Ch4	Reception DMA request	UART4RX_DMAREQ	-	8	✓	✓
	Transmission DMA request	UART4TX_DMAREQ	-	9	✓	✓

Note: ✓: Available, -: N/A

2.12.6. Internal Signal Connection Specification

2.12.6.1. Trigger Transfer Signal Connection

Transfer function of the UART has a trigger signal control.
A trigger control signal is selected with the trigger source and use it as the following table.

Table 2.58 UART Trigger Transfer Signal Connection: Input

Channel	Function input		Trigger selector	Trigger source	
		Signal name		Input trigger signal	Signal name
ch0	Trigger transmission signal input	UART0TRGIN	***[TSEL0CR6]*** <INSEL24>	T32A ch3 timer register A1 match trigger	T32A03TRGOUTCMPA1
				T32A ch3 timer register B1 match trigger	T32A03TRGOUTCMPB1
ch1	Trigger transmission signal input	UART1TRGIN	***[TSEL0CR6]*** <INSEL25>	T32A ch1 timer register A1 match trigger	T32A01TRGOUTCMPA1
				T32A ch1 timer register B1 match trigger	T32A01TRGOUTCMPB1
ch2	Trigger transmission signal input	UART2TRGIN	***[TSEL0CR6]*** <INSEL26>	T32A ch1 timer register A1 match trigger	T32A01TRGOUTCMPA1
				T32A ch1 timer register B1 match trigger	T32A01TRGOUTCMPB1
ch3	Trigger transmission signal input	UART3TRGIN	***[TSEL0CR6]*** <INSEL27>	T32A ch4 timer register A1 match trigger	T32A04TRGOUTCMPA1
				T32A ch4 timer register B1 match trigger	T32A04TRGOUTCMPB1
ch4	Trigger transmission signal input	UART4TRGIN	***[TSEL0CR7]*** <INSEL28>	T32A ch4 timer register A1 match trigger	T32A04TRGOUTCMPA1
				T32A ch4 timer register B1 match trigger	T32A04TRGOUTCMPB1

Note: The trigger source for the trigger signal is selected by the trigger selector: ***[TSEL0CRn]***<INSELm>.
For the detail of connection, refer to the "2.2.Trigger Selector (TRGSEL)".

2.12.6.2. T32A Connection

In the UART, there is a signal connected with the peripheral function inside in addition to this as shown in the following table.

Table 2.59 UART Inside Connection List: Output

Channel	Function output		Trigger selector	Output destination		
		Signal name		Peripheral function		Signal name
ch0	Transmission completion trigger	UART0TXTRG	***[TSEL0CR10]*** <INSEL42>	TRGSEL	INSEL36 input	-
	Reception completion trigger	UART0RXTRG				
ch1	Transmission completion trigger	UART1TXTRG	***[TSEL0CR10]*** <INSEL40>	TRGSEL	INSEL32 input	-
	Reception completion trigger	UART1RXTRG				
ch2	Transmission completion trigger	UART2TXTRG	***[TSEL0CR10]*** <INSEL40>	TRGSEL	INSEL32 input	-
	Reception completion trigger	UART2RXTRG				
ch3	Transmission completion trigger	UART3TXTRG	***[TSEL0CR10]*** <INSEL43>	TRGSEL	INSEL38 input	-
	Reception completion trigger	UART3RXTRG				
ch4	Transmission completion trigger	UART4TXTRG	***[TSEL0CR10]*** <INSEL43>	TRGSEL	INSEL38 input	-
	Reception completion trigger	UART4RXTRG				

2.13. I²C Interface Version A (EI2C)

2.13.1. Built-in Channel

The following table shows the I²C interface version A built-in channel.
In the TMPM471F10FG, the I²C interface version A supports Standard mode, Fast mode, and Fast mode plus.

Table 2.60 EI2C Built-in Channel

Product	Channel (✓: Available, -: N/A)	
	ch0	ch1
TMPM471F10FG	✓	✓

2.13.2. Function Pin and Port

The function pins are assigned to the port of the following table.

Table 2.61 EI2C Function Pin and Port

Channel	Function pin		Port
ch0	EI2C0SCL	I/O	PN1
	EI2C0SDA	I/O	PN0
ch1	EI2C1SCL	I/O	PK1
	EI2C1SDA	I/O	PK0

2.13.3. Clock for Prescaler

The I²C interface version A uses the clock of the following table as a prescaler clock.

Table 2.62 EI2C Clock for Prescaler

Clock
fsysm

2.13.4. Wakeup Function

TMPM471F10FG does not support I²C interface version A wakeup function.

2.13.5. DMA Request

The following table shows the DMA request in the I²C interface version A.

Table 2.63 EI2C DMA Request

Channel	Request	Signal name	DMA request channel		
				Single transfer	Burst transfer
ch0	Receiving DMA request	I2C0ARXDMAREQ	10	-	✓
	Transmitting DMA request	I2C0ATXDMAREQ	11	-	✓
ch1	Receiving DMA request	I2C1ARXDMAREQ	12	-	✓
	Transmitting DMA request	I2C1ATXDMAREQ	13	-	✓

Note: ✓: Available, -: N/A

2.14. Serial Peripheral Interface (TSPI)

2.14.1. Built-in Channel

The following table shows the TSPI built-in channel.
In TMPM471F10FG, maximum communication speed of TSPI is 20MHz as master and 15MHz as slave.

Table 2.64 TSPI Built-in Channel

Product	Channel (✓: Available, -: N/A)			
	ch0	ch1	ch2	ch3
TMPM471F10FG	✓	✓	✓	✓

2.14.2. Function Pin and Port

The function pins are assigned to the port of the following table.
Please do not use simultaneously the same function currently assigned to two or more pins.

Table 2.65 TSPI Function Pin and Port

Channel	Function pin		Port
ch0	TSPI0SCK	I/O	PE2
	TSPI0TXD	Output	PE0
	TSPI0RXD	Input	PE1
	TSPI0CSIN	Input	PE3
	TSPI0CS0	Output	PE4
	TSPI0CS1	Output	PE5
ch1	TSPI1SCK	I/O	PA4
	TSPI1TXD	Output	PA5
	TSPI1RXD	Input	PA6
	TSPI1CSIN	Input	PA7
	TSPI1CS0	Output	PA2
	TSPI1CS1	Output	PA3
ch2	TSPI2SCK	I/O	PD4
	TSPI2TXD	Output	PD5
	TSPI2RXD	Input	PD6
	TSPI2CSIN	Input	PD3
	TSPI2CS0	Output	PD1
	TSPI2CS1	Output	PD2
ch3	TSPI3SCK	I/O	PF2
	TSPI3TXD	Output	PF3
	TSPI3RXD	Input	PF4
	TSPI3CSIN	Input	PF0
	TSPI3CS0	Output	PF1
	TSPI3CS1	Output	PB0

Note: In TMPM471F10FG, there is no TSPIxCS2 pin and TSPIxCS3 pin.

2.14.3. *[TSPIxCR2]*<RXDLY[2:0]> Set Value

TMPM471F10FG setting value of TSPI control register 2 ([TSPIxCR2]<RXDLY[2:0]>) is as follows:

Table 2.66 *[TSPIxCR2]*<RXDLY[2:0]> Set Value

Bit	Bit symbol	After reset	Function
18:16	<RXDLY[2:0]>	001	000: fsysm ≤ 40MHz 001: fsysm > 40MHz

2.14.4. Clock for Prescaler

The TSPI uses the clock of the following table as a prescaler clock.

Table 2.67 TSPI Clock for Prescaler

Clock
ΦT0m

2.14.5. DMA Request

The following table shows the DMA request in the TSPI.

Table 2.68 TSPI DMA Request

Channel	Request	Signal name	Trigger selector	DMA request channel		
					Single transfer	Burst transfer
ch0	Receive DMA request	TSPI0RX_DMA	***[TSEL0CR0]*** <INSEL0>	0	✓	✓
	Transmit DMA request	TSPI0TX_DMA	***[TSEL0CR0]*** <INSEL1>	1	✓	✓
ch1	Receive DMA request	TSPI1RX_DMA	***[TSEL0CR0]*** <INSEL2>	2	✓	✓
	Transmit DMA request	TSPI1TX_DMA	***[TSEL0CR0]*** <INSEL3>	3	✓	✓
ch2	Receive DMA request	TSPI02X_DMA	***[TSEL0CR1]*** <INSEL4>	4	✓	✓
	Transmit DMA request	TSPI2TX_DMA	***[TSEL0CR1]*** <INSEL5>	5	✓	✓
ch3	Receive DMA request	TSPI3RX_DMA	***[TSEL0CR1]*** <INSEL6>	6	✓	✓
	Transmit DMA request	TSPI3TX_DMA	***[TSEL0CR1]*** <INSEL7>	7	✓	✓

Note: ✓: Available, -: N/A

2.14.6. Internal Signal Connection Specification

2.14.6.1. Trigger Transfer Signal Connection

Transfer start function of the TSPI has a trigger signal control.
A trigger control signal is selected with the trigger source and use it as the following table.

Table 2.69 TSPI Trigger Transfer: Input

Channel	Function input		Trigger selector	Trigger source	
		Signal name		Input trigger signal	Signal name
ch0	Trigger input for start communication	TSPI0TRG	***[TSEL0CR6]*** <INSEL24>	T32A ch3 timer register A1 match trigger	T32A03TRGOUTCMPA1
				T32A ch3 timer register B1 match trigger	T32A03TRGOUTCMPB1
ch1	Trigger input for start communication	TSPI1TRG	***[TSEL0CR6]*** <INSEL25>	T32A ch1 timer register A1 match trigger	T32A01TRGOUTCMPA1
				T32A ch1 timer register B1 match trigger	T32A01TRGOUTCMPB1
ch2	Trigger input for start communication	TSPI2TRG	***[TSEL0CR6]*** <INSEL26>	T32A ch1 timer register A1 match trigger	T32A01TRGOUTCMPA1
				T32A ch1 timer register B1 match trigger	T32A01TRGOUTCMPB1
ch3	Trigger input for start communication	TSPI3TRG	***[TSEL0CR6]*** <INSEL27>	T32A ch4 timer register A1 match trigger	T32A04TRGOUTCMPA1
				T32A ch4 timer register B1 match trigger	T32A04TRGOUTCMPB1

Note: The trigger source for the trigger signal is selected by the trigger selector: ***[TSEL0CR6]***<INSEL24> to <INSEL27>. For the detail of connection, refer to the "2.2.Trigger Selector (TRGSEL)".

2.14.6.2. T32A Connection

In the TSPI, there is a signal connected with the peripheral function inside in addition to this as shown in the following table.

Table 2.70 TSPI Inside Connection: Output

Channel	Function output		Trigger selector	Output destination		
		Signal name		Peripheral function		Signal name
ch0	Transmit completion trigger	TSPI0TXEND	***[TSEL0CR10]*** <INSEL42>	TRGSEL	INSEL36 input	-
	Receive completion trigger	TSPI0RXEND				
ch1	Transmit completion trigger	TSPI1TXEND	***[TSEL0CR10]*** <INSEL40>	TRGSEL	INSEL32 input	-
	Receive completion trigger	TSPI1RXEND				
ch2	Transmit completion trigger	TSPI2TXEND	***[TSEL0CR10]*** <INSEL40>	TRGSEL	INSEL32 input	-
	Receive completion trigger	TSPI2RXEND				
ch3	Transmit completion trigger	TSPI3TXEND	***[TSEL0CR10]*** <INSEL43>	TRGSEL	INSEL38 input	-
	Receive completion trigger	TSPI3RXEND				

2.15. Digital Noise Filter (DNF)

2.15.1. Built-in Unit

The following table shows the DNF built-in unit.

Table 2.71 DNF Built-in Unit

Product	Unit (✓: Available, -: N/A)
	A
TMPM471F10FG	✓

2.15.2. External Interrupt List for each Product

The DNF corresponds to the following external interrupt pins.

Table 2.72 External Interrupt and DNF

External interrupt pin (Signal name)	Port	Unit	Setting register name
INT0	PH0	A	***[DNFAENCR]***<NFEN0>
INT1	PH1		***[DNFAENCR]***<NFEN1>
INT2	PH2		***[DNFAENCR]***<NFEN2>
INT3	PA0		***[DNFAENCR]***<NFEN3>
INT4	PA2		***[DNFAENCR]***<NFEN4>
INT5	PE4		***[DNFAENCR]***<NFEN5>
INT6	PE6		***[DNFAENCR]***<NFEN6>
INT7	PE7		***[DNFAENCR***]<NFEN7>
INT8	PA7		***[DNFAENCR]***<NFEN8>
INT9	PD3		***[DNFAENCR]***<NFEN9>
INTA	PL1		***[DNFAENCR]***<NFEN10>
INTB	PL0		***[DNFAENCR***]<NFEN11>
INTC	PJ6		***[DNFAENCR]***<NFEN12>
INTD	PJ7		***[DNFAENCR]***<NFEN13>
INTE	PK0		***[DNFAENCR]***<NFEN14>
INTF	PK1		***[DNFAENCR]***<NFEN15>

2.15.3. Sampling Source Clock

The clock shown in the following table is used as a sauce clock for a sampling in DNF.

Table 2.73 DNF Sampling Source Clock

Clock
fc

2.16. Voltage Detection Circuit (LVD)

2.16.1. Built-in List

The following table shows the built-in list.

Table 2.74 Built-in LVD

Product	Built-in LVD (✓: Available, -: N/A)
TMPM471F10FG	✓

2.16.2. Detection Power Supply

A voltage detecting circuit monitors the power supply of the following tables

Table 2.75 LVD Detection Power Supply

Detection power supply	Power supply name
Digital power source	DVDD5A/DVDD5B/DVDD5C/DVDD5D

2.16.3. LVD Control Register Setting

The after reset value and possible settings of LVD control register ***[LVDCR]*** <LVL[2:0]> are as follows:

Table 2.76 LVD Control Register *[LVDCR]*<LVL[2:0]> Setting

Bit	Bit symbol	After reset	Function
6:4	<LVL[2:0]>	100	Detection/release voltage setting Detection voltage Release voltage 100: 4.0V 4.05V 101: 4.2V 4.25V 110: 4.4V 4.45V 111: 4.6V 4.65V Others: Reserved

2.17. CRC Calculation Circuit (CRC)

2.17.1. Built-in List

The following table shows the built-in list.

Table 2.77 Built-in CRC

Product	Built-in CRC (✓: Available, -: N/A)
TMPM471F10FG	✓

2.18. RAM Parity (RAMP)

2.18.1. Built-in Channel

The built-in channel is shown in the following table.

Table 2.78 Built-in RAMP Channel

Product	Channel (✓: Available, -: N/A)	
	ch0	ch1
TMPM471F10FG	✓	✓

2.18.2. Error Detection Block Area

The following table shows the detection RAM block area of each product.

Table 2.79 RAM Area and Address of RAMP

Channel	Register name	RAM area address
ch0	***[RPAR0ST]***<RPARFG0>	0x20000000 to 0x20001FFF
	[RPAR0ST]<RPARFG1>	0x20002000 to 0x2000DFFF
ch1	***[RPAR1ST]***<RPARFG0>	0x2000E000 to 0x2000FFFF

2.19. Trimming Circuit (TRM)

2.19.1. Built-in List

The following table shows the built-in list.

Table 2.80 Built-in TRM

Product	Built-in TRM (✓: Available, -: N/A)
TMPM471F10FG	✓

2.19.2. Target Oscillator

The target oscillator of the trimming circuit is the oscillator shown in the following table.

Table 2.81 TRM Trimming Target Oscillator

Target oscillator	Oscillator
Internal high-speed oscillator 1	IHOSC1

3. Revision History

Table 3.1 Revision History

Revision	Date	Description
1.0	2024-08-30	- First release

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