

TK099U60Z1

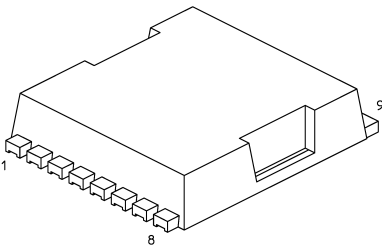
1. Applications

- Switching Power Supplies

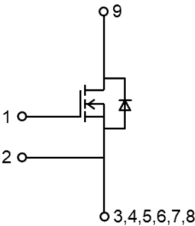
2. Features

- (1) Low drain-source on-resistance: $R_{DS(ON)} = 0.083 \Omega$ (typ.)
- (2) High-speed switching properties with the lower capacitance.
- (3) Enhancement mode: $V_{th} = 3$ to 4 V ($V_{DS} = 10$ V, $I_D = 0.93$ mA)

3. Packaging and Internal Circuit



TOLL



1: Gate
2: Source 2
3, 4, 5, 6, 7, 8: Source 1
9: Drain (heatsink)

Notice: Only use source 2 pin for gate input signal return. Please make sure that the main current flows into the source 1 pins.

4. Absolute Maximum Ratings (Note) ($T_a = 25$ °C unless otherwise specified)

Characteristics	Symbol	Rating	Unit
Drain-source voltage	V_{DSS}	600	V
Gate-source voltage	V_{GSS}	± 30	
Drain current (DC)	I_D	25	A
Drain current (pulsed)	I_{DP}	100	
Power dissipation	P_D	176	W
Single-pulse avalanche energy	E_{AS}	278	mJ
Single-pulse avalanche current	I_{AS}	4.8	A
Reverse drain current (DC)	I_{DR}	25	
Reverse drain current (pulsed)	I_{DRP}	100	
Channel temperature	T_{ch}	150	°C
Storage temperature	T_{stg}	-55 to 150	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Start of commercial production
2025-02

5. Thermal Characteristics

Characteristics	Symbol	Max	Unit
Channel-to-case thermal resistance	$R_{th(ch-c)}$	0.71	°C/W

Note 1: Ensure that the channel temperature does not exceed 150 °C.

Note 2: $V_{DD} = 90$ V, $T_{ch} = 25$ °C (initial), $L = 21.4$ mH, $I_{AS} = 4.8$ A

Note: This transistor is sensitive to electrostatic discharge and should be handled with care.

6. Electrical Characteristics

6.1. Static Characteristics ($T_a = 25$ °C unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current	I_{GSS}	$V_{GS} = \pm 30$ V, $V_{DS} = 0$ V	—	—	± 1	μ A
Drain cut-off current	I_{DSS}	$V_{DS} = 600$ V, $V_{GS} = 0$ V	—	—	2	
Drain-source breakdown voltage	$V_{(BR)DSS}$	$I_D = 10$ mA, $V_{GS} = 0$ V	600	—	—	V
Gate threshold voltage	V_{th}	$V_{DS} = 10$ V, $I_D = 0.93$ mA	3	—	4	
Drain-source on-resistance	$R_{DS(ON)}$	$V_{GS} = 10$ V, $I_D = 8.1$ A	—	0.083	0.099	Ω

6.2. Dynamic Characteristics ($T_a = 25$ °C unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Input capacitance	C_{iss}	$V_{DS} = 300$ V, $V_{GS} = 0$ V, $f = 100$ kHz	—	2050	—	pF
Reverse transfer capacitance	C_{rss}		—	2.4	—	
Output capacitance	C_{oss}		—	52	—	
Effective output capacitance (Note 3) (energy related)	$C_{O(er)}$	$V_{DS} = 0$ to 400 V, $V_{GS} = 0$ V	—	90	—	
Effective output capacitance (Note 4) (time related)	$C_{O(tr)}$		—	605	—	
Gate resistance	r_g	$V_{DS} = \text{OPEN}$, $f = 1$ MHz	—	3.3	—	Ω
Switching time (rise time)	t_r	See Figure 6.2.1	—	18	—	ns
Switching time (turn-on time)	t_{on}		—	43	—	
Switching time (fall time)	t_f		—	4.6	—	
Switching time (turn-off time)	t_{off}		—	82	—	
MOSFET dv/dt ruggedness	dv/dt	$V_{DS} \leq V_{DSS}$, $I_D \leq 12.5$ A	90	—	—	V/ns

Note 3: $C_{O(er)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 V to 400 V.

Note 4: $C_{O(tr)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 V to 400 V.

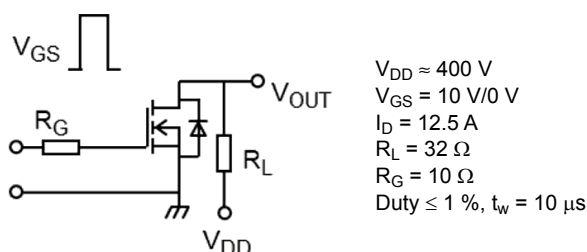


Fig. 6.2.1 Switching Time Test Circuit

6.3. Gate Charge Characteristics ($T_a = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Total gate charge (gate-source plus gate-drain)	Q_g	$V_{DD} \approx 400\text{ V}$, $V_{GS} = 10\text{ V}$, $I_D = 25\text{ A}$	—	36	—	nC
Gate-source charge 1	Q_{gs1}		—	12	—	
Gate-drain charge	Q_{gd}		—	10	—	

6.4. Source-Drain Characteristics ($T_a = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Diode forward voltage	V_{DSF}	$I_{DR} = 25\text{ A}$, $V_{GS} = 0\text{ V}$	—	—	-1.7	V
Reverse recovery time	t_{rr}	$V_{DD} = 400\text{ V}$, $I_{DR} = 12.5\text{ A}$, $V_{GS} = 0\text{ V}$ $-dI_{DR}/dt = 100\text{ A}/\mu\text{s}$	—	297	—	ns
Reverse recovery charge	Q_{rr}		—	3.6	—	μC
Peak reverse recovery current	I_{rr}		—	24.5	—	A
Diode dv/dt ruggedness	dv/dt	$V_{DD} \leq 400\text{ V}$, $I_{DR} \leq 12.5\text{ A}$, $V_{GS} = 0\text{ V}$	40	—	—	V/ns

7. Marking (Note)

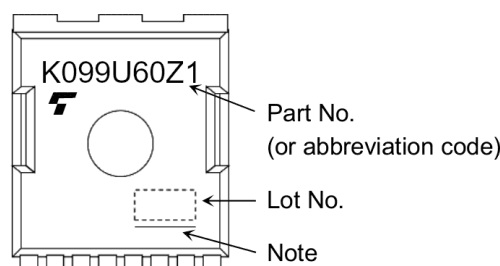


Fig. 7.1 Marking

Note: A line under a Lot No. identifies the indication of product Labels.

Not underlined: $[[Pb]]/INCLUDES > MCV$

Underlined: $[[G]]/RoHS\ COMPATIBLE$ or $[[G]]/RoHS\ [[Pb]]$

Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS compatibility of Product.

The RoHS is the Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment.

8. Characteristics Curves (Note)

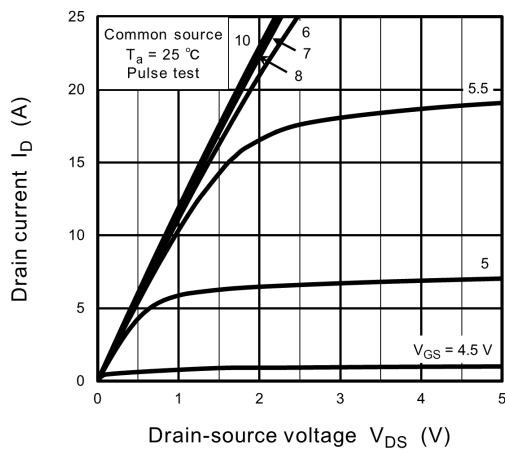


Fig. 8.1 $I_D - V_{DS}$

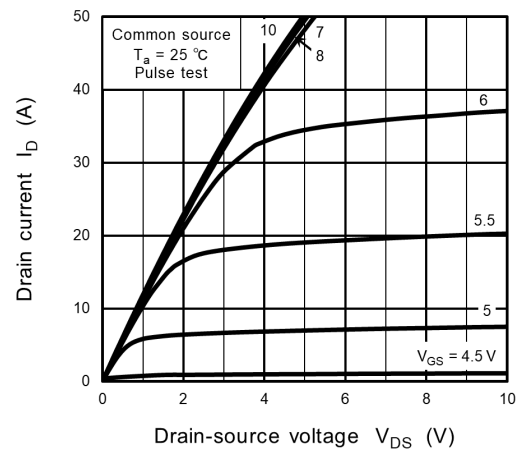


Fig. 8.2 $I_D - V_{DS}$

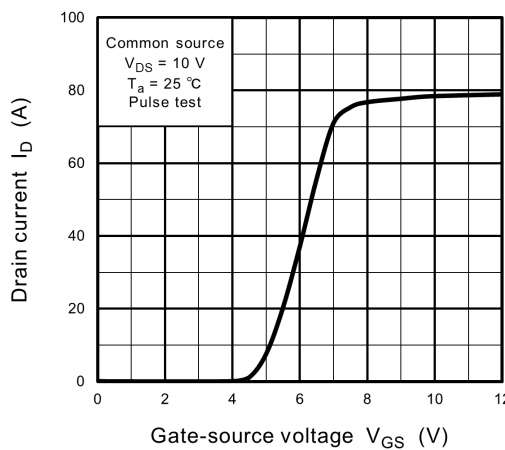


Fig. 8.3 $I_D - V_{GS}$

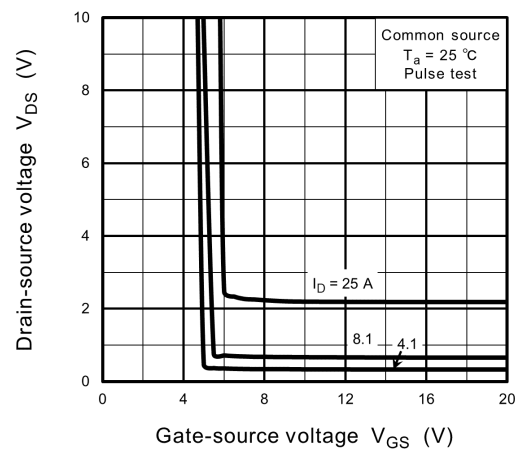


Fig. 8.4 $V_{DS} - V_{GS}$

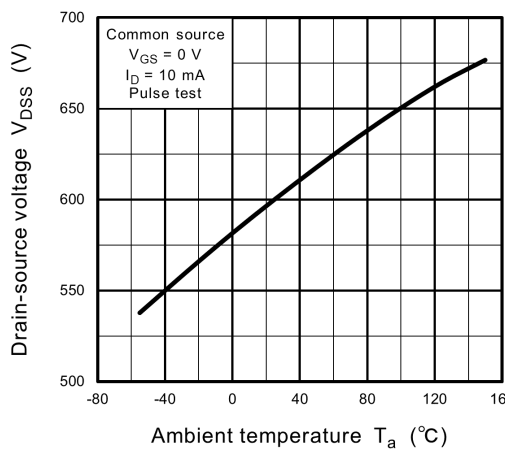


Fig. 8.5 $V_{DSS} - T_a$

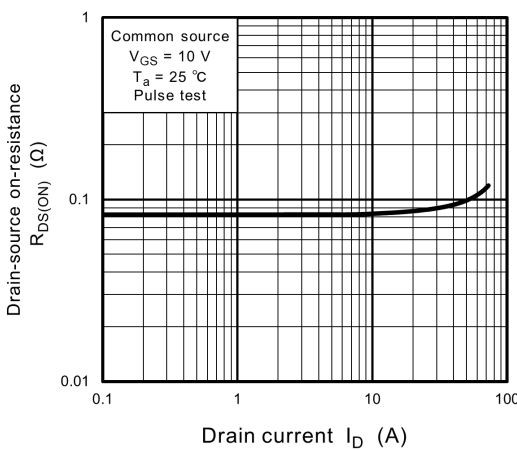


Fig. 8.6 $R_{DS(ON)} - I_D$

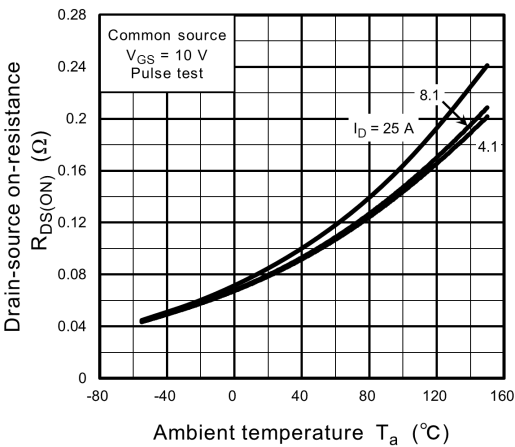


Fig. 8.7 $R_{DS(ON)} - T_a$

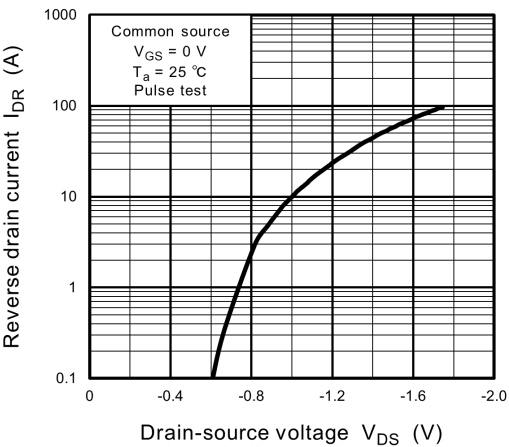


Fig. 8.8 $I_{DR} - V_{DS}$

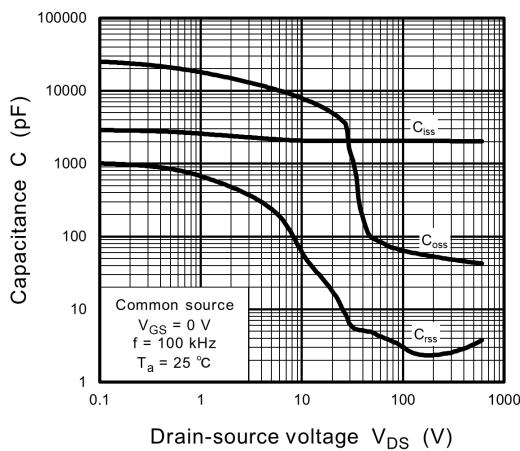


Fig. 8.9 $C - V_{DS}$

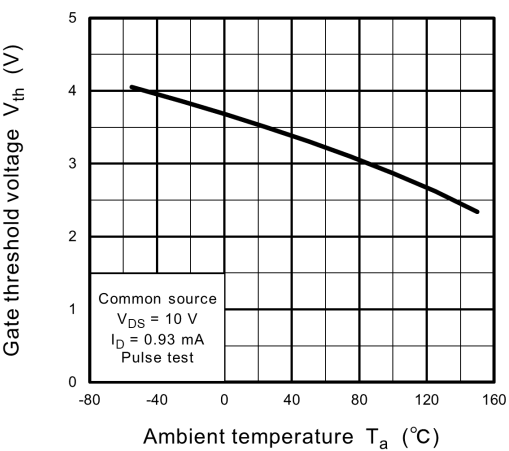


Fig. 8.10 $V_{th} - T_a$

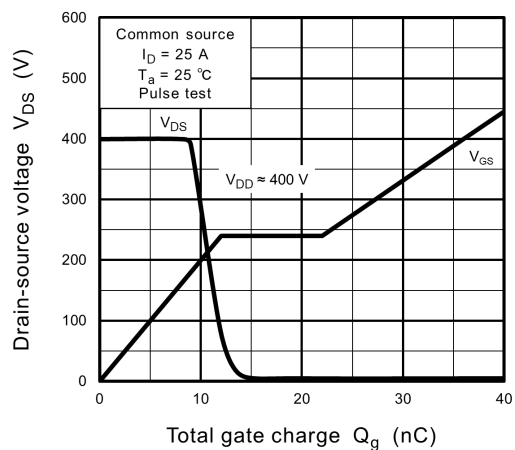


Fig. 8.11 Dynamic Input/Output Characteristics

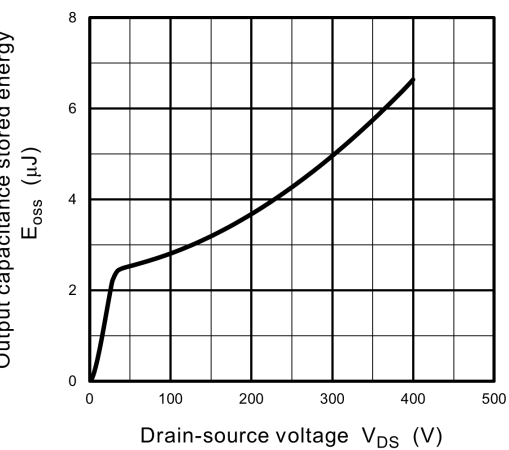


Fig. 8.12 $E_{oss} - V_{DS}$

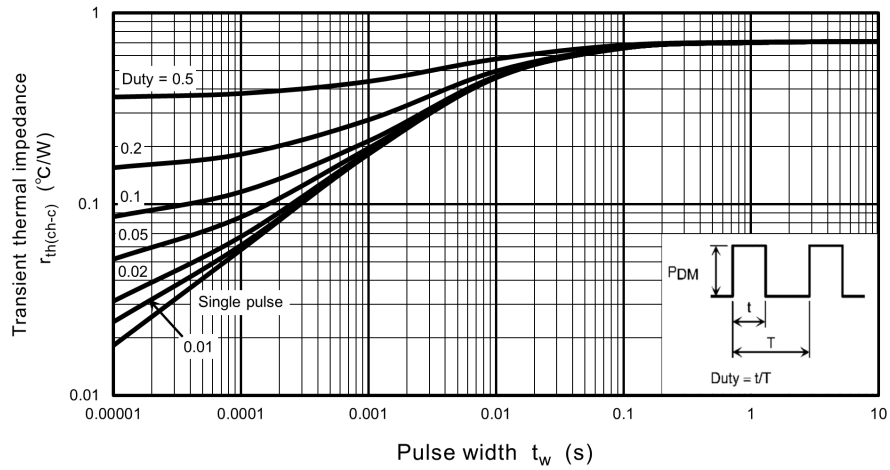


Fig. 8.13 $r_{th} - t_w$
(Guaranteed Maximum)

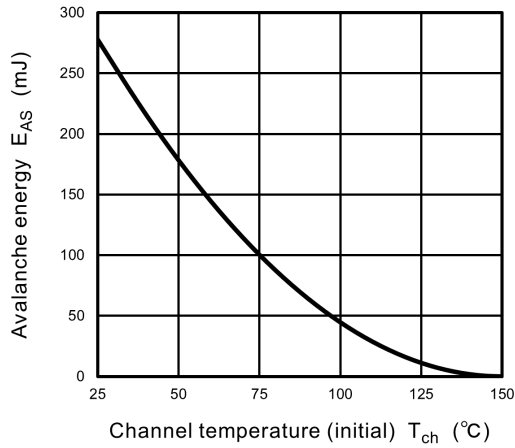


Fig. 8.14 $E_{AS} - T_{ch}$
(Guaranteed Maximum)

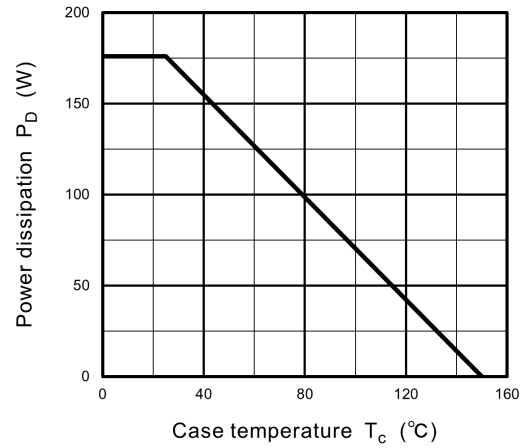


Fig. 8.15 $P_D - T_c$
(Guaranteed Maximum)

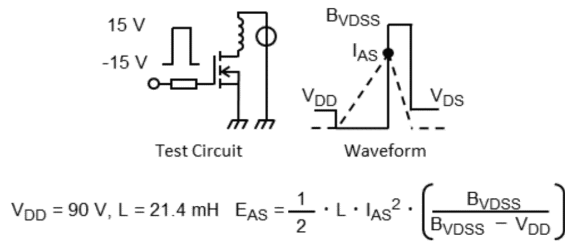


Fig. 8.16 Test Circuit/Waveform

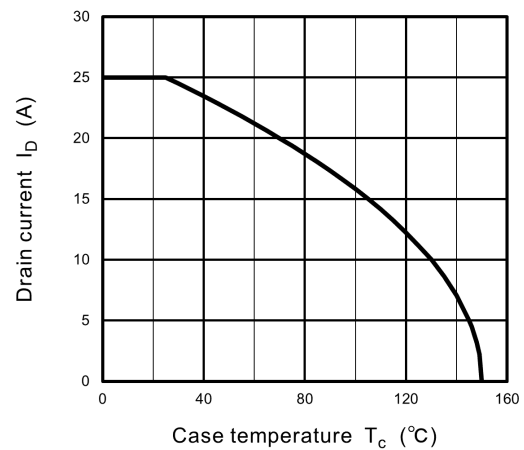
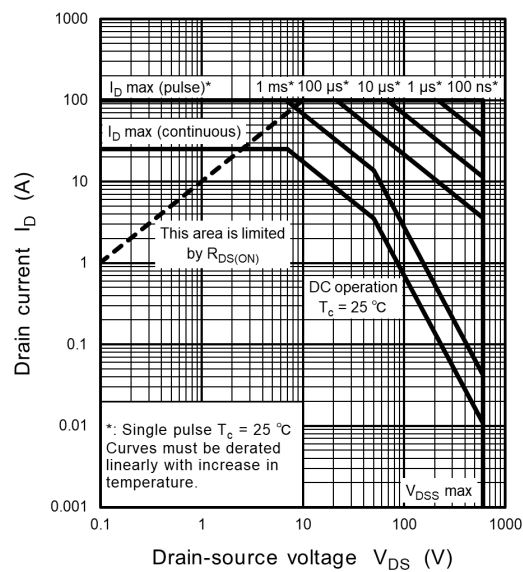


Fig. 8.17 $I_D - T_c$
(Guaranteed Maximum)



**Fig. 8.18 Safe Operating Area
(Guaranteed Maximum)**

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

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