

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74HC40102AP, TC74HC40102AF TC74HC40103AP, TC74HC40103AF

TC74HC40102AP/AF Dual BCD Programmable Down Counter

TC74HC40103AP/AF 8-Bit Binary Programmable Down Counter

The TC74HC40102A and TC74HC40103A are high speed CMOS PROGRAMMABLE DOWN COUNTERS fabricated with silicon gate C²MOS technology.

They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The output terminal ($\overline{CO/ZD}$) goes to an active low state when the down count reaches zero. Since the TC74HC40102A is designed as a BCD counter, programming up to 99 counts is possible. The TC74HC40103A, with its 8-bit binary construction, can be set to provide up to 255 counts.

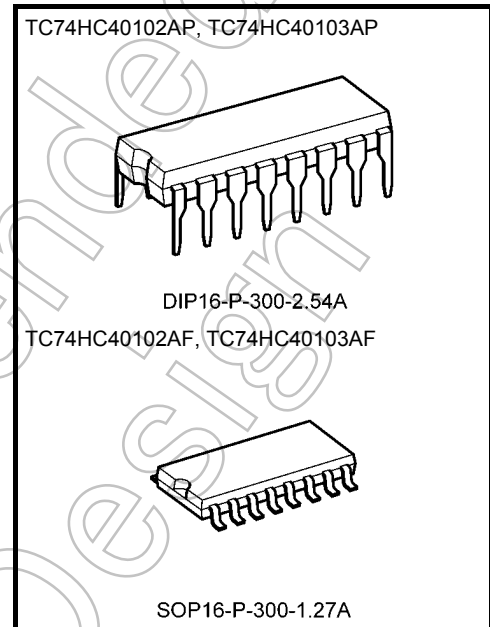
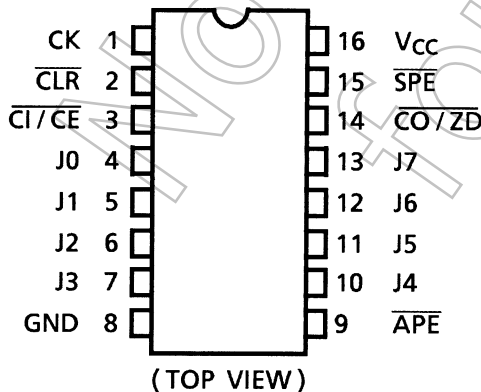
Both devices have Inhibit Clock ($\overline{CI/CE}$), Asynchronous Preset Control (\overline{APE}), Synchronous Preset (\overline{SPE}) and Clear Control (\overline{CLR}) inputs for setting the counter to the maximum counting mode.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

Features

- High speed: f_{max} 40 MHz (typ.) at $V_{CC} = 5$ V
- Low power dissipation: $I_{CC} = 4 \mu A$ (max) at $T_a = 25^\circ C$
- High noise immunity: $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (min)
- Output drive capability: 10 LSTTL loads
- Symmetrical output impedance: $|I_{OH}| = I_{OL} = 4$ mA (min)
- Balanced propagation delays: $t_{pLH} \approx t_{pHL}$
- Wide operating voltage range: $V_{CC} (opr) = 2$ to 6 V
- Pin and function compatible with 40102B, 40103B

Pin Assignment

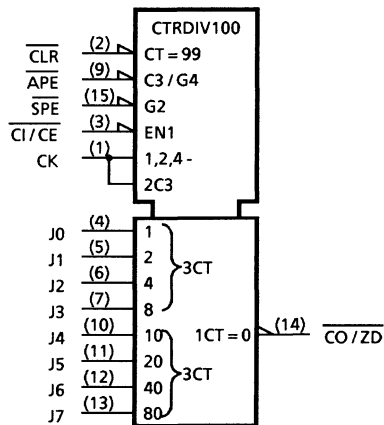


Weight	
DIP16-P-300-2.54A	: 1.00 g (typ.)
SOP16-P-300-1.27A	: 0.18 g (typ.)

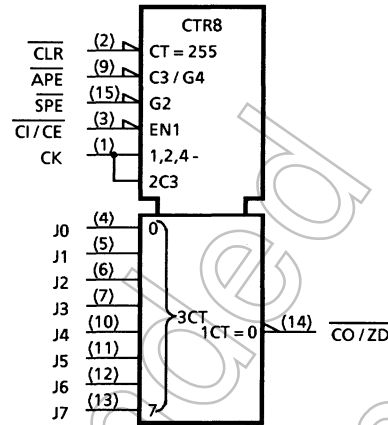
Start of commercial production
1988-11

IEC Logic Symbol

TC74HC40102A



TC74HC40103A



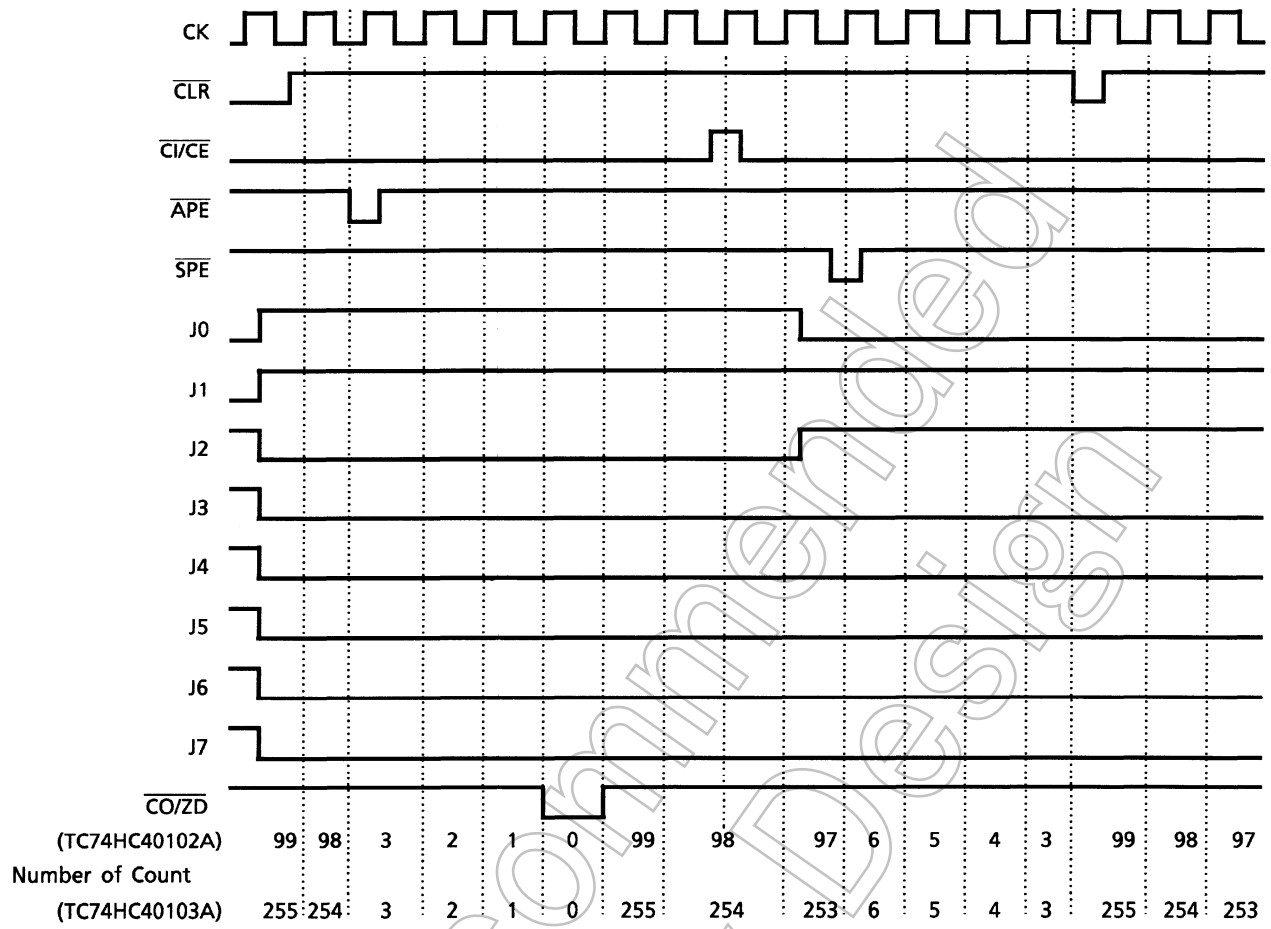
Truth Table

Control Inputs				Mode	Functional Description
CLR	APE	SPE	CI/CE		
H	H	H	H	Count Inhibit	Count is inhibited regardless of other inputs.
H	H	H	L	Regular Count	Down count on the rising edge of CK
H	H	L	X	Synchronous Preset	Input data is preset on the rising edge of CK
H	L	X	X	Asynchronous Preset	Input data is asynchronously preset to CK
L	X	X	X	Clear	Counter is set to maximum count.

X: Don't care

Maximum count: TC74HC40102A "99", TC74HC40103A "255"

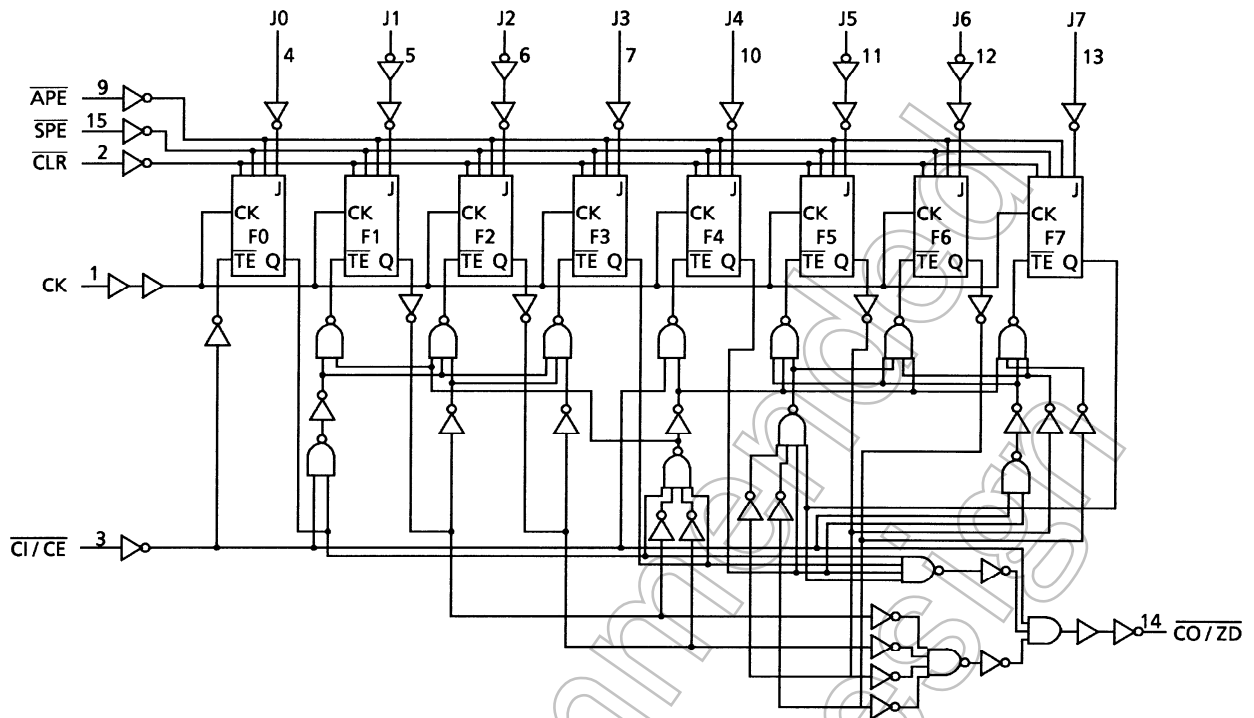
Timing Chart



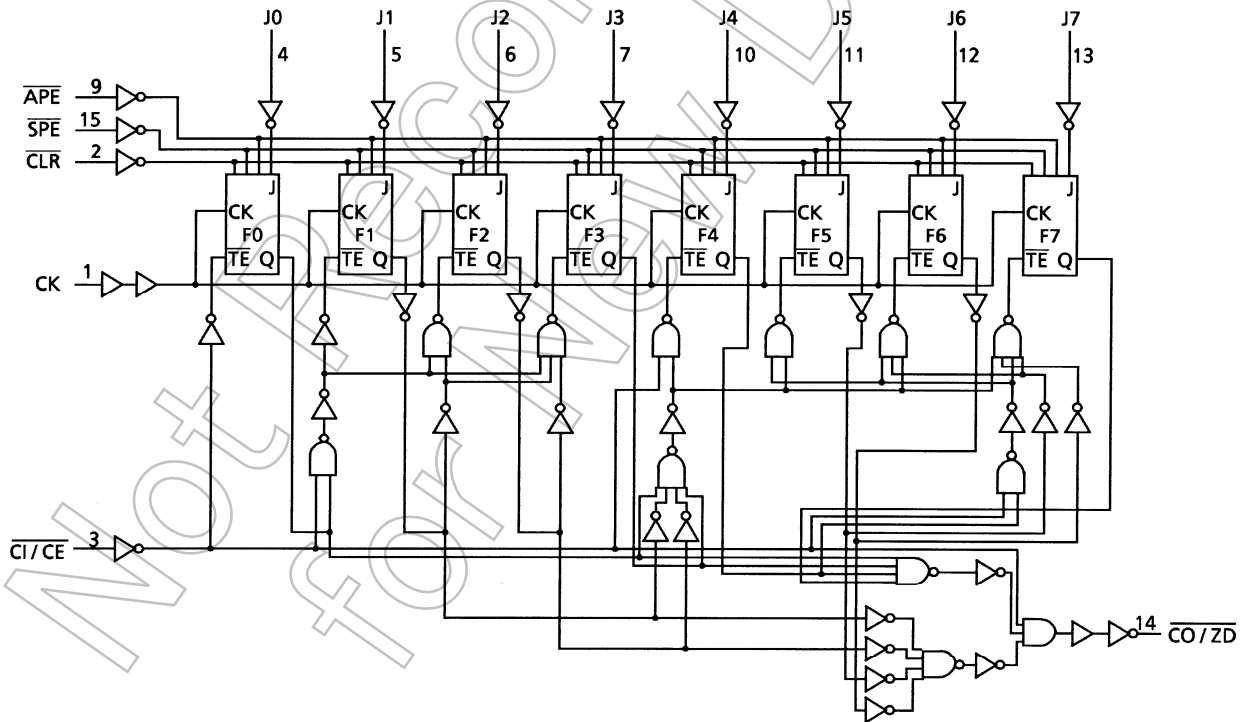
Not Recommended for New

System Diagram

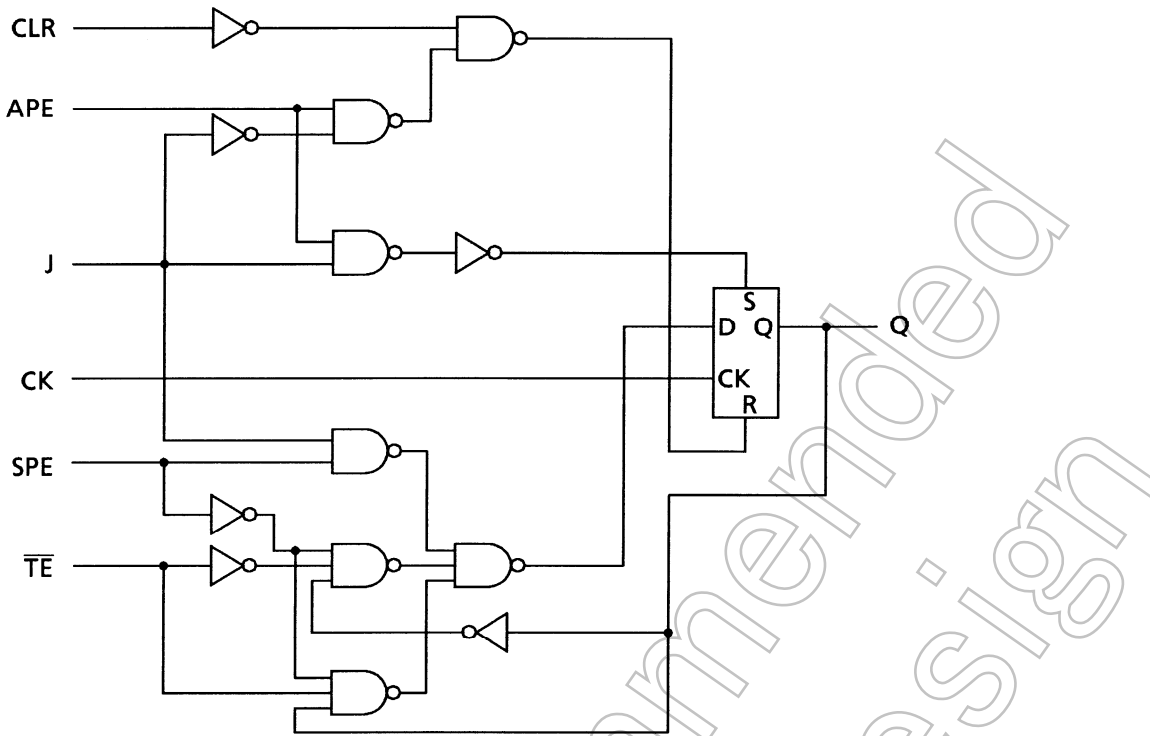
TC74HC40102A



TC74HC40103A



Logic Diagram



Inputs						Output
CLR	APE	SPE	J	\overline{TE}	CK	Q
H	X	X	X	X	X	L
L	H	H	H	H	X	H
L	H	H	L	H	X	L
L	L	H	H	X	\uparrow	H
L	L	H	L	X	\uparrow	L
L	L	L	X	L	\uparrow	\overline{Qn}
L	L	L	X	L	\downarrow	Qn
L	L	L	X	H	X	Qn

Function Description

The TC74HC40102A and TC74HC40103A are 8-stage presetable synchronous down counters.

Carry Out/Zero Detect ($\overline{CO/ZD}$) is output at the "L" level for the period of 1 bit when the readout becomes "0". The TC74HC40102A adopts binary coded decimal notation, making setting up to 99 counts possible. While the TC74HC40103A adopts 8-bit binary counter and can set up to 255 counts.

Count Operation

At the "H" level of control input of \overline{CLR} , \overline{SPE} and \overline{APE} , the counter carries out down count operation one by one at the rise of pulse given to CK input. Count operation can be inhibited by setting Carry Input/clock Enable ($\overline{CI/CE}$) to the "H" level.

$\overline{CO/ZD}$ is output at the "L" level when the readout becomes "0", but is not output even if the readout becomes "0" when $\overline{CI/CE}$ is at the "H" level, thus maintaining the "H" level.

Synchronous cascade operation can be carried out by using $\overline{CI/CE}$ input and $\overline{CO/ZD}$ output.

The contents of count jump to maximum count (99 for the TC74HC40102A and 255 for the TC74HC40103A) if clock is given when the readout is "0". Therefore, operation of 100-frequency division and that of 256-frequency division are carried out for the TC74HC40102A and TC74HC40103A, respectively, when clock input alone is given without various kinds of preset operation.

Preset Operation and Reset Operation

When Clear ($\overline{\text{CLR}}$) input is set to the “L” level, the readout is set to the maximum count independently of other inputs. When Asynchronous Preset Enable ($\overline{\text{APE}}$) input is set to the “L” level, readouts given on J0 to J7 can be preset asynchronously to counter independently of inputs other than $\overline{\text{CLR}}$ input. When Synchronous Preset Enable ($\overline{\text{SPE}}$) is set to the “L” level, the readouts given on J0 to J7 can be preset to counter synchronously with rise of clock.

As to these operation modes, refer to the truth table.

Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	-0.5 to 7	V
DC input voltage	V_{IN}	-0.5 to $V_{CC} + 0.5$	V
DC output voltage	V_{OUT}	-0.5 to $V_{CC} + 0.5$	V
Input diode current	I_{IK}	±20	mA
Output diode current	I_{OK}	±20	mA
DC output current	I_{OUT}	±25	mA
DC V_{CC} /ground current	I_{CC}	±50	mA
Power dissipation	P_D	500 (DIP) (Note 2)/180 (SOP)	mW
Storage temperature	T_{stg}	-65 to 150	°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: 500 mW in the range of $T_a = -40$ to 65°C . From $T_a = 65$ to 85°C a derating factor of -10 mW/°C shall be applied until 300 mW.

Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	2 to 6	V
Input voltage	V_{IN}	0 to V_{CC}	V
Output voltage	V_{OUT}	0 to V_{CC}	V
Operating temperature	T_{opr}	-40 to 85	°C
Input rise and fall time	t_r, t_f	0 to 1000 ($V_{CC} = 2.0$ V) 0 to 500 ($V_{CC} = 4.5$ V) 0 to 400 ($V_{CC} = 6.0$ V)	ns

Note: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either V_{CC} or GND.

Electrical Characteristics

DC Characteristics

Characteristics	Symbol	Test Condition	Ta = 25°C			Ta = -40 to 85°C		Unit		
			V _{CC} (V)	Min	Typ.	Max	Min		Max	
High-level input voltage	V _{IH}	—	2.0	1.50	—	—	1.50	—	V	
			4.5	3.15	—	—	3.15	—		
			6.0	4.20	—	—	4.20	—		
Low-level input voltage	V _{IL}	—	2.0	—	—	0.50	—	0.50	V	
			4.5	—	—	1.35	—	1.35		
			6.0	—	—	1.80	—	1.80		
High-level output voltage	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -20 μA	2.0	1.9	2.0	—	1.9	—	V
				4.5	4.4	4.5	—	4.4	—	
				6.0	5.9	6.0	—	5.9	—	
			I _{OH} = -4 mA	4.5	4.18	4.31	—	4.13	—	
				6.0	5.68	5.80	—	5.63	—	
Low-level output voltage	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 20 μA	2.0	—	0.0	0.1	—	0.1	V
				4.5	—	0.0	0.1	—	0.1	
				6.0	—	0.0	0.1	—	0.1	
			I _{OL} = 4 mA	4.5	—	0.17	0.26	—	0.33	
				6.0	—	0.18	0.26	—	0.33	
Input leakage current	I _{IN}	V _{IN} = V _{CC} or GND	6.0	—	—	±0.1	—	±1.0	μA	
Quiescent supply current	I _{CC}	V _{IN} = V _{CC} or GND	6.0	—	—	4.0	—	40.0	μA	

AC Characteristics (C_L = 15 pF, V_{CC} = 5 V, Ta = 25°C, input: t_r = t_f = 6 ns)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Output transition time	t _{TLH}	—	—	4	8	ns
	t _{THL}					
Propagation delay time (CK - CO/ZD)	t _{pLH}	—	—	25	43	ns
	t _{pHL}					
Propagation delay time (APE - CO/ZD)	t _{pLH}	—	—	25	49	ns
	t _{pHL}					
Propagation delay time (CI/CE - CO/ZD)	t _{pLH}	—	—	10	19	ns
	t _{pHL}					
Propagation delay time (CLR - CO/ZD)	t _{pLH}	—	—	24	36	ns
Maximum clock frequency	f _{max}	—	23	40	—	MHz

AC Characteristics (C_L = 50 pF, input: t_r = t_f = 6 ns)

Characteristics	Symbol	Test Condition	V _{CC} (V)	Ta = 25°C			Ta = -40 to 85°C		Unit
				Min	Typ.	Max	Min	Max	
Output transition time	t _{TLH} t _{THL}	—	2.0	—	30	75	—	95	ns
			4.5	—	8	15	—	19	
			6.0	—	7	13	—	16	
Propagation delay time (CK - $\overline{CO/ZO}$)	t _{pLH} t _{pHL}	—	2.0	—	95	245	—	305	ns
			4.5	—	28	49	—	61	
			6.0	—	22	42	—	52	
Propagation delay time ($\overline{APE} - \overline{CO/ZO}$)	t _{pLH} t _{pHL}	—	2.0	—	100	300	—	375	ns
			4.5	—	30	60	—	75	
			6.0	—	25	51	—	64	
Propagation delay time ($\overline{CI/CE} - \overline{CO/ZO}$)	t _{pLH} t _{pHL}	—	2.0	—	38	115	—	145	ns
			4.5	—	13	23	—	29	
			6.0	—	11	20	—	25	
Propagation delay time ($\overline{CLR} - \overline{CO/ZO}$)	t _{pLH}	—	2.0	—	85	240	—	300	ns
			4.5	—	28	48	—	60	
			6.0	—	23	41	—	51	
Maximum clock frequency	f _{max}	—	2.0	4	12	—	3	—	ns
			4.5	20	36	—	16	—	
			6.0	24	42	—	19	—	
Input capacitance	C _{IN}	—	—	5	10	—	10	pF	
Power dissipation capacitance	C _{PD} (Note)	—	—	48	—	—	—	pF	

Note: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

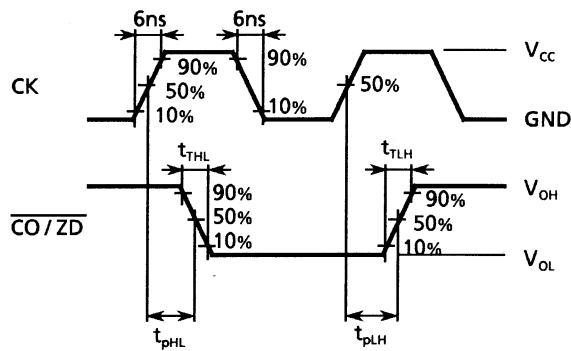
$$I_{CC}(\text{opr}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

Timing Requirements (input: $t_r = t_f = 6 \text{ ns}$)

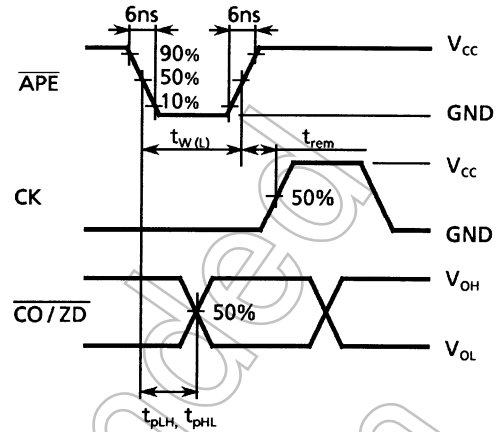
Characteristics	Symbol	Test Condition	Ta = 25°C		Ta = -40 to 85°C	Unit	
			VCC (V)	Typ.	Limit		Limit
Minimum pulse width (CK)	$t_W (H)$ $t_W (L)$	—	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum pulse width ($\overline{\text{CLR}}$, $\overline{\text{APE}}$)	$t_W (L)$	—	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum set-up time ($\overline{\text{SPE}}$ -CK)	t_s	—	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum set-up time ($\overline{\text{CI/CE}}$ -CK)	t_s	—	2.0	—	150	190	ns
			4.5	—	30	38	
			6.0	—	26	32	
Minimum set-up time (Jn-CK)	t_s	—	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum set-up time (Jn- $\overline{\text{APE}}$)	t_s	—	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum hold time ($\overline{\text{SPE}}$ -CK)	t_h	—	2.0	—	0	0	ns
			4.5	—	0	0	
			6.0	—	0	0	
Minimum hold time ($\overline{\text{CI/CE}}$ -CK)	t_h	—	2.0	—	0	0	ns
			4.5	—	0	0	
			6.0	—	0	0	
Minimum hold time (Jn-CK)	t_h	—	2.0	—	0	0	ns
			4.5	—	0	0	
			6.0	—	0	0	
Minimum hold time (Jn- $\overline{\text{APE}}$)	t_h	—	2.0	—	0	0	ns
			4.5	—	0	0	
			6.0	—	0	0	
Minimum removal time ($\overline{\text{CLR}}$, $\overline{\text{APE}}$)	t_{rem}	—	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Clock frequency	f	—	2.0	—	4	3	MHz
			4.5	—	20	16	
			6.0	—	24	19	

Switching Characteristics Test Waveform (Note)

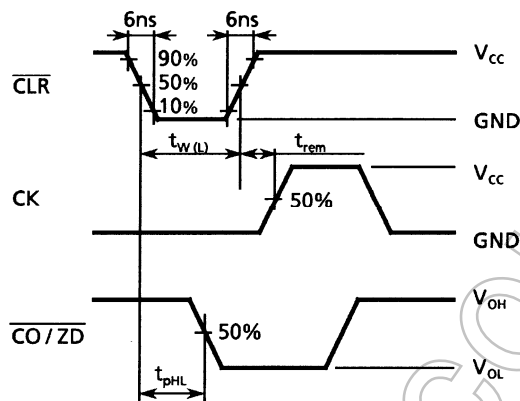
Waveform 1



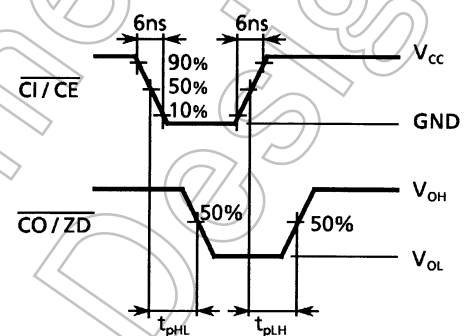
Waveform 2



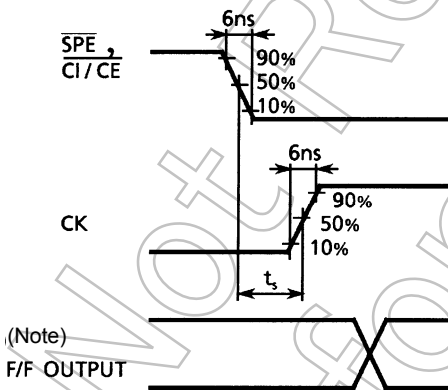
Waveform 3



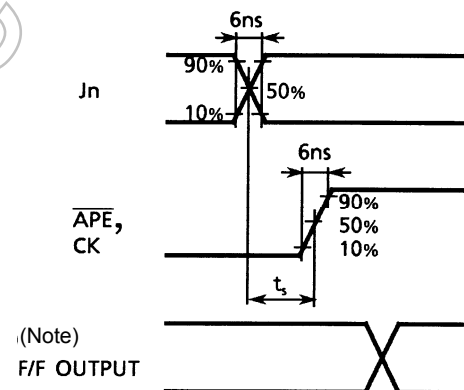
Waveform 4



Waveform 5



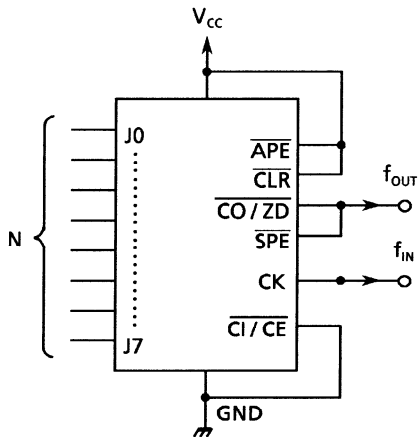
Waveform 6



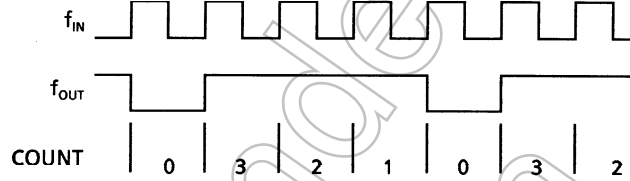
Note: F/F output is internal signal of IC

Example of Typical Application

Programmable Divide-by-N Counter

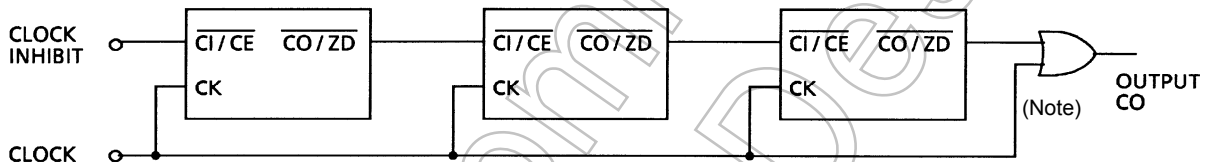


- $f_{OUT} = \frac{f_{IN}}{N + 1}$
- Timing chart when N="3"
(J0, J1 = V_{CC}, J2 to J7 = GND)



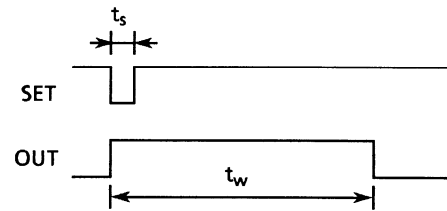
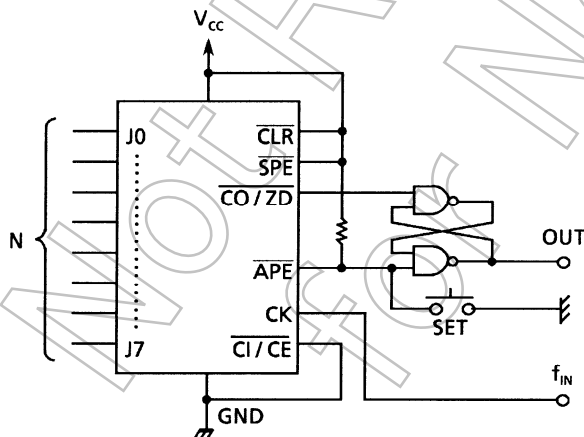
- TC74HC40102A 1/2 to 1/100 are dividable.
- TC74HC40103A 1/2 to 1/256 are dividable.

Parallel Carry Cascading (Note)



Note: At synchronous cascade connection, huzzerd occurs at CO output after its second stage when digit place changes, due to delay arrival. Therefore, take gate form TC74HC32A or the like, not form CO output at the rear stage directly.

Programmable Timer (Note)

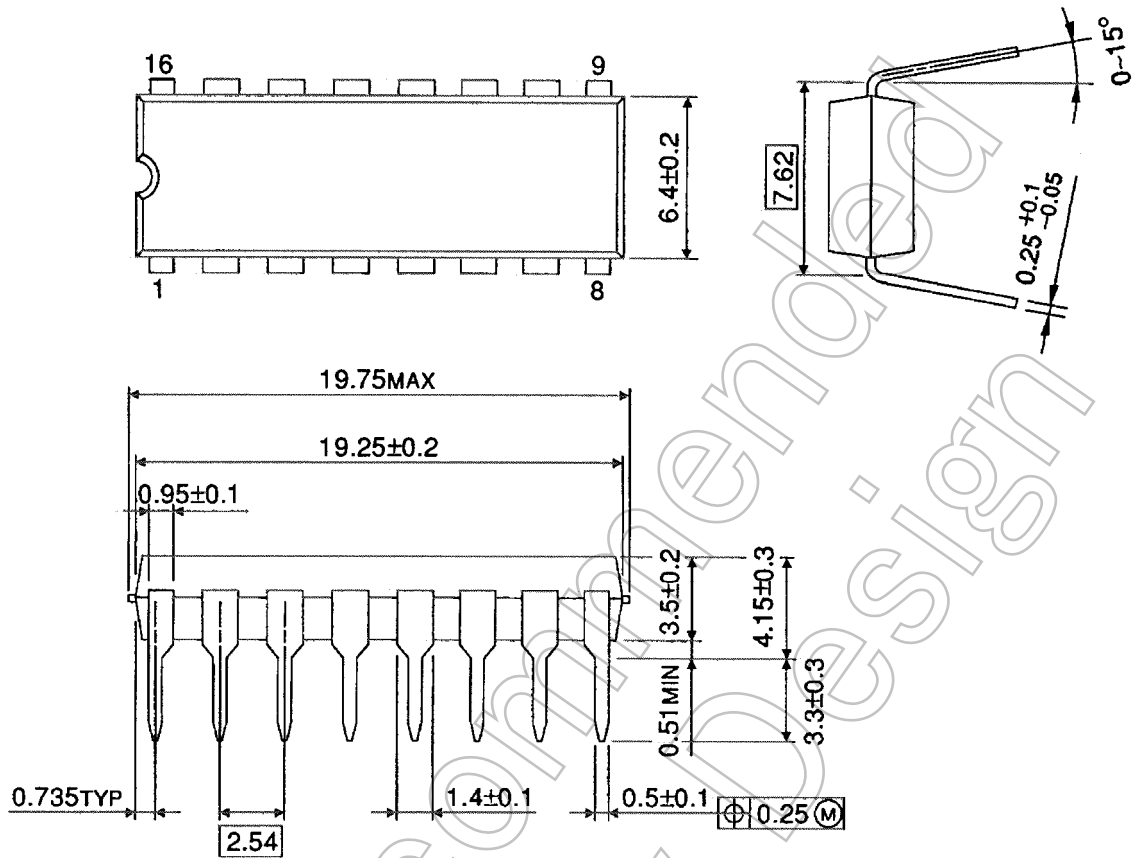


Note: The above formula dose not take into account the phase of ck input.
Therefore, the real pulse width is the distance between the above formula-1/f_{IN} to the above formula.

Package Dimensions

DIP16-P-300-2.54A

Unit : mm



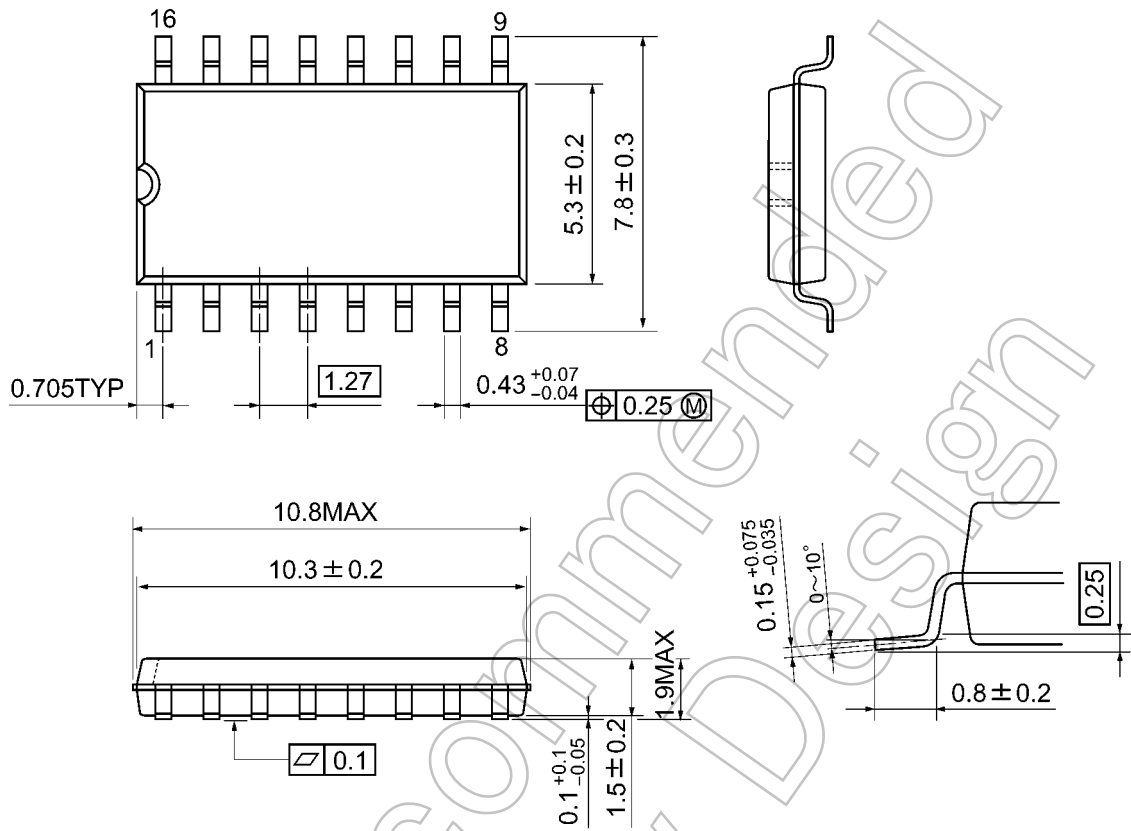
Weight: 1.00 g (typ.)

Not Recommended for New Design

Package Dimensions

SOP16-P-300-1.27A

Unit: mm



Weight: 0.18 g (typ.)

Not Recommended for New Design

RESTRICTIONS ON PRODUCT USE

- Toshiba Corporation, and its subsidiaries and affiliates (collectively "TOSHIBA"), reserve the right to make changes to the information in this document, and related hardware, software and systems (collectively "Product") without notice.
- This document and any information herein may not be reproduced without prior written permission from TOSHIBA. Even with TOSHIBA's written permission, reproduction is permissible only if reproduction is without alteration/omission.
- Though TOSHIBA works continually to improve Product's quality and reliability, Product can malfunction or fail. Customers are responsible for complying with safety standards and for providing adequate designs and safeguards for their hardware, software and systems which minimize risk and avoid situations in which a malfunction or failure of Product could cause loss of human life, bodily injury or damage to property, including data loss or corruption. Before customers use the Product, create designs including the Product, or incorporate the Product into their own applications, customers must also refer to and comply with (a) the latest versions of all relevant TOSHIBA information, including without limitation, this document, the specifications, the data sheets and application notes for Product and the precautions and conditions set forth in the "TOSHIBA Semiconductor Reliability Handbook" and (b) the instructions for the application with which the Product will be used with or for. Customers are solely responsible for all aspects of their own product design or applications, including but not limited to (a) determining the appropriateness of the use of this Product in such design or applications; (b) evaluating and determining the applicability of any information contained in this document, or in charts, diagrams, programs, algorithms, sample application circuits, or any other referenced documents; and (c) validating all operating parameters for such designs and applications. **TOSHIBA ASSUMES NO LIABILITY FOR CUSTOMERS' PRODUCT DESIGN OR APPLICATIONS.**
- **PRODUCT IS NEITHER INTENDED NOR WARRANTED FOR USE IN EQUIPMENTS OR SYSTEMS THAT REQUIRE EXTRAORDINARILY HIGH LEVELS OF QUALITY AND/OR RELIABILITY, AND/OR A MALFUNCTION OR FAILURE OF WHICH MAY CAUSE LOSS OF HUMAN LIFE, BODILY INJURY, SERIOUS PROPERTY DAMAGE AND/OR SERIOUS PUBLIC IMPACT ("UNINTENDED USE").** Except for specific applications as expressly stated in this document, Unintended Use includes, without limitation, equipment used in nuclear facilities, equipment used in the aerospace industry, medical equipment, equipment used for automobiles, trains, ships and other transportation, traffic signaling equipment, equipment used to control combustions or explosions, safety devices, elevators and escalators, devices related to electric power, and equipment used in finance-related fields. **IF YOU USE PRODUCT FOR UNINTENDED USE, TOSHIBA ASSUMES NO LIABILITY FOR PRODUCT.** For details, please contact your TOSHIBA sales representative.
- Do not disassemble, analyze, reverse-engineer, alter, modify, translate or copy Product, whether in whole or in part.
- Product shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable laws or regulations.
- The information contained herein is presented only as guidance for Product use. No responsibility is assumed by TOSHIBA for any infringement of patents or any other intellectual property rights of third parties that may result from the use of Product. No license to any intellectual property right is granted by this document, whether express or implied, by estoppel or otherwise.
- **ABSENT A WRITTEN SIGNED AGREEMENT, EXCEPT AS PROVIDED IN THE RELEVANT TERMS AND CONDITIONS OF SALE FOR PRODUCT, AND TO THE MAXIMUM EXTENT ALLOWABLE BY LAW, TOSHIBA (1) ASSUMES NO LIABILITY WHATSOEVER, INCLUDING WITHOUT LIMITATION, INDIRECT, CONSEQUENTIAL, SPECIAL, OR INCIDENTAL DAMAGES OR LOSS, INCLUDING WITHOUT LIMITATION, LOSS OF PROFITS, LOSS OF OPPORTUNITIES, BUSINESS INTERRUPTION AND LOSS OF DATA, AND (2) DISCLAIMS ANY AND ALL EXPRESS OR IMPLIED WARRANTIES AND CONDITIONS RELATED TO SALE, USE OF PRODUCT, OR INFORMATION, INCLUDING WARRANTIES OR CONDITIONS OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, ACCURACY OF INFORMATION, OR NONINFRINGEMENT.**
- Do not use or otherwise make available Product or related software or technology for any military purposes, including without limitation, for the design, development, use, stockpiling or manufacturing of nuclear, chemical, or biological weapons or missile technology products (mass destruction weapons). Product and related software and technology may be controlled under the applicable export laws and regulations including, without limitation, the Japanese Foreign Exchange and Foreign Trade Law and the U.S. Export Administration Regulations. Export and re-export of Product or related software or technology are strictly prohibited except in compliance with all applicable export laws and regulations.
- Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS compatibility of Product. Please use Product in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. **TOSHIBA ASSUMES NO LIABILITY FOR DAMAGES OR LOSSES OCCURRING AS A RESULT OF NONCOMPLIANCE WITH APPLICABLE LAWS AND REGULATIONS.**