TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74HC40105AP, TC74HC40105AF

4 Bit × 16 Word FIFO Register

The TC74HC40105A is a high speed CMOS 4 bit × 16 word first-in, first-out (FIFO) Strage Register fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation while maintaining the CMOS low power dissipation.

The device is capable of handling 16 four-bit words and it is possible to handle the input and output data at different shifting rates.

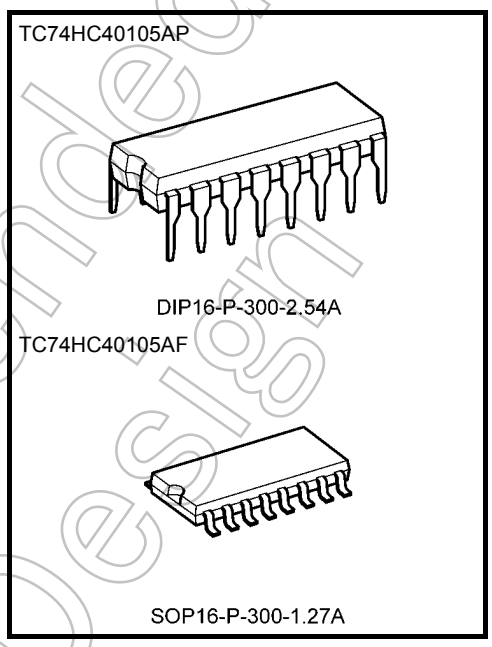
When the DATA-IN-READY (DIR) is high, data is written into the registers by a low to high transition of the SHIFT IN (SI) input. And when DATA-OUT-READY (DOR) is high, data is read out of the registers by a high to low transition of the $\overline{\text{SHIFT OUT}}$ ($\overline{\text{SO}}$) input.

If the MASTER RESET (MR) is high, the DIR goes high and DOR goes low. The data in the internal registers are not changed but are declared invalid.

The TC74HC40105A can be cascaded to form longer registers or wider words.

The DATA OUTPUTs (Qn) are 3-State Outputs. When $\overline{\text{OUTPUT ENABLE}}$ ($\overline{\text{OE}}$) is held high, the Qn's are in high impedance state.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.



Weight
DIP16-P-300-2.54A : 1.00 g (typ.)
SOP16-P-300-1.27A : 0.18 g (typ.)

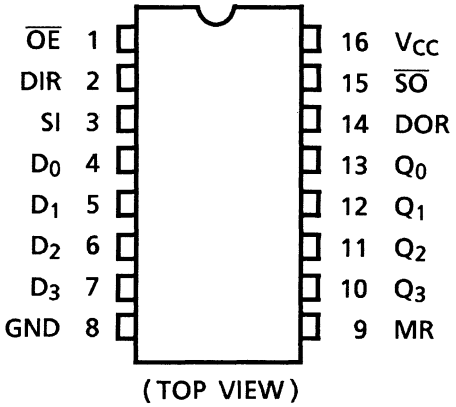
Features

- High speed: f_{max} 25 MHz (typ.) at V_{CC} = 5 V
- Low power dissipation: I_{CC} = 4 μA (max) at Ta = 25°C
- High noise immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC} (min)
- Output drive capability: 10 LSTTL loads for DIR, DOR
  15 LSTTL loads for Q0 to Q3
- Symmetrical output impedance: $|I_{OH}| = I_{OL}$ = 4 mA (min)
  for DIR, DOR
  $|I_{OH}| = I_{OL}$ = 6 mA (min)
  for Q0 to Q3
- Balanced propagation delays: $t_{pLH} \simeq t_{pHL}$
- Wide operating voltage range: V_{CC} (opr) = 2 to 6 V

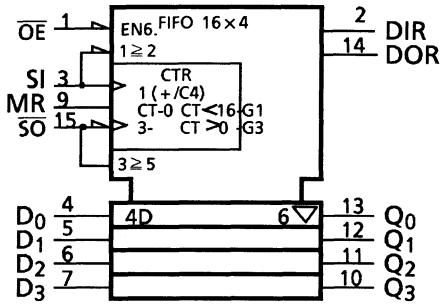
Not Recommended for New Design

Start of commercial production
1986-05

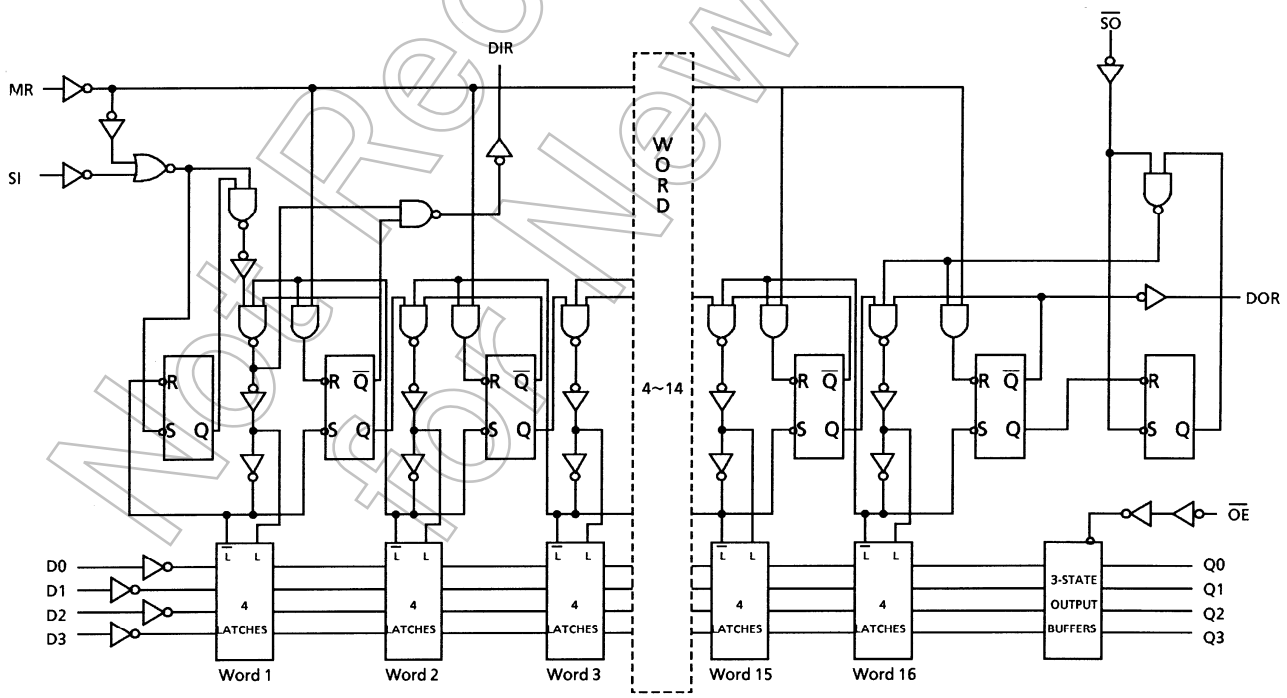
Pin Assignment



IEC Logic Symbol



System Diagram



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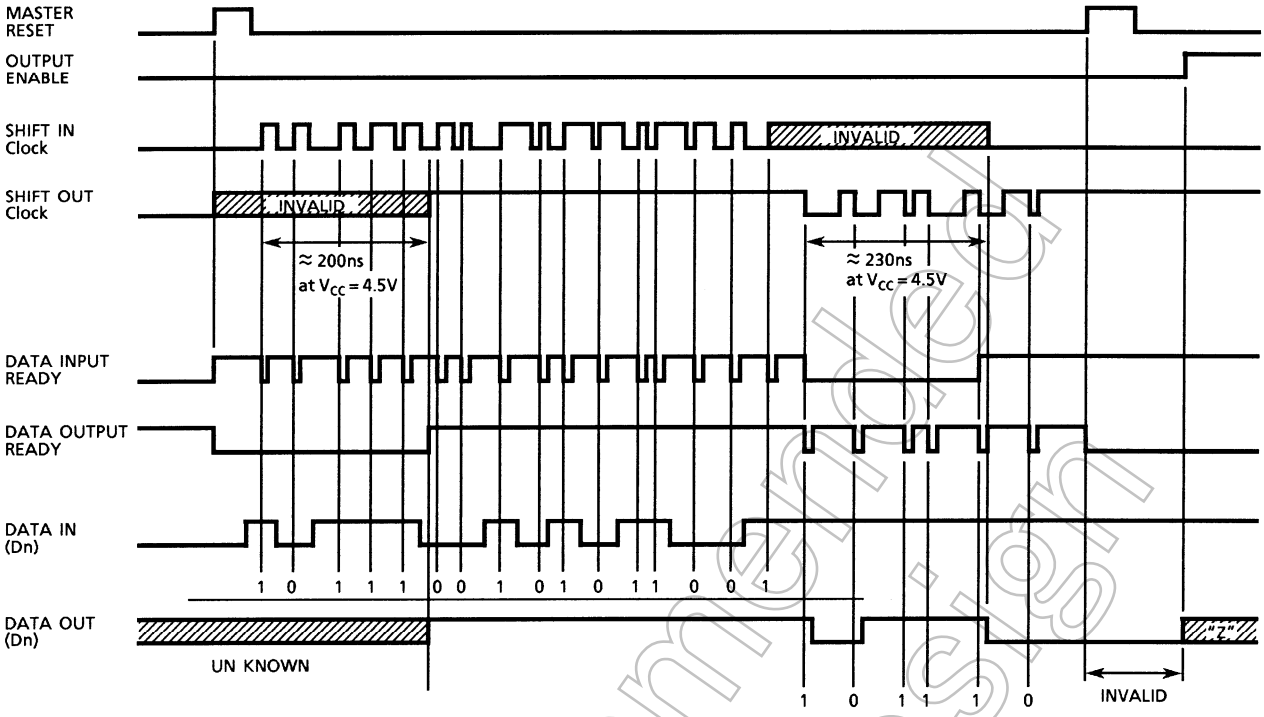
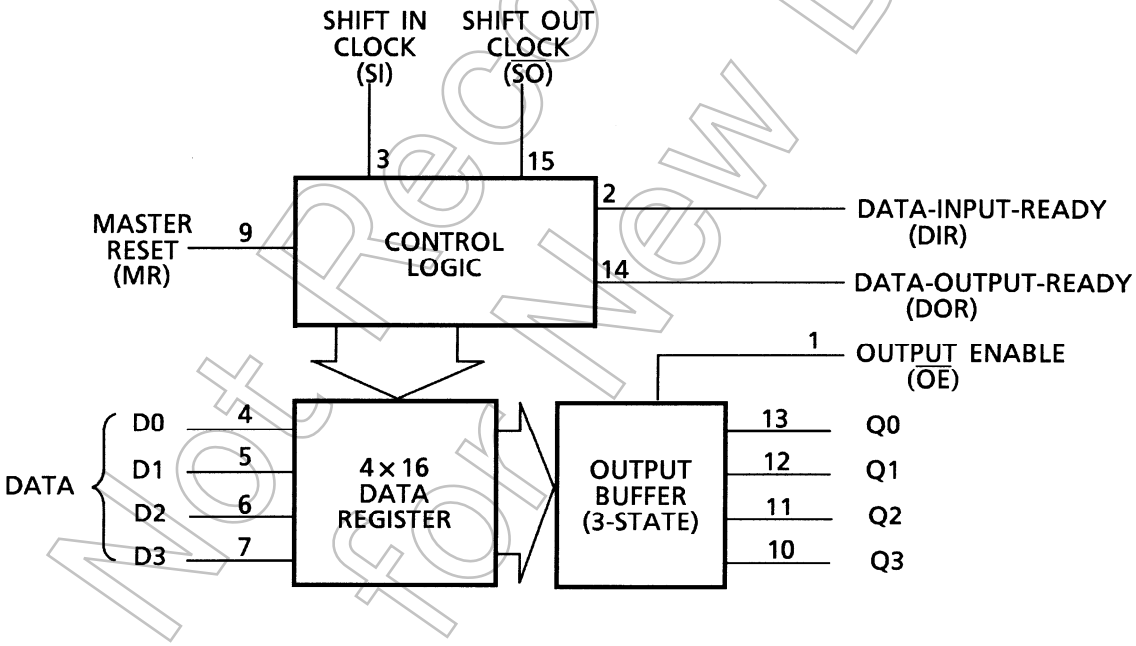
Timing Chart



Z: High impedance

Block Diagram



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Functional Description

(1) Writing data

Data can be written into the FIFO whenever DIR is high and a low to high transition occurs on the SI pin.

DIR will toggle momentarily until the data has been transferred to the second word register.

SI must be toggled before the next 4-bit word can be written. The first and subsequent words will automatically ripple to the output end of the device even if there is not a full 16 words of input data. When all 16 words are filled with data, DIR will go low and additional data cannot be written into the device.

(2) Reading data

When a data word appears in the sixteenth data register (just before the output buffer), DOR goes high and, if $\overline{OE}$ is low, data can be output on the high to low transition of $\overline{SO}$.

The data remaining in the registers now ripples to the next higher word position opening the first word position for new data. DIR goes high and additional data can be written in. During the output of data, DOR toggles momentarily after each read. When the data registers become empty, DOR goes low and $\overline{SO}$ is ignored.

(3) Master rest

When a high is input to MR, the internal control logic is initialized. This causes DIR to go high and DOR to go low. The contents of the data registers are not changed, but are invalid and will be written over when the first word is loaded.

(4) Cascading

The TC74HC40105A can be cascaded to form longer registers simply by connecting DOR of the first device to SI of the second and DIR of the second device to $\overline{SO}$ of the first. Additional devices may be cascaded by repeating the above. Of course, the Qn outputs of the first device must be connected to the Dn inputs of the second.

In this mode, an MR pulse must be applied after the supply voltage is turned on. For words wider than 4-bits, the DIR and DOR outputs from each FIFO must be ANDed respectively and the SI and $\overline{SO}$ inputs must each be paralleled.

Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	−0.5 to 7	V
DC input voltage	V_{IN}	−0.5 to V_{CC} + 0.5	V
DC output voltage	V_{OUT}	−0.5 to V_{CC} + 0.5	V
Input diode current	I_{IK}	±20	mA
Output diode current	I_{OK}	±20	mA
DC output current (DIR, DOR)	I_{OUT}	±25	mA
DC output current (Q0 to Q3)	I_{OUT}	±35	mA
DC V_{CC}/ground current	I_{CC}	±75	mA
Power dissipation	P_D	500 (DIP) (Note 2)/180 (SOP)	mW
Storage temperature	T_{stg}	−65 to 150	°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: 500 mW in the range of Ta = −40 to 65°C. From Ta = 65 to 85°C a derating factor of −10 mW/°C shall be applied until 300 mW.

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Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	2 to 6	V
Input voltage	V_{IN}	0 to V_{CC}	V
Output voltage	V_{OUT}	0 to V_{CC}	V
Operating temperature	T_{opr}	−40 to 85	°C
Input rise and fall time	t_r, t_f	0 to 1000 (V_{CC} = 2.0 V) 0 to 500 (V_{CC} = 4.5 V) 0 to 400 (V_{CC} = 6.0 V)	ns

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either V_{CC} or GND.

Electrical Characteristics

DC Characteristics

Characteristics	Symbol	Test Condition		V_{CC} (V)	Ta = 25°C Min	Ta = 25°C Typ.	Ta = 25°C Max	Ta = −40 to 85°C Min	Ta = −40 to 85°C Max	Unit
High-level input voltage	V_{IH}	—		2.0	1.50	—	—	1.50	—	V
				4.5	3.15	—	—	3.15	—	
				6.0	4.20	—	—	4.20	—	
Low-level input voltage	V_{IL}	—		2.0	—	—	0.50	—	0.50	V
				4.5	—	—	1.35	—	1.35	
				6.0	—	—	1.80	—	1.80	
High-level output voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −20 μA	2.0	1.9	2.0	—	1.9	—	V
				4.5	4.4	4.5	—	4.4	—	
				6.0	5.9	6.0	—	5.9	—	
		(DIR DOR)	I_{OH} = −4 mA	4.5	4.18	4.31	—	4.13	—	
			I_{OH} = −5.2 mA	6.0	5.68	5.80	—	5.63	—	
		(Q0 to Q3)	I_{OH} = −6 mA	4.5	4.18	4.31	—	4.13	—	
			I_{OH} = −7.8 mA	6.0	5.68	5.80	—	5.63	—	
Low-level output voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20 μA	2.0	—	0.0	0.1	—	0.1	V
				4.5	—	0.0	0.1	—	0.1	
				6.0	—	0.0	0.1	—	0.1	
		(DIR DOR)	I_{OL} = 4 mA	4.5	—	0.17	0.26	—	0.33	
			I_{OL} = 5.2 mA	6.0	—	0.18	0.26	—	0.33	
		(Q0 to Q3)	I_{OL} = 6 mA	4.5	—	0.17	0.26	—	0.33	
			I_{OL} = 7.8 mA	6.0	—	0.18	0.26	—	0.33	
3-state output off-state current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		6.0	—	—	±0.5	—	±5.0	μA
Input leakage current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	—	—	±0.1	—	±1.0	μA
Quiescent supply current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	—	—	4.0	—	40.0	μA

Not Recommended for New Design

Timing Requirements (input: $t_r = t_f = 6$ ns)

Characteristics	Symbol	Test Condition		Ta = 25°C		Ta = −40 to 85°C	Unit
			V_{CC} (V)	Typ.	Limit	Limit	
Minimum pulse width (SI)	$t_{W(L)}$ $t_{W(H)}$	—	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum pulse width ($\overline{SO}$)	$t_{W(L)}$ $t_{W(H)}$	—	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum pulse width (MR)	$t_{W(L)}$ $t_{W(H)}$	—	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum set-up time (DATA-SI)	t_s	—	2.0	—	0	0	ns
			4.5	—	0	0	
			6.0	—	0	0	
Minimum hold time (DATA-SI)	t_h	—	2.0	—	100	125	ns
			4.5	—	20	25	
			6.0	—	17	21	
Minimum removal time (MR-SI)	t_{rem}	—	2.0	—	50	65	ns
			4.5	—	10	13	
			6.0	—	9	11	
Clock frequency	f	—	2.0	—	3	2.4	MHz
			4.5	—	15	12	
			6.0	—	18	13	

AC Characteristics ($C_L = 15$ pF, $V_{CC} = 5$ V, Ta = 25°C, input: $t_r = t_f = 6$ ns)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Output transition time (DIR, DOR)	t_{TLH} t_{THL}	—	—	4	8	ns
Propagation delay time ($\overline{SO}$, MR-DOR)	t_{pHL}	—	—	22	39	ns
Propagation delay time ($\overline{SO}$-DIR)	t_{pLH}	—	—	242	365	ns
Propagation delay time (SI-DOR)	t_{pLH}	—	—	187	300	ns
Propagation delay time (SI-DIR)	t_{pHL}	—	—	22	35	ns
Propagation delay time (MR-DIR)	t_{pLH} t_{pHL}	—	—	25	39	ns

Not Recommended for New Design

AC Characteristics (input: $t_r = t_f = 6$ ns)

Characteristics	Symbol	Test Condition			Ta = 25°C			Ta = −40 to 85°C		Unit
			CL (pF)	V_{CC} (V)	Min	Typ.	Max	Min	Max	
Output transition time (Q0 to Q3)	t_{TLH} t_{THL}	—	50	2.0	—	21	60	—	75	ns
				4.5	—	7	12	—	15	
				6.0	—	6	10	—	13	
Output transition time (DIR, DOR)	t_{TLH} t_{THL}	—	50	2.0	—	24	75	—	95	ns
				4.5	—	8	15	—	19	
				6.0	—	7	13	—	16	
Propagation delay time ($\overline{SO}$, MR-DOR)	t_{pHL}	—	50	2.0	—	84	225	—	280	ns
				4.5	—	28	45	—	56	
				6.0	—	24	38	—	48	
Propagation delay time ($\overline{SO}$-DIR)	t_{pLH}	—	50	2.0	—	798	2000	—	2500	ns
				4.5	—	266	400	—	500	
				6.0	—	226	340	—	425	
Propagation delay time (SI-DOR)	t_{pLH}	—	50	2.0	—	624	1650	—	2060	ns
				4.5	—	208	330	—	412	
				6.0	—	177	280	—	350	
Propagation delay time (SI-DIR)	t_{pHL}	—	50	2.0	—	78	200	—	250	ns
				4.5	—	26	40	—	50	
				6.0	—	22	34	—	43	
Propagation delay time ($\overline{SO}$-Qn)	t_{pLH} t_{pHL}	—	50	2.0	—	156	400	—	500	ns
				4.5	—	52	80	—	100	
				6.0	—	44	68	—	85	
			150	2.0	—	171	440	—	550	
				4.5	—	57	88	—	110	
				6.0	—	48	75	—	94	
Propagation delay time (SI-Qn)	t_{pLH} t_{pHL}	—	50	2.0	—	612	1500	—	1875	ns
				4.5	—	204	300	—	375	
				6.0	—	173	255	—	319	
			150	2.0	—	627	1540	—	1925	
				4.5	—	209	308	—	385	
				6.0	—	178	262	—	327	
Propagation delay time (MR-DIR)	t_{pLH} t_{pHL}	—	50	2.0	—	87	225	—	280	ns
				4.5	—	29	45	—	56	
				6.0	—	25	38	—	48	
Output enable time	t_{pZL} t_{pZH}	$R_L = 1\ k\Omega$	50	2.0	—	45	125	—	155	ns
				4.5	—	15	25	—	31	
				6.0	—	13	21	—	26	
			150	2.0	—	60	165	—	205	
				4.5	—	20	33	—	41	
				6.0	—	17	28	—	35	
Output disable time	t_{pLZ} t_{pHZ}	$R_L = 1\ k\Omega$	50	2.0	—	32	125	—	155	ns
				4.5	—	16	25	—	31	
				6.0	—	14	21	—	26	

Not Recommended for New Design

Characteristics	Symbol	Test Condition			Ta = 25°C			Ta = −40 to 85°C		Unit
			CL (pF)	V_{CC} (V)	Min	Typ.	Max	Min	Max	
Maximum clock frequency	f_{max}	—	50	2.0	3	7	—	2.4	—	MHz
				4.5	15	22	—	12	—	
				6.0	18	26	—	14	—	
			150	2.0	2.6	6	—	2	—	
				4.5	13	20	—	10	—	
				6.0	15	24	—	12	—	
Output pulse width (DIR)	$t_{w\ (H)}$ $t_{w\ (L)}$	—	50	2.0	—	95	—	—	—	ns
				4.5	—	25	—	—	—	
				6.0	—	21	—	—	—	
Output pulse width (DOR)	$t_{w\ (H)}$ $t_{w\ (L)}$	—	50	2.0	—	95	—	—	—	ns
				4.5	—	25	—	—	—	
				6.0	—	21	—	—	—	
Input capacitance	C_{IN}	—			—	5	10	—	10	pF
Output capacitance	C_{OUT}	—			—	10	—	—	—	pF
Power dissipation capacitance	C_{PD}	(Note)			—	300	—	—	—	pF

Note: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC}\ (opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

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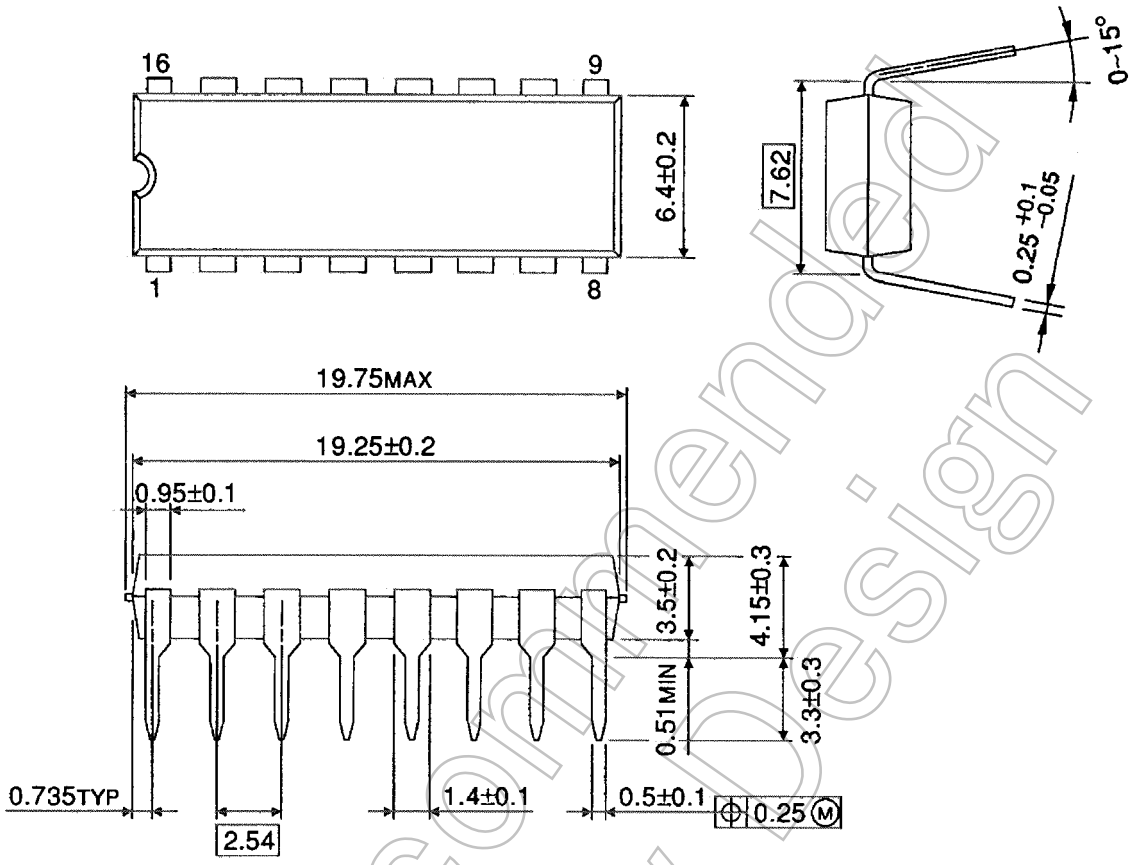
Package Dimensions

DIP16-P-300-2.54A Unit : mm



Weight: 1.00 g (typ.)

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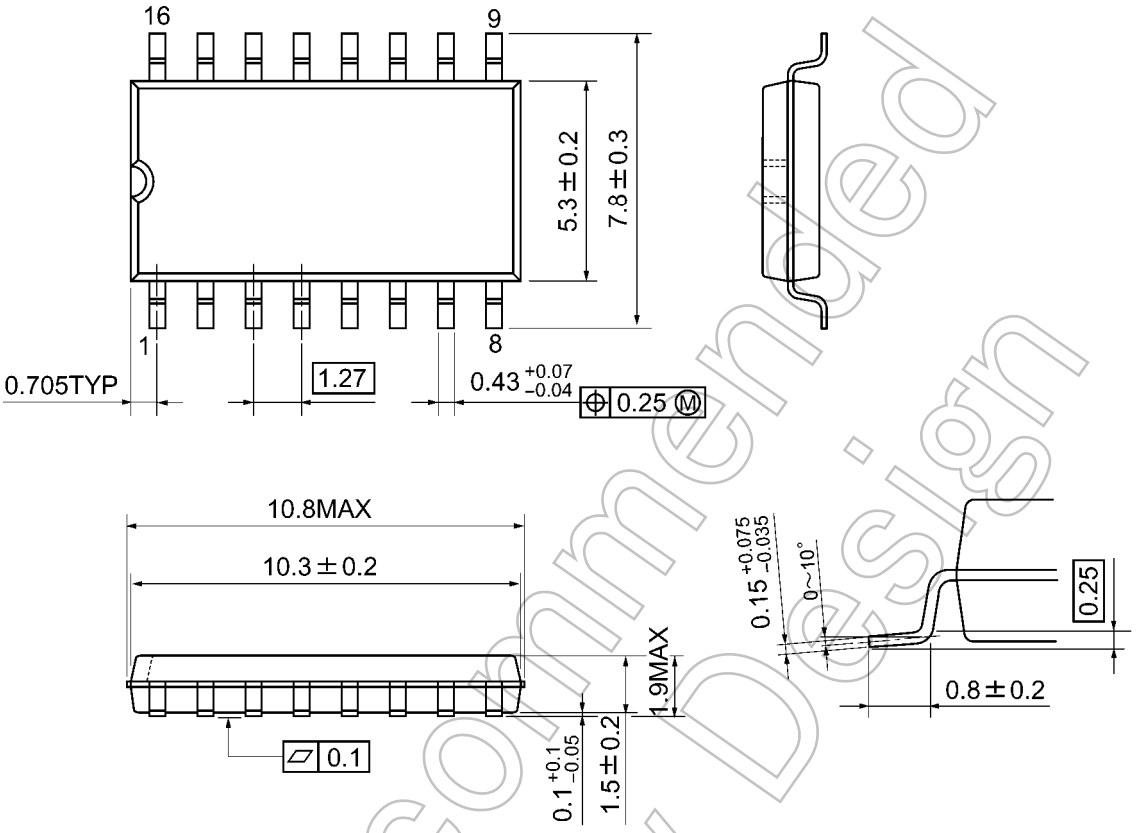
Package Dimensions

SOP16-P-300-1.27A Unit: mm



Weight: 0.18 g (typ.)

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