

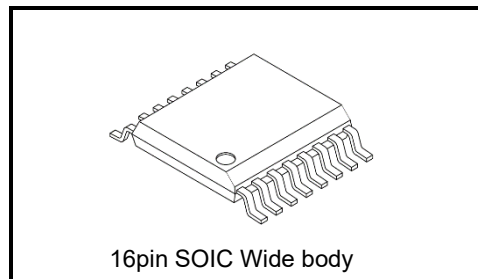
DCM341B01

Quad - channel High speed Logic for Automotive, Input Disable control, Default High output

1. Description

The DCM341B01 is a 16-pin SOIC Wide package default high-output, quad-channel high-speed digital isolator with the primary and secondary sides insulated and coupled by a magnetic coupling structure.

With a high isolation voltage of 5000 V_{rms}, it is suitable for control application applications such as in-vehicle communication line insulation.



16pin SOIC Wide body

Weight: 0.426 g (typ.)

2. Applications

- Battery Control in Automotive Equipment
- Fuel Battery Control in Automotive Equipment
- Application for Electrical Vehicle
- Data Converter Isolation
(Serial Peripheral Interface (SPI), etc.)

3. Features

- Data rate : 50 Mbps (Max)
- Default Output : High
- Control type : Input Disable
- Number of channels : 4 channels (Forward 3 : Revers 1)
- Suitable operating voltage : 3.3 V or 5 V
- Isolation voltage : 5000 V_{rms}
- Common-Mode Transient Immunity : ±100 kV/μs (Typ)
- Safety standards
 - AEC-Q100 (Grade1 qualified)
 - UL : UL1577 , File No. E519997
 - cUL: CSA Component Acceptance Service Notice No. E519997

Note: Typical test conditions: V_{DD1} =V_{DD2} = 3.3V or 5V , T_a = 25 °C; unless otherwise specified.

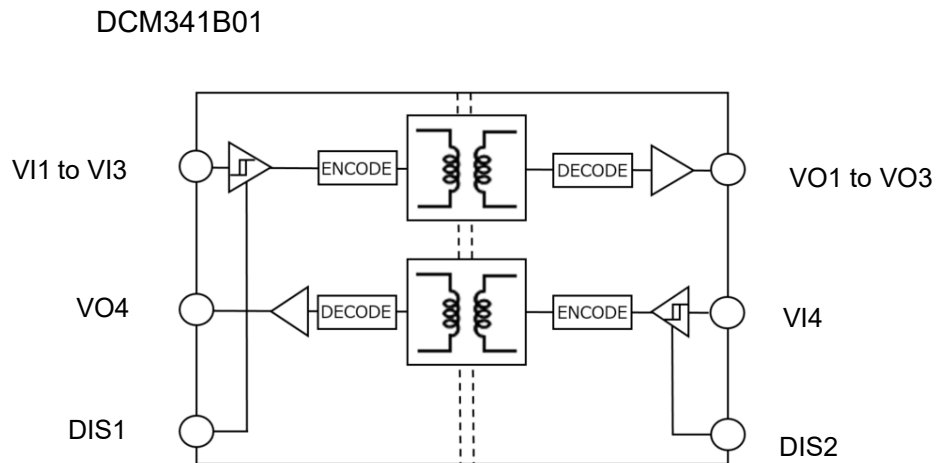
4. Mechanical Parameters

Table 4.1 Mechanical parameters

| Characteristics | Symbol | unit | Unit |
|---------------------------------|--------|-----------|------|
| Creepage distances | CPG | 7.6 (Min) | mm |
| Clearance distances | CLR | 8 (Min) | mm |
| Distance Through the Insulation | DTI | 17 | μm |

Start of commercial production
2024-11

5. Block Diagram



Note: Some of the functional blocks, circuits or constants labels in the block diagram may have been omitted or simplified for clarity.

Figure 5.1 Block Diagram

6. Pin Assignments

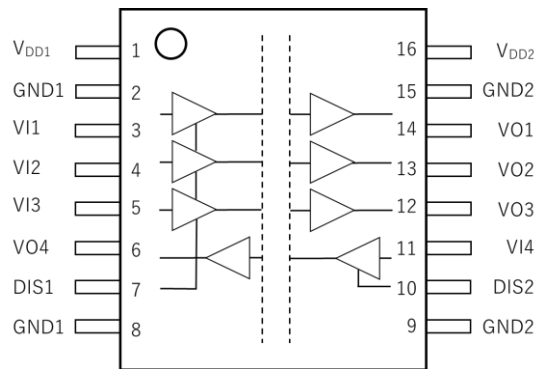


Figure 6.1 Pin Assignments (top view)

7. Pin Description

Table 7.1 Pin Description

| Pin No | Pin name | I/O | Description |
|--------|------------------|-----|--------------------------------------|
| 1 | V _{DD1} | — | Power Supply, side 1 |
| 2 | GND1 | — | GND connection for VDD1 , side 1 |
| 3 | VI1 | IN | Logic Input, Channel1 |
| 4 | VI2 | IN | Logic Input, Channel2 |
| 5 | VI3 | IN | Logic Input, Channel3 |
| 6 | VO4 | OUT | Logic Output, Channel4 |
| 7 | DIS1 | IN | Ch1 to Ch3 Input disable control pin |
| 8 | GND1 | — | GND connection for VDD1, side 1 |
| 9 | GND2 | — | GND connection for VDD2, side 2 |
| 10 | DIS2 | IN | Ch4 Input disable control pin |
| 11 | VI4 | IN | Logic Input, Channel4 |
| 12 | VO3 | OUT | Logic Output, Channel3 |
| 13 | VO2 | OUT | Logic Output, Channel2 |
| 14 | VO1 | OUT | Logic Output, Channel1 |
| 15 | GND2 | — | GND connection for VDD2, side 2 |
| 16 | V _{DD2} | — | Power Supply, side 2 |

8. Functional Description

8.1. Specifications of External Components

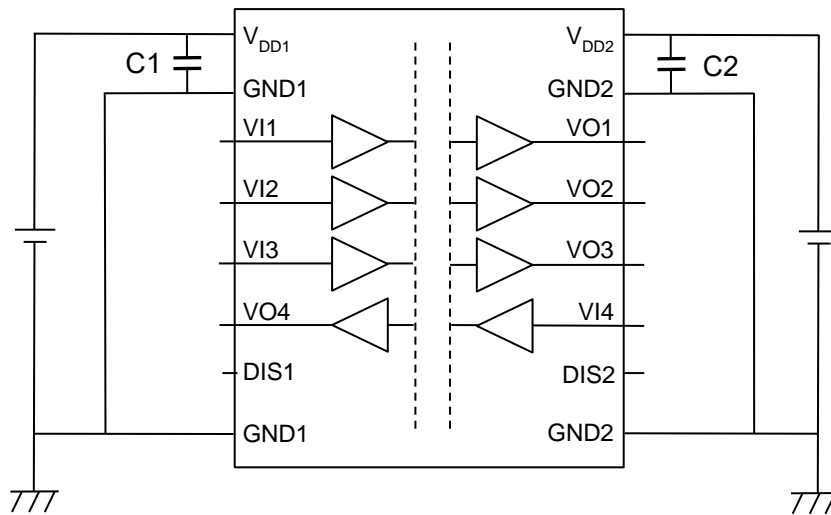


Figure 8.1 Pin Assignments (top view)

Table 8.1 External component specification (Note)

| Component Name | Recommended Value | Pin | Description |
|----------------|-------------------|------------------|-------------|
| C1 | 0.1μF | V _{DD1} | — |
| C2 | 0.1μF | V _{DD2} | — |

Note: Use Ceramic capacitors (C1,C2) with good high frequency characteristics.

Note: Ceramic capacitors (C1,C2) should be connected between pin 1 (V_{DD1}) and pin 2 (GND1) for V_{DD1} and between pin 16 (V_{DD2}) and pin 15 (GND2) for V_{DD2}, and should be the layout on the IC as close as possible (less than 10mm).

Otherwise, the IC may not switch properly.

8.2. IC Startup Procedure

8.2.1. Input Disable

Input signal Enable / Disable control is possible by controlling pin 7 (DIS1 terminal) and pin 10 (DIS2 terminal) to High or Low.

To enable Input, set pin 7 (DIS1 pin) and pin 10 (DIS2 pin) to High or OPEN.

By setting pin 7 (DIS1 pin) to Low, VI1 to VI3 can be disabled, and by setting pin 10 (DIS2 pin) to Low, VI4 can be disabled.

Table 8.2 Input Disable control pin Functional Description (Note)

| | V _{DDI} Input side V _{DD} | V _{DDO} Output side V _{DD} | DIS Pin (DIS1, DIS2) | Input (VI1 to VI4) | Output (VO1 to VO4) | State Description |
|---|--|---|-------------------------|-----------------------|------------------------|---|
| 1 | PU | PU | Low or OPEN | Low | Low | Normal Operation |
| 2 | | | | High | High | |
| 3 | | | | OPEN | High | Default mode |
| 4 | PU | PU | High | Undetermined | High | Default mode (Input disable mode) |
| 5 | PU | PD | Don't care | Undetermined | Undetermined | When V _{DDO} is unpowered, a channel output is undetermined. |
| 6 | PD | PU | Undetermined | Undetermined | Low | Default mode |
| 7 | PD | PD | Undetermined | Undetermined | Undetermined | When V _{DDO} is unpowered, a channel output is undetermined. |

Note: PU = Powered Up (V_{DD} ≥ 2.25 V) , PD = Powered Down (V_{DD} ≤ 1.7 V)

Note: V_{DDI} = Input-side V_{DD}, V_{DDO} = Output-side V_{DD}

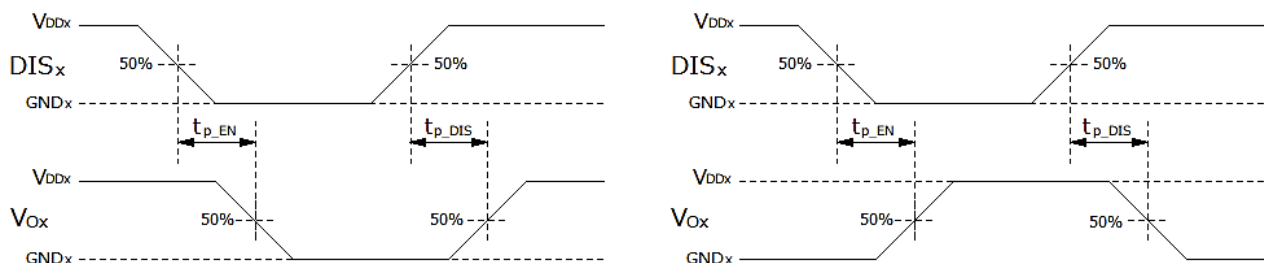


Figure 8.2 Disable Propagation Delay Time Test Waveform Diagram

9. Absolute Maximum Ratings (Note)

Table 9.1 Absolute Maximum Ratings (Note)

($T_a = 25^\circ\text{C}$ unless otherwise specified)

| Characteristics | Condition | Symbol | Rating | Unit |
|-----------------------------|---|----------------------------------|---|------------------|
| Junction temperature | — | T_J | -40 to 150 | $^\circ\text{C}$ |
| Storage temperature range | — | T_{stg} | -65 to 150 | $^\circ\text{C}$ |
| Operation temperature range | — | T_{opr} | -40 to 125 | $^\circ\text{C}$ |
| Soldering temperature | 10s | T_{sol} | 260 | $^\circ\text{C}$ |
| Supply voltage (DC) | — | $V_{\text{DD1}}, V_{\text{DD2}}$ | -0.5 to 6.0 | V |
| | | $V_I(1 \text{ to } 4)$ | -0.5 to $V_{\text{DDI}} + 0.5$ (Note 1) | V |
| | | $V_O(1 \text{ to } 4)$ | 0.5 to $V_{\text{DDO}} + 0.5$ (Note 1) | V |
| | | $\text{DIS1}, \text{DIS2}$ | -0.5 to $V_{\text{DDEN}} + 0.5$ (Note 1) | V |
| Output Current | | I_O | ± 15 | mA |
| Isolation voltage | 1min | BV_s | 5000 | V_{rms} |
| Output current | $V_{\text{DD1}} = V_{\text{DD2}} = 5.5 \text{ V}$, $T_J = 150^\circ\text{C}$, $T_a = 25^\circ\text{C}$ | I_{S1} | 284 | mA |
| | $V_{\text{DD1}} = V_{\text{DD2}} = 3.6 \text{ V}$, $T_J = 150^\circ\text{C}$, $T_a = 25^\circ\text{C}$ | I_{S2} | 434 | mA |
| Power dissipation | $T_J = 150^\circ\text{C}$, $T_a = 25^\circ\text{C}$ | $P_{d \text{ Max}}$ | 1562 | mW |

Note: The absolute maximum ratings of a semiconductor device are a set of specified parameter values, which must not be exceeded during operation, even for an instant.

If any of these rating would be exceeded during operation, the device electrical characteristics may be irreparably altered, and the reliability and lifetime of the device can no longer be guaranteed. Moreover, these operations with exceeded ratings may cause break down, damage, and/or degradation to any other equipment. Applications using the device should be designed such that each maximum rating will never be exceeded in any operating conditions.

Before using, creating, and/or producing designs, refer to and comply with the precautions and conditions set forth in this document.

Note 1: Maximum voltage must not exceed 6V

9.1. Power Dissipation

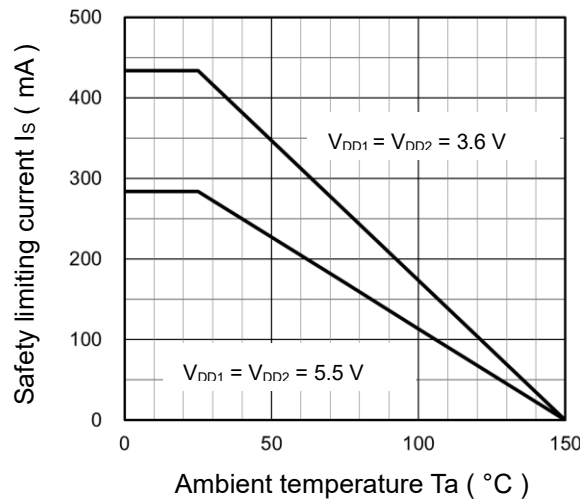


Figure 9.1 Thermal derating curve for safety limiting current - Ta

10. Recommended operating conditions

Table 10.1 Recommended Operating Ranges (Note)

| Characteristics | Symbol | Min | Max | Unit |
|-----------------------|-------------------------------------|-----|-----|------|
| Operation voltage | V _{DD1} , V _{DD2} | 3.0 | 5.5 | V |
| Junction temperature | T _J | -40 | 150 | °C |
| Operating temperature | T _{opr} | -40 | 125 | °C |

Note: The recommended operating conditions are given as a design guide necessary to obtain the intended performance of the device. Each parameter is an independent value. When creating a system design using this device, the electrical characteristics specified in this data sheet should also be considered.

11. Electrical Characteristics

11.1. DC characteristics – 5V Supply

Table 11.1 DC characteristics – 5V Supply (Note)

($V_{DD1} = V_{DD2} = 4.5\text{ V to } 5.5\text{ V}$ over recommended operating conditions unless otherwise noted)

| Characteristics | Symbol | Test condition | Min | Typ | Max | Unit |
|---|---------------------|---|------------------------|------------------------|------------------------|------|
| V _{DD} Under Voltage Lockout threshold Voltage | VDD _{xUV+} | Positive VDD _x Threshold | — | 2.1 | 2.25 | V |
| | VDD _{xUV-} | Negative VDD _x Threshold | 1.7 | 1.9 | — | |
| | VDD _{xUVH} | VDD _x Hysteresis | 0.1 | 0.2 | — | |
| Logic High-level output voltage | V _{OH} | V _{Ix} = High , I _{OH} = -20 μA | V _{DDO} - 0.1 | V _{DDO} | — | V |
| | | V _{Ix} = High , I _{OH} = -4 mA | V _{DDO} - 0.4 | V _{DDO} - 0.2 | — | |
| Logic Low-level output voltage | V _{OL} | V _{Ix} = High , I _{OL} = -20 μA | — | 0 | 0.1 | V |
| | | V _{Ix} = High , I _{OL} = 4 mA | — | 0.2 | 0.4 | |
| Output Impedance | Z _O | — | — | 50 | — | Ω |
| Logic High-level input Threshold voltage | V _{IH} | — | 0.7 x V _{DDI} | — | — | V |
| Logic Low-level input Threshold voltage | V _{IL} | — | — | — | 0.3 x V _{DDI} | V |
| Logic Input threshold voltage hysteresis | V _{HYS} | — | — | 0.37 | — | V |
| DIS pin input Threshold voltage | V _{DISIH} | — | 0.7 x V _{DDI} | — | — | V |
| DIS pin Low-level input Threshold voltage | V _{DISIL} | — | — | — | 0.3 x V _{DDI} | V |
| DIS pin Input threshold voltage hysteresis | V _{DISHYS} | — | — | 0.37 | — | V |
| Input current | I _I | V _I = V _{DDI} or 0 V | — | — | ±10 | μA |

Note: V_{DDI} = Input-side V_{DD}, V_{DDO} = Output-side V_{DD}

11.2. Switching Characteristics – 5 V Supply

Table 11.2 Switching Characteristics – 5 V Supply

($V_{DD1} = V_{DD2} = 4.5\text{ V to }5.5\text{ V}$ over recommended operating conditions unless otherwise noted)

| Characteristics | | Symbol | Test condition | Min | Typ | Max | Unit |
|--|--------------------|--------------------------|--|-----|------|------|-------------|
| Data Rate | | t_{bps} | — | 20 | — | 50 | Mbps |
| Propagation Delay | | t_{PHL} , t_{PLH} | 50 kHz, Duty = 50 %, $C_L = 15\text{ pF}$ | — | 10.9 | 18.4 | ns |
| Pulse Width Distortion | | PWD | $ t_{PHL} - t_{PLH} $ | — | 0.8 | 5.1 | ns |
| Propagation Delay Skew (Between any two units) | | t_{PSK} | (Note1) | — | — | 13.0 | ns |
| Channel Matching | Same Direction | t_{skCD} | — | — | — | 4.4 | ns |
| | Opposing Direction | t_{skOD} | — | — | — | 4.5 | ns |
| Output signal rise time | | t_r | 10% to 90% | — | 0.9 | — | ns |
| Output signal fall time | | t_f | 90% to 10% | — | 0.9 | — | ns |
| Disable control pin Propagation delay | | t_{pEN} | 50 kHz, Duty = 50 %, $C_L = 15\text{ pF}$ | — | — | 23.0 | ns |
| | | t_{p_DIS} | | — | — | 23.0 | ns |
| Common-Mode Transient Immunity | | CMTI | $V_I = V_{DDI}$ or 0 V, $V_{CM} = 1500\text{ V}$ | — | 100 | — | kV/ μ s |

Note1: The Propagation delay skew, t_{PSK} , is equal to the magnitude of the difference in propagation delay. That will be seen between units at the same given conditions (supply voltage, input current, temperature, etc.).

11.3. Supply Current Characteristics – 5 V Supply

Table 11.3 Supply Current Characteristics – 5 V Supply

($V_{DD1} = V_{DD2} = 4.5\text{ V to }5.5\text{ V}$ over recommended operating conditions unless otherwise noted)

| Characteristics | | Symbol | Test condition | Min | Typ | Max | Unit | |
|----------------------------|----------------------------|----------------|---|----------------|------|------|------|----|
| DC Supply Current | Primary side | $I_{DDQ1(0)5}$ | $V_I = \text{High}$ | — | 3.0 | 4.3 | mA | |
| | | $I_{DDQ1(1)5}$ | $V_I = \text{Low}$ | — | 16.6 | 22.5 | | |
| | Secondary side | $I_{DDQ2(0)5}$ | $V_I = \text{High}$ | — | 4.5 | 6.6 | mA | |
| | | $I_{DDQ2(1)5}$ | $V_I = \text{Low}$ | — | 10.2 | 14.1 | | |
| Supply Current (AC signal) | $t_{bps} = 1\text{ Mbps}$ | Primary side | $f_{CLK} = 500\text{ kHz}$, Duty = 50 % square wave, $C_L = 15\text{ pF}$ | $I_{DD1(1)5}$ | — | 10.0 | 15.5 | mA |
| | | Secondary side | | $I_{DD2(1)5}$ | — | 7.6 | 10.2 | |
| | $t_{bps} = 25\text{ Mbps}$ | Primary side | $f_{CLK} = 12.5\text{ MHz}$, Duty = 50 % square wave, $C_L = 15\text{ pF}$ | $I_{DD1(25)5}$ | — | 12.1 | 18.2 | mA |
| | | Secondary side | | $I_{DD2(25)5}$ | — | 10.6 | 15.4 | |
| | $t_{bps} = 50\text{ Mbps}$ | Primary side | $f_{CLK} = 25\text{ MHz}$, Duty = 50 % square wave, $C_L = 15\text{ pF}$ | $I_{DD1(50)5}$ | — | 13.9 | 20.3 | mA |
| | | Secondary side | | $I_{DD2(50)5}$ | — | 14.6 | 22.0 | |

11.4. Supply Current Characteristics – 3.3 V Supply

Table 11.4 Supply Current Characteristics – 3.3 V Supply (Note)

($V_{DD1} = V_{DD2} = 3.0\text{ V to }3.6\text{ V}$ over recommended operating conditions unless otherwise noted)

| Characteristics | Symbol | Test condition | Min | Typ | Max | Unit |
|---|---------------------|--|------------------------|-----------------------|------------------------|------|
| V _{DD} Under Voltage Lockout threshold Voltage | V _{DDxUV+} | Positive VDDx Threshold | — | 2.1 | 2.25 | V |
| | V _{DDxUV-} | Negative VDDx Threshold | 1.7 | 1.9 | — | |
| | V _{DDxUVH} | VDDx Hysteresis | 0.1 | 0.2 | — | |
| Logic High-level output voltage | V _{OH} | V _{Ix} = High , I _{OH} = - 20 μA | V _{DDO} - 0.1 | V _{DDO} | — | V |
| | | V _{Ix} = High , I _{OH} = - 4 mA | V _{DDO} - 0.4 | V _{DDO} -0.2 | — | |
| Logic Low-level output voltage | V _{OL} | V _{Ix} = High , I _{OL} = - 20 μA | — | 0 | 0.1 | V |
| | | V _{Ix} = High , I _{OL} = 4 mA | — | 0.2 | 0.4 | |
| Output Impedance | Z _O | — | — | 50 | — | Ω |
| Logic High-level input Threshold voltage | V _{IH} | — | 0.7 x V _{DDI} | — | — | V |
| Logic Low-level input Threshold voltage | V _{IL} | — | — | — | 0.3 x V _{DDI} | V |
| Logic Input threshold voltage hysteresis | V _{HYS} | — | — | 0.32 | — | V |
| DIS pin input Threshold voltage | V _{DISIH} | — | 0.7 x V _{DDI} | — | — | V |
| DIS pin Low-level input Threshold voltage | V _{DISIL} | — | — | — | 0.3 x V _{DDI} | V |
| DIS pin Input threshold voltage hysteresis | V _{DISHYS} | — | — | 0.32 | — | V |
| Input current | I _I | V _I = V _{DDI} or 0 V | — | — | ±10 | μA |

Note: V_{DDI} = Input-side V_{DD}, V_{DDO} = Output-side V_{DD}

11.5. Switching Characteristics – 3.3 V Supply

Table 11.5 Switching Characteristics – 3.3 V Supply

($V_{DD1} = V_{DD2} = 3.0\text{ V to }3.6\text{ V}$ over recommended operating conditions unless otherwise noted)

| Characteristics | | Symbol | Test condition | Min | Typ | Max | Unit |
|--|--------------------|--------------------------|--|-----|------|------|-------------|
| Data Rate | | t_{bps} | — | 20 | — | 50 | Mbps |
| Propagation Delay | | t_{PHL} , t_{PLH} | 50 kHz, Duty = 50 %, $C_L = 15\text{ pF}$ | — | 11.6 | 19.2 | ns |
| Pulse Width Distortion | | PWD | $ t_{PHL} - t_{PLH} $ | — | 0.8 | 5.1 | ns |
| Propagation Delay Skew (Between any two units) | | t_{PSK} | (Note1) | — | — | 13.0 | ns |
| Channel Matching | Codirectional | t_{skCD} | — | — | — | 4.4 | ns |
| | Opposing Direction | t_{skOD} | — | — | — | 4.5 | ns |
| Output signal rise time | | t_r | 10% to 90% | — | 0.9 | — | ns |
| Output signal fall time | | t_f | 90% to 10% | — | 0.9 | — | ns |
| Disable control pin Propagation delay | | t_{pEN} | 50 kHz, Duty = 50 %, $C_L = 15\text{ pF}$ | — | — | 23.0 | ns |
| | | t_{p_DIS} | | — | — | 23.0 | ns |
| Common-Mode Transient Immunity | | CMTI | $V_I = V_{DD1}$ or 0 V, $V_{CM} = 1500\text{ V}$ | — | 100 | — | kV/ μ s |

Note1: The Propagation delay skew, t_{PSK} , is equal to the magnitude of the difference in propagation delay. That will be seen between units at the same given conditions (supply voltage, input current, temperature, etc.).

11.6. Supply Current Characteristics – 3.3 V Supply

Table 11.6 Supply Current Characteristics – 3.3 V Supply

($V_{DD1} = V_{DD2} = 3.0\text{ V to }3.6\text{ V}$ over recommended operating conditions unless otherwise noted)

| Characteristics | | Symbol | Test condition | Min | Typ | Max | Unit | |
|----------------------------|----------------------------|----------------|---|----------------|------|------|------|----|
| DC Supply Current | Primary side | $I_{DDQ1(0)5}$ | $V_I = \text{High}$ | — | 2.9 | 4.1 | mA | |
| | | $I_{DDQ1(1)5}$ | $V_I = \text{Low}$ | — | 16.5 | 22.3 | | |
| | Secondary side | $I_{DDQ2(0)5}$ | $V_I = \text{High}$ | — | 4.4 | 6.5 | mA | |
| | | $I_{DDQ2(1)5}$ | $V_I = \text{Low}$ | — | 10.1 | 14.0 | | |
| Supply Current (AC signal) | $t_{bps} = 1\text{ Mbps}$ | Primary side | $f_{CLK} = 500\text{ kHz}$, Duty = 50 % square wave, $C_L = 15\text{ pF}$ | $I_{DD1(1)5}$ | — | 9.9 | 14.9 | mA |
| | | Secondary side | | $I_{DD2(1)5}$ | — | 7.5 | 9.5 | |
| | $t_{bps} = 25\text{ Mbps}$ | Primary side | $f_{CLK} = 12.5\text{ MHz}$, Duty = 50 % square wave, $C_L = 15\text{ pF}$ | $I_{DD1(25)5}$ | — | 10.8 | 16.6 | mA |
| | | Secondary side | | $I_{DD2(25)5}$ | — | 9.7 | 12.8 | |
| | $t_{bps} = 50\text{ Mbps}$ | Primary side | $f_{CLK} = 25\text{ MHz}$, Duty = 50 % square wave, $C_L = 15\text{ pF}$ | $I_{DD1(50)5}$ | — | 12.0 | 17.7 | mA |
| | | Secondary side | | $I_{DD2(50)5}$ | — | 12.0 | 17.2 | |

12. Characteristic Chart (Note)

12.1. Supply Current vs Data rate

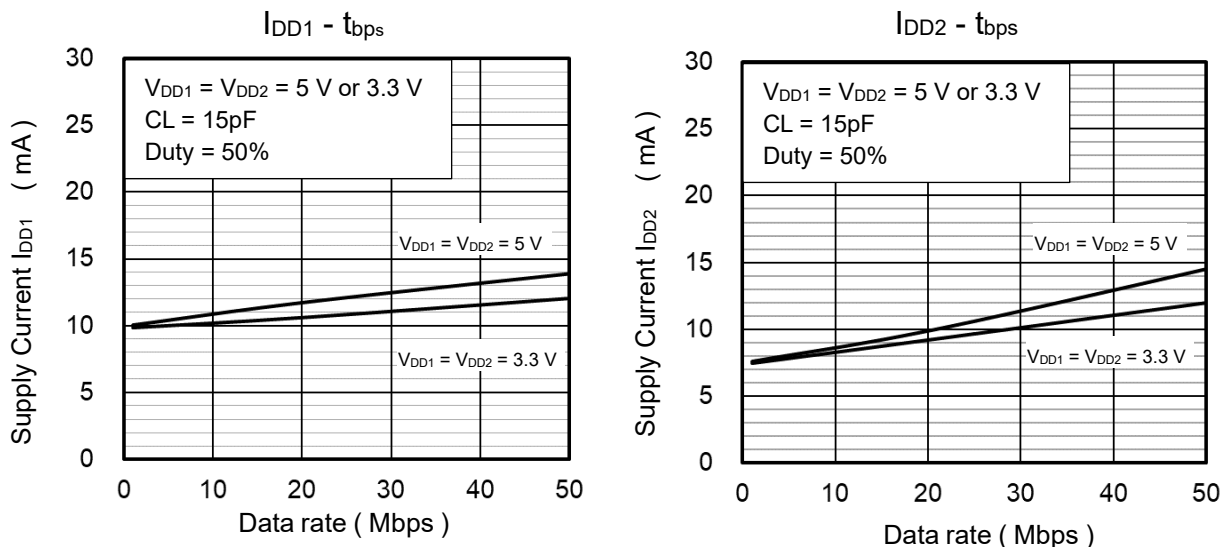


Figure 12.1 Supply Current – Data rate

12.2. Output Voltage vs Output Current

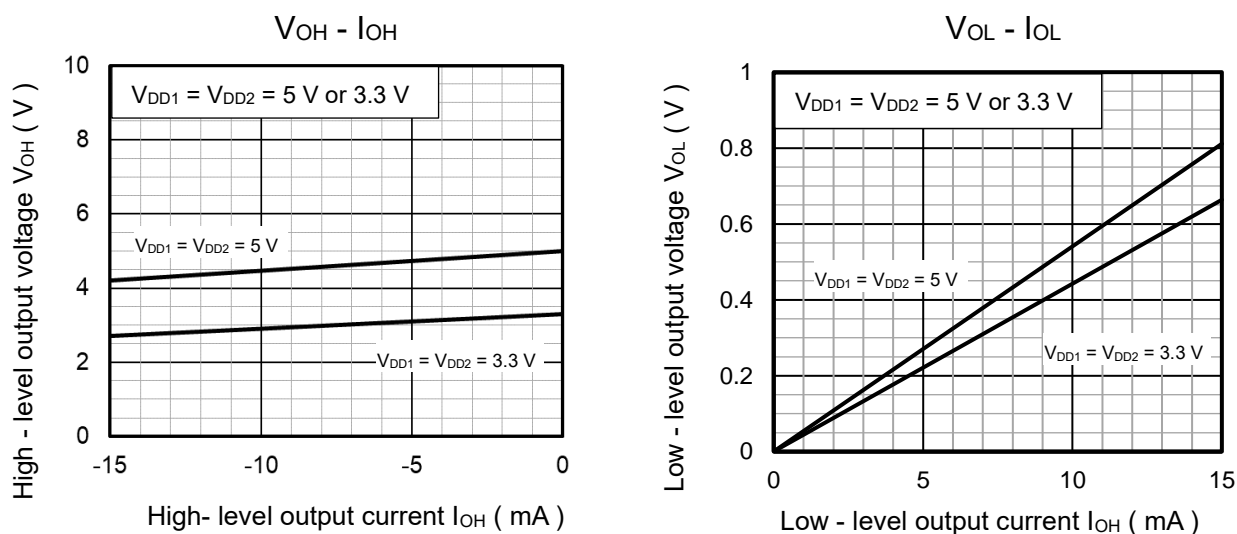


Figure 12.2 Output Voltage – Output Current

Note: The following characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

12.3. Propagation Delay Time vs Ambient Temperature

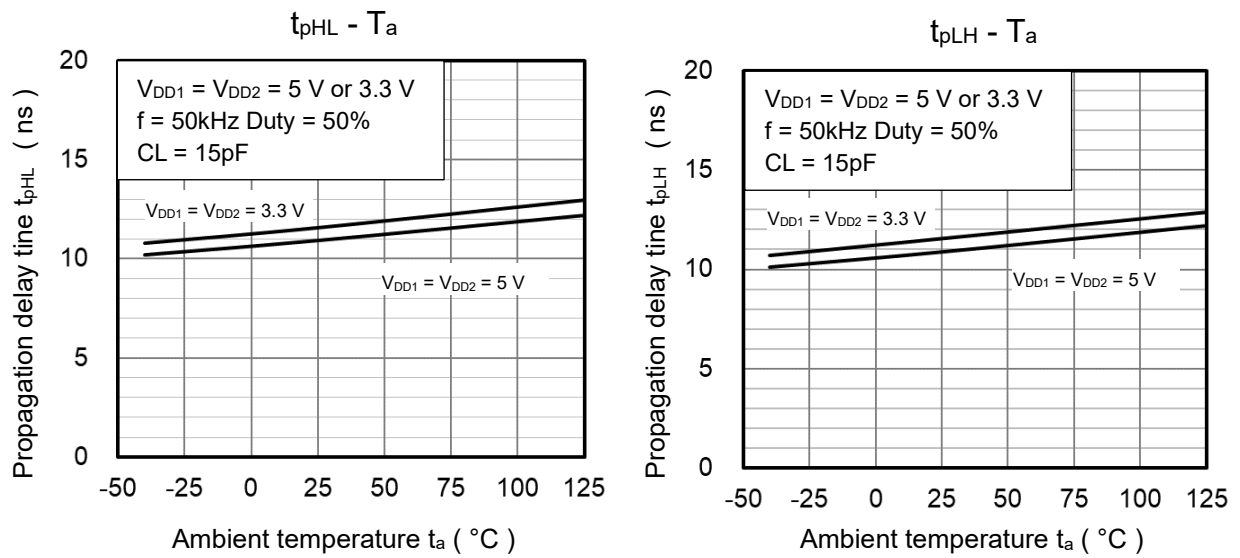


Figure12.3 Propagation Delay Time vs Ambient Temperature

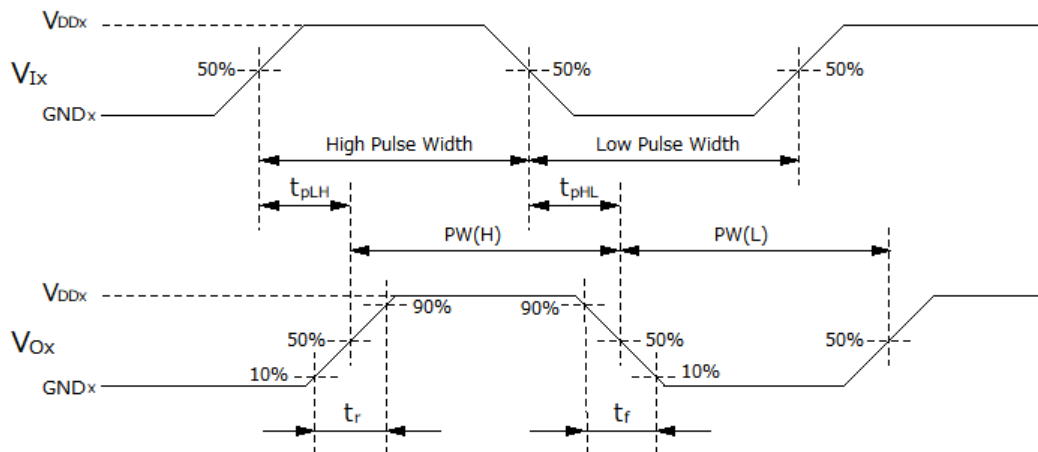


Figure12.4 Switching Waveforms

Note: The following characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

13. Package Information

Table 13.1 Insulation Related Specifications (Note)

| Parameters | Symbol | DCM341B01 | Unit |
|------------------------------|--------|-----------|------|
| Minimum clearance | CLR | 8.0 | mm |
| Minimum creepage distance | CPG | 7.6 | mm |
| Minimum insulation thickness | DTI | 17 | μm |
| Comparative tracking index | CTI | 550 | V |

Note: If a printed circuit is incorporated, the creepage distance and clearance may be reduced below this value. (e.g., at a standard distance between soldering eye centers of 7.5 mm). If this is not permissible, the user shall take suitable measures.

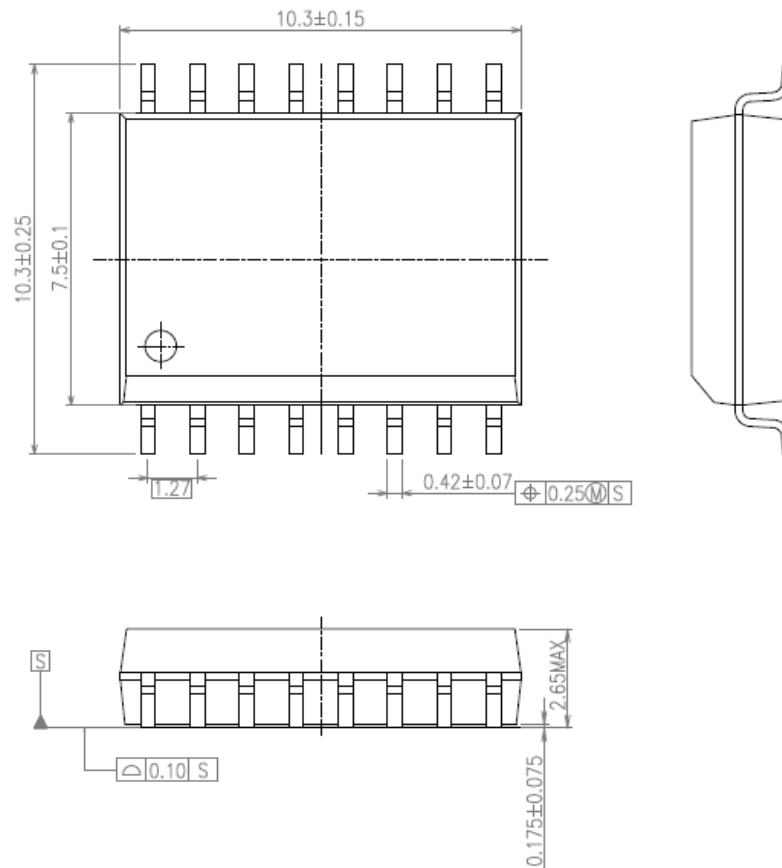
Note: This photocoupler is suitable for safe electrical isolation only within the safety limit data. Maintenance of the safety data shall be ensured by means of protective circuits.

14. Package Information

14.1. Package Dimensions

16pin SOIC Wide body
(P-SOP16-0811-1.27-002)

UNIT: mm



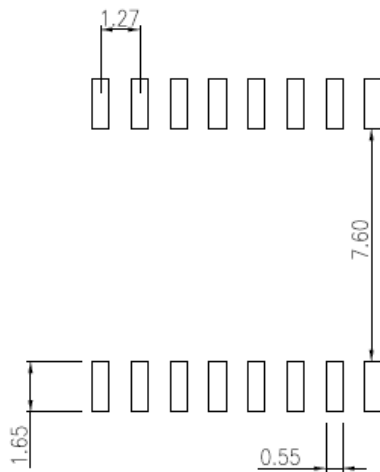
Weight: 0.426 g (typ.)

Figure 14.1 Package Dimensions

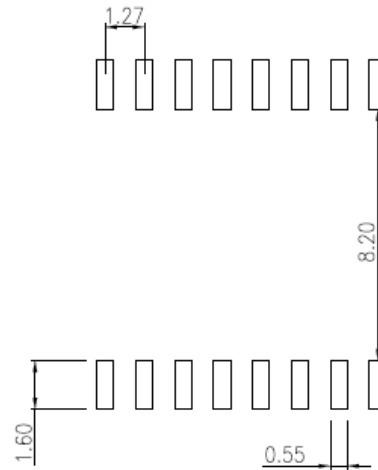
14.2. Land Pattern Dimensions for Reference only

16pin SOIC Wide body
(P-SOP16-0811-1.27-002)

Unit: mm



Complies with JEITA ET-7501 Level 3 Normal
Creepage distance: 7.6 mm



Isolation option
Creepage distance: ≥ 8 mm

Figure 14.2 Land Pattern Dimensions for Reference only

Notes.

- Unless otherwise indicated, dimensions are given in millimeters.
- This document is a reference drawing in accordance with JEITA ET-7501 Level 3. The Company does not guarantee the accuracy or completeness of the diagrams and information.
- The customer should fully evaluate the various conditions (soldering conditions, etc.) and adjust at their own risk.
- The diagrams in this document do not accurately show the actual shape and dimensions. Do not use the dimensions of the actual product as a basis for designing the product.
- When designing and using the product, check the latest information on the product and the operating instructions of the equipment in which the product is to be used, and follow these instructions.

RESTRICTIONS ON PRODUCT USE

Toshiba Corporation and its subsidiaries and affiliates are collectively referred to as "TOSHIBA". Hardware, software and systems described in this document are collectively referred to as "Product".

- TOSHIBA reserves the right to make changes to the information in this document and related Product without notice.
- This document and any information herein may not be reproduced without prior written permission from TOSHIBA. Even with TOSHIBA's written permission, reproduction is permissible only if reproduction is without alteration/omission.
- Though TOSHIBA works continually to improve Product's quality and reliability, Product can malfunction or fail. Customers are responsible for complying with safety standards and for providing adequate designs and safeguards for their hardware, software and systems which minimize risk and avoid situations in which a malfunction or failure of Product could cause loss of human life, bodily injury or damage to property, including data loss or corruption. Before customers use the Product, create designs including the Product, or incorporate the Product into their own applications, customers must also refer to and comply with (a) the latest versions of all relevant TOSHIBA information, including without limitation, this document, the specifications, the data sheets and application notes for Product and the precautions and conditions set forth in the "TOSHIBA Semiconductor Reliability Handbook" and (b) the instructions for the application with which the Product will be used with or for. Customers are solely responsible for all aspects of their own product design or applications, including but not limited to (a) determining the appropriateness of the use of this Product in such design or applications; (b) evaluating and determining the applicability of any information contained in this document, or in charts, diagrams, programs, algorithms, sample application circuits, or any other referenced documents; and (c) validating all operating parameters for such designs and applications. **TOSHIBA ASSUMES NO LIABILITY FOR CUSTOMERS' PRODUCT DESIGN OR APPLICATIONS.**
- **PRODUCT IS NEITHER INTENDED NOR WARRANTED FOR USE IN EQUIPMENTS OR SYSTEMS THAT REQUIRE EXTRAORDINARILY HIGH LEVELS OF QUALITY AND/OR RELIABILITY, AND/OR A MALFUNCTION OR FAILURE OF WHICH MAY CAUSE LOSS OF HUMAN LIFE, BODILY INJURY, SERIOUS PROPERTY DAMAGE AND/OR SERIOUS PUBLIC IMPACT ("UNINTENDED USE").** Except for specific applications as expressly stated in this document, Unintended Use includes, without limitation, equipment used in nuclear facilities, equipment used in the aerospace industry, lifesaving and/or life supporting medical equipment, equipment used for automobiles, trains, ships and other transportation, traffic signaling equipment, equipment used to control combustions or explosions, safety devices, elevators and escalators, and devices related to power plant. **IF YOU USE PRODUCT FOR UNINTENDED USE, TOSHIBA ASSUMES NO LIABILITY FOR PRODUCT.** For details, please contact your TOSHIBA sales representative or contact us via our website.
- Do not disassemble, analyze, reverse-engineer, alter, modify, translate or copy Product, whether in whole or in part.
- Product shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable laws or regulations.
- The information contained herein is presented only as guidance for Product use. No responsibility is assumed by TOSHIBA for any infringement of patents or any other intellectual property rights of third parties that may result from the use of Product. No license to any intellectual property right is granted by this document, whether express or implied, by estoppel or otherwise.
- **ABSENT A WRITTEN SIGNED AGREEMENT, EXCEPT AS PROVIDED IN THE RELEVANT TERMS AND CONDITIONS OF SALE FOR PRODUCT, AND TO THE MAXIMUM EXTENT ALLOWABLE BY LAW, TOSHIBA (1) ASSUMES NO LIABILITY WHATSOEVER, INCLUDING WITHOUT LIMITATION, INDIRECT, CONSEQUENTIAL, SPECIAL, OR INCIDENTAL DAMAGES OR LOSS, INCLUDING WITHOUT LIMITATION, LOSS OF PROFITS, LOSS OF OPPORTUNITIES, BUSINESS INTERRUPTION AND LOSS OF DATA, AND (2) DISCLAIMS ANY AND ALL EXPRESS OR IMPLIED WARRANTIES AND CONDITIONS RELATED TO SALE, USE OF PRODUCT, OR INFORMATION, INCLUDING WARRANTIES OR CONDITIONS OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, ACCURACY OF INFORMATION, OR NONINFRINGEMENT.**
- Do not use or otherwise make available Product or related software or technology for any military purposes, including without limitation, for the design, development, use, stockpiling or manufacturing of nuclear, chemical, or biological weapons or missile technology products (mass destruction weapons). Product and related software and technology may be controlled under the applicable export laws and regulations including, without limitation, the Japanese Foreign Exchange and Foreign Trade Law and the U.S. Export Administration Regulations. Export and re-export of Product or related software or technology are strictly prohibited except in compliance with all applicable export laws and regulations.
- Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS compatibility of Product. Please use Product in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. **TOSHIBA ASSUMES NO LIABILITY FOR DAMAGES OR LOSSES OCCURRING AS A RESULT OF NONCOMPLIANCE WITH APPLICABLE LAWS AND REGULATIONS.**

Toshiba Electronic Devices & Storage Corporation

<https://toshiba.semicon-storage.com/>