

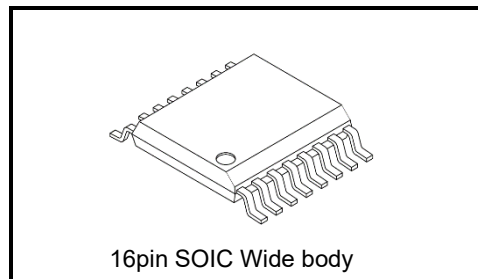
# DCM341A01

Quad - channel High speed Logic for Automotive, Input Disable control, Default Low output

## 1. Description

The DCM341A01 is a 16-pin SOIC Wide package default low-output, quad-channel high-speed digital isolator with the primary and secondary sides insulated and coupled by a magnetic coupling structure.

With a high isolation voltage of 5000 V<sub>rms</sub>, it is suitable for control application applications such as in-vehicle communication line insulation.



16pin SOIC Wide body

Weight: 0.426 g (typ.)

## 2. Applications

- Battery Control in Automotive Equipment
- Fuel Battery Control in Automotive Equipment
- Application for Electrical Vehicle
- Data Converter Isolation  
(Serial Peripheral Interface (SPI), etc.)

## 3. Features

- Data rate : 50 Mbps (Max)
- Default Output : Low
- Control type : Input Disable
- Number of channels : 4 channels (Forward 3 : Revers 1)
- Suitable operating voltage : 3.3 V or 5 V
- Isolation voltage : 5000 V<sub>rms</sub>
- Common-Mode Transient Immunity : ±100 kV/μs (Typ)
- Safety standards
  - AEC-Q100 (Grade1 qualified)
  - UL : UL1577 , File No. E519997
  - cUL: CSA Component Acceptance Service Notice No. E519997

Note: Typical test conditions: V<sub>DD1</sub> =V<sub>DD2</sub> = 3.3V or 5V , T<sub>a</sub> = 25 °C; unless otherwise specified.

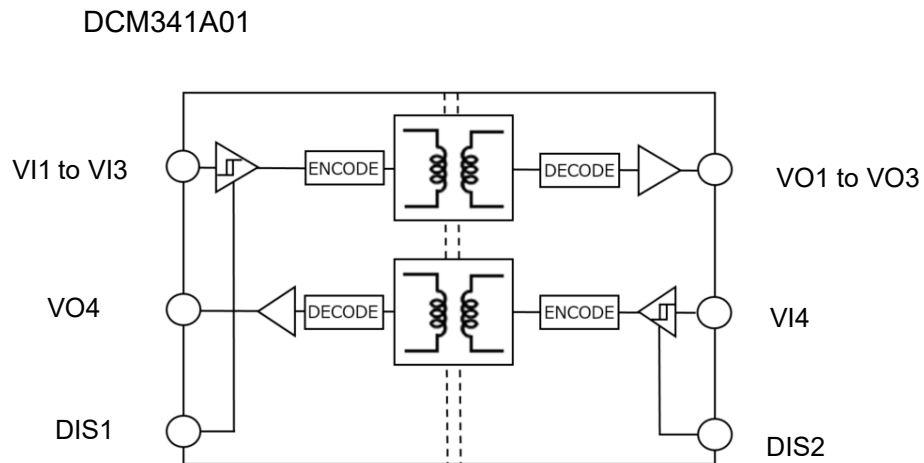
## 4. Mechanical Parameters

**Table 4.1 Mechanical parameters**

Characteristics	Symbol	unit	Unit
Creepage distances	CPG	7.6 (Min)	mm
Clearance distances	CLR	8 (Min)	mm
Distance Through the Insulation	DTI	17	μm

Start of commercial production  
2024-11

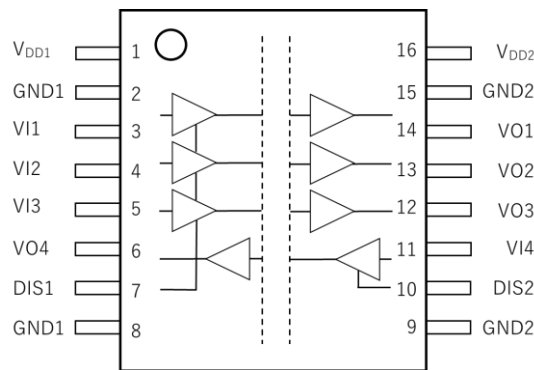
**5. Block Diagram**



Note: Some of the functional blocks, circuits or constants labels in the block diagram may have been omitted or simplified for clarity.

**Figure 5.1 Block Diagram**

## 6. Pin Assignments



**Figure 6.1 Pin Assignments (top view)**

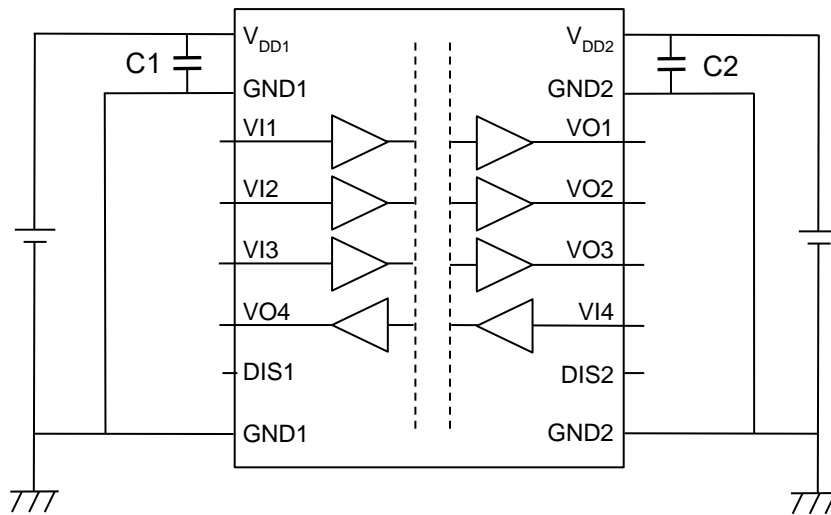
## 7. Pin Description

**Table 7.1 Pin Description**

Pin No	Pin name	I/O	Description
1	V <sub>DD1</sub>	—	Power Supply, side 1
2	GND1	—	GND connection for VDD1 , side 1
3	VI1	IN	Logic Input, Channel1
4	VI2	IN	Logic Input, Channel2
5	VI3	IN	Logic Input, Channel3
6	VO4	OUT	Logic Output, Channel4
7	DIS1	IN	Ch1 to Ch3 Input disable control pin
8	GND1	—	GND connection for VDD1, side 1
9	GND2	—	GND connection for VDD2, side 2
10	DIS2	IN	Ch4 Input disable control pin
11	VI4	IN	Logic Input, Channel4
12	VO3	OUT	Logic Output, Channel3
13	VO2	OUT	Logic Output, Channel2
14	VO1	OUT	Logic Output, Channel1
15	GND2	—	GND connection for VDD2, side 2
16	V <sub>DD2</sub>	—	Power Supply, side 2

## 8. Functional Description

### 8.1. Specifications of External Components



**Figure 8.1 Pin Assignments (top view)**

**Table 8.1 External component specification (Note)**

Component Name	Recommended Value	Pin	
<b>C1</b>	0.1μF	V <sub>DD1</sub>	—
<b>C2</b>	0.1μF	V <sub>DD2</sub>	—

Note: Use Ceramic capacitors (C1,C2) with good high frequency characteristics.

Note: Ceramic capacitors (C1,C2) should be connected between pin 1 (V<sub>DD1</sub>) and pin 2 (GND1) for V<sub>DD1</sub> and between pin 16 (V<sub>DD2</sub>) and pin 15 (GND2) for V<sub>DD2</sub>, and should be the layout on the IC as close as possible (less than 10mm).

Otherwise, the IC may not switch properly.

## 8.2. IC Startup Procedure

### 8.2.1. Input Disable

Input signal Enable / Disable control is possible by controlling pin 7 (DIS1 terminal) and pin 10 (DIS2 terminal) to High or Low.

To enable Input, set pin 7 (DIS1 pin) and pin 10 (DIS2 pin) to High or OPEN.

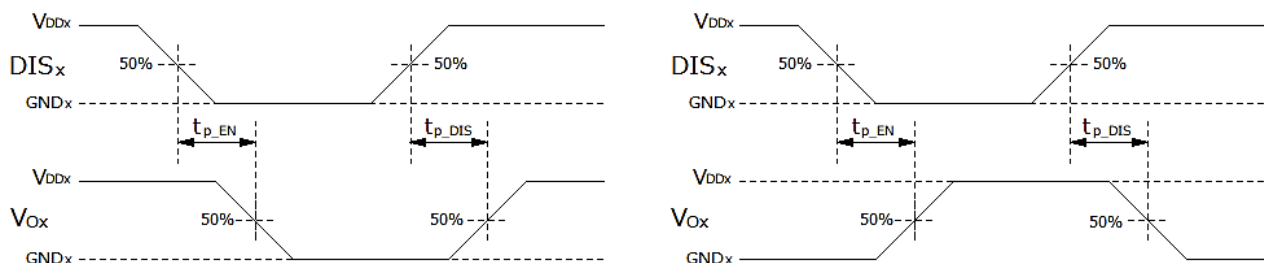
By setting pin 7 (DIS1 pin) to Low, VI1 to VI3 can be disabled, and by setting pin 10 (DIS2 pin) to Low, VI4 can be disabled.

**Table 8.2 Input Disable control pin Functional Description (Note)**

	V <sub>DDI</sub> Input side V <sub>DD</sub>	V <sub>DDO</sub> Output side V <sub>DD</sub>	DIS Pin (DIS1, DIS2)	Input (VI1 to VI4)	Output (VO1 to VO4)	State Description
1	PU	PU	Low or OPEN	Low	Low	Normal Operation
2				High	High	
3				OPEN	Low	Default mode
4	PU	PU	High	Undetermined	Low	Default mode (Input disable mode)
5			PD	Undetermined	Undetermined	Undetermined
6	PD	PU	Undetermined	Undetermined	Low	Default mode
7	PD	PD	Undetermined	Undetermined	Undetermined	When V <sub>DDO</sub> is unpowered, a channel output is undetermined.

Note: PU = Powered Up (V<sub>DD</sub> ≥ 2.25 V), PD = Powered Down (V<sub>DD</sub> ≤ 1.7 V)

Note: V<sub>DDI</sub> = Input-side V<sub>DD</sub>, V<sub>DDO</sub> = Output-side V<sub>DD</sub>



**Figure 8.2 Disable Propagation Delay Time Test Waveform Diagram**

## 9. Absolute Maximum Ratings (Note)

Table 9.1 Absolute Maximum Ratings (Note)

(T<sub>a</sub> = 25°C unless otherwise specified)

Characteristics	Condition	Symbol	Rating	Unit
Junction temperature	—	T <sub>J</sub>	-40 to 150	°C
Storage temperature range	—	T <sub>stg</sub>	-65 to 150	°C
Operation temperature range	—	T <sub>opr</sub>	-40 to 125	°C
Soldering temperature	10s	T <sub>sol</sub>	260	°C
Supply voltage (DC)	—	V <sub>DD1</sub> , V <sub>DD2</sub>	-0.5 to 6.0	V
		V <sub>I</sub> (1 to 4)	-0.5 to V <sub>DDI</sub> + 0.5 (Note 1)	V
		V <sub>O</sub> (1 to 4)	0.5 to V <sub>DDO</sub> + 0.5 (Note 1)	V
		DIS1, DIS2	-0.5 to V <sub>DDEN</sub> + 0.5 (Note 1)	V
Output Current	—	I <sub>O</sub>	±15	mA
Isolation voltage	1min	BVs	5000	V <sub>rms</sub>
Output current	V <sub>DD1</sub> = V <sub>DD2</sub> = 5.5 V, T <sub>J</sub> = 150 °C, T <sub>a</sub> = 25 °C	I <sub>S1</sub>	284	mA
	V <sub>DD1</sub> = V <sub>DD2</sub> = 3.6 V, T <sub>J</sub> = 150 °C, T <sub>a</sub> = 25 °C	I <sub>S2</sub>	434	mA
Power dissipation	T <sub>J</sub> = 150 °C, T <sub>a</sub> = 25 °C	P <sub>d Max</sub>	1562	mW

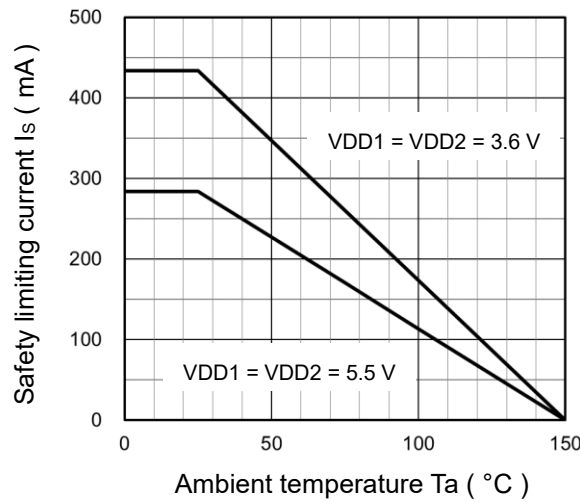
Note: The absolute maximum ratings of a semiconductor device are a set of specified parameter values, which must not be exceeded during operation, even for an instant.

If any of these rating would be exceeded during operation, the device electrical characteristics may be irreparably altered, and the reliability and lifetime of the device can no longer be guaranteed. Moreover, these operations with exceeded ratings may cause break down, damage, and/or degradation to any other equipment. Applications using the device should be designed such that each maximum rating will never be exceeded in any operating conditions.

Before using, creating, and/or producing designs, refer to and comply with the precautions and conditions set forth in this document.

Note 1: Maximum voltage must not exceed 6V

**9.1. Power Dissipation**



**Figure 9.1 Thermal derating curve for safety limiting current -  $T_a$**

**10. Recommended operating conditions**

**Table 10.1 Recommended Operating Ranges (Note)**

Characteristics	Symbol	Min	Max	Unit
Operation voltage	$V_{DD1}, V_{DD2}$	3.0	5.5	V
Junction temperature	$T_J$	-40	150	°C
Operating temperature	$T_{opr}$	-40	125	°C

Note: The recommended operating conditions are given as a design guide necessary to obtain the intended performance of the device. Each parameter is an independent value. When creating a system design using this device, the electrical characteristics specified in this data sheet should also be considered.

## 11. Electrical Characteristics

### 11.1. DC characteristics – 5V Supply

**Table 11.1 DC characteristics – 5V Supply (Note)**

( $V_{DD1} = V_{DD2} = 4.5\text{ V to } 5.5\text{ V}$  over recommended operating conditions unless otherwise noted)

Characteristics	Symbol	Test condition	Min	Typ	Max	Unit
V <sub>DD</sub> Under Voltage Lockout threshold Voltage	V <sub>DDxUV+</sub>	Positive VDDx Threshold	—	2.1	2.25	V
	V <sub>DDxUV-</sub>	Negative VDDx Threshold	1.7	1.9	—	
	V <sub>DDxUVH</sub>	VDDx Hysteresis	0.1	0.2	—	
Logic High-level output voltage	V <sub>OH</sub>	V <sub>Ix</sub> = High , I <sub>OH</sub> = -20 μA	V <sub>DDO</sub> - 0.1	V <sub>DDO</sub>	—	V
		V <sub>Ix</sub> = High , I <sub>OH</sub> = -4 mA	V <sub>DDO</sub> - 0.4	V <sub>DDO</sub> - 0.2	—	
Logic Low-level output voltage	V <sub>OL</sub>	V <sub>Ix</sub> = High , I <sub>OL</sub> = -20 μA	—	0	0.1	V
		V <sub>Ix</sub> = High , I <sub>OL</sub> = 4 mA	—	0.2	0.4	
Output Impedance	Z <sub>O</sub>	—	—	50	—	Ω
Logic High-level input Threshold voltage	V <sub>IH</sub>	—	0.7 x V <sub>DDI</sub>	—	—	V
Logic Low-level input Threshold voltage	V <sub>IL</sub>	—	—	—	0.3 x V <sub>DDI</sub>	V
Logic Input threshold voltage hysteresis	V <sub>HYS</sub>	—	—	0.37	—	V
DIS pin input Threshold voltage	V <sub>DISIH</sub>	—	0.7 x V <sub>DDI</sub>	—	—	V
DIS pin Low-level input Threshold voltage	V <sub>DISIL</sub>	—	—	—	0.3 x V <sub>DDI</sub>	V
DIS pin Input threshold voltage hysteresis	V <sub>DISHYS</sub>	—	—	0.37	—	V
Input current	I <sub>I</sub>	V <sub>I</sub> = V <sub>DDI</sub> or 0 V	—	—	±10	μA

Note: V<sub>DDI</sub> = Input-side V<sub>DD</sub>, V<sub>DDO</sub> = Output-side V<sub>DD</sub>



**11.2. Switching Characteristics – 5 V Supply**

**Table 11.2 Switching Characteristics – 5 V Supply**

( $V_{DD1} = V_{DD2} = 4.5\text{ V to }5.5\text{ V}$  over recommended operating conditions unless otherwise noted)

Characteristics		Symbol	Test condition	Min	Typ	Max	Unit
Data Rate		$t_{bps}$	—	20	—	50	Mbps
Propagation Delay		$t_{PHL}$ , $t_{PLH}$	50 kHz, Duty = 50 %, $C_L = 15\text{ pF}$	—	10.9	18.4	ns
Pulse Width Distortion		PWD	$ t_{PHL} - t_{PLH} $	—	0.8	5.1	ns
Propagation Delay Skew (Between any two units)		$t_{PSK}$	(Note1)	—	—	13.0	ns
Channel Matching	Same Direction	$t_{skCD}$	—	—	—	4.4	ns
	Opposing Direction	$t_{skOD}$	—	—	—	4.5	ns
Output signal rise time		$t_r$	10% to 90%	—	0.9	—	ns
Output signal fall time		$t_f$	90% to 10%	—	0.9	—	ns
Disable control pin Propagation delay		$t_{pEN}$	50 kHz, Duty = 50 %, $C_L = 15\text{ pF}$	—	—	23.0	ns
		$t_{p\_DIS}$		—	—	23.0	ns
Common-Mode Transient Immunity		CMTI	$V_I = V_{DDI}$ or 0 V, $V_{CM} = 1500\text{ V}$	—	100	—	kV/ $\mu$ s

Note1: The Propagation delay skew,  $t_{PSK}$ , is equal to the magnitude of the difference in propagation delay. That will be seen between units at the same given conditions (supply voltage, input current, temperature, etc.).

**11.3. Supply Current Characteristics – 5 V Supply**

**Table 11.3 Supply Current Characteristics – 5 V Supply**

( $V_{DD1} = V_{DD2} = 4.5\text{ V to }5.5\text{ V}$  over recommended operating conditions unless otherwise noted)

Characteristics		Symbol	Test condition	Min	Typ	Max	Unit	
DC Supply Current	Primary side	$I_{DDQ1(0)5}$	$V_I = \text{Low}$	—	3.0	4.3	mA	
		$I_{DDQ1(1)5}$	$V_I = \text{High}$	—	16.6	22.5		
	Secondary side	$I_{DDQ2(0)5}$	$V_I = \text{Low}$	—	4.5	6.6	mA	
		$I_{DDQ2(1)5}$	$V_I = \text{High}$	—	10.2	14.1		
Supply Current (AC signal)	$t_{bps} = 1\text{ Mbps}$	Primary side	$f_{CLK} = 500\text{ kHz}$ , Duty = 50 % square wave, $C_L = 15\text{ pF}$	$I_{DD1(1)5}$	—	10.0	15.5	mA
		Secondary side		$I_{DD2(1)5}$	—	7.6	10.2	
	$t_{bps} = 25\text{ Mbps}$	Primary side	$f_{CLK} = 12.5\text{ MHz}$ , Duty = 50 % square wave, $C_L = 15\text{ pF}$	$I_{DD1(25)5}$	—	12.1	18.2	mA
		Secondary side		$I_{DD2(25)5}$	—	10.6	15.4	
	$t_{bps} = 50\text{ Mbps}$	Primary side	$f_{CLK} = 25\text{ MHz}$ , Duty = 50 % square wave, $C_L = 15\text{ pF}$	$I_{DD1(50)5}$	—	13.9	20.3	mA
		Secondary side		$I_{DD2(50)5}$	—	14.6	22.0	

**11.4. Supply Current Characteristics – 3.3 V Supply**

**Table 11.4 Supply Current Characteristics – 3.3 V Supply (Note)**

( $V_{DD1} = V_{DD2} = 3.0\text{ V to }3.6\text{ V}$  over recommended operating conditions unless otherwise noted)

Characteristics	Symbol	Test condition	Min	Typ	Max	Unit
V <sub>DD</sub> Under Voltage Lockout threshold Voltage	V <sub>DDxUV+</sub>	Positive VDDx Threshold	—	2.1	2.25	V
	V <sub>DDxUV-</sub>	Negative VDDx Threshold	1.7	1.9	—	
	V <sub>DDxUVH</sub>	VDDx Hysteresis	0.1	0.2	—	
Logic High-level output voltage	V <sub>OH</sub>	V <sub>Ix</sub> = High , I <sub>OH</sub> = - 20 μA	V <sub>DDO</sub> - 0.1	V <sub>DDO</sub>	—	V
		V <sub>Ix</sub> = High , I <sub>OH</sub> = - 4 mA	V <sub>DDO</sub> - 0.4	V <sub>DDO</sub> -0.2	—	
Logic Low-level output voltage	V <sub>OL</sub>	V <sub>Ix</sub> = High , I <sub>OL</sub> = - 20 μA	—	0	0.1	V
		V <sub>Ix</sub> = High , I <sub>OL</sub> = 4 mA	—	0.2	0.4	
Output Impedance	Z <sub>O</sub>	—	—	50	—	Ω
Logic High-level input Threshold voltage	V <sub>IH</sub>	—	0.7 x V <sub>DDI</sub>	—	—	V
Logic Low-level input Threshold voltage	V <sub>IL</sub>	—	—	—	0.3 x V <sub>DDI</sub>	V
Logic Input threshold voltage hysteresis	V <sub>HYS</sub>	—	—	0.32	—	V
DIS pin input Threshold voltage	V <sub>DISIH</sub>	—	0.7 x V <sub>DDI</sub>	—	—	V
DIS pin Low-level input Threshold voltage	V <sub>DISIL</sub>	—	—	—	0.3 x V <sub>DDI</sub>	V
DIS pin Input threshold voltage hysteresis	V <sub>DISHYS</sub>	—	—	0.32	—	V
Input current	I <sub>I</sub>	V <sub>I</sub> = V <sub>DDI</sub> or 0 V	—	—	±10	μA

Note: V<sub>DDI</sub> = Input-side V<sub>DD</sub>, V<sub>DDO</sub> = Output-side V<sub>DD</sub>

**11.5. Switching Characteristics – 3.3 V Supply**

**Table 11.5 Switching Characteristics – 3.3 V Supply**

( $V_{DD1} = V_{DD2} = 3.0\text{ V to }3.6\text{ V}$  over recommended operating conditions unless otherwise noted)

Characteristics		Symbol	Test condition	Min	Typ	Max	Unit
Data Rate		$t_{bps}$	—	20	—	50	Mbps
Propagation Delay		$t_{PHL}$ , $t_{PLH}$	50 kHz, Duty = 50 %, $C_L = 15\text{ pF}$	—	11.6	19.2	ns
Pulse Width Distortion		PWD	$ t_{PHL} - t_{PLH} $	—	0.8	5.1	ns
Propagation Delay Skew (Between any two units)		$t_{PSK}$	(Note1)	—	—	13.0	ns
Channel Matching	Codirectional	$t_{skCD}$	—	—	—	4.4	ns
	Opposing Direction	$t_{skOD}$	—	—	—	4.5	ns
Output signal rise time		$t_r$	10% to 90%	—	0.9	—	ns
Output signal fall time		$t_f$	90% to 10%	—	0.9	—	ns
Disable control pin Propagation delay		$t_{pEN}$	50 kHz, Duty = 50 %, $C_L = 15\text{ pF}$	—	—	23.0	ns
		$t_{p\_DIS}$		—	—	23.0	ns
Common-Mode Transient Immunity		CMTI	$V_I = V_{DD1}$ or 0 V, $V_{CM} = 1500\text{ V}$	—	100	—	kV/ $\mu$ s

Note1: The Propagation delay skew,  $t_{PSK}$ , is equal to the magnitude of the difference in propagation delay.  
That will be seen between units at the same given conditions (supply voltage, input current, temperature, etc.).

**11.6. Supply Current Characteristics – 3.3 V Supply**

**Table 11.6 Supply Current Characteristics – 3.3 V Supply**

( $V_{DD1} = V_{DD2} = 3.0\text{ V to }3.6\text{ V}$  over recommended operating conditions unless otherwise noted)

Characteristics		Symbol	Test condition	Min	Typ	Max	Unit
DC Supply Current	Primary side	$I_{DDQ1(0)5}$	$V_I = \text{Low}$	—	2.9	4.1	mA
		$I_{DDQ1(1)5}$	$V_I = \text{High}$	—	16.5	22.3	
	Secondary side	$I_{DDQ2(0)5}$	$V_I = \text{Low}$	—	4.4	6.5	mA
		$I_{DDQ2(1)5}$	$V_I = \text{High}$	—	10.1	14.0	
Supply Current (AC signal)	$t_{bps} = 1\text{ Mbps}$	Primary side	$f_{CLK} = 500\text{ kHz}$ , Duty = 50 % square wave, $C_L = 15\text{ pF}$	—	9.9	14.9	mA
		Secondary side		—	7.5	9.5	
	$t_{bps} = 25\text{ Mbps}$	Primary side	$f_{CLK} = 12.5\text{ MHz}$ , Duty = 50 % square wave, $C_L = 15\text{ pF}$	—	10.8	16.6	mA
		Secondary side		—	9.7	12.8	
	$t_{bps} = 50\text{ Mbps}$	Primary side	$f_{CLK} = 25\text{ MHz}$ , Duty = 50 % square wave, $C_L = 15\text{ pF}$	—	12.0	17.7	mA
		Secondary side		—	12.0	17.2	

## 12. Characteristic Chart (Note)

### 12.1. Supply Current vs Data rate

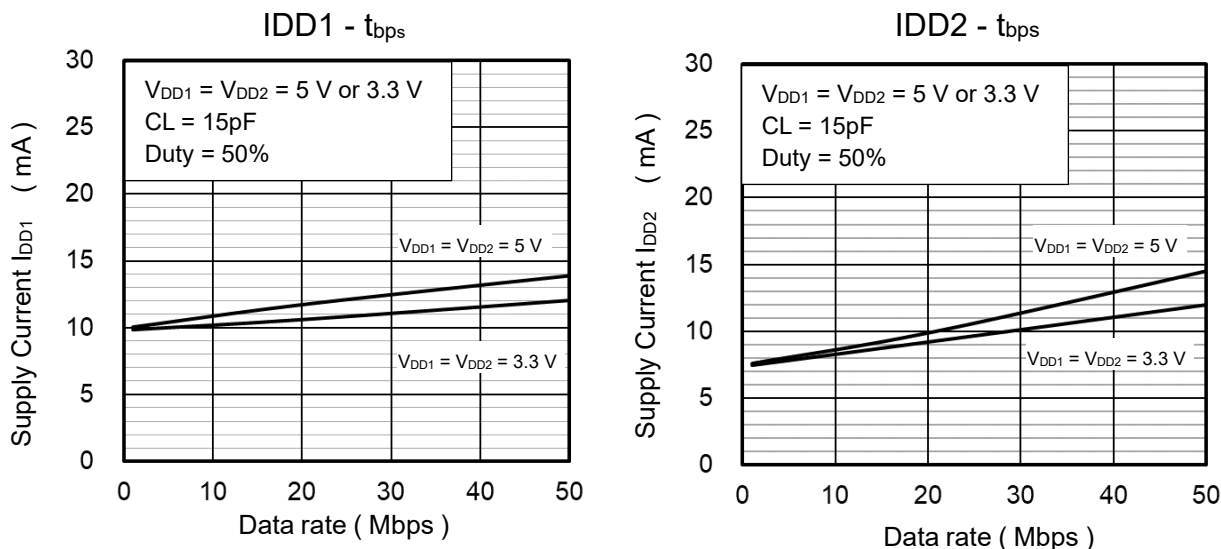


Figure12.1 Supply Current – Data rate

### 12.2. Output Voltage vs Output Current

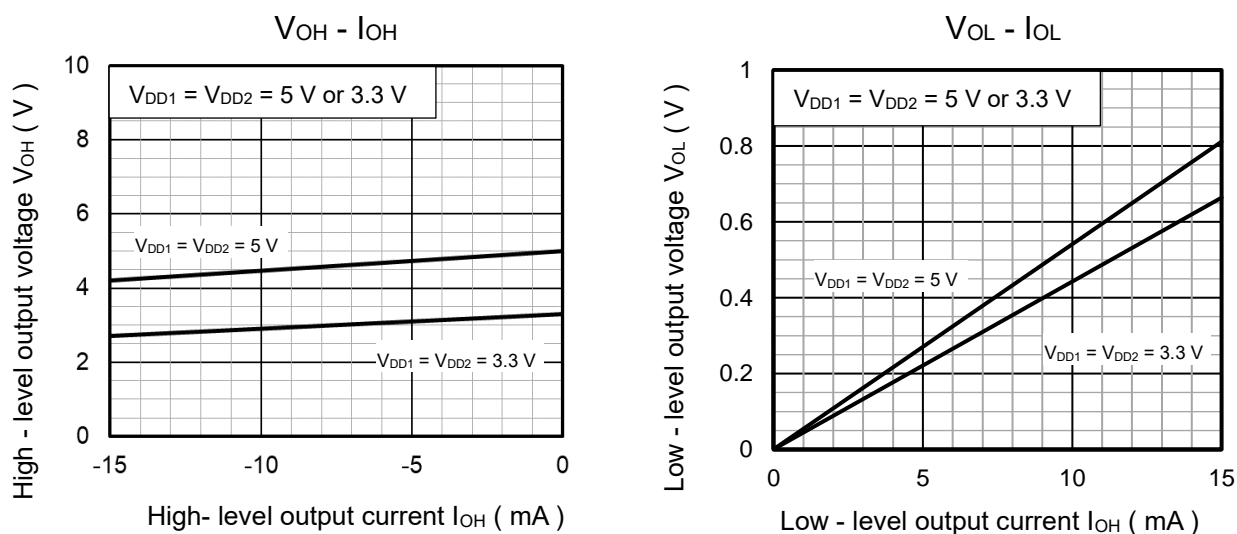


Figure12.2 Output Voltage – Output Current

Note: The following characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

12.3. Propagation Delay Time vs Ambient Temperature

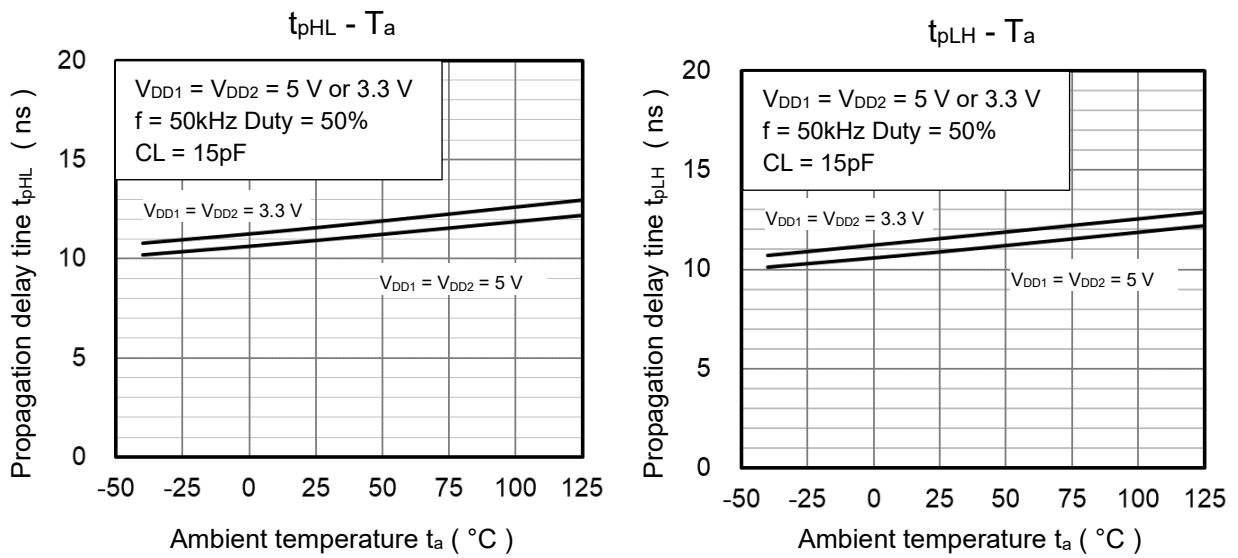


Figure12.3 Propagation Delay Time vs Ambient Temperature

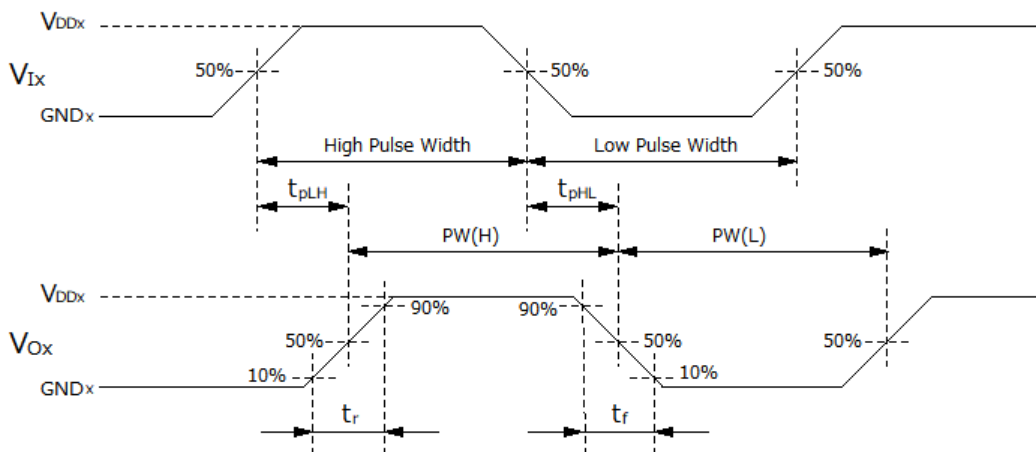


Figure12.4 Switching Waveforms

Note: The following characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

## 13. Package Information

**Table 13.1 Insulation Related Specifications (Note)**

Parameters	Symbol	DCM341A01	Unit
Minimum clearance	CLR	8.0	mm
Minimum creepage distance	CPG	7.6	mm
Minimum insulation thickness	DTI	17	μm
Comparative tracking index	CTI	550	V

Note: If a printed circuit is incorporated, the creepage distance and clearance may be reduced below this value. (e.g., at a standard distance between soldering eye centers of 7.5 mm). If this is not permissible, the user shall take suitable measures.

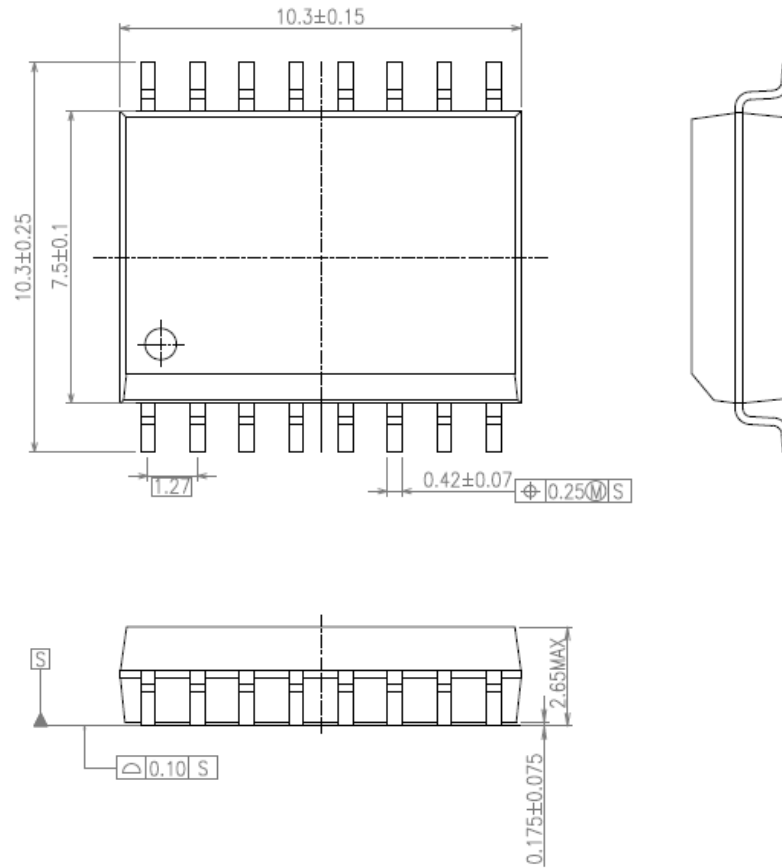
Note: This photocoupler is suitable for safe electrical isolation only within the safety limit data. Maintenance of the safety data shall be ensured by means of protective circuits.

**14. Package Information**

**14.1. Package Dimensions**

16pin SOIC Wide body  
( P-SOP16-0811-1.27-002 )

UNIT: mm



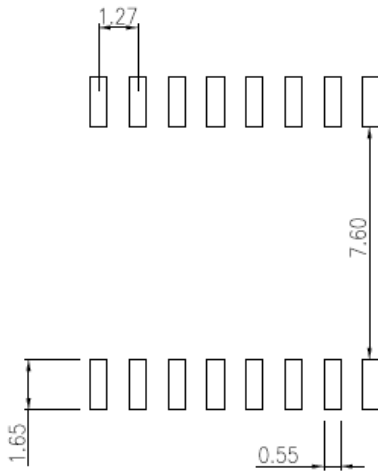
Weight: 0.426 g (typ.)

**Figure 14.1 Package Dimensions**

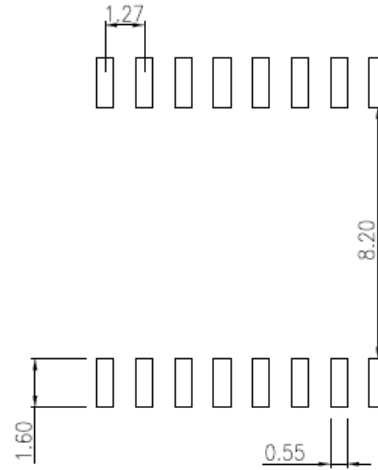
## 14.2. Land Pattern Dimensions for Reference only

16pin SOIC Wide body  
( P-SOP16-0811-1.27-002 )

Unit: mm



Complies with JEITA ET-7501 Level 3 Normal  
Creepage distance: 7.6 mm



Isolation option  
Creepage distance:  $\geq 8$ mm

**Figure 12.2 Land Pattern Dimensions for Reference only**

### Notes.

- Unless otherwise indicated, dimensions are given in millimeters.
- This document is a reference drawing in accordance with JEITA ET-7501 Level 3. The Company does not guarantee the accuracy or completeness of the diagrams and information.
- The customer should fully evaluate the various conditions (soldering conditions, etc.) and adjust at their own risk.
- The diagrams in this document do not accurately show the actual shape and dimensions. Do not use the dimensions of the actual product as a basis for designing the product.
- When designing and using the product, check the latest information on the product and the operating instructions of the equipment in which the product is to be used, and follow these instructions.



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