

# **32-bit RISC Microcontroller Reference Manual**

## **Clock Selective Watchdog Timer (SIWDT-A)**

### **Revision 3.4**

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**2026-08**

**Toshiba Electronic Devices & Storage Corporation**

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## Preface

### Notices and Legal Information

All other company names, product names, and service names mentioned herein may be trademarks of their respective companies.

### Related Document

| Document name                    |
|----------------------------------|
| Datasheet                        |
| Clock Control and Operation Mode |
| Exception                        |
| Interrupt Control Circuit        |
| Power Supply and Reset Operation |
| Power Control and Reset          |
| Product Information              |

### Terms and Abbreviations

Some of abbreviations used in this document are as follows:

SIWDT      Clock Selective Watchdog Timer

### Conventions

- Numeric formats follow the rules as shown below:
  - Hexadecimal:      0xABC
  - Decimal:            123 or 0d123      - Only when it needs to be explicitly shown that they are decimal numbers.
  - Binary:             0b111      - It is possible to omit the "0b" when the number of bits can be distinctly understood from a sentence.
- "\_N" is added to the end of signal names to indicate low active signals.
- It is called "assert" that a signal moves to its active level, "deassert" to its inactive level.
- When two or more signal names are referred, they are described like as [m:n].  
Example: S[3:0] shows four signal names S3, S2, S1 and S0 together.
- The characters surrounded by [ ] defines the register.  
Example: [ABCD]
- "N" substitutes suffix number of two or more same kind of registers, fields, and bit names.  
Example: [XYZ1], [XYZ2], [XYZ3] → [XYZn]
- "x" substitutes suffix number or character of units and channels in the register list.
- In case of unit, "x" means A, B, and C, ...  
Example: [ADACR0], [ADBCR0], [ADCCR0] → [ADxCR0]
- In case of channel, "x" means 0, 1, and 2, ...  
Example: [T32A0RUNA], [T32A1RUNA], [T32A2RUNA] → [T32AxRUNA]
- The bit range of a register is written like as [m: n].  
Example: Bit[3: 0] expresses the range of bit 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.  
Example: [ABCD]<EFG> = 0x01 (hexadecimal), [XYZn]<VW> = 1 (binary)
- Word and byte represent the following bit length.  
Byte:                8 bits

Half word: 16 bits  
Word: 32 bits  
Double word: 64 bits

- Properties of each bit in a register are expressed as follows:  
R: Read only  
W: Write only  
R/W: Read and write are possible.
- Unless otherwise specified, register access supports only word access.
- The register defined as "Reserved" must not be rewritten. Moreover, do not use the read value.
- The value read from the bit having default value of "-" is unknown.
- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value. In the cases that default is "-", follow the definition of each register.
- Reserved bits of the write-only register should be written with their default value. In the cases that default is "-", follow the definition of each register.
- Do not use read-modified-write processing to the register of a definition which is different by writing and read out.

### 1. Outlines

When the CPU executes mal function (a runaway) caused by a noise or others, the watchdog timer (SIWDT) detects it and gives a trigger to the CPU to resume the correct function.

| Function classification | Function                                                                                                      | Operation                                                                                                                                                                      |
|-------------------------|---------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Timer control           | Clock selection                                                                                               | It is possible to select the source clock of runaway detection from "fsys/4", "flHOSC1", "flHOSC2".                                                                            |
|                         | Detection time control                                                                                        | It is possible to select the detection time between $2^{15}$ to $2^{29}$ count of the selection clock.                                                                         |
| Decision control        | Window selection                                                                                              | It is possible to select the clear window of runaway detection from "No settings", "Later 1/2" and "Last 1/4".                                                                 |
| Detection control       | Detection behavior                                                                                            | It is possible to select behavior of the runaway detection from "Interrupt" and "Reset".                                                                                       |
| Protection control      | Mode selection                                                                                                | It is possible to select the "Protection A mode" which cannot be released except for RESET, and "Protection B mode" which can be released by <b>[SIWDXPRO]</b> <PROTECT[7:0]>. |
|                         | Control of modification of the oscillation clock control bit of the internal high-speed oscillator 2 (IHOSC2) | It is possible to control modification of the oscillation clock control bit of the internal high-speed oscillator 2 (IHOSC2).                                                  |

## 2. Configuration

Figure 2.1 shows the block diagram of SIWDT.

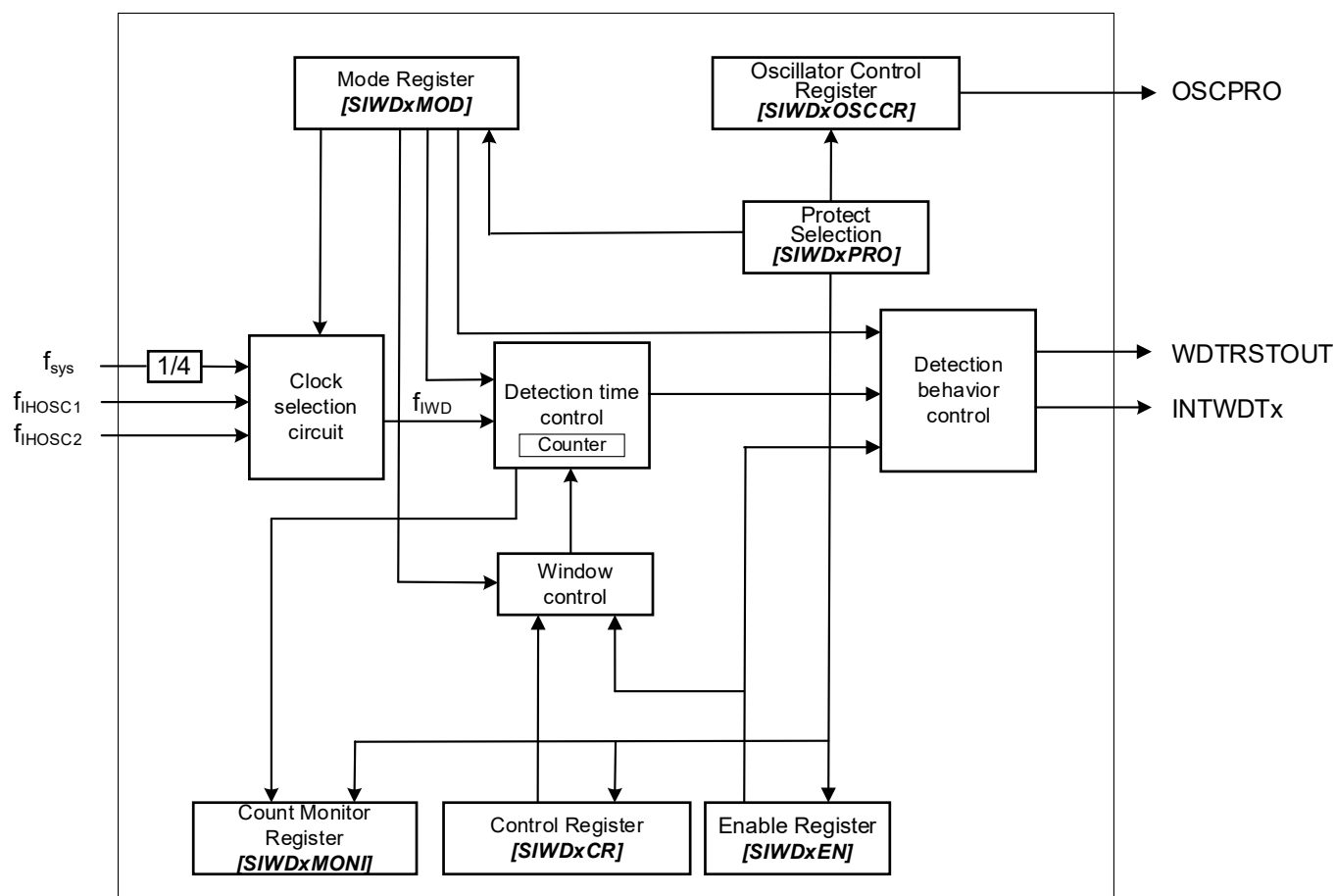


Figure 2.1 SIWDT Block Diagram

Table 2.1 List of Signals

| No. | Symbol   | Signal name                                                                                                   | I/O    | Related reference manual (Note1)                                                                |
|-----|----------|---------------------------------------------------------------------------------------------------------------|--------|-------------------------------------------------------------------------------------------------|
| 1   | fsys     | System clock                                                                                                  | Input  | Clock Control and Operation Mode                                                                |
| 2   | fIHOSC1  | Internal oscillator 1                                                                                         | Input  | Clock Control and Operation Mode                                                                |
| 3   | fIHOSC2  | Internal oscillator 2                                                                                         | Input  | Clock Control and Operation Mode                                                                |
| 4   | INTWDTx  | Watchdog timer interrupt                                                                                      | Output | Exception Interrupt Control Circuit                                                             |
| 5   | WDRSTOUT | Watchdog timer reset                                                                                          | Output | Power Supply and Reset Operation<br>Clock Control and Operation Mode<br>Reset Control and Reset |
| 6   | OSCPRO   | Control of modification of the oscillation clock control bit of the internal high-speed oscillator 2 (IHOSC2) | Output | Product Information                                                                             |

Note1: Related reference manuals may differ depending on the product. For detail, refer to the table of "Reference Manuals" of datasheet.

## 3. Function and Operation

### 3.1. Basic Operation

SIWDT is for detecting malfunctions (runaway) of the CPU caused by noises or other disturbances and remedying them to return the CPU to normal operation.

Writing the clear code (0x4E) to *[SIWDTxCR]<WDCR[7:0]>* before the configured detection time has elapsed clears the counter and causes it to restart counting.

When the configured detection time elapses, a runaway is detected, and either an INTWDTx interrupt is generated or the microcontroller is reset. If an INTWDTx interrupt is generated, write the clear code (0x4E) to *[SIWDTxCR]<WDCR[7:0]>* while the counter is working (*[SIWDTxEN]<WDTF>* = 1). This clears both the counter and the interrupt request.

### 3.2. Clock Supply

The SIWDT starts the count immediately after the reset is deasserted. The selected clock is "the system clock (fsys) of 4 division" at that time. If SIWDT is not used, it should be disabled. When the setting is changed, it should be disabled, too.

### 3.3. Clock Selection Circuit

For clock control, refer to the reference manual "Clock Control and Operation Mode".

#### 3.3.1. Clock Selection

The clock which is selected from "the system clock (fsys) of 4 division", "internal oscillation clock "1" ( $f_{IHOSC1}$ )", and "internal oscillation clock 2 ( $f_{IHOSC2}$ )" by *[SIWDTxMOD]<WDLCS[1:0]>*, is used as input clock.

#### 3.3.2. Clock Run and Stop

When a counter clock to SIWDT is stopped, the SIWDT must be stopped.

The operation of SIWDT set to "1" to *[SIWDTxEN]<WDTE>*.

The *[SIWDTxCR]<WDCR[7:0]>* should be set to disable code (0xB1) after the *[SIWDTxEN]<WDTE>* set to "0" for stopping SIWDT. The SIWDT is disabled, and counter is cleared.

### 3.4. Detection Time Control

The detection time is selected from among  $2^{15}$ ,  $2^{17}$ ,  $2^{19}$ ,  $2^{21}$ ,  $2^{23}$ ,  $2^{25}$ ,  $2^{27}$  and  $2^{29}$  by *[SIWDTxMOD]<WDTP[2:0]>*.

### 3.5. Detection Operation Control

The generator which is selected by the *[SIWDTxMOD]<RESCR>* after the elapse of detection time, is "watchdog timer interrupt (INTWDTx)", or "reset".

### 3.6. Window Control

#### 3.6.1. Clear Window Setting

The clear window is selected with  $[SIWDxMOD]<WDCWD[1:0]>$  from among none specified, the latter half of the detection interval, and the last quarter of the detection interval.

If the clear code is written during the clear window interval, the counter is cleared and re-starts the count.

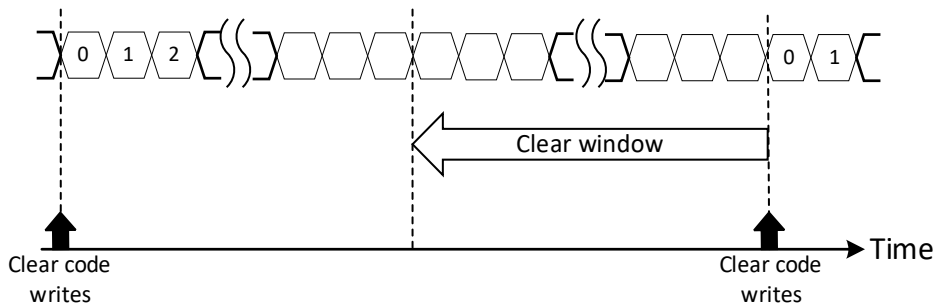


Figure 3.1 Clear Code Writes during Clear Window Interval

If the clear code is written before the clear window, the operation is as follows according to the setting of  $[SIWDxMOD]<RESCR>$ .

When  $[SIWDxMOD]<RESCR> = 1$  and the reset generation is enabled, the reset is asserted and the SIWDT becomes the initialization state.

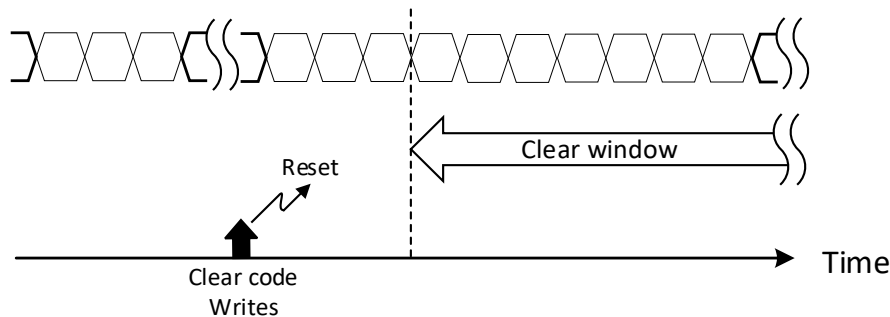


Figure 3.2 Clear Code Writes before Clear Window (1)

When  $[SIWDxMOD]<RESCR> = 0$  or the INTWDTx generation is enabled, the INTWDTx is generated and  $[SIWDxMOD]<INTF>$  is set to "1" every write of the clear code. The counter continues the count and the INTWDTx is generated at the detection time, again.

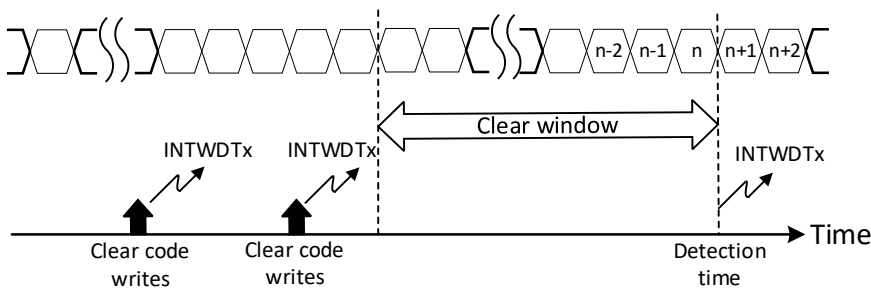


Figure 3.3 Clear Code Writes before Clear Window (2)

## 3.7. Protection Control

### 3.7.1. Protection Mode

There are two types of protection modes to prevent from unexpected writing. Its setting should be done while *[SIWDxEN]<WDTE>* is "1".

(a) Protection A mode

*[SIWDxPRO]<PROTECT[7:0]>* should be set to 0xA9 to select the protection A mode.

Only 0x4E (Clear code) can be written to *[SIWDxCR]<WDCR[7:0]>* in this mode. Other code write is ignored.

The protection A mode can be cleared only by the reset initialization.

(b) Protection B mode

*[SIWDxPRO]<PROTECT[7:0]>* should be set to 0x74 to select the protection B mode.

Only 0x4E (Clear code) can be written to *[SIWDxCR]<WDCR[7:0]>* and only 0x1E (protection B mode clear) can be written to *[SIWDxPRO]<PROTECT[7:0]>*. Other code write to the fields is ignored.

### 3.7.2. Oscillation Control of Internal High-speed Oscillator 2 (IHOSC2)

When *[SIWDxOSCCR]<OSCPRO>* is set to "1", the write is inhibited to the oscillation clock control bit of the internal high-speed oscillator 2 (IHOSC2).

For the internal oscillation clock control bit, refer to reference manual "Product Information".

## 3.8. Count Monitor

The *[SIWDxMONI]<MONI[29:0]>* should be read multiple times. When the read value is different, it is shown that the counter is working.

## 3.9. Operation Status of Counter

In debug halt, the counter of SIWDT is stopped.

Refer to reference manual "Clock Control and Operation Mode" for each operation mode.

## 4. Registers

### 4.1. List of Registers

The control registers and their addresses are shown as follows:

| Peripheral function |       | Channel /Unit | Base address |            |            |
|---------------------|-------|---------------|--------------|------------|------------|
|                     |       |               | TYPE1        | TYPE2      | TYPE3      |
| Watchdog Timer      | SIWDT | ch0           | 0x400BB400   | 0x400A0600 | 0x40040600 |
|                     |       | ch1           | -            | 0x400A0700 | 0x40040700 |

Note: The channel/unit and base address type are different by products. Please refer to "Products Information" of the reference manual for the details.

| Register name                              | Address (Base+)            |
|--------------------------------------------|----------------------------|
| Protection Register                        | <b>[SIWDxPRO]</b> 0x0000   |
| Enable Register                            | <b>[SIWDxEN]</b> 0x0004    |
| Control Register                           | <b>[SIWDxCR]</b> 0x0008    |
| Mode Register                              | <b>[SIWDxMOD]</b> 0x000C   |
| Count Monitor Register                     | <b>[SIWDxMONI]</b> 0x0010  |
| Oscillation Clock Protect Control Register | <b>[SIWDxOSCCR]</b> 0x0014 |

## 4.2. Details of Registers

### 4.2.1. [SIWDxPRO] (Protection Register)

| Bit  | Bit symbol   | After reset | Type | Function                                                                                                                                            |
|------|--------------|-------------|------|-----------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | -            | 0           | R    | Read as "0".                                                                                                                                        |
| 7:0  | PROTECT[7:0] | 0x1E        | R/W  | Protection mode<br>0x1E: No protection<br>0xA9: Protection A mode setting<br>0x74: Protection B mode setting<br><br>The other settings are ignored. |

Note: When **[SIWDxEN]<WDTF>** = 1, this field can be written except in the protection A mode.

### 4.2.2. [SIWDxEN] (Enable Register)

| Bit  | Bit symbol | After reset | Type | Function                                                                          |
|------|------------|-------------|------|-----------------------------------------------------------------------------------|
| 31:2 | -          | 0           | R    | Read as "0".                                                                      |
| 1    | WDTF       | 1           | R    | Operation flag<br>0: Stop<br>1: Operating<br><br>SIWDT operation status is shown. |

| Bit | Bit symbol | After reset | Type | Function                                                                                                                                                                                                                                                                                                   |
|-----|------------|-------------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0   | WDTE       | 1           | R/W  | Enable or disable control<br>0: Disabled<br>1: Enabled<br><br>When SIWDT is disabled, it is necessary to disable that <WDTE> should be set to "0" and then the disable code (0xB1) should be written to <b>[SIWDTxCR]&lt;WDCR[7:0]&gt;</b> .<br><WDTE> should be set to "1" to return to the enable state. |

### 4.2.3. [SIWDTxCR] (Control Register)

| Bit  | Bit symbol | After reset | Type | Function                                                                                                         |
|------|------------|-------------|------|------------------------------------------------------------------------------------------------------------------|
| 31:8 | -          | 0           | R    | Read as "0".                                                                                                     |
| 7:0  | WDCR[7:0]  | Undefined   | W    | Disable code and clear code<br>0xB1: Disable code<br>0x4E: Clear code<br><br>The other codes writing is ignored. |

### 4.2.4. [SIWDTxMOD] (Mode Register)

| Bit   | Bit symbol | After reset | Type | Function                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-------|------------|-------------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:14 | -          | 0           | R    | Read as "0".                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 13:12 | WDCLS[1:0] | 00          | R/W  | Clock selection<br>00: fsys/4<br>01: Internal oscillation clock 1 (fIHOSC1)<br>10: Internal oscillation clock 2 (fIHOSC2)<br>11: Reserved                                                                                                                                                                                                                                                                                           |
| 11    | -          | 0           | R    | Read as "0".                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 10:8  | WDTP[2:0]  | 000         | R/W  | Detection time selection<br>(f <sub>WD</sub> = The clock which is selected by <WDCLS[1:0]>)<br>000: 2 <sup>15</sup> /f <sub>WD</sub><br>001: 2 <sup>17</sup> /f <sub>WD</sub><br>010: 2 <sup>19</sup> /f <sub>WD</sub><br>011: 2 <sup>21</sup> /f <sub>WD</sub><br>100: 2 <sup>23</sup> /f <sub>WD</sub><br>101: 2 <sup>25</sup> /f <sub>WD</sub><br>110: 2 <sup>27</sup> /f <sub>WD</sub><br>111: 2 <sup>29</sup> /f <sub>WD</sub> |
| 7:6   | -          | 0           | R    | Read as "0".                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 5:4   | WDCWD[1:0] | 00          | R/W  | Clear window setting<br>00: No setting<br>01: Second half<br>10: Last quarter<br>11: Reserved                                                                                                                                                                                                                                                                                                                                       |
| 3:2   | -          | 0           | R    | Read as "0".                                                                                                                                                                                                                                                                                                                                                                                                                        |

| Bit | Bit symbol | After reset | Type | Function                                                                                                      |
|-----|------------|-------------|------|---------------------------------------------------------------------------------------------------------------|
| 1   | INTF       | 0           | R    | INTWDTx generation by the clear code write before the clear window<br>0: Not generated<br>1: Generated        |
|     |            |             | W    | The clear set of flag<br>0: don't care<br>1: clear to "0".                                                    |
| 0   | RESCR      | 1           | R/W  | Operation after the runaway detection<br>0: INTWDTx interrupt request is generated.<br>1: Reset is generated. |

Note: This can be written when  $[SIWDxEN] < WDTF = 0$  except in the protection setting state.

### 4.2.5. $[SIWDxMONI]$ (Count Monitor Register)

| Bit   | Bit symbol | After reset | Type | Function                                                                                                                                                                                                                      |
|-------|------------|-------------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:30 | -          | 0           | R    | Read as "0".                                                                                                                                                                                                                  |
| 29:0  | MONI[29:0] | Undefined   | R    | Counter monitor<br>This register should be read multiple times. When the read values are different, it is shown that the counter is working. The read value is not precisely correct. It should be used as a reference value. |

### 4.2.6. $[SIWDxOSCCR]$ (Oscillation Clock Protect Control Register)

| Bit  | Bit symbol | After reset | Type | Function                                                                                                                                      |
|------|------------|-------------|------|-----------------------------------------------------------------------------------------------------------------------------------------------|
| 31:1 | -          | 0           | R    | Read as "0".                                                                                                                                  |
| 0    | OSCPRO     | 0           | R/W  | Write protection for the oscillation clock control bit of the internal high-speed oscillator 2 (IHOSC2). (Note1)<br>0: Disabled<br>1: Enabled |

Note: When  $[SIWDxEN] < WDTF = 0$ , this bit can be written except in the protection setting state.

Note1: For the oscillation clock control bit of the internal high-speed oscillator 2 (IHOSC2), refer to reference manual "Product Information".

### 5. Precaution

- When **[SIWDxPRO]<PROTECT[7:0]>** is "0x1E" (No protection) or "0x74" (Protection B mode)  
Before CPU transfers low-power consumption mode (STOP1/STOP2/IDLE) from NORMAL mode, SIWDT should be disabled. For details of setting procedure, refer to the reference manual "Clock Control and Operation Mode".
- When **[SIWDxPRO]<PROTECT[7:0]>** is "0x9A" (Protection A mode)  
The count clock operation in each low-power consumption mode is shown in Table 5.1. For the oscillation clock control bit of the internal high-speed oscillator 2 (IHOSC2), refer to the reference manual "Product Information".

**Table 5.1 Count Clock Operation in Each Low-power Consumption Mode**

| Count clock |                                                                        | IDLE mode | STOP1 mode |
|-------------|------------------------------------------------------------------------|-----------|------------|
| fsys/4      |                                                                        | Keep up   | Stopped    |
| fIHOSC1     |                                                                        | Keep up   | Stopped    |
| fIHOSC2     | When oscillation clock control bit is <b>[CGOSCCR]&lt;IHOSC2EN&gt;</b> | Keep up   | Stopped    |
|             | When oscillation clock control bit is <b>[RLMLOSCCR]&lt;POSCEN&gt;</b> | Keep up   | Keep up    |

## 6. Revision History

Table 6.1 Revision History

| Revision | Date       | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|----------|------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1.0      | 2017-09-08 | First release                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 2.0      | 2018-03-23 | <ul style="list-style-type: none"> <li>- 3.5 Detection Behavior Control<br/>Added INTWDTx in "watchdog timer interrupt"</li> <li>- 3.9 Operation Mode and Operation Status<br/>Added Table 3.1</li> <li>- 4.1 List of Register<br/>Modified Note</li> <li>- 4.2.4 <b>[SIWDxMOD]</b><br/>Modified INTWDT to INTWDTx of &lt;INTF&gt;&lt;RESCR&gt;</li> <li>- Precaution<br/>Modified explanation</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 3.0      | 2018-06-19 | <ul style="list-style-type: none"> <li>- 1 Outlines<br/>Deleted Table title</li> <li>- 4.1 List of Registers<br/>Added base address of TYPE2(ch1) and TYPE3</li> <li>- 4.2.3 <b>[SIWDxCR]</b><br/>Modified after reset value of &lt;WDCR[7:0]&gt; to undefined</li> <li>- 4.2.5 <b>[SIWDxMONI]</b><br/>Modified after reset value of &lt;MONI[29:0]&gt; to undefined</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 3.1      | 2023-06-14 | <ul style="list-style-type: none"> <li>- 1. Outlines<br/>Name and description of the 2nd function of "Protection Control" are changed.</li> <li>- Table 2.1 List of Signals<br/>Signal name and related reference manual of OSCPRO are changed.</li> <li>- 3.2. Clock Supply<br/>The description is changed.</li> <li>- 3.7.2. Oscillation Clock Control Bit of Internal High-speed Oscillator 2 (IHOSC2)<br/>The description for the oscillation clock control bit of the internal high-speed Oscillator 2 (IHOSC2) is changed.</li> <li>- 3.9. Operation Status of Counter<br/>A table is deleted.<br/>The description for the counter is changed.</li> <li>- 4.2.6. <b>[SIWDxOSCCR]</b> (Oscillation Enable Register)<br/>The description for &lt;OSCPRO&gt; is changed.<br/>Note 2 is changed.</li> <li>- 5. Precaution<br/>The description is changed.</li> </ul> |
| 3.2      | 2023-09-15 | <ul style="list-style-type: none"> <li>- Table 2.1 List of Signals<br/>Corrected reference manual name for WDTRSTOUT.</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 3.3      | 2024-10-31 | <ul style="list-style-type: none"> <li>- Appearance updated</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 3.4      | 2026-08-21 | <ul style="list-style-type: none"> <li>- Related Document<br/>The documents are added.</li> <li>- Table 2.1 List of Signals<br/>The related reference manuals are added.</li> <li>- 3.1. Basic Operation<br/>The description is changed.</li> <li>- 3.3. Clock Selection Circuit<br/>The description is added.</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |

### RESTRICTIONS ON PRODUCT USE

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